Terawins, Inc.

***Brief Information***
***Version 1.00***

*May 12, 2009*

# T118ES Video Display Controller

# Contents

# 1 Introduction

## 1.1 Features

- **Cost Effective Highly Integrated Triple ADC + + 2D Video Decoder + OSD + Scaler + TCON**
  - Integrates 10-bit Analog to Digital Converters (ADC) & Phase Locked Loop (PLL)
  - Scaler supports 2-D adaptive intra-field de-interlacer and non-linear 16:9 aspect ratio.
  - Requires no external Frame Buffer Memory for deinterlacer.
  - Advanced On Screen Display (OSD) function
  - Programmable Timing Controller (TCON) for Car TV applications
  - Multi-standard color decoder with 2D adaptive comb filter

- **Triple 10-bit Analog to Digital Converters (ADC)**
  - 86 MSPS Conversion Rate
  - Built-in Pre-amp, mid-level & ground clamp circuit
  - Automatic Clamp Control for CVBS, Y/C and YPbPr(480i)
  - Programmable Static Gain Control or Automatic Gain Control for CVBS ,Y/C or YPbPr(480i)
  - Max Input configuration up to 5xCVBS, 2xS-video and 1xCVBS or 1xS-Video and 1xYPbPr(480i)

- **Digital Video Enhancement**
  - Separate Luminance and Chroma Enhancer
  - Y Supports Luminance Peaking, DLTI, Black Level Expansion, Contrast and Brightness adjustment
  - C Supports DCTI, Saturation and Hue adjustment.

- **Advanced Scaling Engine**
  - Two Dimensions FIR Scaler
  - Coefficient based sharpness filters
  - 2-D edge enhancement
  - Independent vertical and horizontal scaling ratio
  - 16:9 Non-linear Aspect ratio

- **Color Management**
  - Coef. Programmable YCbCr-to-RGB Color Space Converter
  - Independent RGB Gamma Correction

- **LCD Interface**
  - Provides 256-entry TBL Gamma correction for panel compensation
  - Supports image pan functions
  - Programmable Timing Controller
  - Built-in software adjustable VCOM voltage
  - 4.0v RGB Triple DAC output or Digital Serial RGB
  - Integrated high efficiency DC-DC power conversion unit for gate and source drivers reduces energy consumption
  - Integrated LCD backlight inverter drive unit supports LED typed backlight
  - Software adjustable lamp dimming

- **Built-in On Screen Display Engine**
  - 3K-word OSD SRAM memory
  - 1K-word Built-in font ROM
  - Supports font or bitmap modes
  - Supports character blinking, overlay, shadow and border functions
  - Fully programmable character mapping
  - Supports alpha blending & Zoom-in/Zoom-out function
  - Optional fonts can be stored in off-chip serial EEPROM

- **Crystal Oscillator Circuit**
  - Direct interface to a (27.0MHz) Crystal
  - Also provide a buffered clock output for external Micro-controller

- **Digital Test Pattern Generator**
  - Programmable standard & special panel burn-in test patterns
  - Support special border frame blocking mode

- **Misc.**
  - Supports 2-wire $I^2C$ (Slave/Master)
  - Supports free run OSD mode
  - Pulse Width Modulation Outputs

- **Power Supply: +1.8V, +3.3V and +4.7V**

- **Package: 48-pin LQFP**

## 1.2 General Description

The T118E is a highly integrated All-in-one Visual Processor that provides major cost saving solution for the portable applications. T118E has built-in high performance dual ADCs, TCON, Triple DACs, Scaling Machine with sophisticated upscaling and downscaling algorithms. The Innovative integrated “Frame-Buffer-Less” De-interlacer can significantly reduce system cost. The T118E also integrates On Screen Display engine with 3K words of font RAM and built-in 1K words of font ROM. The device can interface to an external micro-controller through 2-wire serial bus interface.

## 1.3 Applications

1. Small to medium sized displayer, In-car TV
2. Video Door Phone
3. Digital Photo Frame

## 1.4 System Architecture

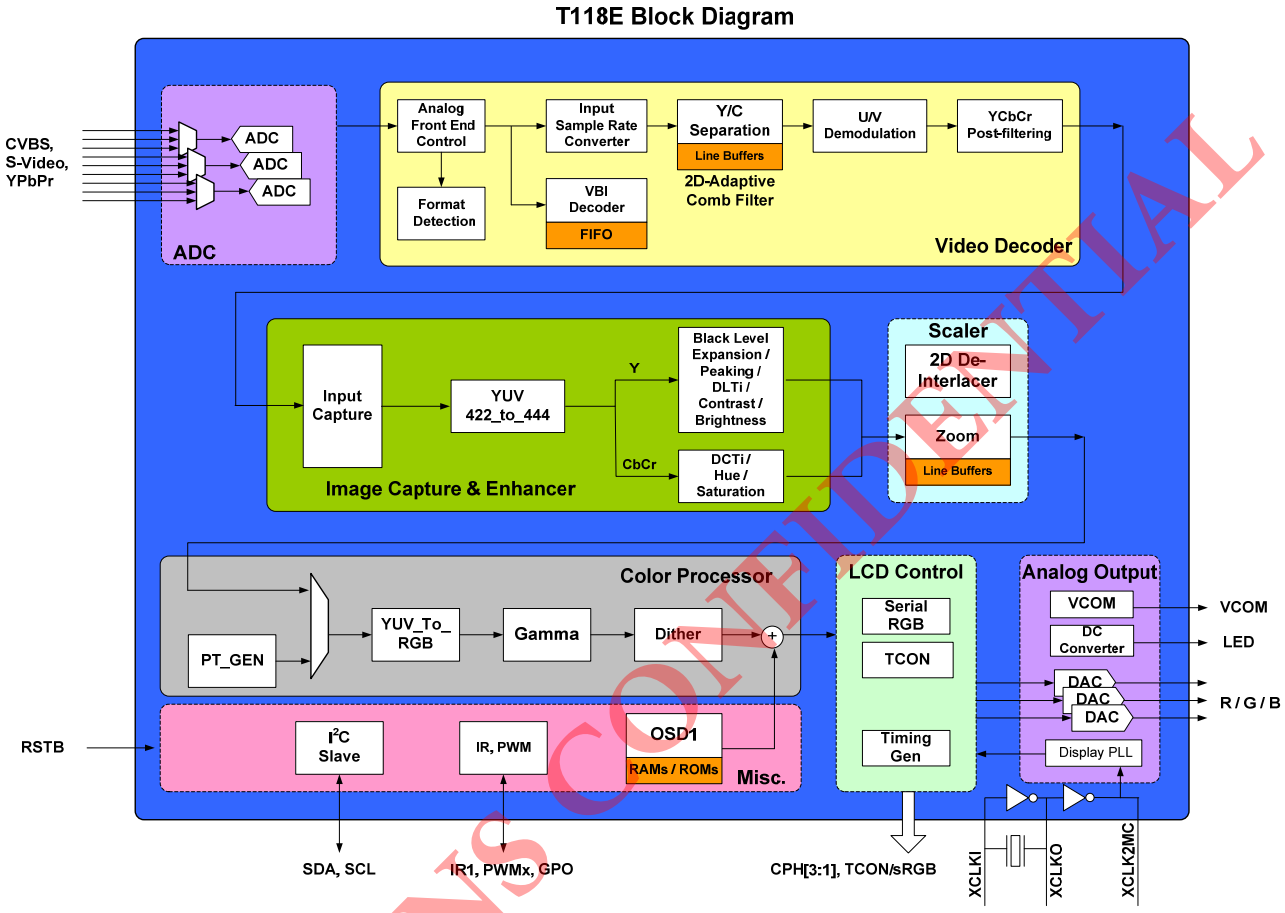



**Figure 1-1 System Architecture**

## 1.5 System Configurations

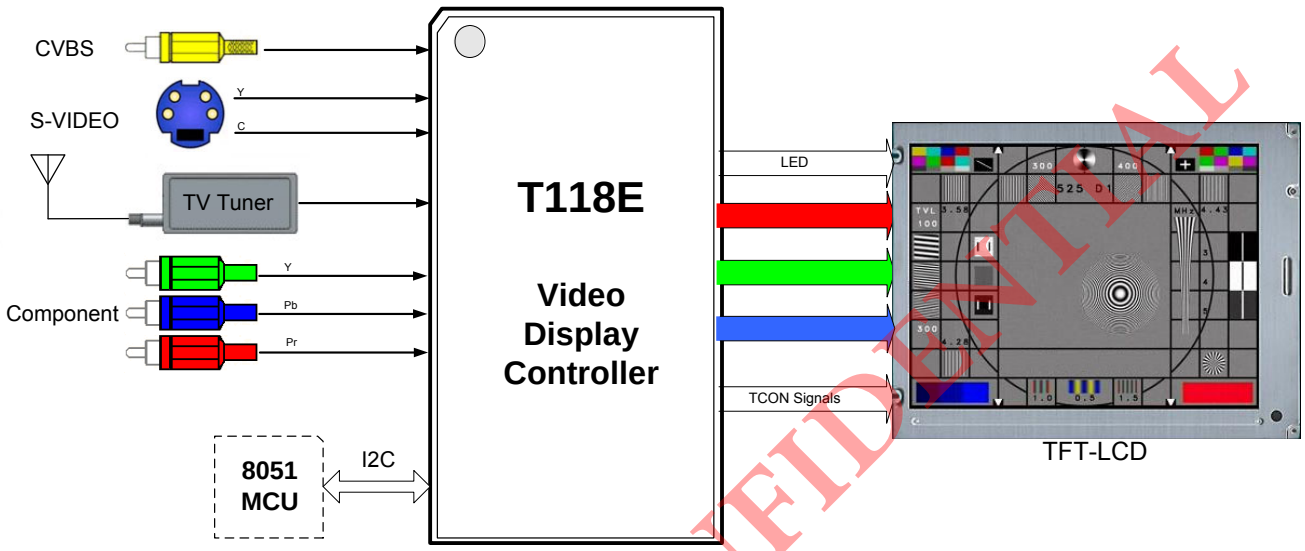



**Figure 1-2 System Configurations**

## 1.6 Pinout Diagram-T118ES

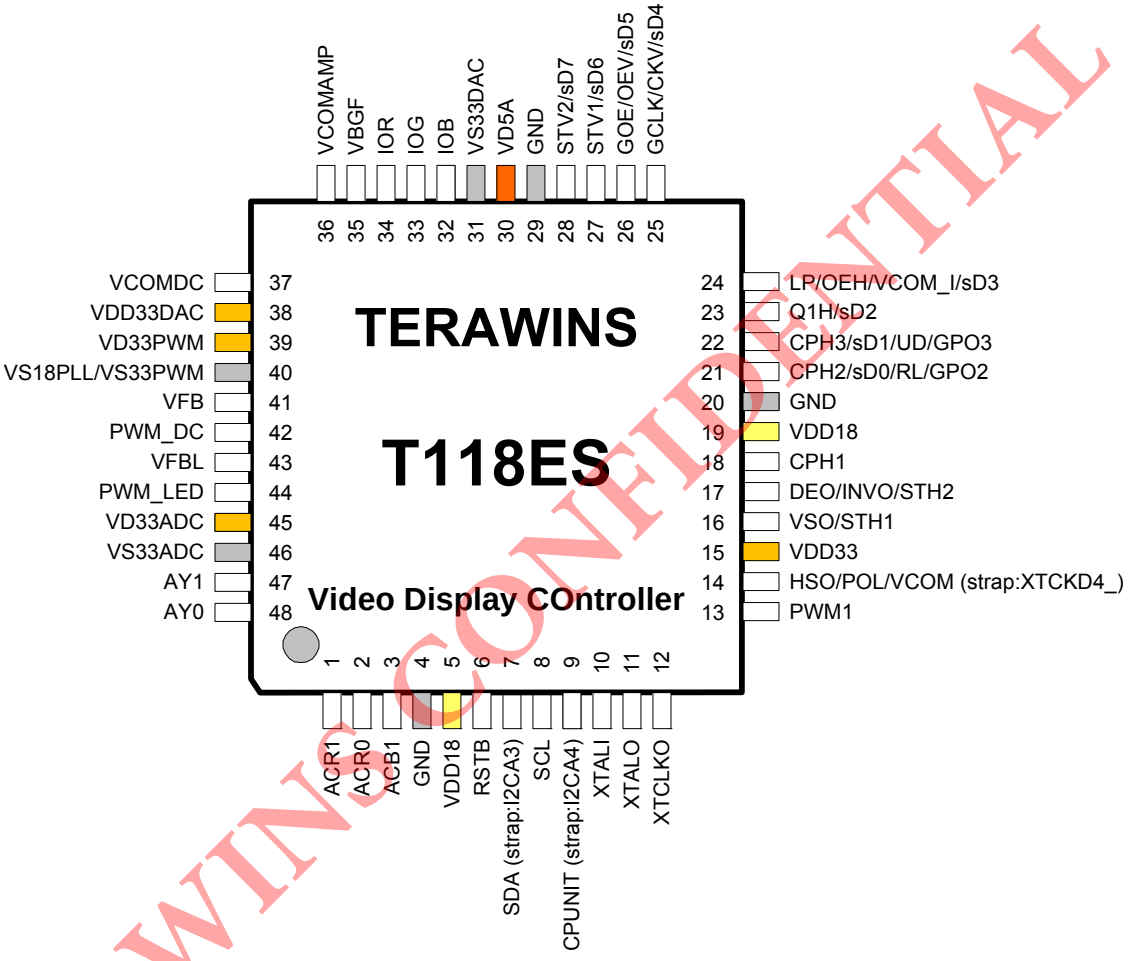



**Figure 1-3 T118ES Pinout Diagram**

## 1.7 Pin Description-T118ES

**Table 1-1 T118ES Pin Description**

| Symbol | Pin # | Type | Description |
|---|---|---|---|
| **Power Supplies** | | | |
| VDD18 | 5,19 | PWR | +1.8V digital core power supply |
| VDD33 | 15 | PWR | +3.3V digital output power supply, |
| VD5A | 30 | PWR | +4.7V analog power supply |
| VD33ADC | 45 | PWR | +3.3V analog power supply for ADC |
| VD33DAC | 38 | PWR | +3.3V analog power supply for DAC |
| VD33PWM | 39 | PWR | +3.3V analog power supply for analog PWM |
| GND | 4,20,29 | GND | Digital ground |
| VS18PLL | 40 | GND | Analog ground for PLL |
| VS33ADC | 46 | GND | Analog ground for ADC |
| VS33DAC | 31 | GND | Analog ground for DAC |
| VS33PWM | 40 | GND | Analog ground for backlight inverter |
| **Output Interface Signals** | | | |
| VBFG | 41 | AO | Voltage reference output |
| IOR | 34 | AO | Channel R current output |
| IOG | 33 | AO | Channel G current output |
| IOB | 32 | AO | Channel B current output |
| CPH1 | 18 | DO | Output data clock |
| CPH2/sD0 | 21 | DO | Output data clock/the bit 0 of serial interfaced panel |
| CPH3/sD1 | 22 | DO | Output data clock/the bit 1 of serial interfaced panel |
| VSO/STH1 | 16 | DO | Vertical synchronization output signal. |
| HSO/POL | 14 | DO | Horizontal synchronization output signal.<br>XTCLKO strap |
| DEN/STH2 | 17 | DO | Horizontal data enable |
| **Timing Controller Interface Signals** | | | |
| UD | 22 | DO | Vertical Up/Down control |
| RL | 21 | DO | Horizontal Right/Left control |
| Q1H/sD2 | 23 | DO | Source Driver Q1H/the bit 2 of serial interfaced panel |
| LP/sD3 | 24 | DO | Latch pulse for source driver/the bit 3 of serial interfaced panel |
| GCLK/sD4 | 25 | DO | Gate driver clock/the bit 4 of serial interfaced panel |
| GOE/sD5 | 26 | DO | Gate driver output enable/the bit 5 of serial interfaced panel |
| STV1/sD6 | 27 | DO | Gate Driver start pulse/the bit 6 of serial interfaced panel |
| STV2/sD7 | 28 | DO | Gate Driver start pulse/the bit 7 of serial interfaced panel |
| VCOMAMP | 36 | AO | Analog VCOM amplitude |
| VCOMDC | 37 | AO | Analog VCOM DC offset |
| **2-wire serial bus Interface Signals** | | | |
| SCL | 8 | DI | 2-wire serial bus clock. Power down does not affect SCL. |
| SDA/IICA3 | 7 | I/O | 2-wire serial bus data. Power down does not affect SDA.<br>I2C slave strap 1 |
| **Configuration interface Signals** | | | |
| CPUINT | 9 | I/O | Internal Interrupt.<br>I2C slave strap 2 |

| Symbol | Pin # | Type | Description |
|---|---|---|---|
| RSTB | 6 | DI | Whole chip reset. (Internal Pull-up) |
| **ADC Interface** | | | |
| AY1 | 47 | AI | Analog input 1 of input channel 2 |
| AY0 | 48 | AI | Analog input 0 of input channel 2 |
| ACR1 | 1 | AI | Analog input 1 of input channel 1 |
| ACR0 | 2 | AI | Analog input 0 of input channel 1 |
| ACB1 | 3 | AI | Analog input 1 of input channel 3 |
| **PLL Reference Clock** | | | |
| XTALI | 10 | DI | Output PLL reference clock input |
| XTALO | 11 | DO | Output PLL reference clock output |
| XCLK2MC | 12 | DO | Buffered XTALI for external microprocessor. |
| **Power Management Interface Signals** | | | |
| PWM1 | 13 | DO | Pulse Width Modulation for volume/backlight control. |
| VFB | 41 | AO | Feedback of Lamp current |
| PWM_DC | 42 | AO | PWM output, connect to external N-channel power MOSFET |
| VFBL | 43 | AI | Feedback of Lamp current |
| PWM_LED | 44 | AO | PWM output, drive MOSFET switch |
| **Peripheral** | | | |
| GPO2~3 | 21, 22 | DI | General purpose digital output |

# 2 Electrical Characteristics

## 2.1 Digital I/O Pad Operation Condition

**Table 2-1 Operation Condition**

| | Parameter | Min | Typ | Max |
|---|---|---|---|---|
| VDD18 | Digital Core Power Supply | 1.62V | 1.8V | 1.98V |
| VD33 | Digital I/O Power Supply | 3.0V | 3.3V | 3.6V |
| $V_{IL}$ | Input Low Voltage | -0.3V | | 0.8V |
| $V_{IH}$ | Input High Voltage | 2.0V | | 5.0V |
| $V_{T+}$ | Schmitt Trigger Low-to-High Threshold | 1.44V | 1.58V | 1.71V |
| $V_{T+}$ | Schmitt Trigger High-to-Low Threshold | 1.09V | 1.19V | 1.31V |
| $I_I$ | Input Leakage Current@ $V_I$=3.3V or 0V | | | ±1μA |
| $I_{OZ}$ | Tri-state Output Leakage Current@ $V_o$=3.3V or 0V | | | ±1μA |
| $I_{OL}$ | Low level Output Current@ $V_{OL}$=0.4V | | | |
| | 2mA | 2.1mA | 3.4mA | 4.2mA |
| | 4mA | 4.2mA | 6.9mA | 8.6mA |
| | 8mA | 8.4mA | 13.9mA | 17.2mA |
| | 12mA | 12.5mA | 20.8mA | 25.8mA |
| $I_{OH}$ | High level Output Current@ $V_{OH}$=2.4V | | | |
| | 2mA | 3.0mA | 6.2mA | 10.0mA |
| | 4mA | 5.7mA | 11.6mA | 18.6mA |
| | 8mA | 9.5mA | 19.4mA | 30.9mA |
| | 12mA | 13.3mA | 27.1mA | 43.3mA |
| $R_{PU}$ | Pull-up resistor | 74KΩ | 104KΩ | 177KΩ |
| $R_{PD}$ | Pull-down resistor | 62KΩ | 90KΩ | 176KΩ |

Note: $R_{PU}$ and $R_{PD}$ are always present no matter normal operation or power down mode is enabled. A typical 30~40μA false leakage current is resulted from $R_{PU}$ and $R_{PD}$ when a tester forces I/O to 3.3V or 0.0 V.

## 2.2 DC Characteristics

( VDD18=1.8V; VD33=3.3V; AVDDR=AVDDG=AVDDB=AVDDP=AVDDAC=3.3V; VREF=1.235V; RL=37.5ohm, CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted )

**Table 2-2 DC Characteristics**

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating voltage range | AVDDR/G/B AVDDP AVDDAC VD33 | 3.0 | 3.3 | 3.6 | V | |
| Operating voltage range | VDD18 | 1.62 | 1.8 | 1.98 | V | |
| Operating voltage range | VD5A | 4.6 | 4.7 | 4.8 | V | |
| AVDDR supply current | IAVDDR | -- | 15 | 20 | mA | SL=0, SLR=0 |
| AVDDG supply current | IAVDDG | -- | 15 | 20 | mA | SL=0, SLG=0 |
| AVDDB supply current | IAVDDB | -- | 15 | 20 | mA | SL=0, SLB=0 |
| VD33 supply current | IVD33 | -- | 30 | 35 | mA | SL=0 |
| VDD18 supply current | IVDD18 | -- | 40 | 44 | mA | |
| VD5A supply current | IVD5A | -- | 30 | 33 | mA | |
| Full scale current | IOFS | 2.00 | 34.08 | -- | mA | Full-Scale adjust resistor. A resistor should be connected between this pin and AVS33 to control the magnitude of the full-scale video signal. RSET(ohm)=VREFIN(V)*10.66/IOFS(A) ,where IOFS is full-scale output current. |
| Output voltage range | V(IO) | -- | 4.0 | -- | V | . |
| DAC resolution | -- | -- | 8 | -- | bits | . |
| Integral non-linearity error | INL | -- | 0.5 | +-2 | LSB | . |
| Differential non-linearity error | DNL | -- | 0.5 | +-1 | LSB | . |

## 2.3 AC Characteristics

(VDD18=1.8V; VD33=3.3V; AVDDR=AVDDG=AVDDB=AVDDP=AVDDAC =3.3V; VREF=1.235V; RL=37.5ohm; CL=10pF; RSET=386ohm; Temp=75oC, unless otherwise noted)

**Table 2-3 AC Characteristics**

| Parameter | Sym | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| CK period | Tck | 5 | -- | -- | Ns | |
| CK to valid output | Tdelay | -- | -- | 0.5*Tck+2 | Ns | |
| Output rise time | Tr | -- | -- | 4 | Ns | 10% to 90% IOFS; assume no package inductance. |
| Output fall time | Tf | -- | -- | 4 | Ns | 90% to 10% IOFS; assume no package inductance. |
| Output settling time | Tsettle | -- | -- | TBD | Ns | assume no package inductance |
| Glitch energy | -- | -- | -- | -- | pvs | assume no package inductance |
| DAC to DAC crosstalk | -- | -- | TBD | -- | Db | . |

## 2.4 Analog Processing and A/D Converters

**Table 2-4 Analog Characteristics**

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Zi | Input impedance, analog video inputs | By design | 500 | | | kΩ |
| Ci | Input capacitance, analog video inputs | By design | | 10 | | pF |
| Vi(pp) | Input voltage range† | Ccoupling = 0.1µF | 0.7 | 1.0 | 1.3 | V |
| △G | Gain control range | | 0 | | 12 | dB |
| DNL | DC differential nonlinearity | A/D only | | ±0.5 | | LSB |
| INL | DC integral nonlinearity | A/D only | | ±1 | | LSB |
| Fr | Frequency response | 6 MHz | | −0.9 | | dB |
| | | | −3 | | | |
| SNR | Signal-to-noise ratio | 6 MHz, 1.0 Vp-p | | 50 | | dB |
| NS | Noise spectrum | 50% flat field | | 50 | | dB |
| DP | Differential phase | | 1.5 | | | |
| DG | Differential gain | | | 0.5% | | |

## 2.5 I²C Host Interface Timing

**Table 2-5 I²C Host Interface Timing**

| | Parameter | Min | Typ | Max |
|---|---|---|---|---|
| t1 | Bus free time between a Stop and Start condition | 4.7us | | |
| t2 | Hold time (repeated) Start condition | 4.0us | | |
| t3 | Rise time of both SDA and SCL | | | 1000ns |
| t4 | Data hold time | 5.0us | | |
| t5 | Data setup time | 250ns | | |
| t6 | Fall time of both SDA and SCL | | | 300ns |
| t7 | Setup time for a repeated Start condition | 4.7us | | |
| t8 | Setup time for Stop condition | 4.0us | | |
| tLow | Low period of the SCL | 4.7us | | |
| tHigh | High period of the SCL | 4.0us | | |
| fSCL | SCL clock frequency | | | 1Mhz |
| Cb | Capacitive load for each bus line | | | 400pF |

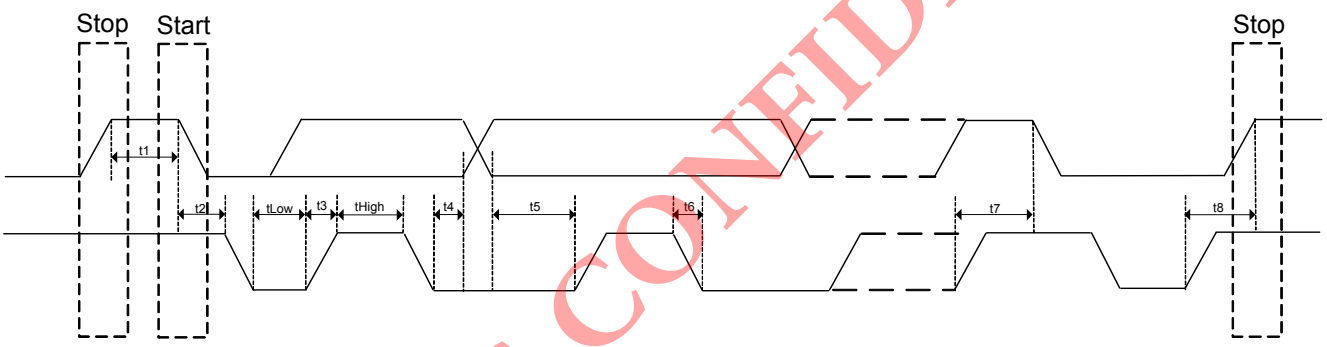
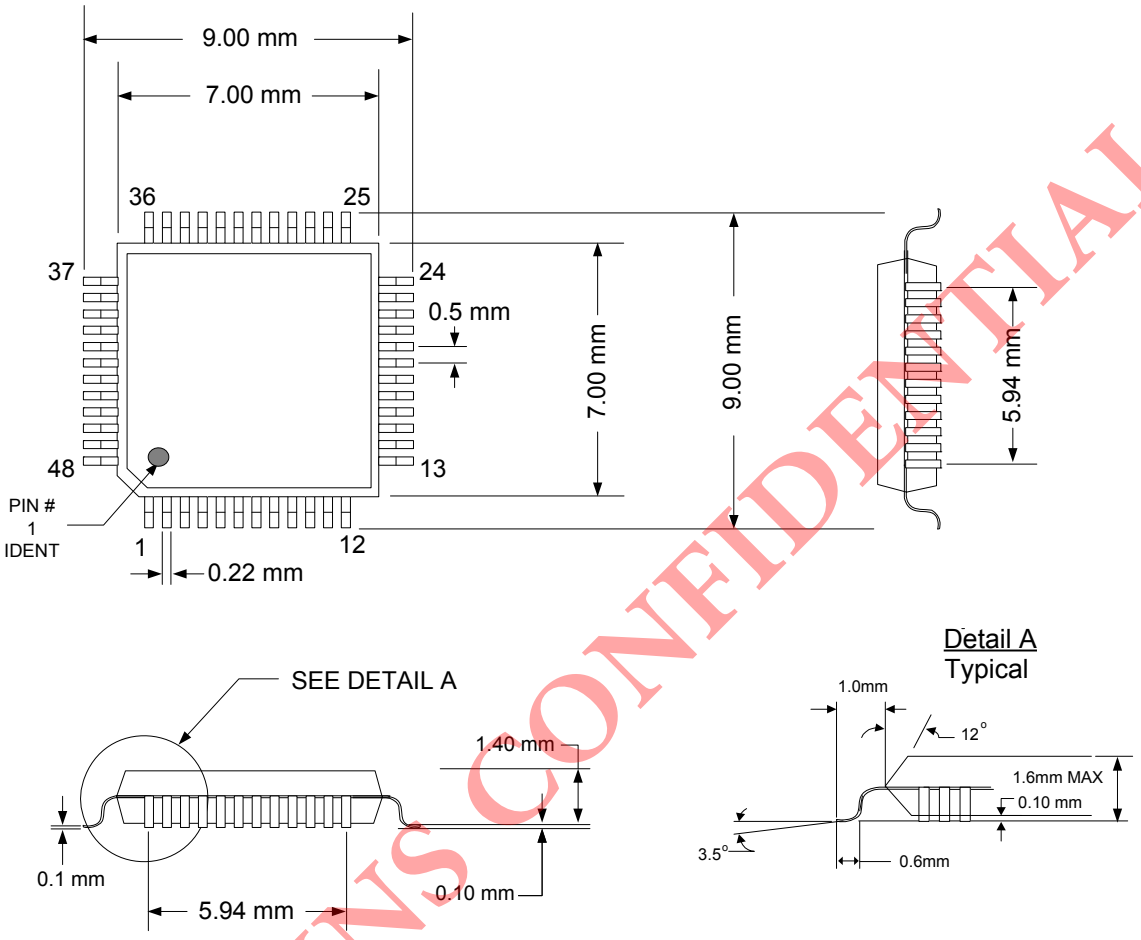



**Figure 2-1 I²C Timing**

# 3 Package Dimensions




**48 LQFP 7 X 7 X 1.5 mm**

**Figure 3-1 48-Pin LQFP Dimensions**

# 4 Ordering Information

**Table 4-1 Ordering Information**

| Part No. | Package |
|---|---|
| T118ES | 48 LQFP |

# 5 Revisions Note

**Table 5-1 Revision Note**

| Revisions | Description of changes | Date | Note |
|---|---|---|---|
| 0.1 | First draft | November 28, 2008 | |
| 1.00 | First release | May 12, 2009 | |
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# 6 General Disclaimer

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# 7 Contact Information

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