SS-HQ1 Application Notes

Sony Corporation
Semiconductor Solutions Network Company

CONTENTS

1. System Concept

1.1. Comparison of SS-HQ1 and SS-1M System Specifications

The SS-HQ1 system processes camera signals using a two-chip configuration consisting of a DSP (CXD3172AR) and a digital CCD camera head amp (CXA2096N).
The following table summarizes the major differences between the SS-HQ1 and the specifications for our SS-1M system, in which CXD2163BR is used as the DSP.

Table 1.1-1 Comparison of SS-HQ1 and SS-1M System Specifications

	SS-HQ1	SS-1M
Supported CCDs	510H, 760H	360H, 510H, 720H, 760H
System Configuration	2-chip configuration (AFE, DSP) TG, V-Dr, and EVR are built into DSP	3-chip configuration (AFE, TG/V-Dr, DSP) (separate EVR is required)
Package	LQFP 100pin	LQFP 100pin
Horizontal resolution	Excellent	Good
Blemish detection and compensation	Static & Dynamic detection, maximum 32 points	Compensation only, maximum 2 points (no detection)
Privacy masking	Up to 8 locations can be set	None
Mirror Function	○	None
Port Driver	16 ports	None
External synchronization	LL/VS/VBS/VRHR	LL/VS/VBS/VRHR
Pre-White Balance Adjustment	Semi-auto	Manual
Color rolling suppression	Excellent	None
Flickerless	Shutter fixing + AGC modulation	Shutter fixing only
System clock	1 clock permitted (contains digital chroma encoder)	2 clock inputs
Internal ADC	10bit	8bit
Analog Output	Composite video and Y/C component video both supported	Y/C component video only
Digital Output	Conforms to ITU-Rec.601 Conforms to ITU-Rec.656	Conforms to ITU-Rec.601
AWB control	Feed Forward method	Feed Back method
External LPF	Built into DSP (performance ensured without LPF)	Required

1.2. New Functions in SS-HQ1 System

The SS-HQ1 system contains the new functions listed in the following table.

Table 1.2-1 New Functions in SS-HQ1 System

New function	Basic description	Detailed description
High resolution mode	Improves horizontal resolution	Uses an aperture compensation generation block to provide high resolution within brightness signal processing
Color rolling-less mode	Color rolling suppression	Allows a color rolling-only operation frame to be set, in addition high precision, high speed operation control
MODESEL control	Automatic control of system-related parameters	Automatically changes parameters which have different settings depending on the particular clock system
Internal burst separator	Extracts burst signal for VBS Lock	Extracts a burst signal from an incoming VBS signal and outputs a phase comparison signal for burst PLL
OUTGAIN function	Simultaneously increases gain in chroma and brightness signals	Simultaneously increases gain in chroma and brightness signals using a single parameter (a single switch)

2. System Configuration

2.1. IC Configuration

The SS-HQ1 is the digital signal processing system for single CCD color camera.
The main LSIs are shown in **Table 2.1-1**.

Table 2.1-1 Main LSIs

Main LSIs	Type name	Outline	Package
DSP	CXD3172AR	1. Luminance and Chroma signal processing 2. Built-in digital encoder 3. Built-in microcontroller with AE/AWB 4. Built-in AE/AWB integral circuit 5. Built-in external synchronization function 6. Built-in 10bit A/D converter 7. Built-in 10bit D/A converter (Y/C 2ch) 8. Built-in PLL 9. Built-in Burst Separator and Sync Separator 10. Built-in EVR3ch 11. Built-in timing generator 12. Built-in vertical driver 13. Built-in serial communication circuit that supports RS-232C and microcomputer communication 14. Built-in ITU REC656 conformity digital output function 15. Built-in ITU REC601 conformity digital output function	LQFP 100 pin
CDS/AGC	CXA2096N	1. Correlated double sampling (CDS) 2. Built-in AGC circuit 3. Built-in interface circuit for A/D converter	SSOP 24 pin

*Please refer to the specification of each LSI about detail.

The peripheral ICs shown in **Table 2.1-2** are needed to configurate the system in addition to the above-mentioned 2LSIs.

Table 2.1-2 Peripheral ICs

Peripheral IC	Type name (Brand name)	Description	Package
EEPROM	AK6480AF (AKM) or BR9080AF-W (ROHM)	8kbit EEPROM (Note that other substitutions are not possible due to limitations in the communication format.)	SSOP 8pin
RS-232C Transceiver	MAX3232CSE (Considerable) (Maxim integrated Products, Inc.)	PC control I/F External u-Com I/F	SO 16pin
System Reset	PST9127N (Considerable) (MITSUMI ELECTRIC CO.,LTD)	Vth 2.7V	SOT-25 5pin

In SS-HQ1, 3ch EVRs are built-in in the camera DSP (CXD3172AR).
External EVRs shown in **Table 2.1-3** are possible to use as peripheral IC.

Table 2.1-3 Peripheral IC (External EVR)

Peripheral IC	Type name (Brand name)	Description	Package
External EVR	MB88347LPFV (Fujitsu Device Inc.)	8bit D/A Converter (built in 8sets) (Power supply : 3.3V)	SSOP 16pin

2.2. Clock Configuration

2.2.1. 1 clock / digital encoder system configuration

DSP can be operated by using only one clock in this system. The clock for driving system in DSP is generated by supplying the clock for encoder (ECK).

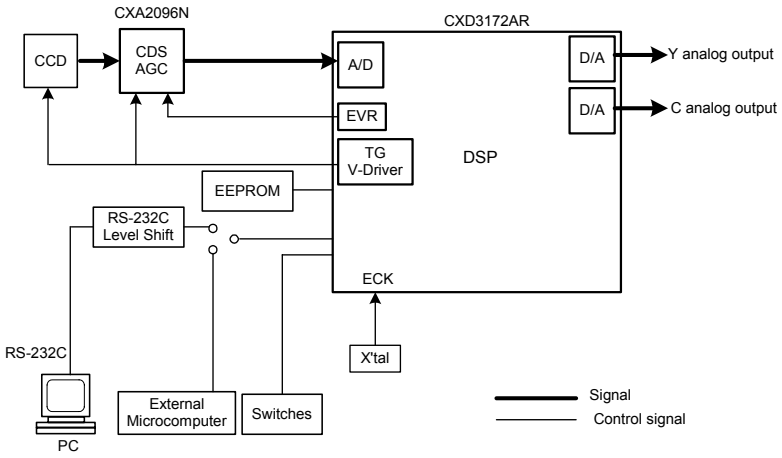


Fig 2.2-1 Signal path of 1 clock / digital encoder system configuration

2.2.2. 2 clock / ECK master - MCK PLL system configuration

DSP can be operated by using both the clock (ECK) which is for encoder oscillated by the crystal and the clock(MCK) which is for driving system oscillated by the PLL.

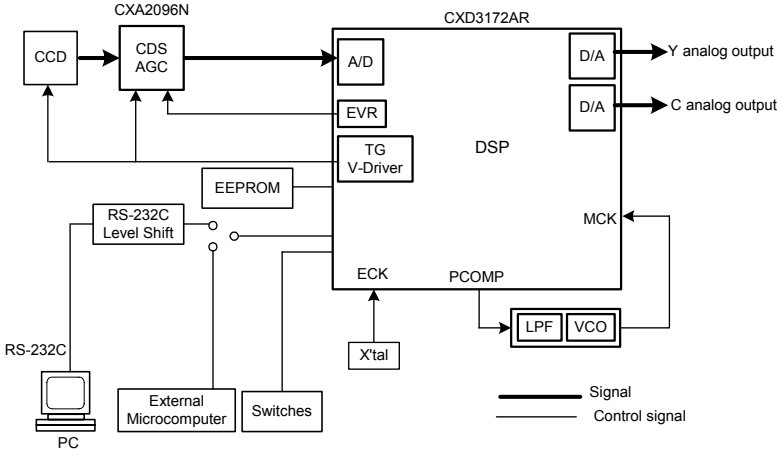


Fig 2.2-2 Signal path of 2 clock / ECK master - MCK PLL system

2.3. Output Configuration

2.3.1. Analog Composite (YCMIX) Output System Configuration

Analog composite (YCMIX) output is also possible in SS-HQ1.

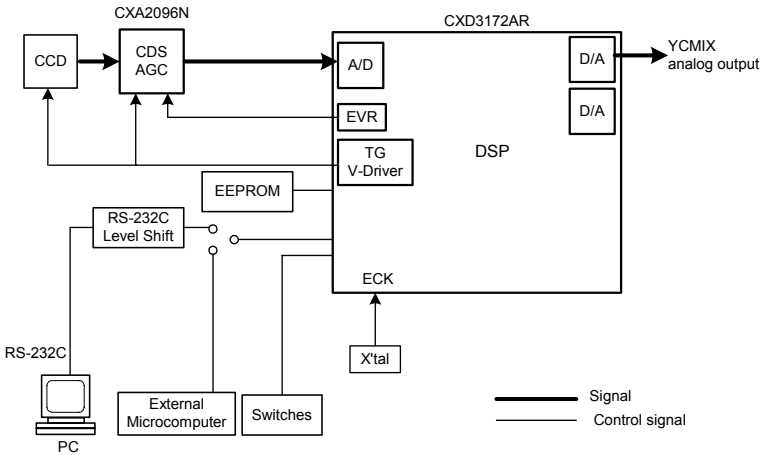


Fig 2.3-1 Signal Path of Analog Composite (YCMIX) Output System

2.3.2. Digital Output System Configuration (REC656, REC601)

SS-HQ1 has two digital output modes. One is the output which is compliant with ITU REC656. The other is the output which is compliant with ITU REC601.

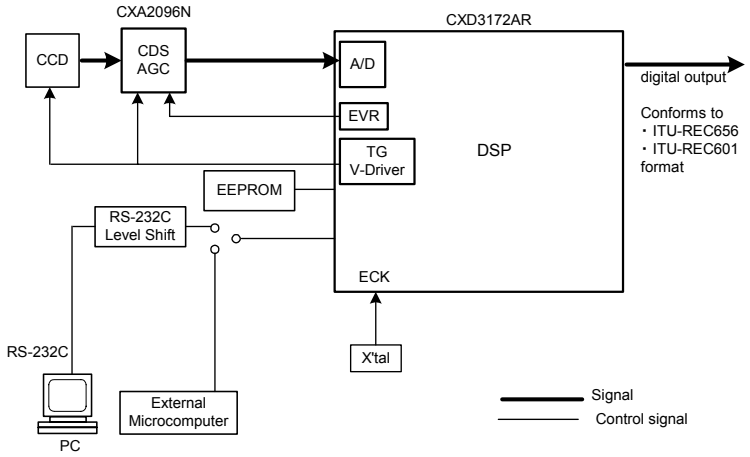


Fig 2.3-2 Signal Path of Digital Output System

3. Peripheral Circuits

3.1. Initially Occupied Terminals

3.1.1. If No Valid Data in EEPROM

If there is no valid data in EEPROM (AK6480AF or BR9080AF-W), data is read from internal memory of CXD3172AR. At this time parameters are assigned from CXD3172AR internal memory for the terminals indicated in the following table (the port driver). Thus, setup does not apply user-designated settings.

Table 3.1-1 Initially Occupied Terminals

Pin Name	Pin No	Parameter Name	Description
P0	91	AWBMODE	AWB operation mode switching
P1	92		
P2	93		
P3	94	CRLESSON	Switches anti-color rolling mode ON and OFF
P4	96	BLCOFF	Switches backlight compensation ON and OFF
P5	97	AEREF	Switches AE reference ON and OFF
P6	98	NORMFLC	Switches the flickerless function ON and OFF
P7	99	AGCMAX	Switches the AGC maximum value ON and OFF
P8	76	AEME	Switches between AE and ME
P9	77	AESHUT	Switches the electronic shutter fixed speed ON and OFF
P10	78	SGMODE0	Switches between INT and LL
P11	79	GAMSEL	Switches the gamma parameters
P12	80	MODESEL	DSP operation mode switching
P13	82		
P14	83		
P15	84		

3.2. Processing of Empty Pins

3.2.1. Processing of Empty Pins in Each Mode

Perform pin processing for the CXD3172AR depending on each mode as follows.

Table 3.2-1 Processing of Empty Pins in Each Mode

Pin Name	Pin No	Internal sync		External sync				Digital output
		1 clock digital encoder	2 clock ECK master MCK PLL	Line Lock	VS Lock	VBS Lock	VRHR	
TEST1	12	GND	GND	GND	GND	GND	GND	GND
PCOMP	42	OPEN	*	*	*	*	*	*
MCK	43	GND	*	*	*	*	*	*
S0	44	3.3V	3.3V	*	*	3.3V	*	*
S1	46	OPEN	OPEN	OPEN	*	OPEN	*	*
S2	47	OPEN	OPEN	OPEN	OPEN	*	*	OPEN
S3	48	OPEN	OPEN	OPEN	OPEN	*	OPEN	OPEN
PCK	51	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
VCTRLIN	53	GND	GND	GND	GND	GND	GND	GND
CPOUT	54	GND	GND	GND	GND	GND	GND	GND
EXVIDEOY	57	3.3V	3.3V	3.3V	*	*	3.3V	3.3V
EXVIDEO	58	3.3V	3.3V	3.3V	3.3V	*	3.3V	3.3V
TEST2	61	GND	GND	GND	GND	GND	GND	GND
TEST3	62	GND	GND	GND	GND	GND	GND	GND
DCK	90	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	*

* Terminals used in each mode (see separate explanation)

3.2.2. Processing of Empty Pins in case DAC is not used

When Y-DAC and C-DAC are not used by YCMIX output (DACMODE=0[h]), digital output, etc. Perform pin processing for the CXD3172AR as follows.

Table 3.2-2 Processing of Empty Pins in case C-DAC is not used

Pin Name	Pin No	When C-DAC is not used
IOC	67	3.3V
VGC	69	
VREFC	68	GND
IREFC	70	

Table 3.2-3 Processing of Empty Pins in case Y-DAC is not used

Pin Name	Pin No	When Y-DAC is not used
IOY	75	3.3V
VGY	72	
VREFY	73	GND
IREFY	71	

3.2.3. Processing of Empty Pins in case Internal EVR is not used

When Internal EVR are not used. Perform pin processing for the CXD3172AR as follows.

Table 3.2-4 Processing of Empty Pins in case Internal EVR is not used

Pin Name	Pin No	When Internal EVR is not used
EVR0	63	Connects with GND through 0.1uF capacitor.
EVR1	64	
EVR2	66	

3.2.4. Processing of the power supply Pins for analog cells

When an analog cell is not used. Perform Processing of the power supply Pin for analog cells as follows.

Table 3.2-5 Processing of the power supply Pins for analog cells

Pin Name	Pin No	When Analog Cells is not used
AVD4	55	3.3V
AVD5	56	
AVD6	74	
AVS4	52	GND
AVS5	59	
AVS6	65	

3.3. Oscillator Circuit Periphery

3.3.1. Clock oscillator circuit for 1 clock/digital encoder system

Providing an encoder clock (ECK) for the CXD3172AR enables internal generation in the CXD3172AR of the clock that drives the system.

Fig 3.3-1 shows the composition of an oscillator circuit using X'tal.

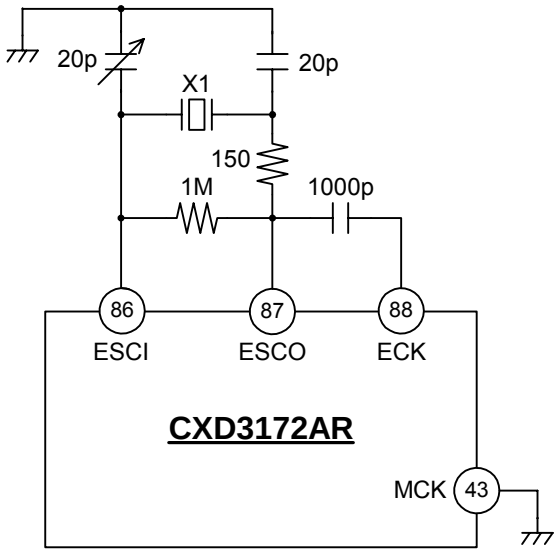


Fig 3.3-1 X'tal Oscillator Circuit Configuration (Evaluation Board)

Table 3.3-1 X'tal Oscillating Frequency

Number of pixels	TV System	X1
510H	NTSC	38.13986MHz
	PAL	37.87500MHz
760H	NTSC	28.63636MHz
	PAL	28.37500MHz

3.3.2. Clock oscillator circuit for 2 clock/ECK master MCK PLL

Operate the CXD3172AR with two clocks: the encoder clock (ECK), oscillated by X'tal, and the driving system clock (MCK), oscillated by PLL.

Fig 3.3-2 shows the configuration and evaluation board circuit constants (**Table 3.3-2**) for a clock oscillator circuit for MCK PLL using X'tal.

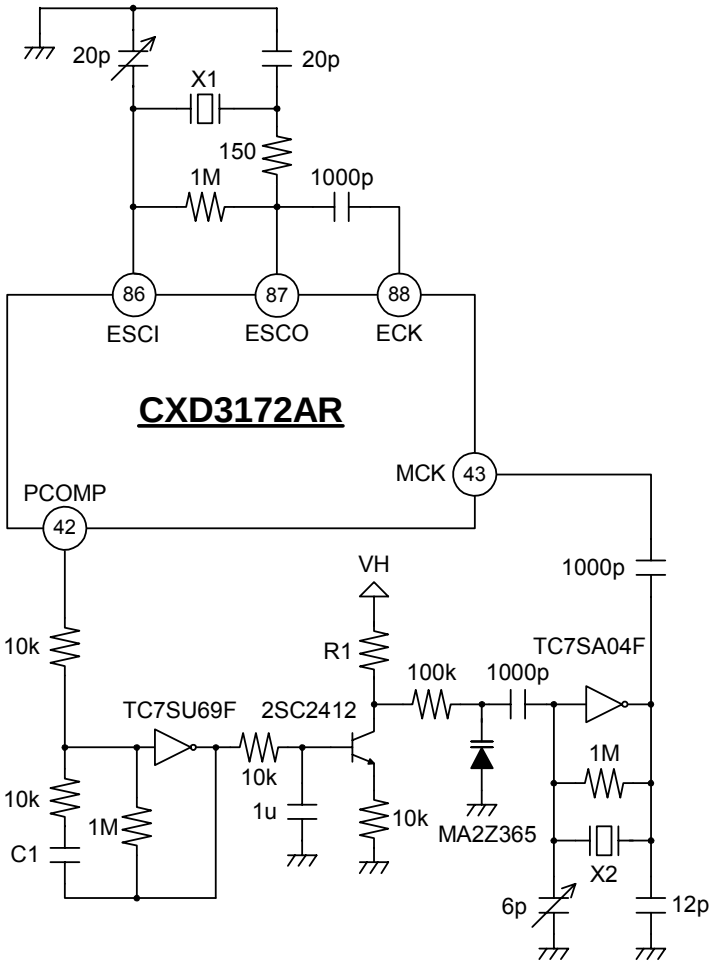


Fig 3.3-2 Configuration of Clock Oscillator Circuit for 2 Clock /ECK Master MCK PLL Using X'tal Oscillation

Table 3.3-2 Evaluation Board Circuit Constants

TV System	X1	R1		C1
		VH=15V	VH=12V	
NTSC	See **Table 3.3-1**	56k	47k	0.01uF
PAL				1uF

Fig 3.3-3 shows the configuration and evaluation board circuit constants (**Table 3.3-3**) for a clock oscillator circuit for MCK PLL using LC.

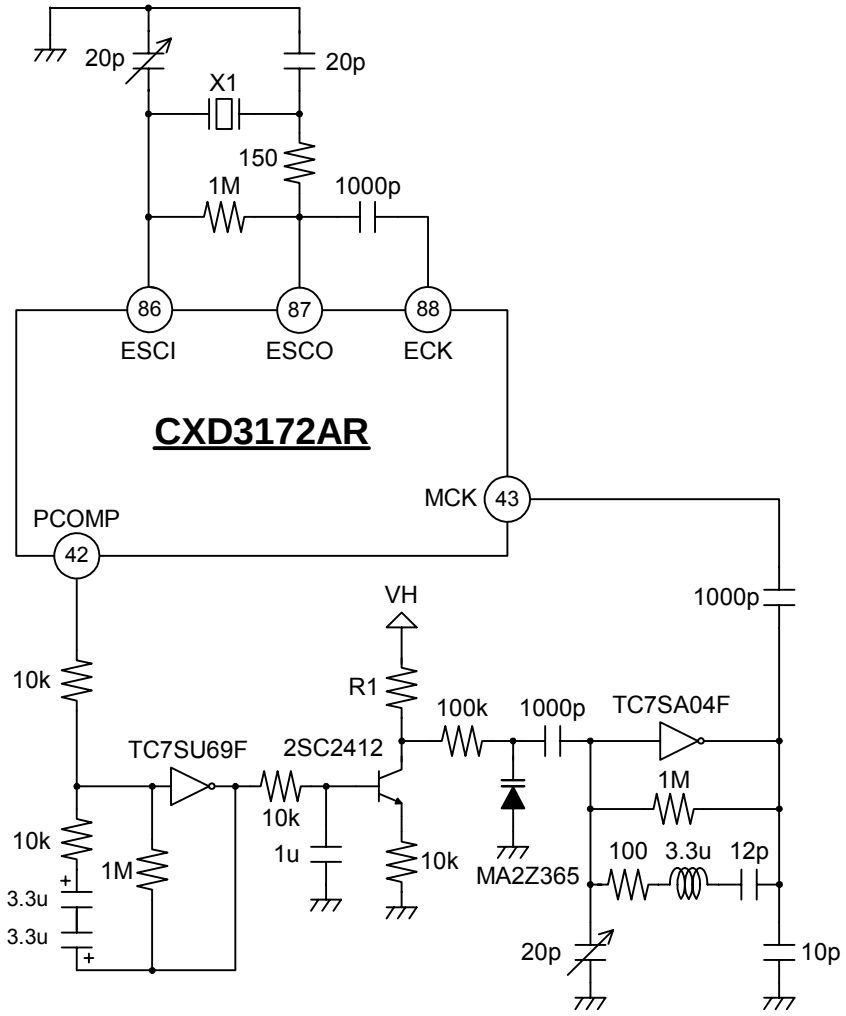


Fig 3.3-3 Configuration of Clock Oscillator Circuit for 2 Clock /ECK Master MCK PLL Using LC Oscillation

Table 3.3-3 Evaluation Board Circuit Constants

TV System	R1	
	VH=15V	VH=12V
NTSC	56k	47k
PAL		

These three figures give examples of oscillator circuits introduced with the SS-HQ1 evaluation board: **Fig 3.3-1**, **Fig 3.3-2**, and **Fig 3.3-3**. The circuit constants presented here has been verified in operation using a Sony evaluation board equipped with the crystal oscillator shown in **Table 3.3-4**. Understand that no performance guarantee is implied for different board layouts, component selection, or temperature characteristics.
For VCO circuits, LC and X'tal oscillation circuits are available. Choose the one that suits your application.

Table 3.3-4 Components Used on the Evaluation Board

Component name	Manufacturer	Model	Frequency	Load capacitance
Crystal oscillator	RIVER ELETEC CORPORATION	HC-49/U03	28.63636MHz	12pF
			28.37500MHz	
			38.13986MHz	
			37.87500MHz	
Variable capacitance diode	Panasonic	MA2Z365	-	* 3.4pF to 36pF

*: The diode capacity is the minimum value when 17V to 2V reverse voltage is applied.

3.4. Reset Circuit

3.4.1. Outline

This circuit performs system reset to enable stable operation when the CXD3172AR and peripheral ICs start up after power is supplied.
However, problems may also be caused by a transient power supply. For a reliable way to avoid such problems, add a circuit that meets the following conditions.

3.4.2. Example Circuit and Timing Chart

The sample reset circuit is shown in "**Fig 3.4-1** Example Reset Circuit," and the timing chart is shown in **Fig 3.4-2**.
If the 3.3V voltage supply surges to exceed 2.7V after power is supplied or other events, set the CXD3172AR XRST terminal to Low (at least 500ns) and be sure to reset it. Additionally, if the 3.3V power supply falls under 2.7V, set the XRST terminal to Low and be sure to reset it.
* The guaranteed voltage for DSP operation is 3.0 to 3.6V. For details refer to the product specifications.

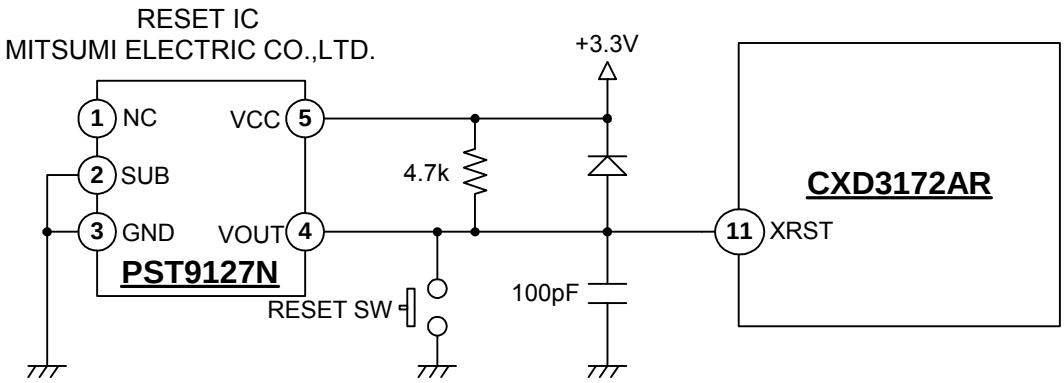


Fig 3.4-1 Example Reset Circuit

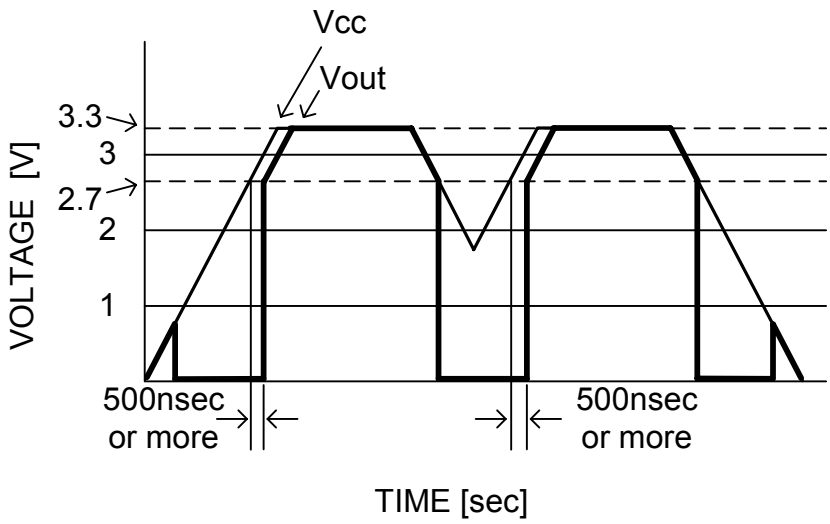


Fig 3.4-2 Timing Chart

3.4.3. ICs Requiring Reset after Power-On

Of the ICs used by the SS-HQ1 system, only CXD3172AR must be reset.

3.5. EVR Connection

3.5.1. Integrated EVR and Reserved Channels (AGC control)

The CXD3172AR is equipped with a 3-channel, 8-bit D/A converter (EVR).
It can produce nearly linear voltage up to approximately 0V-3.3V.

Table 3.5-1 System Configuration of Integrated EVR

ch	Pin	Parameter		Control details	Control method
EVR0	63	AGCCNT	CAT8_Byte3_bit0-7	AGC gain control	Field-controlled User-adjusted
EVR1	64	IRISVCNT	CAT8_Byte4_bit0-7	Control parameter value of EVR1	User-adjusted
EVR2	66	EVR2CNT	CAT8_Byte5_bit0-7	Control parameter value of EVR2	User-adjusted

We recommend connecting EVR0 (Pin 63) to AGCCONT (Pin 14) of the CXA2096N unless an external microcomputer or other means is used for AGC because AGC of the CXA2096N is performed by the CXD3172AR firmware. EVR0 output can be controlled on a per-field basis.
EVR1 and EVR2 (Pins 64 and 66, respectively) are not controlled by the firmware.

The output value of the integrated EVR is as follows. (This is a reference value.)

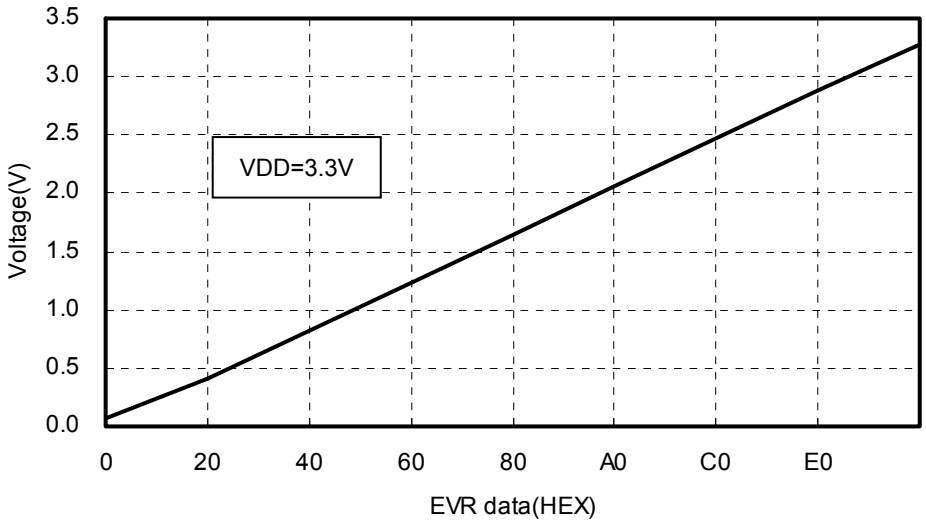


Fig 3.5-1 Measured EVR Output Value (Reference Value)

EVR0 can be controlled by means of the user settings shown in Table 3.5-2 Integrated EVR User Settings without relying on firmware control. These are also the user settings for EVR1.

Table 3.5-2 Integrated EVR User Settings

ch	Parameter		Setting value
EVR0	AEHOLD	CAT12_Byte5_bit2	1[h]:AE HOLD
EVR1	MIRIS	CAT14_Byte1_bit1	0[h]:Mechanical IRIS control OFF
EVR2	Always the user setting		

If no control is needed, any suitable setting values can be designated in each channel parameter, or the channels can be set to standby. If channels are set for standby as shown in Table 3.5-3 Integrated EVR Standby Settings the each channel state will be undefined.
However, even when not using integrated EVR, a power supply is supplied to the power supply terminal AVD6 (74pin). AVD6 serves as a D/A converter and a common power supply.

Table 3.5-3 Integrated EVR Standby Settings

ch	Parameter		Setting value
EVR0	EVR0STB	CAT8_Byte2_bit5	0[h]: EVR control 1[h]: EVR standby
EVR1	EVR1STB	CAT8_Byte2_bit6	
EVR2	EVR2STB	CAT8_Byte2_bit7	

3.5.2. Communication Control with an External EVR

External EVR Connection

As for external EVRs, the CXD3172AR can be connected to the Fujitsu MB88347L.
External EVRs enable control of eight channels through the following parameters. Note that each parameter controls specific pins, so be sure to refer to the following settings if an external EVR is used.

Table 3.5-4 External EVR Configuration

MB88347L output		Parameter		Control details	Data transmission timing
Pin Name	Pin				
AO1	15	EVRUSR0	CAT18_Byte8_bit0-7	User-adjustable value, 0h-FFh	Output from each field
AO2	2	EVRUSR1	CAT18_Byte9_bit0-7		
AO3	3	EVRUSR2	CAT18_Byte10_bit0-7		
AO4	4	EVRUSR3	CAT18_Byte11_bit0-7		
AO5	5	EVRUSR4	CAT18_Byte12_bit0-7		Output from groups of four fields
AO6	6	EVRUSR5	CAT18_Byte13_bit0-7		
AO7	7	EVRUSR6	CAT18_Byte14_bit0-7		
AO8	10	EVRUSR7	CAT18_Byte15_bit0-7		

External EVR Communication Control

Each field is used in communication between the CXD3172AR and an external EVR (MB88347L).
Send setting values in parameters EVREUSR0-7 as shown in Table 3.5-4 External EVR Configuration to have them applied to the MB88347L output voltage.
The timing of transmissions from the CXD3172AR to the MB88347L varies depending on the EVR pin. Communication to AO1-AO4 is on a per-field basis, but to AO5-AO8, transmissions rotate among individual fields or are sent to groups of four fields.

External EVR Chip Selection Pin Connection

Chip selection signal output from the CXD3172AR of the external EVR offers control through connection to one of the following pins depending on the CSEVRSEL parameter setting. Initial setting is CSEVRSEL=0[h] and a chip selection signal is outputted from pin S4.

Table 3.5-5 External EVR Chip Selection Pin Connection Settings

CSEVRSEL (CAT12_Byte10_bit1)	Chip Selection signal output pin		Parameter setting		Setting value
0[h]	S4	49pin	S4SEL	CAT1_Byte8_bit6-7	0[h]
1[h]	P3	94pin	-	-	-

Multiple signals can be sent from pin S4, so additional parameter settings besides CSEVRSEL are required. To send the chip selection signal, use the settings shown in the above table.
For output from pin P3, making CSEVRSEL=1[h] will send the chip selection signal. Thus, other parameter settings are not required.

However, note that the following limitations apply for chip selection signal output from pin P3.

1. Pin P3 cannot be used for port driver functions.
2. The parameter settings are enabled only after the device is reset.

3.6. Noise Countermeasures

3.6.1. Introduction

Important Information for Mounting

We recommend a board design of four layers or more to reduce as much noise as possible at the stage of board design.

Ensure that ground connections are done properly. In addition to employing a multilayer board design, use a ground plane or other means to minimize ground impedance. Employ sufficient noise countermeasures with respect to signal separation, such as using a ground layer.

The CXD3172AR uses a mixed power supply consisting of digital (VDD and VSS) and analog (AVD and AVS) power supplies. Regarding the digital and analog pattern configuration of multilayer boards, it makes no difference in the effect on noise whether the power supply (for VDD and AVD) is separate or together. However, better noise resistance has been verified on evaluation boards with pattern configurations featuring a common ground (VSS and AVS) instead of separate grounds.

Unused input pins should be pulled up or down as necessary. For details on pin processing, refer to the Empty Pin processing shown in "3.2.1 Processing of Empty Pins in Each Mode".

Care should be taken in the component layout and wiring because the CXD3172AR includes several analog cells (for A/D, D/A, EVR, and other functions). In particular, do not arrange the oscillator for the encode clock (connected to ESCI, ESCO, and ECK - pins 86, 87, and 88, respectively) or the pattern route near the pins or pattern used for the analog cell. This may cause noise, so position the oscillator as close as possible to the ESCI, ESCO, and ECK pins.

For systems spanning multiple camera boards, we recommend arranging the three chips (CCD, CXA2096N, and CXD3172AR) on the same board if possible.

Disadvantages of Multiple Boards

If the CCD and CXD3172AR are on separate boards, connectors and the like increase the H1, H2, and RG loads, which pose a risk that the conditions for driving the CCD may not be met. This may also increase CXD3172AR power consumption. For separate boards, set the parameters to adjust drivability, delay, and duty to match the drive clock waveform conditions of your CCD. For details on the parameter settings for adjusting drivability, delay, and duty, sees 11.3, "Adjustment of TG Phase."

Special care is needed if the CCD and CXA2096N are on separate boards because this lengthens the CCD output signal line, making it more susceptible to noise from nearby circuits.

Arranging the CXA2096N and CXD3172AR on separate boards also increases loads of PBLK, CLPOB, XSHP, XSHD, XRS, and CLPDM. This poses a risk that the conditions for driving the CXA2096N may not be met.

3.6.2. Countermeasures for Areas around Individual Devices

Countermeasures for the CCD and Surrounding Areas

1. To prevent noise from entering the CCD, be sure the ground pattern is sufficient and connect individual LC filters to power supply pins VDD (+15V or +12V) and VL (-5.0V or -7.0V) to keep the power supply separate from other circuits.

2. Noise may be generated if ringing is observed in the waveform of reset gate (RG) clock input, or if overshoot or undershoot is observed in the waveform of horizontal register transfer clock input (H1 and H2). To deal with it, insert a damping resistance of approximately 100 ohms in the signal line for waveform adjustment.

3. In addition, be sure to connect a buffering transistor near the CCD signal output (VOUT) because it is susceptible to noise and has low load driving capability.

4. For details, see the CCD data sheet and application circuit diagrams.

Countermeasures for the CXA2096N and Surrounding Areas

1. For the power supply of VCC (pins 5, 16, and 23), connect LC filters to prevent crosstalk from other circuits causing interference. Additionally, connect bypass capacitors between each pin and ground.

2. PIN and DIN (pins 21 and 22) are input pins for the CCD signal, so make the signal lines from the CCD as short as possible and surround them with a ground shield.

3. VRB and VRT (pins 7 and 8) are output pins for ADC reference voltage. Be sure to connect a bypass capacitor near them because they are susceptible to noise.
   We recommend connecting the capacitance of around 4.7 uF and around 0.1 uF in parallel.

4. To reduce horizontal clamp noise, increase the capacitance of the capacitor between AGCCLP (pin 13) and the ground. However, caution is advisable because excessive capacitance may cause slower startup and impair clamp operation. We recommend a capacitance of around 0.1 uF.

5. XRS, SHP, and SHD (pins 11, 17, and 18, respectively) are input pins for sample hold. Noise may be generated if overshoot or undershoot is observed in the waveform. To deal with it, insert a damping resistance of approximately 100 ohms in the signal lines for waveform adjustment.

Countermeasures for the CXD3172AR and Surrounding Areas

1. For the power supply of AVD 1-6 (pins 2, 21, 29, 55, 56, and 74) and SVD 1 and 2 (pins 50 and 100), connect LC filters by the source to prevent crosstalk from other circuits causing interference. Additionally, connect bypass capacitors between each power supply pin and ground.

2. For the power supply of VDD, connect LC filters by the source to prevent crosstalk from other circuits causing interference. Additionally, VDD1 (pin14), VDD2 (pin45), and VDD4 (pin95) which are a power supply are unified to the same VDD as noise countermeasures. (See the application circuit diagram.) Additionally, connect bypass capacitors between each pin and ground.

3. VRT, VIN, and VRB (pins 1, 3, and 5, respectively) are ADC input pins, so make their signal lines with the CXA2096N as short as possible. Noise may be generated if these ADC patterns are too close to a high-speed pulse (H1, H2, RG, XSHP, XSHD, or XSR), oscillator or oscillator circuit pattern, so be sure to take this into consideration during layout design.

4. RG, H1, and H2 (pins 19, 22, and 23, respectively) are output pins for the reset gate pulse and horizontal register transfer pulse. If there is overshoot or undershoot in the waveform, it may cause noise. To deal with it, insert a serial resistance of approximately 100 ohms for each. Additionally, set the parameters to adjust waveform duty, delay, and drivability to match the waveform conditions of the clock driving the CCD.
   If connectors are used in the connection with the CCD element, use a ground shield between signals to prevent signal degradation. For the connectors, provide many ground pins to strengthen the earth coupling.
   Furthermore, shorten the H1 and H2 wiring length between ICs as much as possible. Before use, make sure that the H1 and H2 amplitudes conform to the CCD specifications.

5. XSHP, XSHD, and XRS (pins 28, 27, and 25, respectively) are output pins for sample hold pulse to the CXA2096N. If there is overshoot or undershoot in the waveform, it may cause noise. To deal with it, insert a serial resistance of approximately 100 ohms for each. Additionally, set the parameters to adjust duty, delay, and drivability so that the sample hold waveform matches the CCD input waveform.
   Arrange the CXD2096N and CCD element on the same board if possible. Use a ground shield between signals to prevent signal degradation.
   If separate boards are used, provide many connector ground pins to strengthen the earth coupling as an additional countermeasure.

6. If PLL (the phase comparator) is used by means of phase comparator output PCOMP (pin 42) and system drive clock input MCK (pin 43), make the signal line of the PLL oscillator circuit as short as possible and surround it with a ground shield to make it less susceptible to nearby circuits.
   We also recommend positioning the PLL oscillator circuit and the board's inner layer away from other circuits and removing the board's inner layer pattern so they are not affected by floating capacitance.

7. For a two-clock system configuration, design the layout to ensure separation of the oscillator circuits that generate the clocks for input to the encoder clock input pin ECK (pin 88) and system drive clock input pin MCK (pin 43). Arrange them as close as possible to each pin. Noise may occur if the clocks interfere with each other.

8. EVR 0-2 (pins 63, 64, and 66, respectively) are DAC output pins. Connect a bypass capacitor of approximately 0.1 uF between each pin and ground.

9. IOC and IOY (pins 67 and 75) are analog output pins. Separating them too much makes them more susceptible to noise, so keep the wiring as short as possible. Ensure that these lines are designed not to cross the pattern of AVD, VG, IREF, or VREF.
   VGC and VGY (pins 69 and 72) are pins for connection with a capacitor for DAC. Connect a bypass capacitor of approximately 0.1 uF between each pin and ground.

10. ECK (pin 88) is an input pin for the encoder clock, that is, for X'tal oscillator input. Make the signal line as short as possible and surround it with a ground shield so that it will not be affected by nearby circuits. We also recommend positioning X'tal components and the board's inner layer away from other circuits and removing the board's inner layer pattern so they are not affected by floating capacitance. Additionally, ESCI and ESCO (pins 86 and 87) are I/O pins for the CXD3172AR's internal oscillator cell. We recommend designing the configuration so that these pins are used in the oscillator circuit of the clock providing input to ECK. If the clock sent to ECK is generated by external means such as an inverter, it enlarges the oscillator circuit, so nearby circuits may be affected by noise.

11. If pins 0-15 are used for digital output, make the signal lines as short as possible so that the surrounding analog circuits will not be affected by noise. Cover the surrounding area with a ground shield to separate the signal lines from analog circuits.

3.6.3. If Noise Occurs

If noise on the screen from in the designed board is confirmed, identify the source of the noise before taking appropriate measures. Means of identifying noise sources are described below.
One method that simplifies checking how noise is generated is to block the lens and set AGC to maximum that is, set AGCMAX (CAT14_Byte1_bit4) to 1. This makes investigating noise easier.

1. Using the pattern generator function
   The pattern generator (PG) function inserts a generated signal immediately after the CXD3172AR's internal A/D signal input area. This pattern generator can be used to identify the general area where the noise is occurring.
   If the noise is eliminated when the pattern generator is displayed, then the noise is occurring on the portion from the CCD to the CXA2096N or on the front end of the CXD3172AR. If the noise remains, it may be occurring at a later point (including the CXD3172AR).

2. Separating ECK
   ECK (pin 88) is an input pin for the encoder clock. Depending on the layout of the X'tal oscillator connected to this pin, the oscillator clock may become mixed in signal lines and generate noise on the screen.
   If so, remove the X'tal and connect the input side (ESCI, pin 86) of the DSP's internal inverter to the ground. In this state send the clock from an external source to ECK. If the noise is eliminated, the cause of noise is the X'tal oscillator layout or the pattern design of another signal line.

3. Separating VIN
   VIN (pin 3) is an input pin for ADC analog signals. Separate this pin from the CXA2096N and connect it to a stabilization DC power supply to check for noise on the screen. If the noise is eliminated, it may be occurring at a source closer to the front end than the CXA2096N (including the CCD) before it enters the CXD3172AR. If the noise remains the cause may be back-end sites, including the CXD3172AR.

4. Eliminating the PLL loop
   The PLL circuit, which inputs the clock in MCK (pin 43), performs feedback control to maintain a constant phase in the oscillating circuit. If noise enters the PLL circuit control signal, the noise appears on screen. In MCK, the PLL oscillator circuit input pin, supply a signal of a fixed wavelength (such as the X'tal's) that does not use PLL. Check if the noise is eliminated. If it is, the cause of noise is the layout or pattern design of circuits around PLL.

5. Separating the power supplies
   It is difficult to identify sources of noise propagating over power lines. Therefore, disconnect the primary circuit and IC power supplies. Supply power from a clean external source to identify the point where the noise is eliminated.

3.7. External LPF

3.7.1. Outline

The CXD3172AR contains an LPF with improved characteristics, so sufficient performance can be obtained even if an LPF is not connected to the luminance signal output pin IOY (pin 75).

3.7.2. High Resolution and LPF

The characteristics of the CXD3172AR's internal LPF have been improved, so high resolution can be obtained without connecting an external LPF. Conversely, connecting an external LPF makes it impossible to obtain high resolution due to attenuation of the luminance signal.

3.8. Example Characteristics and Circuit for External BPF

3.8.1. Outline

In cases where the CXD3172AR's chroma signal output pin IOC (Pin 67) is used, add a band-pass filter circuit to ensure that signal components other than the sub-carrier component are removed. This circuit also shapes the sub-carrier signal, in which digital components remain, into a sine wave.

3.8.2. BPF Circuit Example

Fig 3.8-1 indicates BPF Circuit Example.

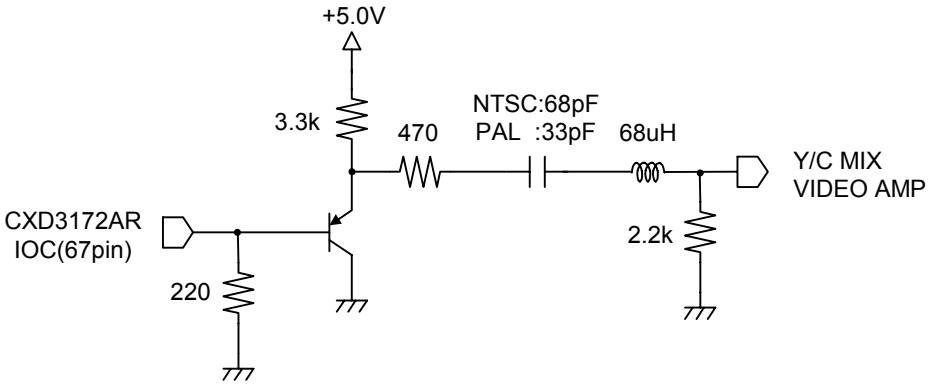


Fig 3.8-1 BPF Circuit Example

3.8.3. Example BPF Characteristics

The following graph shows example characteristics measured on an evaluation board using the BPF formed in **Fig 3.8-1**.

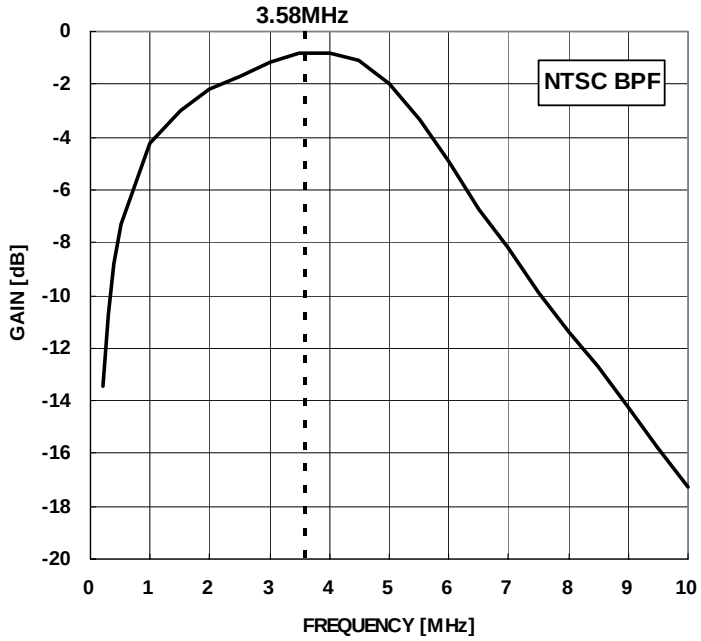


Fig 3.8-2 Example BPF Frequency Characteristics (NTSC)

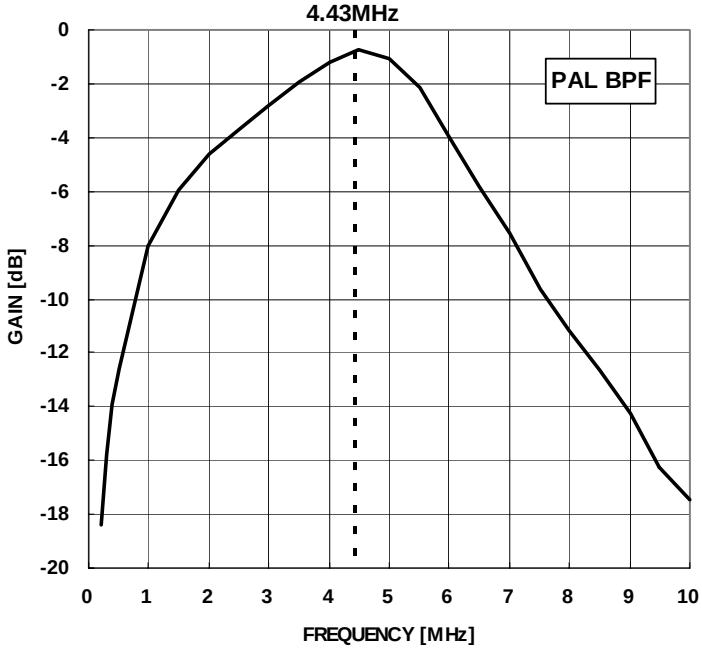


Fig 3.8-3 Example BPF Frequency Characteristics (PAL)

3.9. DAC Mode and YC-mix External Analog Circuit

3.9.1. DAC Mode

Either composite signal output or component signal output can be selected as the analog signal output method for output from the CXD3172AR. Refer to **Table 3.9-1** below to set the appropriate setting for the output method you want to use. It is not necessary to connect an external LPF in either case.

Table 3.9-1 DAC Mode Selection Method

Parameter		Setting value	Description	
			DAC1 *	DAC2 *
DACMODE	CAT1_Byte3_bit2	0[h]	Composite output	Not used
		1[h]	Component Y output	Component C output

* DAC1: IOY, VREFY, VGY, IREFY
DAC2: IOC, VREFC, VGC, IREFC

3.9.2. Circuit Configuration for Component Output

When component output is used (DACMODE=1[h]), the CXD3172AR's internal DAC (2ch) outputs Y/C signals through the IOY pin (pin 75) and IOC pin (pin 67), respectively. **Fig 3.9-1** illustrates an example circuit for component output.

The signal level output from the IOY/IOC pins changes depending on the setting for the voltage being input to the VREFY/VREFC pins. Input and adjust the voltage as appropriate.

Note that the voltage input to the VREFY/VREFC pins must be in the range of 0.6 to 1.1V based on the specifications for the CXD3172AR's internal DAC. Therefore, use a configuration in which an amplifier circuit is placed in the final stage. Note that proper operations cannot be guaranteed if the voltage is input using any other type of configuration.

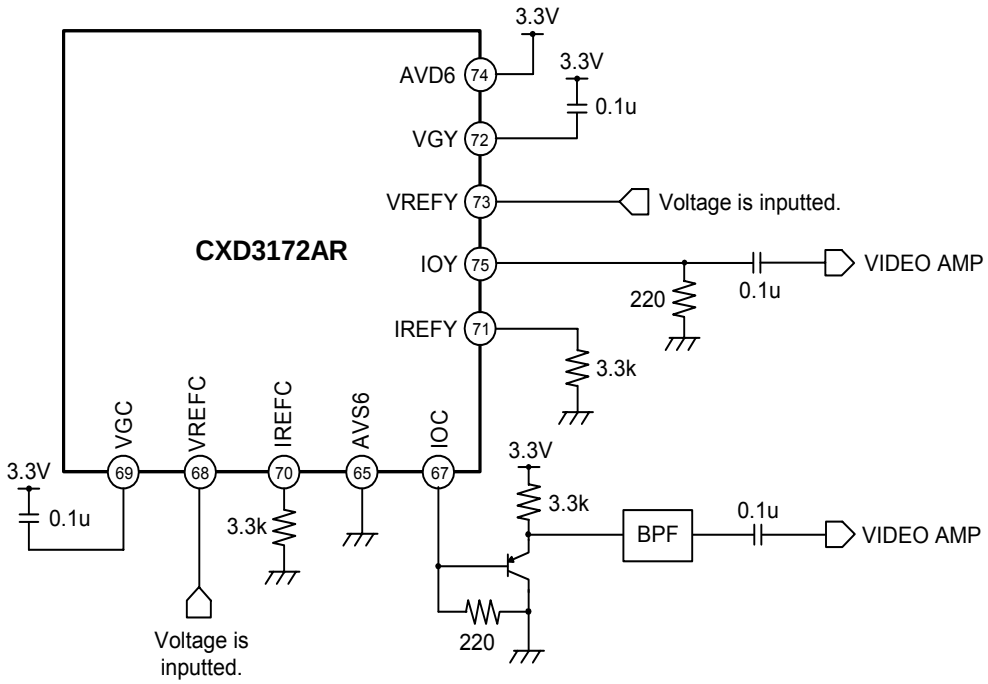


Fig 3.9-1 Example Circuit for Component Output

3.9.3. Circuit Configuration for Composite Output

When composite output is used (DACMODE=0[h]), the Y/Composite signals are mixed inside the CXD3172AR and output through the IOY pin (pin 75). With this configuration, the IOC pin (pin 67) is not used. **Fig 3.9-2** illustrates an example circuit for composite output.
Note that with composite output, it is not possible to completely remove the digital components of the sub-carrier signal because a BPF is not connected.

The signal level output from the IOY pin changes depending on the setting for the voltage being input to the VREFY pin. Input and adjust the voltage as appropriate.
Note that the voltage input to the VREFY pin must be in the range of 0.6 to 1.1V based on the specifications for the CXD3172AR's internal DAC. Therefore, use a configuration in which an amplifier circuit is placed in the final stage. Note that proper operations cannot be guaranteed if the voltage is input using any other type of configuration.

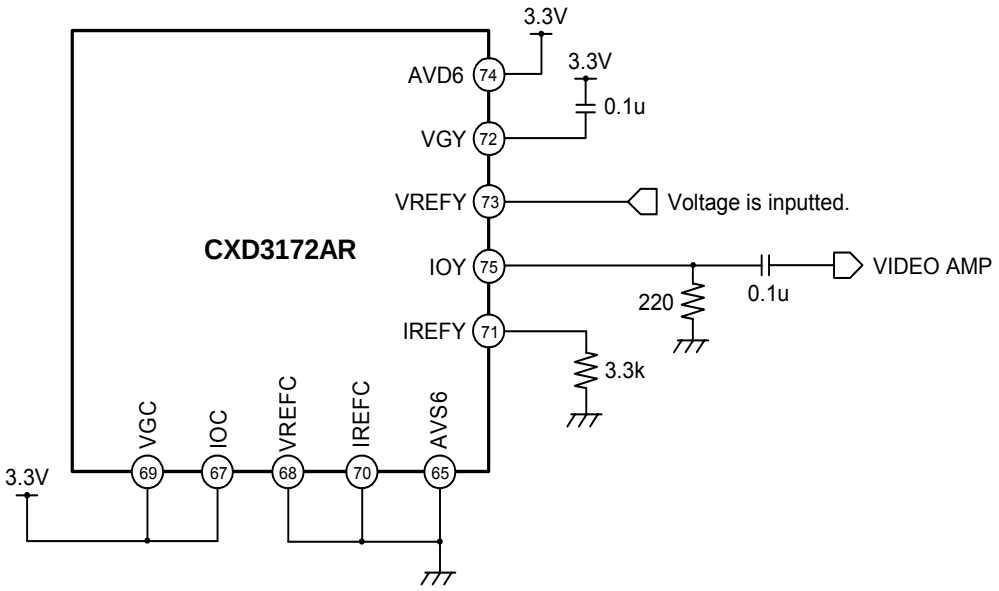


Fig 3.9-2 Example Circuit for Composite Output

3.10. Optical Filters

3.10.1. Outline

When a subject with a high spatial frequency is shot using a color camera containing CCDs, a moiré effect (false signal) occurs. In order to suppress this moiré effect (false signal), always use an optical low pass filter (optical LPF) which matches the type of CCD being used.
Note that an optical LPF is required even when using high resolution.

Table 3.10-1 summarizes the optical LPFs used with our evaluation board for your reference.

Table 3.10-1 CCD Types and Optical LPF Model Numbers

CCD Type	Optical size	Optical LPF Model Number
510H	1/3”	* SV-T634A
	1/4”	* SV-T635A
760 H	1/3”	* SV-T636AS
	1/4”	* SV-T618S

(* made by KYOCERA KINSEKI Corporation)

Sony uses the optical LPFs (three-layer configuration) shown in **Table 3.10-1** for all function and performance evaluations, including high resolution. Note that Sony does not support two-layer configurations or optical LPFs lacking an IR cut filter.

4. Parameter Configuration

4.1. Communication Parameter Concept

4.1.1. Communication Category Concept

The communication parameters for SS-HQ1 are divided into the 24 categories shown below.

Communication categories are divided into separate segments for each control target, so that the byte positions of the individual parameters are easy to remember.

4.1.2. Communication Category Details

Table 4.1-1 Serial Communication Classification Table

Category number	Category name	Description
CAT1	SYSCON	Parameters related to general setting of system
CAT2	PICT1	Image quality setting parameters 1
CAT3	AE1	Parameters related to AE 1
CAT4	AWB1	Parameters related to AWB 1
CAT5	OPDWIND1	Parameters related to OPD window 1
CAT6	TG	Parameters related to TG
CAT7	EXTSYNC1	Parameters related to external synchronization 1
CAT8	FEADJ(EVRI)	Parameters related to built-in EVR
CAT9	MASKPG	Parameters related to mask function and PG
CAT10	DIF	Parameters related to digital interface
CAT11	BLMDETS1	Parameters related to blemish detection and compensation 1
CAT12	CPU	Built-in controller setting and operation mode setting
CAT13	PICT2	Image quality setting parameters2
CAT14	AE2	Parameters related to AE 2
CAT15	AWB2	Parameters related to AWB 2
CAT16	OPDWIND2	Parameters related to OPD window 2
CAT17	EXTSYNC2	Parameters related to external synchronization 2
CAT18	FEADJ(EVREXT)	Parameters related to external EVR
CAT19	PREADJ	Parameters related to line adjustment
CAT20	PORT	Port driver setting parameters
CAT21	BLMDET2	Parameters related to blemish detection and compensation 2
CAT22	SOUT1	Serial output setting parameters 1
CAT23	SOUT2	Serial output setting parameters 2
CAT24	TEST	Parameters related to LSI

CAT24 (TEST) is an undisclosed parameter for testing purpose.

CAT20 is a port driver control setting parameter, while CAT12-19, CAT-22, and CAT-23 are firmware control parameters of the built-in CPU.

CAT1-11 are hardware parameters. Note however, that care is necessary because even if the values of parameters for controlling port drivers (CAT20) and firmware (CAT12-19) are set directly by external communication, they will be overwritten by port drivers or the firmware. To directly control these parameters for control using external microcomputer and so on, port driver controls are required to be reset and firmware to be stopped (HOLD processing).

(For details of list of parameters for firmware control and the setting method, refer to "13.3 Tables: The parameters controlled by FW".)

Do not change MODESEL and SGMODE control parameters because they are controlled by firmware.

4.2. Parameter Control by Built-in CPU

4.2.1. Processing by CPU

Processing by CPU consists of initial (power-on/sequence) processing and main processing. Note that the settings below are valid for only one initial process.

- Overwriting of parameters in EEPROM
- Settings of functions of port drivers (reflecting CAT20)
- System settings by running MODESEL (CAT12_Byte1_bit0-3)
- Serial communication protocol setting

4.2.2. CPU Main Processing and Firmware Applications

The main processing of CPU includes the sequencing of each field.

• Execute firmware applications and overwrite the hardware parameters (CAT1-11) for control.

• Execute the port drivers (= parameter control by setting port terminal)

* The values reflected by firmware application may be overwritten again.
Take care to ensure that controls are not duplicated while setting the port drivers.

• Execute commands through communication from PC or external microcomputer

* It is recommended that the execution of firmware application or execution of port drivers be stopped in order to correctly reflect the parameter overwrite command. These should be stopped in Category 12 (CPU).

CPUHOLD (CAT12_Byte5_bit0) (=1[h]: Stop all firmware processes)

PDRHOLD (CAT12_Byte5_bit5) (=1[h]: Stop only port driver execution)

Parameters such as the above exist.

Sometimes EEPROM write and restart (reflected in initial processing) may be necessary for changes in parameters for firmware applications such as settings of functions of port drivers.

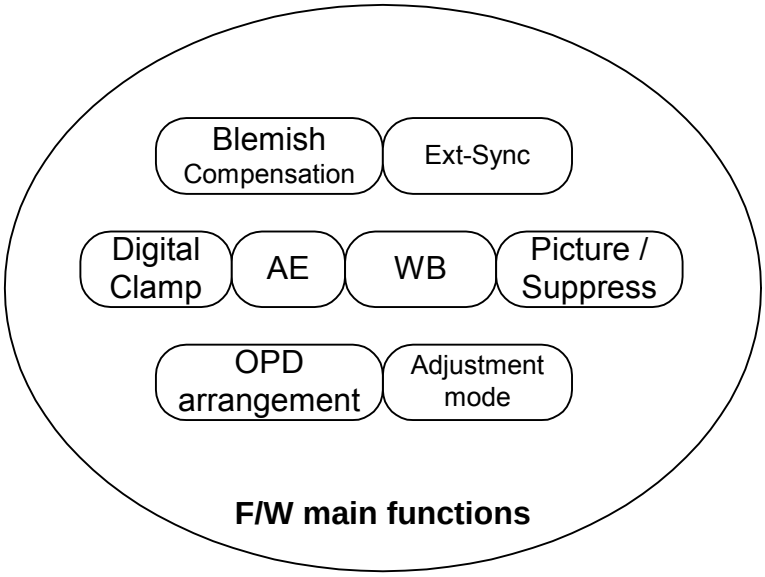


Fig 4.2-1 Main Firmware Applications

Various applications are available for main processing by the CPU. All applications run by default.

< Main Applications >

Adjustment mode	: Adjustment of AGC min, Pre-WB, and so on.
Ext-Sync	: External sync identification, PLL clock selection, shifter control
Blemish Compensation	: CCD blemish detection, compensation
Digital Clamp	: Black clamp process of CCD output
AE	: Automatic exposure control (electronic shutter, AGC, backlight, flicker compensation)
WB	: White balance compensation
Picture / Suppress	: Macro signal processing, aperture compensation suppress, chroma suppress
OPD arrangement	: Detection window settings for AE, AWB, and weighting

For details and method of usage of the various applications, refer to "10. Description of Operation of Each Function," " 11. Functions for Adjustment" and "12. Supporting Functions for applications."

4.3. Parameter Changes through Communication

Parameter changes are made by executing commands through communication from PC or external microcomputer. For details of communication commands, refer to "9.1.4 Communication Format" of "9.1 RS-232C Communication" and "12.4.2 Communication Protocol with External Microcomputers" of "12.4 When Using the External Microcomputer".

When parameters are meant for the controls mentioned below, the transmitted values may not be reflected correctly.

(1) Controls for initial processing
(2) Controls for port drivers
(3) Firmware application controls
(4) Parameters specially for output

For parameters relevant to (1), (2) and (3) above, either the higher order parameters performing control need to be changed, or the control needs to be stopped. Sometimes, it may be necessary to change the data saved in EEPROM and restart.

4.4. Saving Parameters to EEPROM

4.4.1. EEPROM Write Command and Address Map

EEPROM can be connected to DSP (CXD3172AR), and parameters can be saved and loaded at restart in the SS-HQ1 system.
The "EEPROM write command" is a "command to write parameter values saved in registers in DSP (including firmware controlled parameter values) to EEPROM". To write parameter values in the PC or external microcomputer to EEPROM, the firmware controls need to be stopped beforehand and the register values changed (temporarily stored) beforehand.
The address map to EEPROM shown in the figure below is accessed in SS-HQ1. Mapping is performed in 1-byte units, therefore, the address length becomes 512 words x 2 bytes = 1024 bytes, address (0-3FF[h]).

Table 4.4-1 EEPROM Map of SS-HQ1 System

Map Address	contents	EEP Word
000h 001h	Chip_ID code	000h
002h - 131h	CAT_12-21 parameters	001h - 098h
132h - 27Bh	CAT_1-4, 6-11,24 parameters	099h - 13Dh
27Ch - 3FFh	Prohibition of use	13Eh - 1FFh

CAT5 (undisclosed, for firmware control) and CAT22, CAT23 (serial output) categories fall outside the scope of parameter saves to EEPROM.
Do not overwrite address 27C[h] - 3FF[h].

< Important Items >

During the power-on sequence (initial processing), DSP (CXD3172AR) reads the EEPROM addresses 000[h], 001[h], and refers to the "chip ID code". If the specified value does not coincide, access to EEPROM (both read and write) is terminated recognizing that "EEPROM is invalid".
To write "chip ID code," the "EEPROM ALL WRITE command" must be executed.

4.4.2. "EEPROM ALL WRITE" Command

This is the command for "writing all parameters that can be saved to EEPROM and that are currently retained by the chip ID code and DSP." The procedure described below is recommended to prevent write errors to EEPROM.

< Preparations >

(1) Keep ready in the PC or in the external microcomputer the parameter file you wish to save to EEPROM.
To avoid problems in system settings, check parameters of CAT20 (port driver setting) and CAT12 (CPU setting) thoroughly.

(2) Send CPUHOLD (CAT12_Byte5_bit0)=1[h] and stop the entire CPU.

(3) Send all parameters while retaining CPUHOLD=1[h], and store it temporarily in the register in DSP.
To send all parameters with the SS-HQ1 control software, click the All Write button in the Register Read/Write menu. For communication with external microcomputer, send all bytes of each category to the DSP.

< Write process >

(1) Primary write: Execute the EEPROM ALL WRITE command with CPUHOLD=1[h].
In the SS-HQ1 control software, click in the following sequence: EEPROM sub-menu -> procedure Send -> Write -> Read -> All Select button -> Start button. Immediately after the EEPROM write, verify will be executed. Confirm that the result shows that all parameters are OK.
If write is not possible, or if an error occurs, check whether an EEPROM or serial communication connect fault (CASI, CASO, CASCK, CSROM) has occurred.

(2) Restart: Reset power-on (Pin11: XRSTL -> H) to identify EEPROM to the DSP. The EEPROM value will be reflected during start, but the firmware stops because CPUHOLD=1[h].

(3) Secondary write: Change value stored in EEPROM to CPUHOLD=0[h]. First, send CPUHOLD=0[h].
Overwrite only CAT12(CPU) using the EEPROM Category WRITE Command.
In the SS-HQ1 control software, click in the following sequence: EEPROM sub-menu -> procedure Send -> Write -> Read -> Click CAT12 -> Start button. When the verify result of CAT12 is displayed, confirm by clicking OK.
* We recommend that you save the parameter files to the PC.

(4) Restart: At the next power-on reset (Pin11: XRSTL -> H), start in the CPUHOLD=0[h] condition.

5. Power-on Sequence

5.1. Power-on Sequence

In the SS-HQ1 system, only initial operations for the DSP (CXD3172AR) are required after startup.
Initial operations for the DSP assume that power has been supplied to the CCD and peripheral ICs. Connect reset input XRST (pin 11) to the reset circuit.
We recommend that setting parameters of the SS-HQ1 system be stored in EEPROM. The initialization sequence varies depending on whether or not there are valid parameters in EEPROM.
Please keep these things in mind when designing a system reset for the entire camera set (as when an external microcomputer is used).

5.1.1. DSP (CXD3172AR) Initialization Sequence

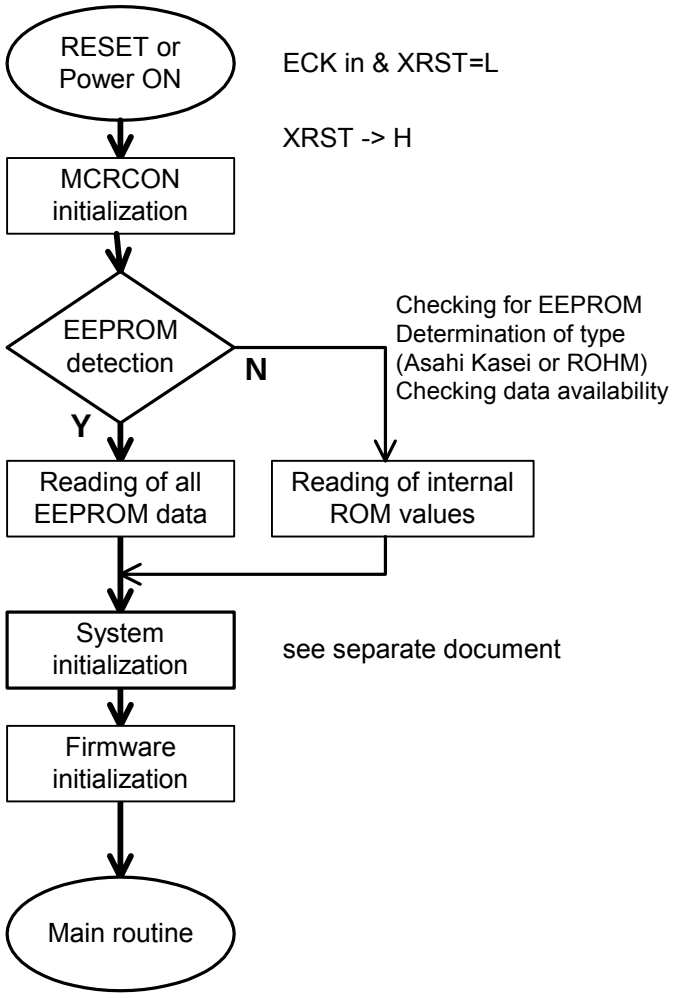


Fig 5.1-1 General DSP (CXD3172AR) Initialization Sequence for SS-HQ1

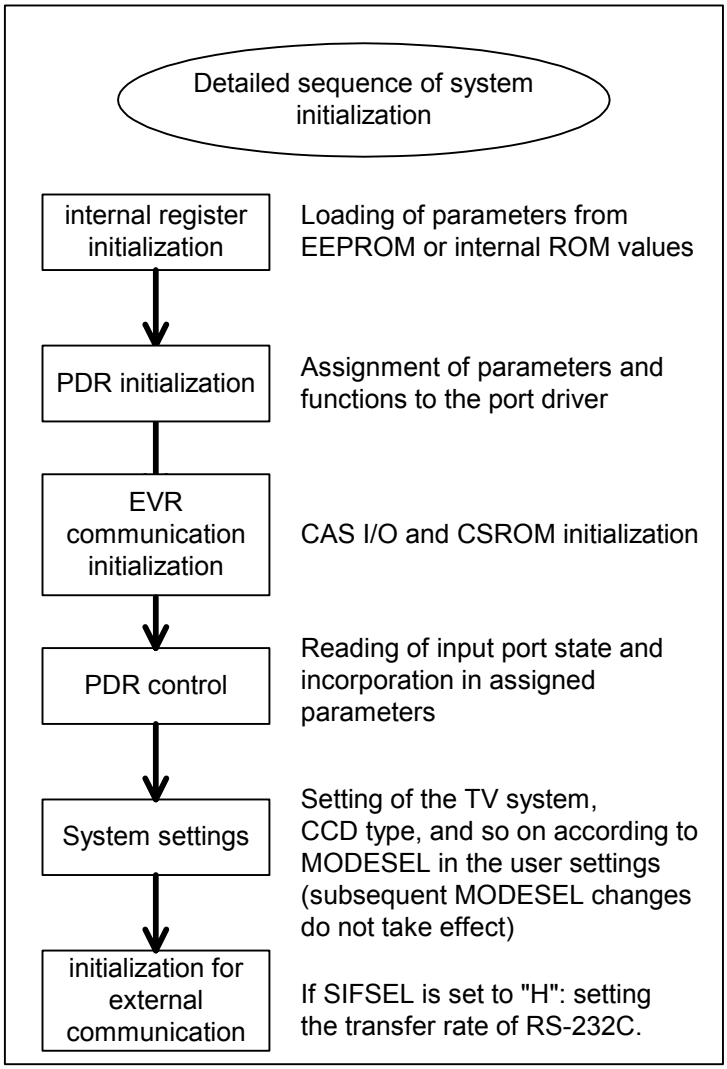


Fig 5.1-2 Detailed DSP (CXD3172AR) System Initialization Sequence for SS-HQ1

Important

- After reset is canceled (XRST L-> H), EEPROM is still accessed for 80 ms, so save XRST=H. During this time, if the power is cut or the system is reset again, the data stored in EEPROM may be corrupted.
- It takes 11 fields from when reset is canceled until initialization is complete (start of AE operation). This does not include the time for black clamp, AE, or AWB convergence. (This is main routine processing.)
- If there is communication with an external microcomputer, it starts after the 11th field.

5.1.2. Parameters Exclusively for Initialization

Parameters in the following table are only valid during initialization operations. After the initialization, both external communication and port driver control are disabled. To change this, the following procedure is required:

(CPUHOLD) -> overwrite the EEPROM values -> XRST=L (reset again) -> read from EEPROM -> reinitialize

Table 5.1-1 Parameters Valid Only during Power-on Sequence (Initialization Operations)

CAT	Byte	Bit	Parameter	Initial settings
12_CPU	1	0-3	MODESEL	Loaded from P12-P15 (CAT20 setting)
	10	0	BPSSEL	1 : RS-232C 19200bps
	10	1	EVRLDSEL	0 : CSROM -> S4 out
	13	1	SYSSELON	0 : OFF
	13	2	SYSSELFLG	Disabled if SYSSELON = 0
	16	0-7	MODESEL0	
	17	0-7	MODESEL1	
	18	0-7	SGMODE0	
	19	0-7	SGMODE1	
	20	0-7	EVR20	
	21	0-7	EVR21	
15_AWB2	4	0-7	GGAIN	&H26
	62	0-7	MASKCNT	&H07
20_PORT	1-48	0-7	(all parameters)	See the port driver chapter

6. CCD Type Selection

6.1. Supported CCD type

The SS-HQ1 supports the following types of CCDs.
Note that the types shown below are the types supported at the time these Application Notes were prepared.
Some types may be added or eliminated due to CCD version upgrades or discontinued production.

Table 6.1-1 CCD Image Sensors Supported by the SS-HQ1

Number of pixels	Optical size	TV system	Product name
510H	Type 1/3	NTSC	ICX254AK
			ICX404AK
		PAL	ICX255AK
			ICX405AK
	Type 1/4	NTSC	ICX206AK
			ICX226AK
		PAL	ICX207AK
			ICX227AK
760H	Type 1/3	NTSC	ICX258AK
			ICX408AK
		PAL	ICX259AK
			ICX409AK
	Type 1/4	NTSC	ICX228AK
			ICX278AK
		PAL	ICX229AK
			ICX279AK

6.2. List of Clock Configurations for Each CCD type

The basic clock system for the SS-HQ1 comprises both an oscillator and a PLL that uses two types of oscillators.
In addition, the clock system of 4MCK (or 2MCK), 8fsc and 27MHz can be constituted for every type of CCD as operation mode.
The clock frequency (oscillator frequency) combinations for each CCD type are as follows.

4MCK (or 2MCK) = CXD3172AR 88pin ECK input or CXD3172AR 43pin MCK PLL input
8fsc = CXD3172AR 88pin ECK input
27MHz = CXD3172AR 88pin ECK input or CXD3172AR 43pin MCK PLL input

Table 6.2-1 Relationship between CCD type and Clock Frequencies

TV system	CCD type	MODE SEL *1	ECK			1MCK (PLL input)
			8fsc	4MCK(2MCK)	27MHz	
NTSC	510H	0[h]	-	38.13986MHz	-	-
		1[h]	28.63636MHz	-	-	38.13986MHz
		2[h]	-	-	27.00000MHz	
	760H	6[h]	-	28.63636MHz	-	-
		8[h]	-	-	27.00000MHz	28.63636MHz
PAL	510H	3[h]	-	37.87500MHz	-	-
		4[h]	35.46895MHz	-	-	37.87500MHz
		5[h]	-	-	27.00000MHz	
	760H	9[h]	-	28.37500MHz	-	-
		A[h]	35.46895MHz	-	-	28.37500MHz
		B[h]	-	-	27.00000MHz	

*1: Setup of MODESEL is shown in the below-mentioned **Table 6.3-2**.

6.3. Important information on Wiring

The drive circuit must be changed according to the type of CCD used. The main differences are as follows.

1. Changes in the drive circuit due to different CCD image sensor drive specifications
2. Changes in the clock system due to different CCD types and TV systems (NTSC/PAL)
3. Changes in the frequency response due to different CCD types
4. Changes in the modes due to different CCD types and TV systems (NTSC/PAL)

6.3.1. Drive Circuit Changes

The drive specifications of CCD image sensors that can be driven by the SS-HQ1are shown in the Table below.

Table 6.3-1 CCD Image Sensors and Drive Conditions

CCD type Optical size		Product name	DC voltage specifications		AC voltage specifications			Drive circuit example
			Vsub voltage	RG voltage	H	RG	V	
510H	Type 1/3	ICX254AK	Generated internally, adjustment free	Generated internally, adjustment free	5.0V	5.0V	-7.0V	**Fig 6.3-4**
		ICX255AK						
		ICX404AK		Clamped high, adjustment free	5.0V	5.0V	-7.0V	**Fig 6.3-1**
		ICX405AK						
	Type 1/4	ICX206AK		Generated internally, adjustment free	3.3V	3.3V	-7.0V	**Fig 6.3-2**
		ICX207AK						
		ICX226AK			3.3V	3.3V	-5.0V	**Fig 6.3-3**
		ICX227AK						
760H	Type 1/3	ICX258AK			5.0V	5.0V	-7.0V	**Fig 6.3-4**
		ICX259AK						
		ICX408AK		Clamped high, adjustment free	5.0V	5.0V	-7.0V	**Fig 6.3-1**
		ICX409AK						
	Type 1/4	ICX228AK		Generated internally, adjustment free	3.3V	3.3V	-5.0V	**Fig 6.3-3**
		ICX229AK						
		ICX278AK			3.3V	3.3V	-7.0V	**Fig 6.3-2**
		ICX279AK						

As mentioned above, the following drive circuit points must be changed when the CCD type differs.

1. RG clamp circuit
2. CXD3172AR supply voltages

See the drive circuit examples on the following figure (**Fig 6.3-1**, **Fig 6.3-2**, **Fig 6.3-3**, and **Fig 6.3-4**) for each change.

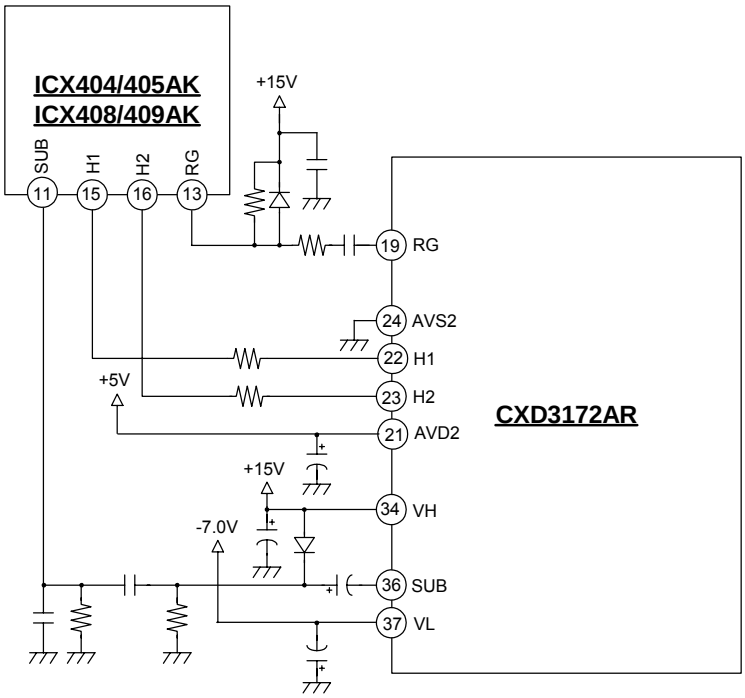


Fig 6.3-1 SS-HQ1 CCD Drive Circuit Example (ICX404/405AK, ICX408/409AK)

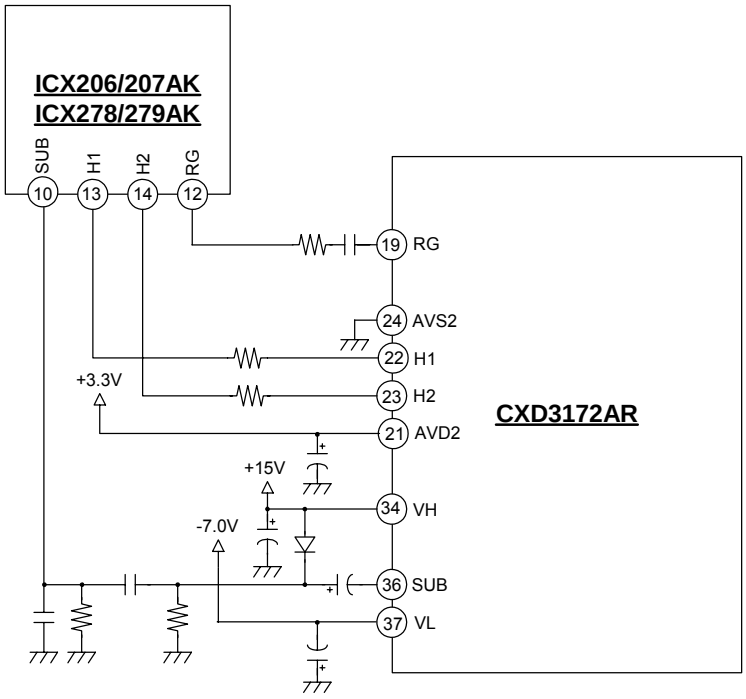


Fig 6.3-2 SS-HQ1 CCD Drive Circuit Example (ICX206/207AK, ICX278/279AK)

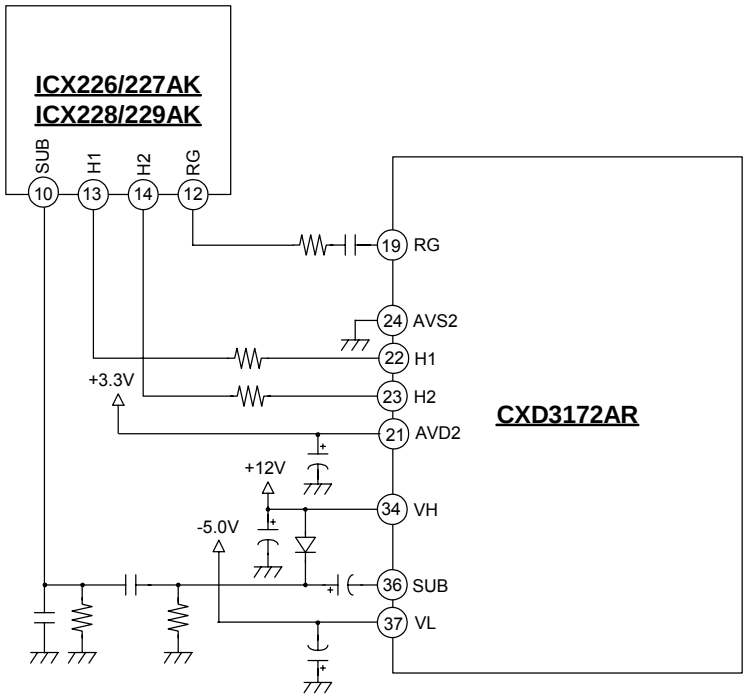


Fig 6.3-3 SS-HQ1 CCD Drive Circuit Example (ICX226/227AK, ICX228/229AK)

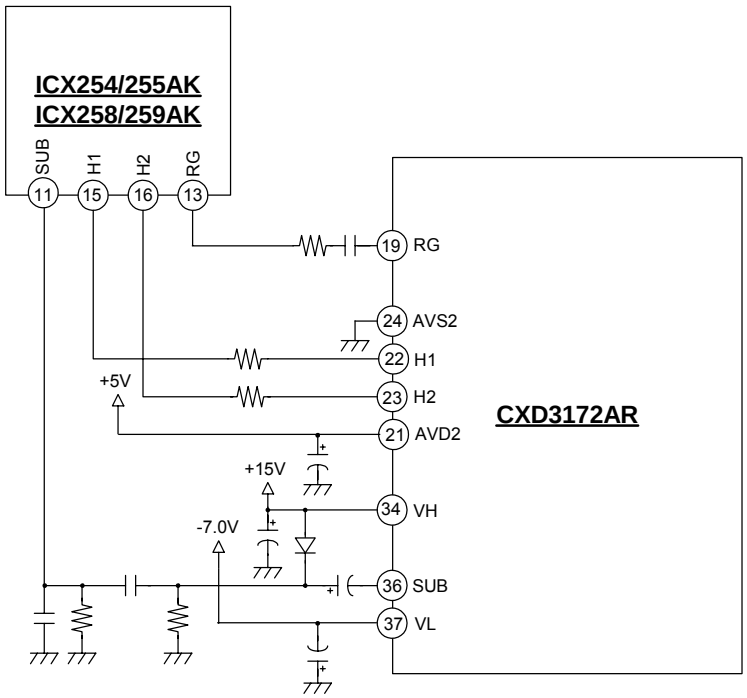


Fig 6.3-4 SS-HQ1 CCD Drive Circuit Example (ICX254/255AK, ICX258/259AK)

Fig 6.3-1 SS-HQ1 CCD Drive Circuit Example (ICX404/405AK, ICX408/409AK) shows the drive circuit when using 1/3 type CCD image sensors (ICX404/405AK, ICX408/409AK). Both Vsub voltage and RG voltage are adjustment-free. Vsub is a voltage generated inside the CCD and is used to clamp the shutter pulse, so an external clamping circuit is not required. The CXD3172AR SUB (36pin) output is input via capacitor to the CCD's SUB pin.
The CXD3172AR RG (19pin) is input to the CCD after its DC component is cut by a capacitor. But the high clamp circuit is need.

Fig 6.3-2 SS-HQ1 CCD Drive Circuit Example (ICX206/207AK, ICX278/279AK) shows the drive circuit when using 1/4 type CCD image sensors (ICX206/207AK, ICX278/279AK). Both Vsub voltage and RG voltage are adjustment-free. Vsub is a voltage generated inside the CCD and is used to clamp the shutter pulse, so an external clamping circuit is not required. The CXD3172AR SUB (pin 36) output is input via a capacitor to the CCD's SUB pin. The CXD3172AR RG (19pin) is input to the CCD after its DC component is cut by a capacitor.

Fig 6.3-3 SS-HQ1 CCD Drive Circuit Example (ICX226/227AK, ICX228/229AK) shows the drive circuit when using 1/4 type CCD image sensors (ICX226/227AK, ICX228/229AK). Both Vsub voltage and RG voltage are adjustment-free. Vsub is a voltage generated inside the CCD and is used to clamp the shutter pulse, so an external clamping circuit is not required. The CXD3172AR SUB (pin 36) output is input via a capacitor to the CCD's SUB pin. The CXD3172AR RG (19pin) is input to the CCD after its DC component is cut by a capacitor.

Fig 6.3-4 SS-HQ1 CCD Drive Circuit Example (ICX254/255AK, ICX258/259AK) shows the drive circuit when using 1/3 type CCD image sensors (ICX254/255AK, ICX258/259AK). Both Vsub voltage and RG voltage are adjustment-free. Vsub is a voltage generated inside the CCD and is used to clamp the shutter pulse, so an external clamping circuit is not required. The CXD3172AR SUB (pin 36) output is input via a capacitor to the CCD's SUB pin. The CXD3172AR RG (19pin) is input to the CCD after its DC component is cut by a capacitor.

6.3.2. Clock System Changes

In the internal synchronization mode, the composition which operates only by one X'tal is the basic system. And it can be made to operate even if it does not constitute PLL.
And when it constitutes the clock system inputted into ECK/MCK using two VCO, it is necessary to constitute PLL and to input into MCK. We recommend to use LC VCO or X'tal VCO properly according to a use to the MCK VCO in that case. By exchanging ECK VCO, it corresponds to change of the number of CCD pixels, and TV system (NTSC/PAL).

6.3.3. Frequency Response Changes

As mentioned above, the encoder clock (ECK) frequency differs according to the type of CCD image sensor used. Therefore, the bandwidth and carrier frequency of the luminance signal output from CXD3172AR IOY (pin 75) also differ.
In addition, the NTSC and PAL subcarrier frequencies differ from each other, making it necessary to also change the characteristics of the BPF connected to the rear end of the CXD3172AR IOC (pin67).

6.3.4. Clock System Selection

The internal clock of CXD3172AR is switched according to the operation mode. Please wire the VDD or GND side from P12 to P15 setup of CXD3172AR and set by pull up/down according to the system conditions to be used. Since the clock system does not operate normally when the following setup is not correct, please ensure a setup.

The pins from P12 to P15 of CXD3172AR are assigned to the parameter (MODESEL) which switches operation modes as the initial setting and pins for the port driver. The parameter (MODESEL) controls CCD types, TV system and clock setting in a lump. It isn't necessary of resetting these parameters.

Table 6.3-2 Setting Method of Operation Mode pins (P12 - 15)

MODESEL	P15 (84pin)	P14 (83pin)	P13 (82pin)	P12 (80pin)	TV system	CCD	Clock pin	
							ECK (88pin)	MCK (43pin)
0[h]	Low	Low	Low	Low	NTSC	510H	ECK	-
1[h]	Low	Low	Low	High				MCK
2[h]	Low	Low	High	Low				
3[h]	Low	Low	High	High	PAL			-
4[h]	Low	High	Low	Low				MCK
5[h]	Low	High	Low	High				
6[h]	Low	High	High	Low	NTSC	760H		-
8[h]	High	Low	Low	Low				MCK
9[h]	High	Low	Low	High	PAL			-
A[h]	High	Low	High	Low				MCK
B[h]	High	Low	High	High				

Table 6.3-3 Operation Mode in MODESEL and System Condition

MODESEL	Operation mode	System condition	
		PLL	MCK
0[h]	Analog / Digital output	-	-
1[h]	8fsc Analog output	PLL configuration	MCK input
2[h]	27M master MCK PLL		
3[h]	Analog / Digital output	-	-
4[h]	8fsc Analog output	PLL configuration	MCK input
5[h]	27M master MCK PLL		
6[h]	Analog / Digital output	-	-
8[h]	27M master MCK PLL	PLL configuration	MCK input
9[h]	Analog / Digital output	-	-
A[h]	8fsc Analog output	PLL configuration	MCK input
B[h]	27M master MCK PLL		

6.3.5. Wiring Changes When EEPROM is not written

When the effective data are not written to EEPROM, set according to the system which uses P12-15 (CXD3172AR 80, 82, 83 and 84pin).

Wire the VDD side or GND side and set by pull-up or pull-down so that setting method is shown in the **Table 6.3-2**.

DSP reads the setting of port into the register by initial process of built-in program after being powered on, and distinguishes the type of CCD and TV system.

When the setting of the ports are not right, the communication for peripheral LSIs incorrect-operates

6.4. CCD Primary Color Separation Matrix

6.4.1. The Sequence of Parameter Changes

There are the parameters which can't write to EEPROM directly, because some parameters are controlled by built-in firmware.

Primary color separation matrix parameters which are shown in next section are the parameters which can't write to EEPROM directly. For example, the change sequence of RMATY (CAT2_Byte31_bit0-7) is shown below.

1. Set CPUHOLD (CAT12_Byte5_bit0) to 1 or Set RGBMATCTL(CAT12_Byte8_bit1) to 1
2. Change the value of RMATY(CAT2_Byte31_bit0-7)
3. Write CAT2 to EEPROM. (Note: Don't write CAT12 to EEPROM in this case.)
4. Operate Initialization processing

6.4.2. Recommended Parameter's Value

The spectral characteristics of the color filter differ according to the type of CCD. The SS-HQ1 initial settings are designed in consideration of the spectral characteristics of a 1/4 type CCD image sensor. Therefore, resetting the parameters on the following table and writing this data to the EEPROM is recommended when using other types of CCD image sensors.

Table 6.4-1 CCD Types and Recommended Primary Color Separation Matrix Parameters

CAT			2 (PICT1)					
Byte			31	32	33	34	35	36
Bit			0 to 7	0 to 7	0 to 7	0 to 7	0 to 7	0 to 7
Parameter name			RMATY	RMATC	BMATY	BMATC	GMATCR	GMATCB
510H	Type 1/3	ICX404/405AK	2F[h]	14[h]	28[h]	DC[h]	80[h]	80[h]
760H		ICX408/409AK						
510H		ICX254/255AK	2B[h]	10[h]	2F[h]	CF[h]		
760H		ICX258/259AK						
510H	Type 1/4	ICX206/207AK	2D[h]	00[h]	45[h]	BB[h]		
		ICX226AK	21[h]	F9[h]	2C[h]	E0[h]		
		ICX227AK	23[h]	05[h]	2C[h]	FC[h]		
760H		ICX228/229AK	27[h]	05[h]	30[h]	E0[h]		
		ICX278/279AK	2F[h]	14[h]	2F[h]	DC[h]		

Table 6.4-2 CCD Types and Linear Matrix Parameters (Reference Values)

CAT			2 (PICT1)			
Byte			37	38	39	40
bit			0 to 7	0 to 7	0 to 7	0 to 7
Parameter name			RYGAIN1	BYGAIN1	RYHUE1	BYHUE1
510H	Type 1/3	ICX254/255AK	3F[h]	21[h]	80[h]	FF[h]
		ICX404/405AK				
760H		ICX258/259AK				
		ICX408/409AK				
510H	Type 1/4	ICX206/207AK				
		ICX226/227AK				
760H		ICX228/229AK				
		ICX278/279AK				

* The above linear matrix parameters are example setting determined with an emphasis on color reproducibility for skin color in representative samples of each CCD type. Please note that they are not intended to be adjusted to the target displayed on the vector scope.

*Use the above linear matrix parameters as reference values. In actual practice, we recommend that each user set their own values to match the color reproducibility they desire, according to factors such as the circuits/ICs to be connected at the rear end of the DSP, the gain settings, and the video camera screen makeup.

7.Power Supply

7.1. Supply Voltage

The SS-HQ1 requires the following four types of power supplies as the system power supplies.

+3.3V : Analog power supply for CXD3172AR
Logic power supply for CXD3172AR
Power supply for CXA2096N
Power supply for EEPROM
Power supply for RS-232C transceiver

+5.0V : Analog power supply for CXD3172AR (H1,H2,RG driver)

VH : Power supply for CXD3172AR (V driver, shutter driver)
Power supply for CCD image sensor
Power supply for reset gate pulse clamp

VL : Power supply for CXD3172AR (V driver, shutter driver)
Protective transistor input voltage for CCD image sensor

*Care should be taken as the voltage (**+5.0V, VH, VL)** differs according to the drive specification of the CCD image sensor.

7.1.1. Supply Voltage Accuracy

When using SS-HQ1, the power supply tolerances are as follows.

Table 7.1-1 SS-HQ1 Supply Voltage and Accuracy

Supply Voltage (typ.)	Tolerance
+3.3V	±0.3V or Refer to the CCD data sheet
+5.0V	Refer to the CCD data sheet
VH	
VL	

7.1.2. Power Consumption

Examples of measured current consumption values when driving ICX408AK are shown in the table below. These values were measured using a Sony Semiconductor evaluation board, and should be used as reference values.

Table 7.1-2 Power Consumption Measurements(when driving ICX408AK)

Item	IC type name	Supply voltage	Current consumption
CCD	ICX408AK	15.0V	4.20mA
DSP	CXD3172AR	15.0V	0.18mA
		5.0V	33.7mA
		3.3V	171.9mA
		-7.0V	1.19mA
CDS	CXA2096N	3.3V	39.3mA

* The current consumption value of each IC is adding together the analog power supply and the digital power supply.

7.1.3. Power-on Sequence

When turning on the power, be sure to turn on the VL last. The +3.3V, +5.0V and VH power supplies may be turned on in any order.

When turning off the power, the VL, +3.3V, +5.0V and VH power supplies may be turned off in any order.

8. Level Diagram

8.1. SS-HQ1 Level Diagram

8.1.1. Signal Standard Level Diagram of Analog Output

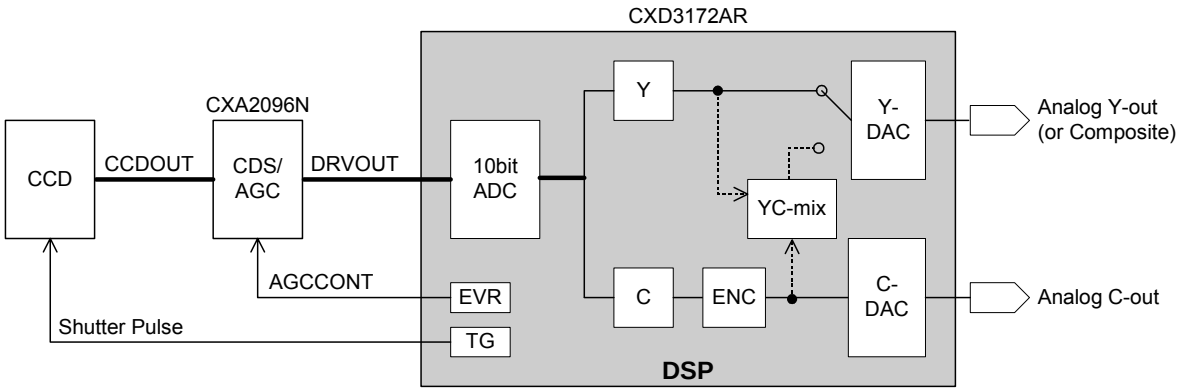


Fig 8.1-1 SS-HQ1 System Composition Figure

The color camera picture quality design generally ensures a dynamic-range of two to three times the standard level to avoid the Video output's saturation of the high light subjects. The SS-HQ1 system sets up the dynamic-range of 2.5 times the standard level.

A level diagram for an SS-HQ1 system is described below.
The recommended values and signal levels presented here have been verified on our evaluation boards. Please note that this is no guarantee of performance, including board layout changes, parts selection, and temperature characteristics.

8.1.1.1. The Output of CCD

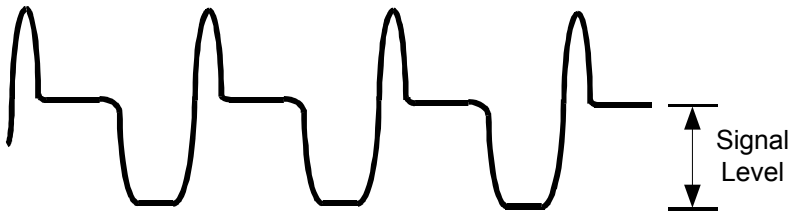


Fig 8.1-2 an example of CCD Output Signal

The saturation signal level differs for each type of CCD image sensor. The SS-HQ1 is mainly designed for CCD image sensors with the saturation signal level of 600 - 1000 [mV]. To ensure the dynamic-range of 2.5 times the standard level, the standard CCD output (Y-level) of the SS-HQ1 is 250 - 400 [mV]. The exposure time and the output level of CCD can be controlled by the shutter pulse of built-in TG of CXD3172AR. When using the mechanical-iris, some control-circuit is necessary.

8.1.1.2. The Output of CDS/AGC

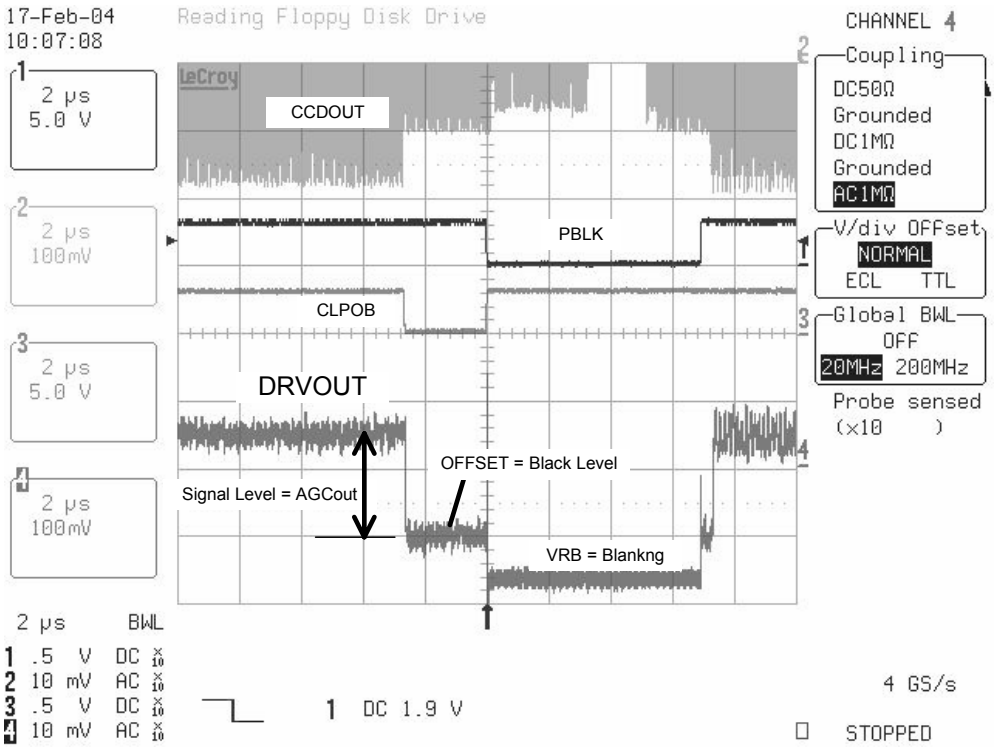


Fig 8.1-3 an example of DRVOUT

CCD output signal is processed CDS, AGC, black-level clamping, preblanking with CXA2096N. And the output signal of CXA2096N is DRVOUT. DRVOUT, and A/D reference voltages (VRT, VRB) are connected to the built-in A/D converter of CXD3172AR. In order to reject the black-level change by noises, an offset level can be added to DRVOUT. In the black-clamping processing of CXD3172AR, the offset level is subtracted in the integral mean. So the proper signal level is extracted.
The built-in EVR of CXD3172AR can control AGC of CXA2096N by AGCCONT input. CCD output level is small and gained-up in AGC processing at low-light-condition. If the lowest AGC value is short, the unevenness (dirty spots) of CCD saturation can be seen at high-light-condition. AGC minimum value is adjusted so that DRVOUT signal must be saturated (about 1[Vp-p]) before the CCD output level becomes saturated. During AE on, it is gained over the AGCMIN value.

For example, if it is set up in AGCMIN =4[dB], in theory, the unevenness of saturation can be prevented toward the CCD which saturation signal level is 650[mV] and more. In addition, when you decide an AGCMIN value, please actually see drawing and perform the check of S/N and saturation unevenness.

8.1.1.3. The Input of A/D Converter

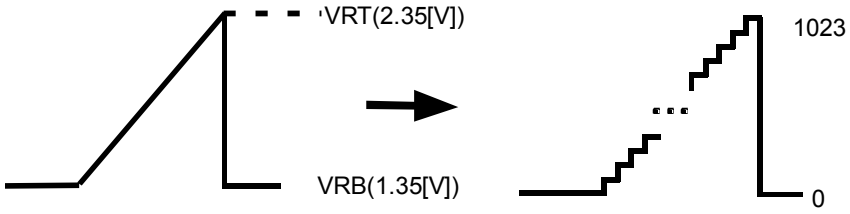


Fig 8.1-4 an example of 10 bit-A/D conversion

DRVOUT level = A/D converter input level : Standerd signal level = 400[mV] -> D range of 2.5 times.

The built-in A/D converter of CXD3172AR is an input range 1000m[Vp-p], and can be driven directly by the outputs of CXA2096N (VRT VRB, DRVOUT).

The input signal of A/D converter is changed into the 10bit -digital signals(= 1024 grade).

The effective maximum value of A/D output signal (high-light side) decreases only the advantages of the OFFSET (black level) put on DRVOUT.

8.1.1.4. Y,C Signal processing and D/A conversion

Targeting the digital output signal of built-in A/D converter, luminance signal processing, and chrominance signal processing are done in the CXD3172AR. Finally processed signals are loaded to built-in 10bit-DAC, and converted to the analog Video signal.

The digital output signal of built-in A/D converter contains both of luminance element and chrominance element. And the signal is processed suppress, aperture compensation, and gamma, so that the output signal form of DAC may different from the input signal form of A/D converter. The chrominance output signal is moderated with sub-career, too. CXD3172AR uses the same analog-cell with Y-DAC, C-DAC.

The luminance signal processing and Y-DAC are described below.

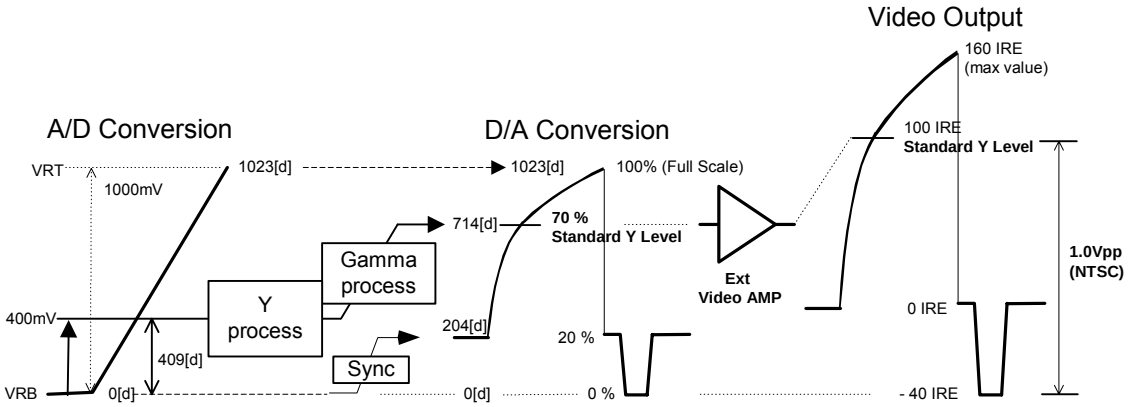


Fig 8.1-5 the standard level of the luminance signal (NTSC)

The **Fig 8.1-5** shows luminance signal processing with the NTSC form and relations with the standard output level of Y-DAC.
SS-HQ1 system sets up the standard output level of the luminance signal (with gamma processing) as NTSC-100[IRE] when an A/D input level is the standard 400[mV]. And Sync-level as NTSC=-40[IRE] is added, too.
Therefore,
The standard output level (Y-DAC) = 70[%] / full scale 100[%].
The Sync-level (Y-DAC) = 20[%] / full scale 100[%].

--- Parameter reference (the luminance signal, NTSC standard setting) ---
(CAT1_Byte5_bit0-4) SYNCLV = 9[h] (Sync-level as -40[IRE])
(CAT2_Byte7_bit2-4) YGAMSEL= 4[h]
(CAT2_Byte7_bit5-7) YKNEESEL = 3[h]
(CAT2_Byte8_bit0-7) YGAIN = 80[h]
(CAT2_Byte10_bit0-5) SETUP = C[h] (7.5[IRE])
When an A/D input level is the maximum 1000[mV] (=250[%]), Y-DAC outputs the full scale as NTSC=160 [IRE] (the luminance signal with gamma processing).
The built-in Y-DAC is controllable by reference voltage (VREFY). The output of Y-DAC is the current-flow type and must be converted to voltage level by the terminal-resistance 200[ohm].
See “3.9 DAC Mode and YC-mix External Analog Circuit” of “3.Peripheral Circuits”, for internal Y-DAC peripheral circuit examples and usage notes.

The chrominance signal is not discussed here because it differs according to the spectral characteristics of the CCD image sensor and the imaged subject. And its standard level cannot be defined.

--- Parameter reference (the chrominance signal, NTSC standard setting) ---
(CAT1_Byte13_bit0-6) BSTLV = 38[h] (burst-amplitude = 40[IRE])

The chroma signal is output from the internal C-DAC when (CAT1_Byte3_bit2) DACMODE is set to 1[h].
The built-in C-DAC is controllable by reference voltage (VREFC). The output of C-DAC is the current-flow type and must be converted to voltage level by the terminal-resistance 200[ohm].
See “3.9 DAC Mode and YC-mix External Analog Circuit” of “3.Peripheral Circuits”, for internal C-DAC peripheral circuit examples and usage notes.

8.1.1.5. In a case of the Composite Output mode

In a case,
(CAT1_Byte3_bit2) DACMODE = 0[h]
This is the composite output mode through the built-in YC-MIX block. The composite signal of luminance and chrominance (moderated with sub-career) is made in YC-MIX block. And Y-DAC outputs the composite signal.
In this case, C-DAC outputs no signal.

See “3.9 DAC Mode and YC-mix External Analog Circuit” of “3.Peripheral Circuits”, for notes on composite output mode.

8.1.2. The Standard Level Diagram of Digital Outputs

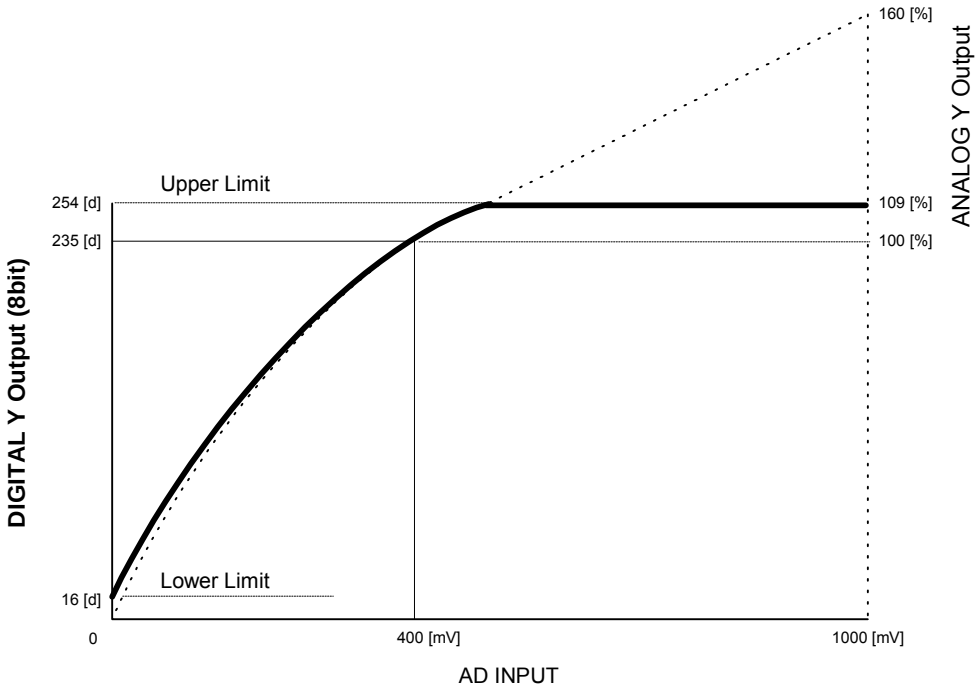


Fig 8.1-6 Digital output (Y signal) characteristics

Digital output at 8 bits is defined in ITU-R-BT.656 and 601 as follows:

100[%] Y output = 235 [d]

0[%] Y output = 16 [d]

Therefore, the maximum Y output is limited to 109 [%] = (254-16) [d] / (235-16) [d].

This means that the digital output D range has a maximum of 1.09, and is less than the analog output D range (2.5).

To the extent that the D range value is small, one might consider increasing the standard AD input level. However, the standard A/D input level (400 [mV]), which is the same level setting used in analog output, should be used because “even in cases where only digital output is used, the same H/W and F/W as are used in analog output are used with respect to the AE and AWB convergence settings, as well as basic Y signal processing and chroma signal processing.”

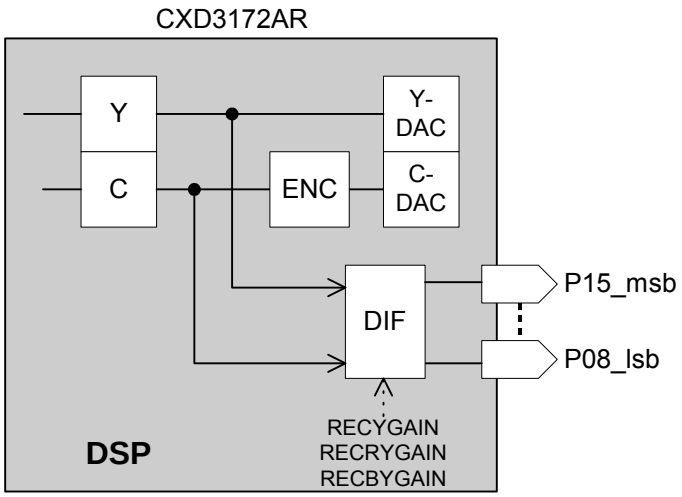


Fig 8.1-7 Digital output configuration

The data immediately preceding Y-DAC and ENC in analog output are used, so Y and C signal processes are the same as for analog output.

For details on the digital output parameter settings, see “12.1 Using Digital Output”.

Use the following parameter settings to match the analog output and digital output levels.

Table 8.1-1 Digital output level adjustment parameters

Parameter	Address	Description	Theoretical recommended value
RECYGAIN	CAT10_Byte8_bit0-7	Digital Y output gain coefficient (0- x1.99)	B1[h] : x1.38
RECRYGAIN	CAT10_Byte9_bit0-7	Digital R-Y output gain coefficient (0- x3.99)	90[h] : x2.25
RECBYGAIN	CAT10_Byte10_bit0-7	Digital B-Y output gain coefficient (0- x3.99)	90[h] : x2.25
<Note> When digital output is used, the apparent gain coefficient on the screen may be offset due to factors such as the type of connected equipment, the device’s color difference conversion process, and color reproducibility. This can be corrected by altering the individual gain coefficients.			

9. RS-232C Communication and Communication with Peripheral ICs

9.1. RS-232C Communication

9.1.1. Interface

The SS-HQ1 system supports the RS-232C format (half duplex mode) as a means of communication with external PCs. However, RS-232C communication requires an external IC for converting the 3.3V logic to the RS-232C level (recommended product: MAX3232, made by Maxim), as well as pin settings. Please see the application circuit we have provided for information on the connections with the MAX3232 and the RS-232C connector (D-sub 9 pin).

In cases where the SS-HQ1 system is controlled through an external microcomputer, we recommend using that because it includes serial communication specifications which are more efficient than RS-232C. For details, see “12.4 When Using the External Microcomputer”.

Use the pin settings in the following table on a CXD3172AR which is to be used in RS-232C.
If you switch SIFSEL, be sure to reset the system.

Table 9.1-1 Pin Settings for Communication

Signal name	Pin No	I / O	Description
XCS(XCTS)	15	IN	Always High
SI(RXD)	16	IN	Serial settings data input
SO(TXD)	17	OUT	Serial settings data output
SCK(XRTS)	18	OUT	Pull Up (Resistance of 100k ohm) *1
SIFSEL	13	IN	Always High

*1 Because 18pin becomes an input terminal by SIFSEL=L, it uses it with Pull up as a floating measures.
18pin becomes L output by SIFSEL=H.

9.1.2. Communication Procedure

The “SS-HQ1 Control Software” provided by Sony is designed for use with RS-232C communication. The sending and receiving processes, as well as EEPROM write/read processes, have been optimized for the SS-HQ1 system, so you do not have to worry about factors like communication format and byte length. The following settings should be used in the PCs.

Table 9.1-2 PC Settings for Communication

Item	Setting
COM PORT	Any (1-16)
Communication speed *	19200 bps
PARITY	NONE
DATA bits	8 bit
STOP bits	1 bit
Handshaking	Nothing

* The speeds listed below can be selected through a parameter as communication speeds.
This setting is applied after it is written to the EEPROM and a reset is performed.

Table 9.1-3 Communication Speed Settings

Parameter		Description
BPSSEL	CAT12_Byte10_bit0	0[h]:9600bps
		1[h]:19200bps

Note that if the communication speed set in the “SS-HQ1 Control Software” does not match the communication speed in the following parameter, communication will not work. BPSSEL is initially set to 1[h] (19200bps). The setting is the same even when there is no EEPROM.

For information on the “SS-HQ1 Control Software”, see “SS-HQ1 Control Software Operating Manual”.

9.1.3. Communication Timing

The CXD3172AR acquires data in byte increments according to a timing determined by the communication speed from the point in time that SI falls. Serial output is output after all data have been acquired. Communication data are LSB-first.

If the number of received bytes from the leading byte totals 33 or more, all received data will be discarded. In such cases, re-execute after setting the number of bytes to 32 or less.

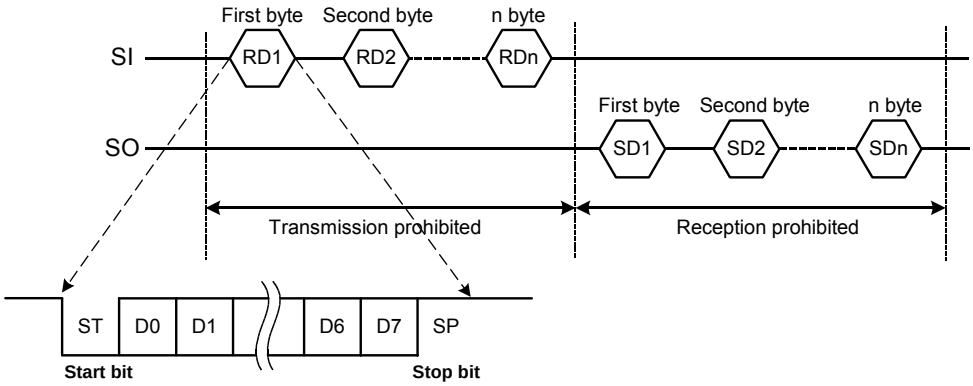


Fig 9.1-1 Communication Timing

If a communication error occurs, an error code is sent to the host after the reception of the valid byte count.

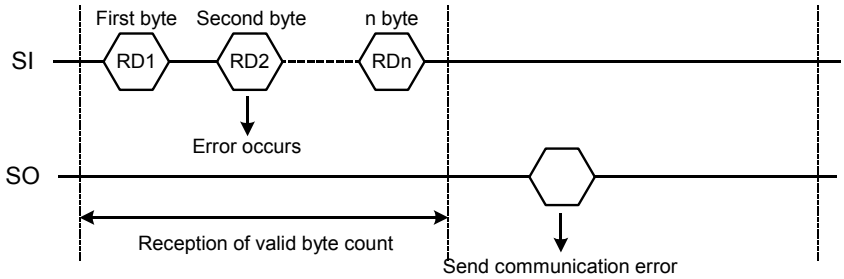


Fig 9.1-2 Communication Timing When Communication Error Occurs

If the received byte count does not change for 15 fields or more, then an error code is sent to the host as a Timeout Error, after which the state transitions to the reception wait state.

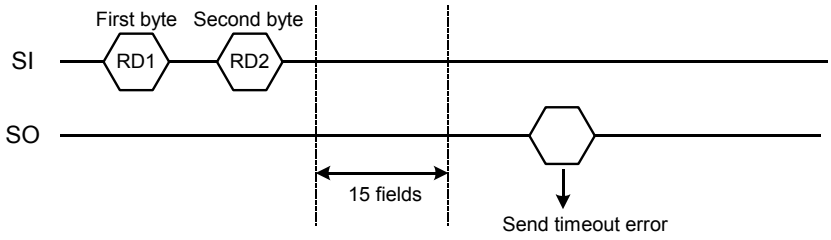


Fig 9.1-3 Communication Timing When Timeout Error Occurs

9.1.4. Communication Format

A single packet consists of 2 to 32 bytes. After receiving one packet of data, the CXD3172AR analyzes the data and performs command execution controls. See **Table 9.1-4** for the command specifications.

Data are sent in category increments. The first byte sends the byte count for the number of bytes to be sent. Commands are sent in the second byte, and communication data corresponding to the individual commands are sent in the third and subsequent bytes.

A maximum of 32 bytes can be sent and received, including heads for commands and the like, and the valid communication byte count.

Table 9.1-4 Command Specification Summary

Command	Description	Communication format						
		1	2	3	4	5	6-29	30-32
Register Category specification Read	CMD	05[h]	01[h]	CAT	Byte	Data Num 01[h]-1F[h]		
	Reply	Data Num +1	Read Data					
Register Category specification Write	CMD	Data Num +4	02[h]	CAT	Byte	Write Data		
	Reply	Data Num +1	Write Data					
EEPROM Category specification Read	CMD	05[h]	03[h]	CAT	Byte	Data Num 01[h]-1F[h]		
	Reply	Data Num +1	Read Data					
EEPROM Category specification Write	CMD	05[h]	04[h]	CAT	Byte	Data Num 01[h]-FF[h]		
	Reply	02[h]	01[h]					
EEPROM Actual address specification Read	CMD	05[h]	05[h]	EEPROM Address MSB	EEPROM Address LSB	Data Num 01[h]-1F[h]		
	Reply	Data Num +1	Read Data					
EEPROM Actual address specification Write	CMD	Data Num +4	06[h]	EEPROM Address MSB	EEPROM Address LSB	Write Data		
	Reply	02[h]	01[h]					
EEPROM Batch write	CMD	05[h]	07[h]	00[h]	01[h]	02[h]		
	Reply	02[h]	01[h]					

* CMD : A command is sent from the PC to the CXD3172AR

Reply : A reply is sent to the PC after the CXD3172AR receives a command

< Explanation of command specifications >

- Data in byte 1 : Total valid byte count in one packet
- Data in byte 2 (CMD) : Command code
  Setting range : 01[h] to 07[h]
- CAT : Write/Read category number
  Setting range : 01[h] to 18[h] (note: 05[h],16[h], and 17[h] are excluded)
- BYTE : Write/Read leading byte number
  Setting range : 01[h] ≦ BYTE ≦ Total byte count for specified category
- Data Num : Write/Read byte count
  Setting range : Presented in **Table 9.1-4** (access across different categories is not allowed)
- EEPROM Address MSB/LSB : EEPROM actual address (byte increments)
  Setting range : 0000[h] ≦ EEPROM Address ≦ 02FF[h]

Note:
Data pertaining to categories 5, 22, and 23 are not written to EEPROM, so it is not possible to specify 05[h], 16[h], or 17[h] in EEPROM category specification write/read commands.
An error occurs if the specified byte count exceeds the count for a given category in the category specification command (codes 01[h], 02[h], 03[h], and 04[h]).

< Error codes >

When a command is received, if any of the following conditions apply an error is recognized and an error code is sent to the external PC.

FC[h] : Communication error (protocol violation such as over-run)
FD[h] : Timeout error
F0[h] : Illegal valid communication byte count
F1[h] : Illegal command code
F2[h] : Illegal category number
F3[h] : Illegal byte number
F4[h] : Illegal access (e.g., communication data are outside range)
F5[h] : EEPROM BUSY state

9.1.5. Serial Communication Prohibited Period

A serial communication prohibited period is set during the time period preceding and following the VD fall. Communication from the exterior is not accepted during the periods shown in the diagram below.

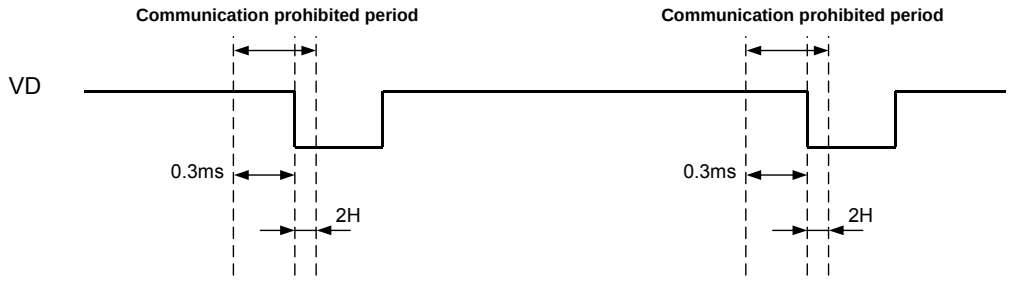


Fig 9.1-4 Serial Communication Prohibited Period

9.1.6. Important Note Regarding Communication

The serial communication clock is made by frequency-dividing the CXD3172AR's encoder clock (ECK). Therefore, communication may not work properly in cases where MODESEL is not set correctly, or when the ECK frequency shifts significantly from the recommended value.

9.1.7. When Communication is Not Used

In order to prevent operation errors in cases where the serial interface is not being used, set the pins as shown in **Table 9.1-5**.

Table 9.1-5 Pin Settings When Communication is Not Used

Pin name	Pin No	State
XCS	15	H
SCK	18	H
SIFSEL	13	L
SI	16	H or L
SO	17	Open

9.2. Communication with Peripheral ICs

9.2.1. Connection of Communication Bus between DSP (CXD3172AR) and Peripheral ICs

With the SS-HQ1 system, the DSP (CXD3172AR), EEPROM (AK6480A or BR9080A) and EVR (MB88347L) are connected through serial communication and the peripheral ICs are controlled through the DSP in order to realize various functions.

Note:

The chip-select signal assignments for peripheral ICs are fixed in the DSP's firmware, and are not customizable by the user. In addition, it is not possible to share the serial communication line with ICs other than those listed in the table below. Use the dedicated serial communication line when adding an external microcomputer to the SS-HQ1 system. For details, see "12.4 When Using the External Microcomputer".

9.2.2. Pin Connections for Serial Communication with Individual ICs

Use the pin connections in the following table to connect the DSP with peripheral ICs.

Table 9.2-1 Serial Communication Pin Connections inside the SS-HQ1 system

CXD3172AR			I / O	Connected IC	Signal name	Pin No	Remarks
Signal name		Pin No					
CASCK		9	OUT	EEPROM	SK	4	Serial clock output (DSP -> ICs)
				EVR	CLK	13	
CASO		8	OUT	EEPROM	DI	5	Serial data output (DSP -> ICs)
				EVR	DI	14	
CASI		7	IN	EEPROM	DO	6	Serial data input (ICs -> DSP)
CSROM		6	OUT	EEPROM	CS	3	EEPROM Chip Select (Low active)
(CSEVR)	S4	49	OUT	EVR	LD	12	EVR Chip Select (High edge)
	P3	94	OUT				
NC (connected prohibited)					DO	11	Use with output pin set to OPEN

* The CXD3172AR does not have a dedicated pin for CSEVR. Assign it to the S4 pin or P3 pin. For details on the setting procedure, see "3.5.2 Communication Control with an External EVR".
The S4 pin is assigned as the initial setting in the CXD3172AR.

9.2.3. Serial Communication Speed and Timing

Communication specifications and required speed vary depending on the peripheral IC. However, because the speed is always switched to the optimum speed by a program in the CXD3172AR's firmware, you do not need to worry about the format or speed. (Please use the EEPROM and EVR products recommended by Sony.) Note that these settings cannot be customized by the user.

Serial communication is performed based on each field VD, except during communication with the EEPROM. Communication with the EEPROM takes place only when a write/read command is received. The communication sequence and communication start timing for each field are optimally controlled by the firmware, so you do not need to worry about them. Note that the sequence and timing cannot be customized by the user.

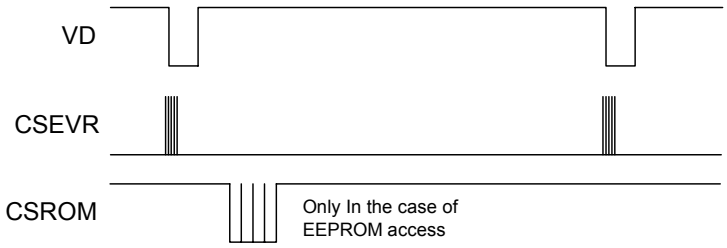


Fig 9.2-1 Overview of Chip-Select Timing in SS-HQ1 System

External EVR communication timing

Communication with an external EVR is performed every field.

The settings in the user-setting parameters EVRUSER0 to EVRUSER7 (CAT18_Byte8 to 15) are sent and applied to the MB88347L's output voltages AO1 to AO8. For details, see "3.5.2 Communication Control with an External EVR".

Following is an example which shows the timing for communication with the CXD3172AR in the MB88347L, which is recommended by Sony.

The timing for transmission from the CXD3172AR to the MB88347L varies depending on the particular MB88347L pin. Transmissions to A01 to A04 are sent every field, while transmissions to A05 to A08 are sent every four fields, rotating among them in field increments.

Table 9.2-2 External EVR Transmission Timing (for MB88347L)

Send timing	MB88347L	Field number								
		N	N+1	N+2	N+3	N+4	N+5	N+6	N+7	・・・
Send every field	AO1	*	*	*	*	*	*	*	*	*
	AO2	*	*	*	*	*	*	*	*	*
	AO3	*	*	*	*	*	*	*	*	*
	AO4	*	*	*	*	*	*	*	*	*
Send every four fields	AO5	*				*				*
	AO6		*				*			
	AO7			*				*		
	AO8				*				*	

(* Sent in fields with asterisks)

EEPROM communication timing

The CXD3172AR communicates with an EEPROM, which is used to store parameter settings. The EEPROMs recommended by Sony are AK6480AF (Asahi Kasei) and BR9080AF (Rohm). The firmware in the DSP automatically identifies the EEPROM.

Parameters are assigned in byte increments to EEPROM addresses. Addresses in byte increments are specified both when reading EEPROM address specifications and writing EEPROM address specifications.

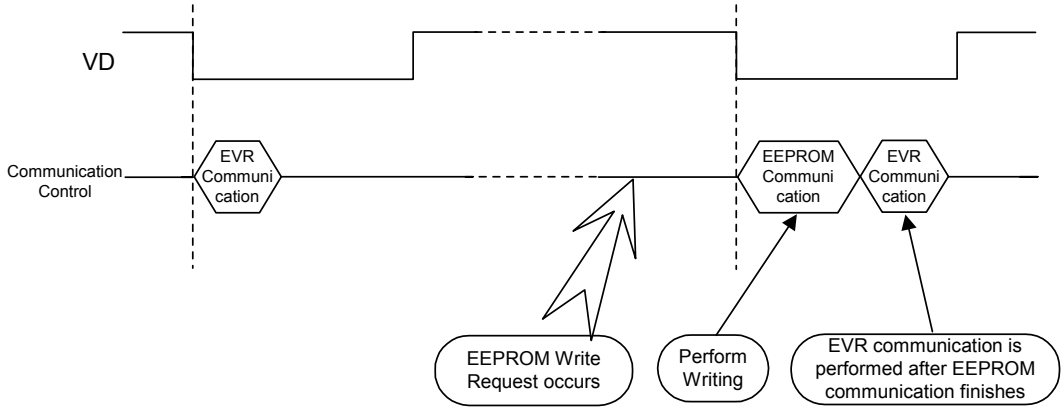


Fig 9.2-2 Overview of Communication Timing when EEPROM Write Request Occurs

The communication sequence and communication start timing for each field are optimally controlled by the firmware, so you do not need to worry about them. Note that the sequence and timing cannot be customized by the user.

Please note that if parameter controls (transmission, reception, and EEPROM access) relating to DSP peripheral ICs are performed through RS-232C communication (SS-HQ1 Control Software) or through an external microcomputer, the application of the results will be delayed by two fields or longer due delays resulting from serial communication control and calculations inside the DSP.

9.2.4. Clock for Communication with Peripheral ICs

All data are CXD3172AR design values. Communication is LSB-first.

The CASCK frequency varies depending on the frequency of the X'tal connected to the ECK (pin 88). Note that this frequency is uniquely determined by the DSP firmware and cannot be set by the user.

Table 9.2-3 Serial Communication Clock Frequency

Clock frequency (MHz)	
X'tal(ECK)	CASCK
27.00000	0.84
28.37500	0.89
28.63636	0.89
35.46895	1.11
37.87500	1.18
38.13986	1.19

External EVR

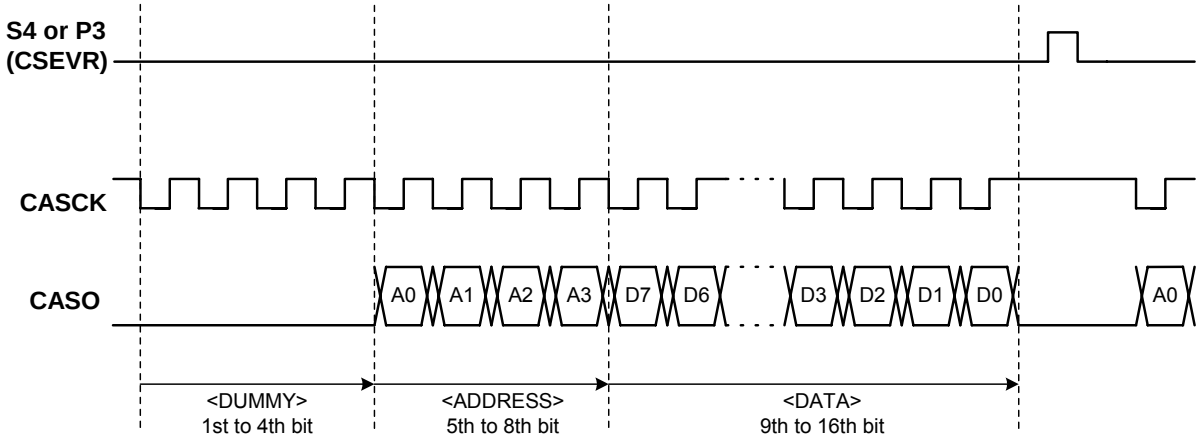


Fig 9.2-3 Communication Protocol - External EVR -

EEPROM

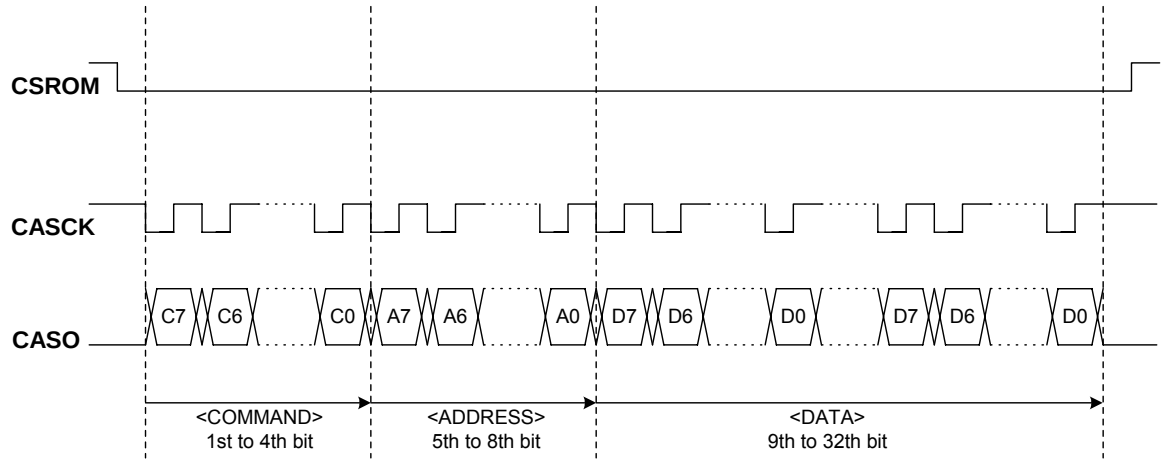


Fig 9.2-4 Communication Protocol – EEPROM Write -

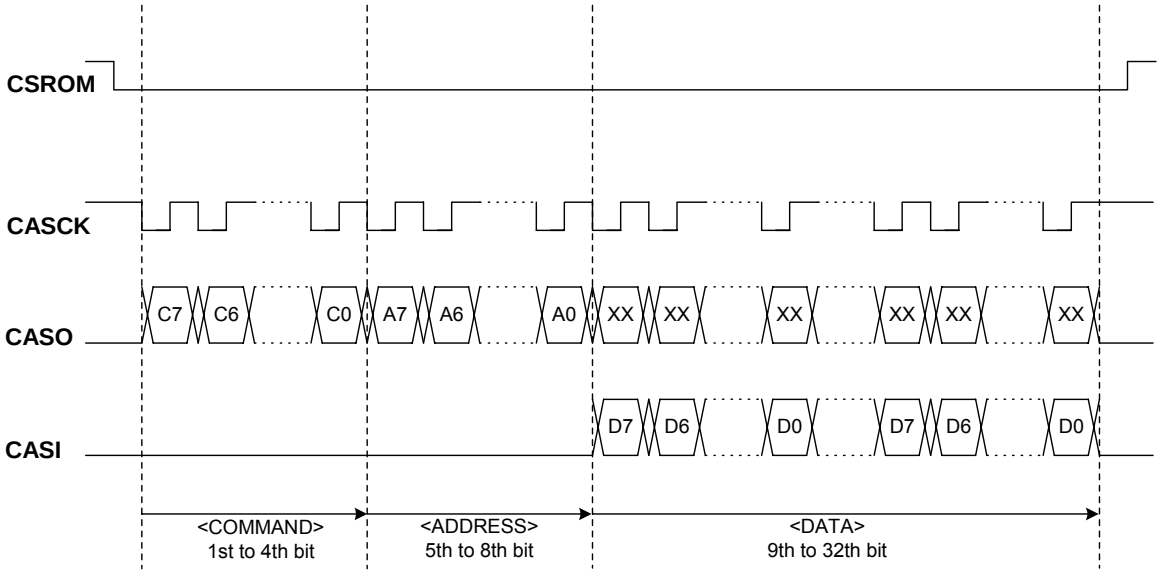


Fig 9.2-5 Communication Protocol – EEPROM Read –

The SS-HQ1 system does not have a pin for inputting the EEPROM BUSY state. Therefore, the BUSY state is monitored using a timer, with a WAIT process (10ms or longer) performed each time one word is written.
The timer setting is determined based on 38MHz, which is the fastest of the clock systems selectable by the SS-HQ1 system. The timer setting is the same regardless of the clock system. Therefore, the write time varies depending on the selected clock system.

Table 9.2-4 EEPROM BUSY WAIT Time

X'tal frequency (MHz)	EEPROM BUSY WAIT (ms)
27.00000	14.7
28.37500	14.0
28.63636	13.9
35.46895	11.2
37.87500	10.5
38.13986	10.4

EEPROM initial recognition process

The EEPROM is initially recognized based on data written to the EEPROM's 00[h] address.
The following are determined during the initial recognition process:

1. Is communication with the EEPROM possible?
2. What is the EEPROM type (Asahi Kasei or Rohm)?
3. Are valid data written to the EEPROM?

Parameter initialization by EEPROM

Parameters are initialized as follows based on the results of the judgments in the above initial recognition process.

1. If the EEPROM data are judged to be valid:
   EEPROM data are read and parameters are initialized.
2. If the EEPROM data are judged to be invalid:
   Parameters are initialized based on the ROM table in the DSP.
   In this case, if the port driver (CXD3172AR's P12 to P15) MODESEL setting does not match the operating mode, then the operation may not work properly and communication may fail.

Limitations when Using EEPROM

When using an empty EEPROM for the first time, first perform a full EEPROM write.
If the system starts without an EEPROM, do not perform an EEPROM category specification write (a full write can be performed).

If the EEPROM does not contain valid data, and the port driver (CXD3172AR's P12 to P15) MODESEL setting does not match the operating mode, then the operation may not work properly and communication may fail. In such cases, it is not possible to write initial value data to the EEPROM.
Change the port driver MODESEL setting so that it matches the operating mode so that the system runs properly, and then write the initial value data to the EEPROM.
Once the initial value data are written to the EEPROM (in cases where the EEPROM contains valid data), the MODESEL value written to the EEPROM will be applied, so another function can be assigned to port driver MODESEL.

10. Description of Operation of Each Function

10.1. Port Driver Function

10.1.1. Port Driver Function Description

The SS-HQ1 system has port driver functions.
With port driver functions, internal parameters can be used for operations by means of switches connected to P0 to P15 (Pins 91 to 94, 96 to 99, 76 to 80, and 82 to 84) of CXD3172AR.

Input Port Driver

Each port can be assigned arbitrary parameters, and the parameter setting values can be switched by switches connected to the respective ports, even without external communication.

(Sample Application)

- CPUHOLD Assign the 1-bit parameter to P0 Switch OFF (Low) = 0[h]/ON (High) = 1[h].
- AESPEED Assign the 8-bit parameter to P2 Switch OFF (Low) = FF[h]/ON (High) = 20[h].

Output Port Driver

Each port can be assigned arbitrary 1-bit parameters, and changes in the 1-bit parameters can be monitored from outside the system by sending the parameter status (High or Low) from the ports.

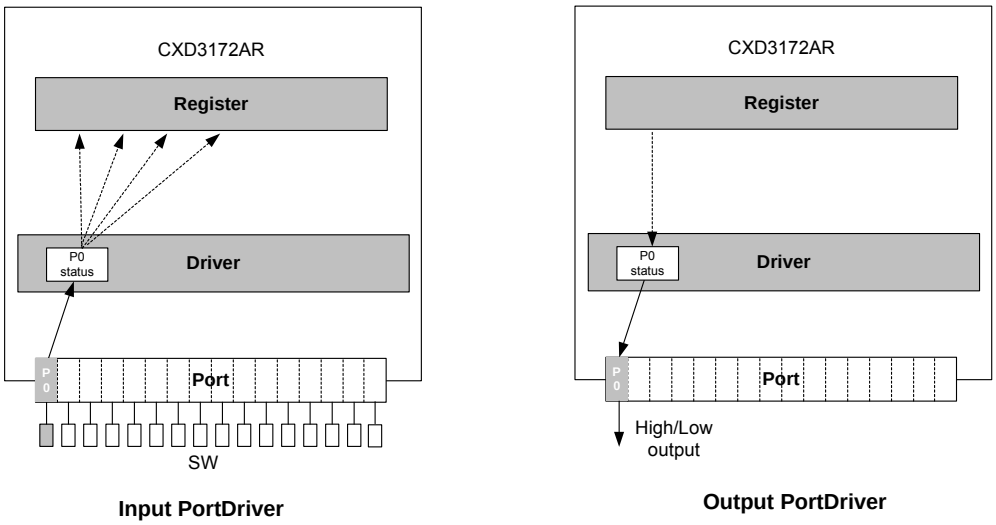


Fig 10.1-1 General Concept

10.1.2. Port Driver Setting Method

This section explains the setting method for the port driver functions.

Description of Port Driver Parameters

Port drivers are configured by means of parameter CAT20 Port.

Complete the settings of each port as follows.

Here, "**n**" represents the port number (0 to 15).

Table 10.1-1 Parameters for Specifying Categories

P "n" CAT			
bit	Parameter	Input port setting	Output port setting
0	P**n**CAT	0: Port driver does not function 1 to 24: Specify the category number 5, 21, and 22: Port driver does not function	
1			
2			
3			
4			
5	P**n**LSB	0 to 7: Specifies LSB of arbitrary parameters	(Unused)
6			
7			

Table 10.1-2 Parameters for Specifying Bytes

PDR "n" Byte			
bit	Parameter	Input port setting	Output port setting
0	P**n**Byte	0: Port driver does not function 1 to 127: Specify the byte number	
1			
2			
3			
4			
5			
6			
7	P**n**IOSEL	0: Input port setting	1: Output port setting

Table 10.1-3 Parameters for Specifying Bits

PDR " n " bit			
bit	**Parameter**	**Input port setting**	**Output port setting**
0	P**n**ADJ	Coefficient parameter 4 bits	(Unused)
1			
2			
3			
4	P**n**WID	0 to 15: bit width (1 to 16 bits)	(Unused)
5			
6			
7			

- **PnCAT (Category Number)**

  PnCAT specifies the category number of arbitrary parameters to be controlled by the port driver.
  - If set to "0[h]", the port will not function as a port driver.
  - It will not function as a port driver if a nonexistent category or CAT5, 21, or 22 is selected.

- **PnLSB (LSB of the Designated Parameter)**

  PnLSB specifies LSB of arbitrary parameters.
  - If it is a parameter of 1-bit width, that parameter itself becomes the LSB.

- **PnBYTE (Byte Number)**

  PnBYTE specifies the byte number of the arbitrary parameter to be controlled by the port driver.
  - If set to "0[h]", the port will not function as a port driver.
  - It will not function as a port driver if the setting has a nonexistent byte number in the category to be specified.

- **PnIOSEL (Port I/O Selection)**

  PnIOSEL sets a port as an input or an output.
  - 0: Input port setting
  - 1: Output port setting

- **PnADJ (Coefficient)**

  PnADJ is used when an input port driver controls a parameter 2 bit or more.

  The arbitrary parameter value written to EEPROM is multiplied by the coefficient which is from 0 to 2 times.
  - If the port input is Low

    The value written to EEPROM is reflected in a parameter.
  - If the port input is High

  The value which is calculated by using the value written to EEPROM and setting value of PnADJ such as following method is reflected in a parameter.

When PnADJ sets it as 0[h]-7[h]

The coefficient can be selected from 0 to 0.875 times.

The parameter value = The value written to EEPROM x PnADJ / 8
(This parameter value is set by high input of port driver.)

When an input port is “High”, the setting value is calculated by multiplying the parameter value written to EEPROM by the coefficient of the following table.

Table 10.1-4 The coefficient.(When PNADJ sets it as 0[h]-7[h])

PnADJ Value	0[h]	1[h]	2[h]	3[h]	4[h]	5[h]	6[h]	7[h]
The coefficient by which a parameter is multiplied (PnADJ／8)	0	0.125	0.25	0.375	0.5	0.625	0.75	0.875

For example) The value written to EEPROM = 60[h], PnADJ = 5[h]
In the case of Low : 60[h]
In the case of High: 60[h](96[d]) × 5[h](0.625) = 3C[h](60[d])
Thus, the parameter is changed as 60[h]/3C[h] by Low/High of port input.

When PnADJ sets it as 8 [h]-F[h]

The coefficient can be selected from 1.125 times to twice.

The parameter value = The value written to EEPROM x (PnADJ + 1) / 8
(This parameter value is set by high input of port driver.)

When an input port is “High”, the setting value is calculated by multiplying the parameter value written to EEPROM by the coefficient of the following table.

Table 10.1-5 The coefficient. (When PnADJ sets it as 8[h]-F[h])

PnADJ Value	8[h]	9[h]	A[h]	B[h]	C[h]	D[h]	E[h]	F[h]
The coefficient by which a parameter is multiplied ((PnADJ+1) / 8)	1.125	1.25	1.375	1.5	1.625	1.75	1.875	2

For example) The value written to EEPROM = 59[h], PnADJ = A[h]
In the case of Low : 59[h]
In the case of High: 59[h](89[d]) × A[h](1.375) = 122.375[d] –> 122[d] = 7A[h]
Thus, the parameter is changed as 59[h]/7A[h] by Low/High of port input.
122.375[d] of an operation result turns into 122[d] by rounding-off processing.
*It is described later about rounding-off processing.

* When the setting value changes to values other than 0[h] and 0[h], the port input should not be set to 0[h] by Low (value written to EEPROM).
Coefficient operation is performed to the value written to EEPROM. Thus, the change of the value by the Low/High input to a port driver cannot be performed. Because the operation result will also be set to 0[h] if the value written to EEPROM is 0[h].

* When the port is set to High, the parameter cannot be set to 1 times of value written to EEPROM.
When the port is set to Low, the parameter set to 1 times of value written to EEPROM.

* The setup of a port input (High) can be set only to the fixed multiple of a value written to EEPROM.
(See: **Table 10.1-4 Table 10.1-5**,)
If setting parameter to arbitrary values, assign plural port drivers to each 1bit of multi-bit parameter For example, if the parameter is 3-bit width, it can be set to arbitrary values by using three port drivers.

Rounding-off processing of the operation result

The value below the decimal point of an operation result is rounded off.

Overflow Processing

If the calculation results exceed the specified bit width, data is incorporated that is within the range of the bit width from the specified LSB. Thus, complete the settings so that the calculation results do not exceed the specified bit width.

▪ **PnWID (Bit Width)**

PnWID specifies the bit width of the arbitrary parameter to be controlled by the port driver.
Set the width from 1 to 16 bits.

If the bit width is 1 bit

For 1-bit width, if the initial value is "0[h]", whatever coefficient from is used to multiply it in PnADJ, the result will be "0[h]". Thus, when the bit width is 1 (and PnWID = 0[h]), use fixed data as shown below, following the High/Low input port designation.

- Port input (Low) : The corresponding parameter is fixed at "0[h]"
- Port input (High) : The corresponding parameter is fixed at "1[h]"

If the bit width is 2 bits or more

For parameters of 2 bits or more, specify the data following the High/Low designation of the input port as follows.

- Port input (Low) : The corresponding parameter uses the initial value (the parameter data when the port driver was initialized)
- Port input (High) : The corresponding parameter uses a value equal to the initial value multiplied by an arbitrary coefficient (PnADJ)

10.1.3. Parameter Setting Instructions

To control a 1-bit parameter with the port driver

(Example 1)

Assign PGON (CAT9_Byte36_bit3) to P2 of the port driver, and from High or Low input to P2 (Pin 93), generate a pattern generator.

- Port input (Low) : Regular images (CAT9_Byte36_bit3 = 0[h])
- Port input (High) : Display the pattern generator (CAT9_Byte36_bit3 = 1[h])

[Parameter Setting Details]

P2ADJ = 0[h] (PGON is 1-bit parameter. Thus, the coefficient is irrelevant. P1ADJ is set as 0[h].)

P2WID = 0[h] (PGON is 1-bit parameter. Thus,P2WID is set as 0[h].)

P2Byte = 24h (PGON is the parameter of 36th Byte of CAT9. Thus,P2Byte is set as 24[h].)

* Parameter value is set up by hex decimal. Thus, it changes into 36[d] from 24[h].

P2IOSEL = 0[h] (P2 is set as an input. Thus,P2IOSEL is set as 0[h].)

P2CAT = 9[h] (PGON is the parameter of CAT9. Thus,P2CAT is set as 9[h].)

P2LSB = 3[h] (LSB of PGON is the 3rd bit. Thus,P2LSB is set as 3[h].)

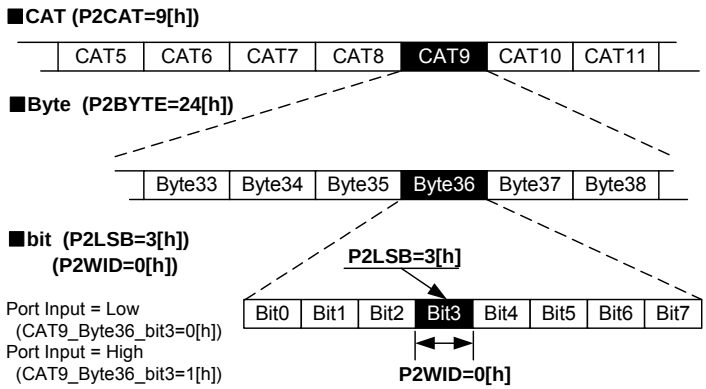


Fig 10.1-2 SETTING IMAGE

To control a multi-bit parameter with the port driver

(Example 2)

Assign the 8-bit wide parameters of PGPAT (CAT2_Byte37_bit0-7) to P1 of the port driver. From High or Low input to P1 (Pin 92), change the GAIN value of RYGAIN1.

- Port input (Low) : RYGAIN1=3Fh setting (CAT2_Byte37_bit0-7 = 3F[h])
- Port input (High) : RYGAIN1=5Fh setting (CAT2_Byte37_bit0-7 = 5F[h])

* At first, set the value of RYGAIN1 to 3Fh and write to EEPROM.
(The setting value in case a port input is Low)

[Parameter Setting Details]

P1ADJ = B[h] (***1**)
P1WID = 7[h] (RYGAIN1 is 8-bit parameter. Thus,P1WID is set as 7[h].)
P1Byte = 25［h］(RYGAIN1 is the parameter of 37th Byte of CAT2. Thus,P1Byte is set as 25[h].)
* Parameter value is set up by hex decimal.
Thus, it changes into 36d from 24[h].
P1IOSEL= 0[h] (P1 is set as an input. Thus,P1IOSEL is set as 0[h].)
P1CAT = 2[h] (RYGAIN1 is the parameter of CAT2. Thus,P1CAT is set as 2[h].)
P1LSB = 0[h] (LSB of RYGAIN1 is the 0th bit. Thus,P1LSB is set as 0[h].)

***1** The P1ADJ setting

The parameter value is 1.5 times of value written to EEPROM. Thus, use the following formula.

(Formula) Parameter value = Value written to EEPROM × (P1ADJ Value + 1) / 8
= 3F[h] × (B[h] + 1) / 8
= 63[d] × (11[d]+1) / 8
= 94.5[d] (The operation result is rounded off by Rounding-off processing.)
= 95[d] (5F[h])

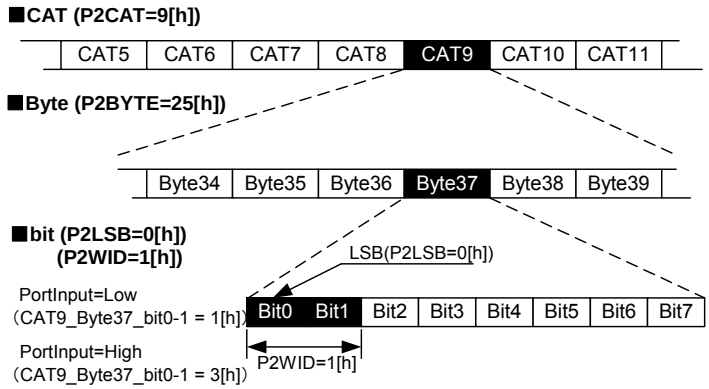


Fig 10.1-3 SETTING IMAGE

To watch the state of a parameter with the output port driver

(Example 3)

Assign MIRROR (CAT1_Byte1_bit4) to P3 of the port driver, and set the output of P3 (94PIN) to change High or Low by parameter value of MIRROR.

- Port input (Low) : Normal image (CAT1_Byte1_bit4 = 0[h])
- Port input (High) : MIRROR image (CAT1_Byte1_bit4 = 1[h])

[Parameter Setting Details]

P3ADJ = 0[h] (PnADJ is not used when it is set as an output port. So please set to 0[h].)
P3WID = 0[h] (Please set to 0[h], because MIRROR is 1bit parameter.)
P3Byte = 1[h] (Please set to 1[h], because MIRROR is the parameter of 1st Byte of CAT1.)
P3IOSEL = 1[h] (Please set to 0[h], because it is set as an output.)
P3CAT = 1[h] (Please set to 1[h], because MIRROR is the parameter of CAT1.)
P3LSB = 4[h] (Please set to 4[h], because LSB of MIRROR is the 4th bit.)

*1 port supports 1bit, when you can watch the state of parameter from output port. Therefore the ports of number of bits are required, when you would like to watch the parameters with output ports.

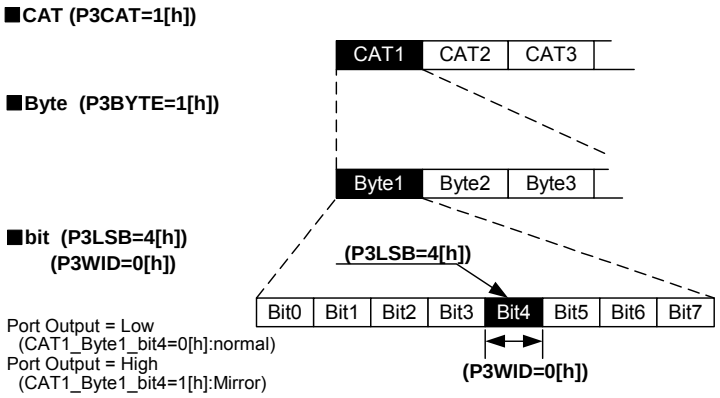


Fig 10.1-4 SETTING IMAGE

10.1.4. Field Processing for Each Port Driver

To reduce the processing load, the SS-HQ1 system divides the port driver processing.
Of the 16 ports, four are controlled by individual 1V (fields), and processing for the other 12 is by every 3V (fields).

Ports processed by 1V each: P0 to P3 (4 ports)
Ports processed by 3V each: P4 to P15 (12 ports)

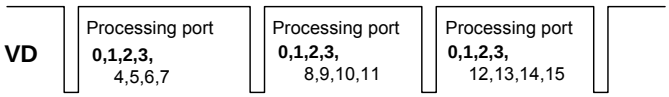


Fig 10.1-5 Control of Port Drivers

10.1.5. Port Driver Initial Settings, Depending on Presence of EEPROM

Port Driver Initial Settings When EEPROM is Valid

The parameters are initialized by data written in EEPROM.

Port Driver Initial Settings When EEPROM is Invalid

When EEPROM is invalid or not connected, the port drivers function by means of initial values stored in the CXD3172AR.

Table 10.1-6 Port Driver Initial Settings When EEPROM is Invalid

Port Name	Parameter Name	Category	Description
P0	AWBMODE	CAT15_Byte1_bit0	AWB mode settings
P1		CAT15_Byte1_bit1	
P2		CAT15_Byte1_bit2	
P3	CRLSON	CAT12_Byte11_bit0	Color rolling control mode
P4	BLCOFF	CAT14_Byte1_bit2	Backlight compensation mode
P5	AEREF	CAT14_Byte1_bit3	AE parameter reference switching
P6	NORMFLC	CAT14_Byte2_bit0	Flicker less mode
P7	AGCMAX	CAT14_Byte1_bit4	AGC switching
P8	AEME	CAT14_Byte1_bit0	AE/ME switching
P9	AESHUT	CAT14_Byte1_bit6	AE shutter mode
P10	SGMODE0	CAT17_Byte17_bit0	SGMODE 0-bit switching
P11	GAMSEL	CAT12_Byte7_bit0	Gamma parameter switching
P12	MODESEL	CAT12_Byte1_bit0	DSP operation mode switching
P13		CAT12_Byte1_bit1	
P14		CAT12_Byte1_bit2	
P15		CAT12_Byte1_bit3	

10.1.6. Precautions for Port Driver Configuration

• Parameters assigned to port drivers cannot be externally controlled. When external control is desired, control must be terminated by removing the port driver assignment or by completing the following parameter settings.

  • PDRHOLD(CAT12_Byte5_bit5) = 1[h]
  • CPUHOLD(CAT12_Byte5_bit0) = 1[h]

• The priority ranking of the parameter setting methods is as follows.

1. Port driver control
2. External communication control (computer, external microcontroller, and so on)
3. EEPROM setting values
4. CXD3172AR register setting values

• The parameter settings assigned to the port drivers are given priority, so note that the settings written in EEPROM will be disabled.

• To enable the EEPROM settings, do not assign the parameters to port drivers.

10.1.7. Port Driver Setting Example

The basic setting method for port drivers is as follows.

If reset after writing to EEPROM

(Example)

Set up the switching control of the 8-bit parameter AESPEED. (CAT14_Byte12_bit0-7).

AESPEED is set to FF[h] when the input port P0 is a "low."

AESPEED is set to 20[h] when the input port P0 is a "High."

(Setting Procedure)

1. Set PDR to OFF (and set PDRHOLD = 1[h]).
2. Set the port driver initial value when the port input is "Low" (make the initial value FF[h]).
3. Set FF[h] in AESPEED (CAT14_Byte12_bit0-7).
4. Set the port P0 setting parameter (CAT20). (See: 10.1.3 Parameter Setting Instructions)
5. Write CAT20 to EEPROM.
6. Reset. -> Port driver initialization
7. Set PDR to ON (and set PDRHOLD = 0[h]).
8. Afterward, the parameter will be switched to AESPEED = FF[h] when the P0 port input is "Low" and to AESPEED = 20[h] when it is "High".

If port driver initialization is performed through external communication

(Example)

Set up the switching control of the 8-bit parameter AESPEED. (CAT14_Byte12_bit0-7).

AESPEED is set to FF[h] when the input port P0 is a "low."

AESPEED is set to 20[h] when the input port P0 is a "High."

(Setting Procedure)

1. Set PDR to OFF (and set PDRHOLD = 1[h]).
2. Set the port driver initial value when the port input is "Low" (make the initial value FF[h]).
3. Set FF[h] in AESPEED (CAT14_Byte12_bit0-7).
4. Set the port P0 setting parameter (CAT20). (See: 10.1.3 Parameter Setting Instructions)
5. Up to this point, the procedure is the same as for the example "If reset after writing to EEPROM."
6. Perform port driver initialization through external communication.
7. Set PDR to ON (and set PDRHOLD = 0[h]).
8. Afterward, the parameter will be switched to AESPEED = FF[h] when the P0 port input is "Low" and to AESPEED = 20[h] when it is "High".

In the case of this setting method, these port driver settings become invalid after reset because they are not written to EEPROM. Thus, if you want to enable these settings as the default settings after reset, write CAT20 to EEPROM.

If reset without EEPROM

When reset without EEPROM, the port drivers function by default settings stored in the system.

The default settings without EEPROM are the same as cited in "10.1.5Port Driver Initial Settings, Depending on Presence of EEPROM."

10.1.8. Conditions for Disabling the Port Drivers

Port driver control is disabled under the following conditions.

Suppression by the parameters

Port drivers do not function with port driver parameters CPUHOLD = 1[h] or PDRHOLD = 1[h].

Judgment to disable them from setting details of the parameter CAT20 PDR corresponding to each port

If the parameter settings meet the following conditions, port drivers set by means of these settings are disabled.

1. If the category number is "0".
2. If the category number exceeds the maximum category number.
3. If the byte number is "0".
4. If the byte number exceeds the maximum byte number of each category.
5. If the byte number with MSB of the data to specify exceeds the maximum byte number of each category.

If CAT5 (OPDWND1), CAT21 (SOUT1), or CAT22 (SOUT2) are set

Specifying CAT5, CAT21, or CAT22 in the parameter number disables the port drivers.

If combined-use signal output is enabled

Ports of the port drivers (P0 to P15) serve as combined-use output ports for digital out signal output, VDHD output, OPD Window output, and external EVR CS signal output. As shown in the following table, port drivers will be disabled from the settings of parameters YDSEL (CAT1_Byte7_bit4), CDSEL (CAT1_Byte7_bit5), VHOUT (CAT1_Byte11_bit6), UWINDOUT (CAT16_Byte8_bit7), and CSEVRSEL (CAT12_Byte10_bit1).

If used as REC601 output, none of the port drivers can be used.
If used as REC656 output, P8 to P15 are disabled. If the settings for P3 to P6 are OPD Window out, VDHD out, or external EVR CS signal output, respectively, the port drivers are disabled.

Table 10.1-7 Combined-Use Terminals for Port Driver Output

Signal output	YDSEL (MSB side)	CDSEL (LSB side)	VHOUT	UWINDOUT	CSEVRSEL	Port driver control
REC656	1	0	Don't care	Don't care	Don't care	P8 to P15 disabled
REC601	Don't care	1	Don't care	Don't care	Don't care	P0 to P15 disabled
VDHD out	Don't care	0	1	Don't care	Don't care	P5 and P6 disabled
OPD Window out	Don't care	0	Don't care	1	Don't care	P4 disabled
External EVR CS signal output	Don't care	0	Don't care	Don't care	1	P3 disabled

10.2. Y Signal Processing

10.2.1. Y (Luminance Signal) Processing Flow

The Y (luminance signal) signal is processed through the block shown below.

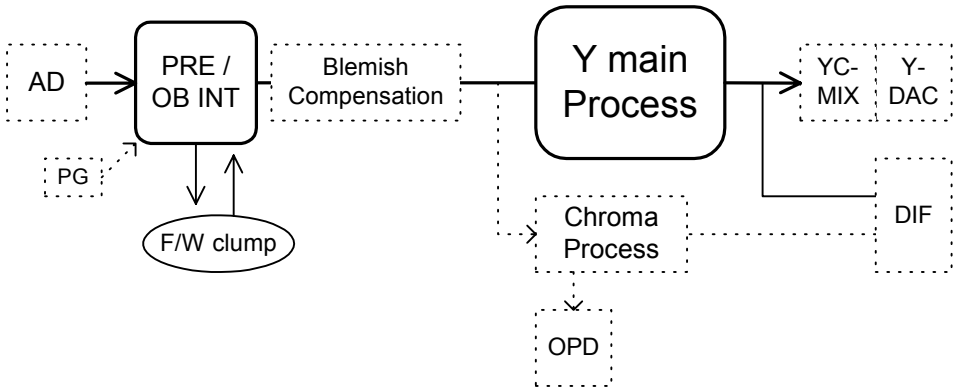


Fig 10.2-1 Overall flow of Y signal processing

Signal processing is divided into two stages: common signal processing (pre-processing), which occurs before branching into OPD (detection integration) and chroma processing; and main processing, which applies only to the Y signal.

10.2.2. Pre-Block Signal Processing

Pre-block (PRE / OB INT) signal processing includes the following:

- Replacement with built-in PG signal -> See 12.5 “Pattern Generator (PG)”.
- System delay adjustment
- Black level digital clamping
- Blemish detection and compensation -> See 11.2 “CCD blemish detection and compensation”.
- Mirror -> See 10.9 “Mirror Function”.

System Delay

System Delay is to set the signal processing reference points (effective video start positions) in the DSP.

If the reference points are off, the preceding or following OB pixels may appear in the video output, or the firmware may not work properly.

Be sure to set the system correspondence values shown in the following table.

Table 10.2-1 System delay correspondence values

Parameter	Address	510H NTSC	510H PAL	760H NTSC	760H PAL
SYSDLY	CAT8_Byte2_bit0-3	D[h]	D[h]	F[h]	F[h]

Black level digital clamping

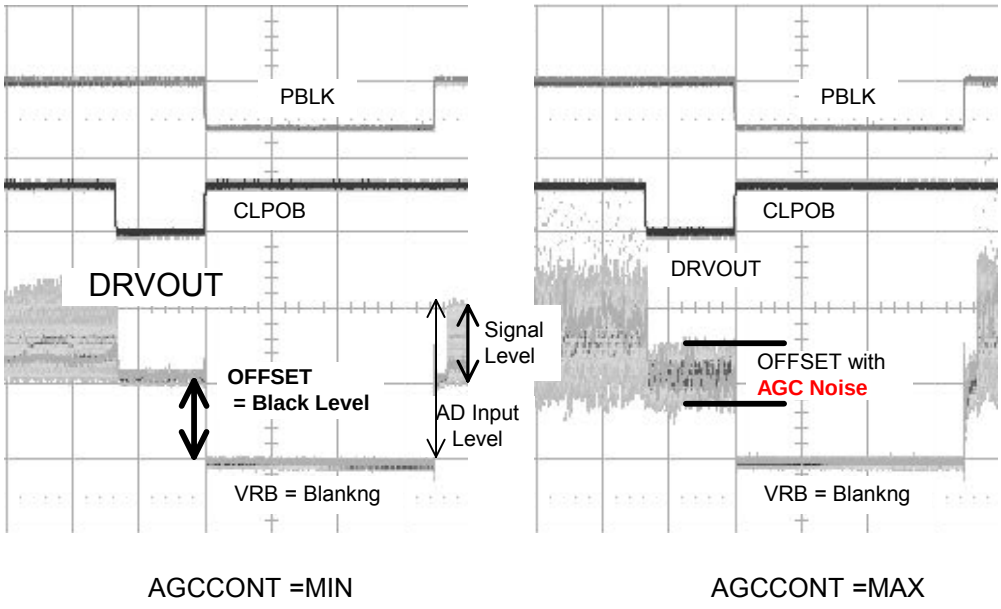


Fig 10.2-2 DRVOUT (AD input signal) and offset level

Under conditions where AGC is raised, such as when shooting a dark subject, the AD input signal (i.e., CXA2096N pin4 DRVOUT signal) contains a noise component. A DC offset (50 to 100[mV]) is added to the DRVOUT signal in order to prevent the black level (OB area output of CCD) becoming under VRB level. (For details, see the CXA2096N product specifications.) Therefore, the same DC offset is also added to the effective video signal.

The processing of removing the DC offset equivalent to the black level from the AD-converted effective video signal inside the DSP is called digital clamping.

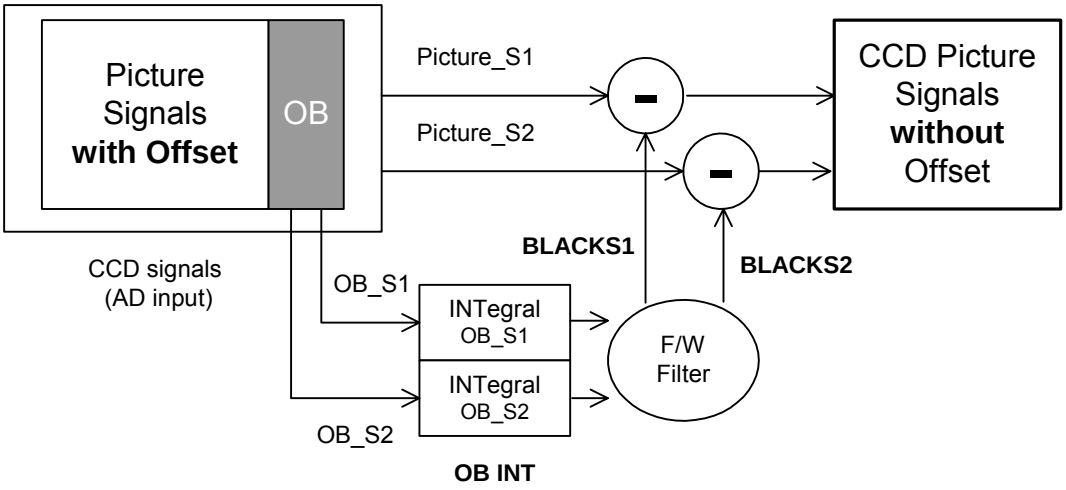


Fig 10.2-3 Digital clamping process

Table 10.2-2 Digital clamp parameter

Parameter	Address	Description
OBLKS1	CAT22_Byte6_bit0-3 (MSB) CAT22_Byte4_bit0-7 (LSB)	S1 series OB area integrated value (output-only parameter). BLACKS1 is calculated by the internal firmware.
OBLKS2	CAT22_Byte6_bit4-7 (MSB) CAT22_Byte5_bit0-7 (LSB)	S2 series OB area integrated value (output-only parameter). BLACKS2 is calculated by the internal firmware.
BLACKS1	CAT2_Byte55_bit0-7	Black level of S1 series (control subject of firmware). Used to remove S1 series offset level.
BLACKS2	CAT2_Byte56_bit0-7	Black level of S2 series (control subject of firmware). Used to remove S2 series offset level.
Remarks If CLMPHOLD (CAT12_Byte5_bit3) is 1, then the processing of overwriting BLACKS1 and BLACKS2 is stopped. Do not set BLACKS1 and BLACKS2 to port driver input control.		

<Reference Information>

In the digital clamping process, the S1 series and S2 series are separately integrated to determine the accurate black levels (BLACKS1 and BLACKS2) for each system based on the CCD pixel array.

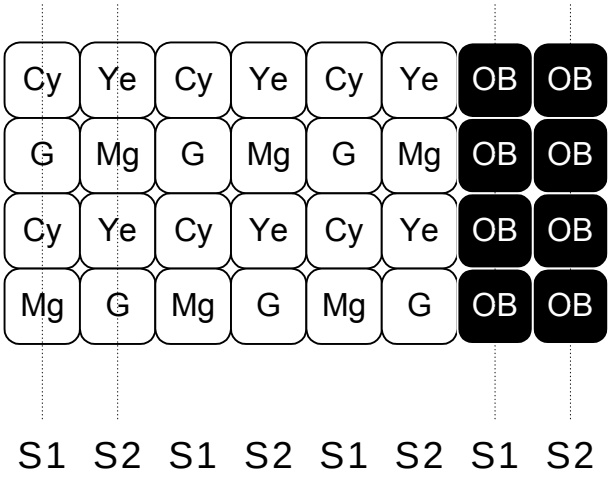


Fig 10.2-4 (Reference) CCD pixel array and S1/S2 series

If this signal process is not performed properly, the black level will be off, resulting in significant errors in subsequent Y signal processing, chroma signal processing, AE/AWB control, etc. Even if an external microcomputer is used to externally control AE or AWB, the CXD3172AR's internal firmware should be used for the digital clamping process.

10.2.3. Y Signal Main Process

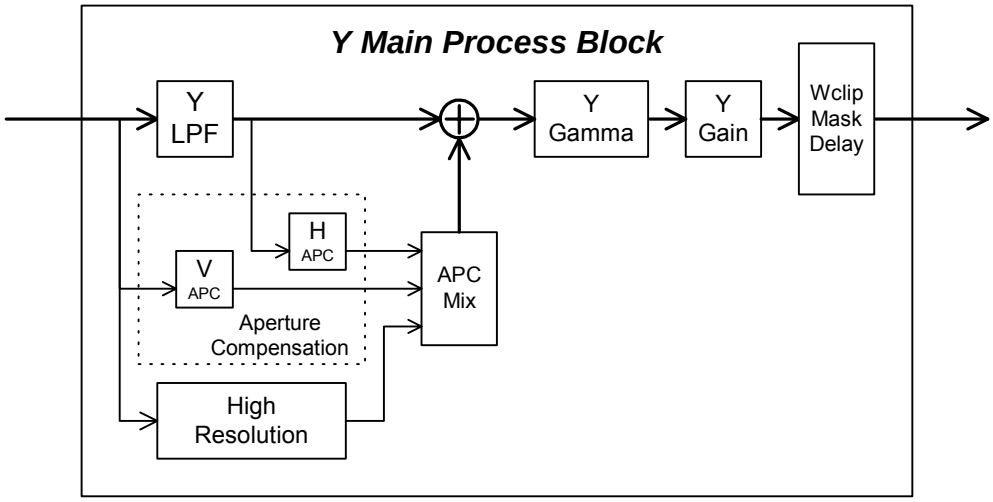


Fig 10.2-5 Y Signal Main Process block

The Y signal main process includes the following:

- High Resolution Mode -> See 10.2.4 “High Resolution Mode”.
- Low pass filter (Y-LPF)
- Aperture compensation -> See 10.2.5 “Aperture Compensation Function”.
- Detail enhancement
- Aperture compensation suppression -> See 10.8 “Suppress Function”.
- Gamma curve correction -> See 10.4 “Variable Gamma Function”
- Negative output
- SETUP level addition
- High luminance clip (White Clip)
- Output delay

Y-LPF

This low pass filter removes the carrier component of the CCD color on-chip filter.

This filter can be bypassed by setting YLPFOFF (CAT2_Byte1_bit3) to 1[h].

Set YLPFOFF to 0[h] in order to remove carrier component interference when using high resolution mode, aperture compensation, etc.

Detail Enhancement

When DEON (CAT2_ Byte10_bit7) is set to 1[h], the SS-HQ1 system's built-in detail enhancer operates, enhancing faint signals that are hidden by ordinary aperture compensation.
The available enhancement level settings are as follows:
DELVSEL (CAT2_ Byte11_bit0) = 0 [h]: Weak; 1 [h]: Strong

Negative Output

This function black/white inverts the Y signal after gamma curve correction.
Negative output is used when POSNEG (CAT2_ Byte10_bit6) is set to 1[h]. (The chroma signal is simultaneously inverted to a complementary color.)

SETUP Level Addition

A setup level can be added to the video output pedestal.
The results are as follows:
NTSC: SETUP (CAT2_ Byte10_bit0-5) = 0C [h]: 7.5 [IRE]
PAL: SETUP = 00 [h]: 0 [%]
This is not affected by gamma curve correction.

High Luminance Clip (White Clip)

The high luminance level can be clipped in the final output of the Y signal. This function can be used as a maximum output limiter.

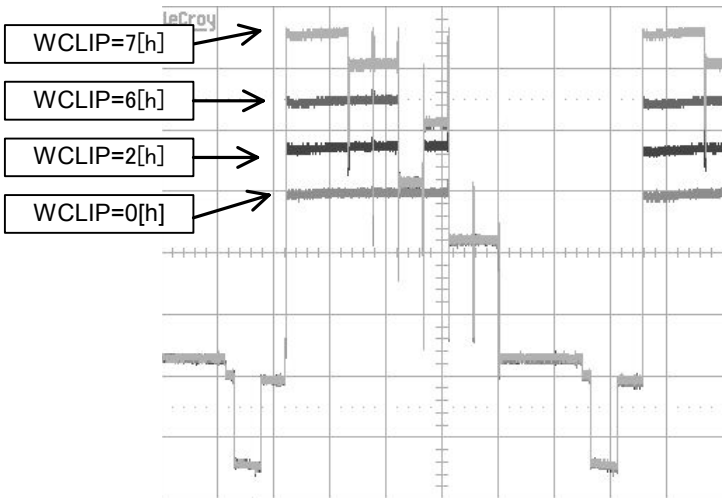


Fig 10.2-6 Example of high luminance clip (White Clip)

Table 10.2-3 High luminance clip (White Clip) parameter

Parameter	Address	Description	Setting value
WCLIP	CAT2_Byte9_bit4-6	Clips luminance signal output level	0 [h]: 78%, 1 [h] : 89%, 2 [h]: 100%, 3 [h]: 105%, 4 [h] :111%, 5 [h]: 116%, 6 [h]: 120%, 7 [h]: 153%

Output Delay

The Y signal output can be independently delayed. This function can be used to add a delay difference compared to the chroma signal output or sync signal output.

Table 10.2-4 Y signal output delay parameter

Parameter	Address	Description	Setting value
YDLY	CAT2_Byte11_bit1-4	Independently delays the luminance signal output	0 [h] -F [h]: 0- 15 pixel delay

10.2.4. High resolution mode

The high resolution mode of SS-HQ1 is able to realize by using a general lens and general optical LPF. We use the optical LPF of Kyocera Kinseki, Ltd. in our evaluation board. Please refer to the chapter “3.10 Optical Filters” about the details of optical LPF.

In addition, it can check more effectively by the following setup.

• 760H system

• Without external Y-LPF

• DACMODE(CAT1_Byte3_bit2)=1[h] (YC separate)

High resolution processing

In SS-HQ1, as shown in the following figure, the newly generated high frequency horizontal aperture signal is added to a luminosity signal processing system.

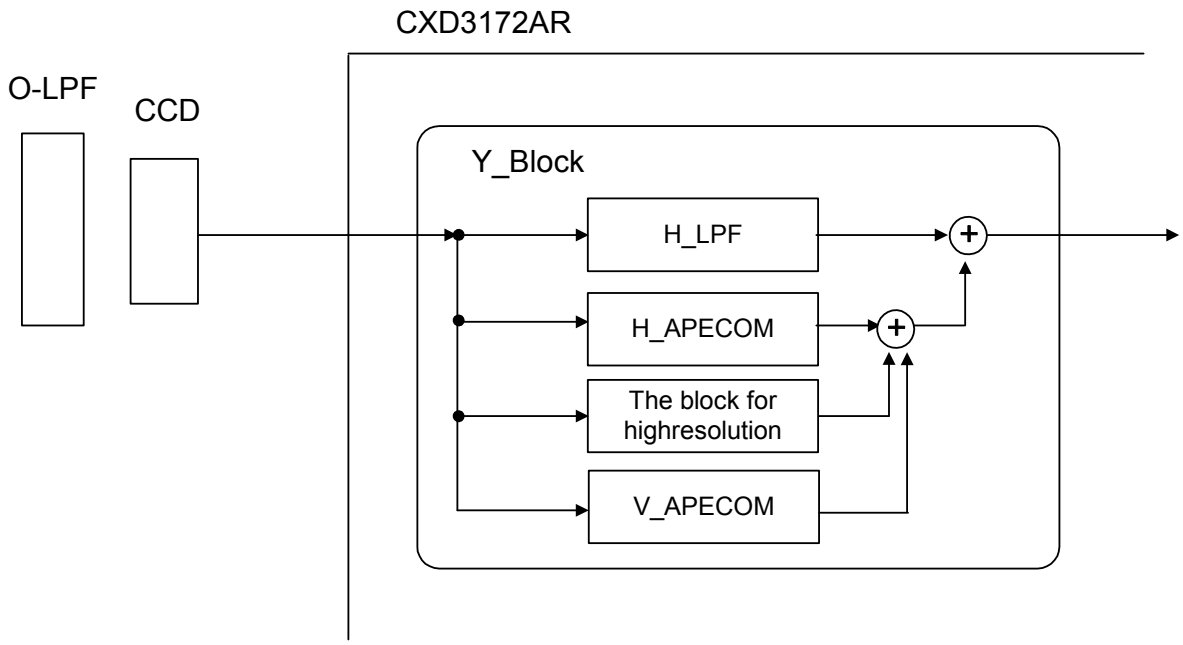


Fig 10.2-7 Aperture Compensation Block and High Resolution Block

High resolution signal processing algorithm

A high resolution signal processing line is added in parallel to the main line of luminosity signal processing. The flow of signal processing is as follows.

(1) A high frequency ingradient is extracted by filter processing.

(2) Noise filter processing is performed by form detection processing.

(3) It amplifies and a high region signal is generated.

(4) It adds to the main line.

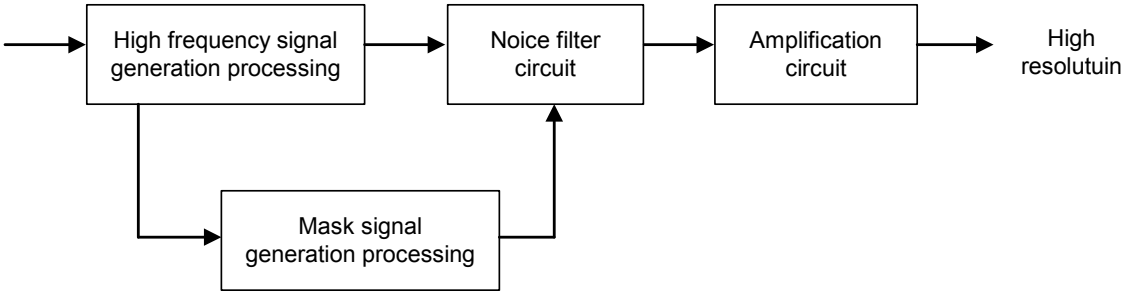


Fig 10.2-8 Block configulation for high resolution signal processing

High resolution related parameter

High resolution mode can be turned on and off by switching REON(CAT2_Byte12_bit3). When this parameter is OFF, a high resolution signal is not added.

Table 10.2-5 High resolution related parameter

Parameter	Description	Settings range
REON(CAT2_Byte12_bit3)	Switches the high resolution mode ON and OFF.	0[h]:High resolution mode OFF 1[h]:High resolution mode ON
RETGAIN(CAT2_Byte12_bit0-2)	Specifies the high resolution aperture gain.	from x0(0[h]) to x7(7[h])

10.2.5. Aperture Compensation Function

Aperture Compensation processing performed by the SS-HQ1 includes H aperture compensation processing, V aperture compensation processing, VH aperture compensation processing which adds V and H aperture compensation processing, and highlight aperture compensation processing which boosts the aperture compensation of highlighted portions after gamma.

Each aperture compensation signal has the related parameters shown in the table below.

Since the parameters of CAT2 are controlled by Built-in FW, it should stop built-in FW to change the parameter of CAT2 (CPUHOLD=1).

Table 10.2-6 Horizontal Aperture Compensation Related Parameters

Parameter name		Description	Initial value
HAPGH	CAT2 Byte1_bit4-5	Sets the horizontal aperture compensation high frequency gain 0:x0 1:x1 2:x2 3:x4	2
HAPGL	CAT2 Byte1_bit6-7	Set the horizontal aperture compensation low frequency gain 0:x0 1:x1/2 2:x1 3:x2	2

Table 10.2-7 Vertical Aperture Compensation Related Parameters

Parameter name		Description	Initial value
VAPG	CAT2 Byte2_bit0-3	Sets the V aperture compensation gain. from x0(0[h]) to x1(F[h])	A
VAPSL	CAT2 Byte2_bit4-6	Applies slice to V aperture compensation 0: Slice level 0 -> 7: Slice level Max	2
VLMHOFF	CAT2 Byte2_bit7	Turns the threshold of luminance of the V aperture compensation ON and OFF. 0:ON 1:OFF	0
VLMVOFF	CAT2 Byte3_bit0	Turns the threshold of aperture compensation of the V aperture compensation ON and OFF. 0:ON 1:OFF	0
VAPLMHTH	CAT2 Byte3_bit1-2	Sets the threshold of luminance of the V aperture compensation. 0:75% 1:81.3% 2:87.5% 3:93.8%	2
VAPLMVTH	CAT2 Byte3_bit3-4	Sets the threshold of aperture compensation of the V aperture compensation limiter. 0:28.1% 1:31.3% 2:37.5% 3:40.6%	1
VAPLMON	CAT2 Byte3_bit5	Turns the V aperture compensation limiter ON and OFF. 0:ON 1:OFF	0

Table 10.2-8 VH Aperture Compensation Related Parameters

Parameter name		Description	Initial value
VHAPG	CAT2 Byte4_bit2-5	Sets the gain after adding V and H aperture compensation. from x0(0[h]) to x2(F[h])	6
VHAPSL	CAT2 Byte5_bit0-3	Applies slice after adding V and H aperture compensation	4

Table 10.2-9 Highlight Aperture Compensation Related Parameters

Parameter name		Description	Initial value
HLAPG	CAT2 Byte4_bit6-7	Highlight aperture compensation total gain setting from x0(0[h]) to x2(3[h])	2
HLAPTHLV	CAT2 Byte5_bit4-5	Sets the threshold level of adding highlight aperture compensation. 0:>50% 1:>37.5% 2:>25% 3:>12.5%	3
HLAPPG	CAT2 Byte5_bit6-7	Highlight aperture compensation gain +side setting from x0(0[h]) to x1(3[h])	3
HLAPMG	CAT2 Byte6_bit0-1	Highlight aperture compensation gain –side setting from x0(0[h]) to x1(3[h])	3
HLAPDS	CAT2 Byte6_bit2	Switches the highlight aperture compensation detection point. 0: Before gamma 1: After gamma	0
HLAPSL	CAT2 Byte6_bit3-6	Applies slice to highlight aperture compensation.	4

10.3. Chroma Signal Processing

10.3.1. Block diagram

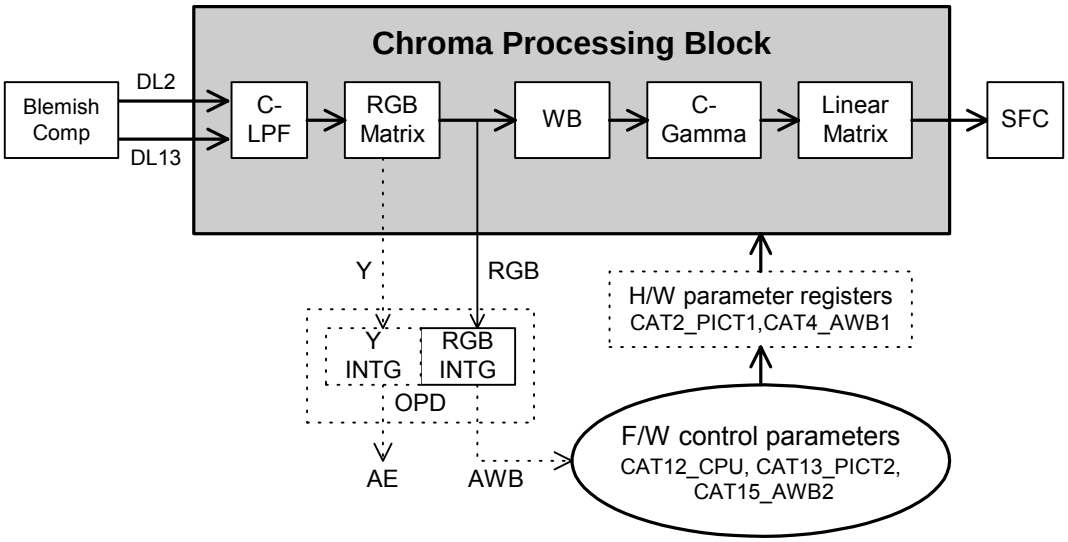


Fig 10.3-1 Chroma Signal Processing Block

Extracts RGB primary color signal from the output signal of complementary color filter CCD, performs white balance and gamma processing, and generates R-Y signal and B-Y signal for video output.
Most of the H/W parameters for these signal processing blocks are controlled by F/W.

Block Explanations

C-LPF(Chroma Low Pass Filter)

Removes high frequency components and prevents false colors. This function cannot be switched off. Pixel clip and highlight edge color compensation can be applied. Refer to "10.3.2 Complementary Color Pixel Clipping" and "10.3.3 Highlight Edge Color Compensation Function".

RGB Matrix (Complementary Color Filter CCD Primary Color Separation Circuit)

Color signals (R, G, B) are extracted from the raw data (Mg, Ye, G, Cy) of complementary color filter CCD by matrix operation.
The spectral characteristics of complementary color filter vary with the type of CCD. Therefore, matrix values that correspond to each CCD are necessary. For proper color reproduction and WB operation, refer to "6.4 CCD Primary Color Separation Matrix " and set the recommended matrix values.
The output signals of RGB matrix are also branched and output to OPD (RGB-INTG), and integrated for AWB.
Signals (Y) of luminance components are also generated in the RGB matrix and output to OPD (Y-INTG). These are used in the integration for AE.

WB(White Balance Gain Circuit)

The change in white color under conditions of the photographed subject such as color temperature, are corrected by changing the gain ratio of R, G, B in F/W control (AWB). Refer to "10.7 WB operation".

C-Gamma(Chroma-Gamma Correction Circuit)

Gamma/ Knee can be corrected independent of luminance signal processing. Refer to "10.4 Variable Gamma Function".

Linear Matrix(Linear Matrix Circuit)

The final primary color signals R, G, B are converted to color difference signals (R-Y), (B-Y).
Reference values are given in “Table 6.4-2 CCD Types and Linear Matrix Parameters (Reference Values)" of "6.CCD Type Selection". However, adjust the parameter values to suit the color reproducibility of the connected equipment. Also, refer to "10.3.4 Using Four-Quadrant Independent Control".
(R-Y) and (B-Y) signals can be suppressed while interlocked with AGC gain. Please refer to "10.8 Suppress".

10.3.2. Complementary Color Pixel Clipping

As CCD output becomes saturated, the ratio among the four pixels S1R, S2R, S1B, and S2B changes, preventing color saturation unevenness from appearing. When a clip level is set for each piece of data prior to chroma signal processing, the data are clipped to the particular set values when a minimum clip level is detected for each of the four pieces of data.
Clip levels can be set using the following parameters. The function can be turned off by setting CLSOFF to 1[h].

Table 10.3-1 Complementary color pixel clip settings

Parameter		Description
CLSOFF	CAT2_Byte29_bit5	Clip function 0[h]: ON 1[h]:OFF
CLS1RL	CAT2_Byte20_bit0-7(LSB)	S1R clip level
CLS1RM	CAT2_Byte25_bit0-3(MSB)	
CLS1BL	CAT2_Byte21_bit0-7(LSB)	S1B clip level
CLS1BM	CAT2_Byte25_bit4-7(MSB)	
CLS2RL	CAT2_Byte22_bit0-7(LSB)	S1R clip level
CLS2RM	CAT2_Byte26_bit0-3(MSB)	
CLS2BL	CAT2_Byte23_bit0-7(LSB)	S1B clip level
CLS2BM	CAT2_Byte26_bit4-7(MSB)	

10.3.3. Highlight Edge Color Compensation Function

When a subject with very large contrast differences is shot, the edges of the subject may be colored. This function temporarily changes the chroma LPF characteristics, making it possible to reduce the apparent amount of edge coloring. Note, however, that caution is needed because the function may act to degrade image quality in the detected area depending on the subject, given that the LPF characteristics are being changed.

Detection may be performed in both the horizontal and vertical directions, with the LPF characteristics being changed in the detected period. Characteristics in LPF are changed by reducing the number of taps by approximately half. Note that the compensation phase and width of the detected signal may be adjusted.

Table 10.3-2 Parameters related to highlight edge color compensation function

Parameter		Description
HLEDLEVL	CAT2_Byte24_bit0-7(LSB)	Sets vertical and horizontal detection levels.
HLEDLEVM	CAT2_Byte27_bit0-2(MSB)	
HLEDDL13	CAT2_Byte27_bit4	Operates the color compensation circuit based on horizontal detection in the delay line output after (1+3HD)/2. 0[h]:OFF 1[h]:ON
HLEDDL2	CAT2_Byte27_bit5	Operates the color compensation circuit based on horizontal detection in the delay line output after 2HD. 0[h]:OFF 1[h]:ON
HLEDV	CAT2_Byte27_bit6	Operates the color compensation circuit based on vertical detection in the delay line output after 2HD and (1+3HD)/2. 0[h]:OFF 1[h]:ON
HLESICH	CAT2_Byte27_bit7	Compensation data selection 0[h]: Color erasure 1[h]: CCD data
HLEPASE	CAT2_Byte29_bit0-1	Shifts the phase with respect to the detected signal. 0[h]-2[h]:0-2 pixel delay
HLEWID	CAT2_Byte29_bit2-4	Can be used to set compensation widths for up to eight pixels with respect to the detected signal. 0[h]-7[h]:1-8 pixels

10.3.4. Using Four-Quadrant Independent Control

The CXD3172AR can set HUE/GAIN for R-Y and B-Y data independently in four quadrants on the R-G/B-G axes prior to conversion to R-Y/B-Y.
The setting procedure is described below.

1. Turn off the suppression function and OUTGAIN.
2. Switch to four-quadrant independent control.
3. Enable HUE/GAIN control.
4. Adjust HUE/GAIN for each quadrant through parameters.

1. Turn off the suppression function and OUTGAIN.
The suppression function and OUTGAIN can be turned off using the following parameters.

Table 10.3-3 Enabling HUE/GAIN control

Parameter		Description
OUTGAIN	CAT12_Byte6_bit1	0[h]:OFF 1[h]:ON
SPRS	CAT12_Byte6_bit2	0[h]:OFF 1[h]:ON

2. Switch to four-quadrant independent control.
If HUE/GAIN control is set to four-quadrant simultaneous control, set the following parameter to 1[h] in order to switch to four-quadrant independent control.

Table 10.3-4 HUE/GAIN adjustment parameters

Parameter		Description
RBQUADON	CAT2_Byte29_bit7	0[h]: Four-quadrant simultaneous 1[h]: Four-quadrant independent

3. Enable HUE/GAIN control.
Set the following parameters to 1[h] to enable HUE/GAIN control.

Table 10.3-5 Enabling HUE/GAIN control

Parameter		Description
CRGAINCTL	CAT12_Byte8_bit2	0[h]: Disable Gain control 1[h]: Enable control
HUECTL	CAT12_Byte8_bit4	0[h]: Disable Hue control 1[h]: Enable control

4. Adjust HUE/GAIN for each quadrant through parameters.

Adjust HUE/GAIN for each quadrant through the parameters listed below.

The HUE/GAIN adjustment parameters for the first quadrant (RYGAIN1, BYGAIN1, RYHUE1, BYHUE1) also serve as the HUE/GAIN adjustment parameters for four-quadrant simultaneous control.

Table 10.3-6 HUE/GAIN adjustment parameters

Parameter		Description
RYGAIN1	CAT2_Byte37_bit0-7	First quadrant : R-Y Gain adjustment
BYGAIN1	CAT2_Byte38_bit0-7	First quadrant : B-Y Gain adjustment
RYHUE1	CAT2_Byte39_bit0-7	First quadrant : R-Y Hue adjustment
BYHUE1	CAT2_Byte40_bit0-7	First quadrant : B-Y Hue adjustment
RYGAIN2	CAT2_Byte41_bit0-7	Second quadrant : R-Y Gain adjustment
BYGAIN2	CAT2_Byte42_bit0-7	Second quadrant : B-Y Gain adjustment
RYHUE2	CAT2_Byte43_bit0-7	Second quadrant : R-Y Hue adjustment
BYHUE2	CAT2_Byte44_bit0-7	Second quadrant : B-Y Hue adjustment
RYGAIN3	CAT2_Byte45_bit0-7	Third quadrant : R-Y Gain adjustment
BYGAIN3	CAT2_Byte46_bit0-7	Third quadrant : B-Y Gain adjustment
RYHUE3	CAT2_Byte47_bit0-7	Third quadrant : R-Y Hue adjustment
BYHUE3	CAT2_Byte48_bit0-7	Third quadrant : B-Y Hue adjustment
RYGAIN4	CAT2_Byte49_bit0-7	Fourth quadrant : R-Y Gain adjustment
BYGAIN4	CAT2_Byte50_bit0-7	Fourth quadrant : B-Y Gain adjustment
RYHUE4	CAT2_Byte51_bit0-7	Fourth quadrant : R-Y Hue adjustment
BYHUE4	CAT2_Byte52_bit0-7	Fourth quadrant : B-Y Hue adjustment

Note: If the gain or phase difference in an individual quadrant is set to a large value, the color changes at the quadrant borders will be large.

10.3.5. False Color Suppress Function

The chroma block has a function for suppressing the chroma signal using the hardware according to the luminance level or V aperture correction level after conversion to R-Y/B-Y.
This function is provided to suppress “false color” during saturation under high luminance or when there is a luminance difference in the vertical direction.
This related parameters are as follows.

Table 10.3-7 Setting the False Color Suppress Amount when the V Aperture Correction is Detected

Parameter		Description
CSVLV	CAT2_Byte53_bit0-1	0[h]: No Suppression 1[h]: Signal suppressed by 50% 2[h]: Signal suppressed by 75% 3[h]: Signal suppressed by 100%

Table 10.3-8 Setting the V-Aperture Correction Level at which False Color Suppress Starts

Parameter		Description
CSVTH	CAT2_Byte53_bit2-3	0[h]: Detection at 25% 1[h]: Detection at 44% 2[h]: Detection at 63% 3[h]: Detection at 81%

Table 10.3-9 Setting the False Color Suppress Amount when the Luminance Level is Detected

Parameter		Description
CSHLV	CAT2_Byte53_bit4-5	0[h]: No Suppression 1[h]: Signal suppressed by 50% 2[h]: Signal suppressed by 75% 3[h]: Signal suppressed by 100%

Table 10.3-10 Setting the Luminance Level at which False Color Suppress Starts

Parameter		Description
CSHTH	CAT2_Byte53_bit6-7	0[h]: Detection at 75% 1[h]: Detection at 81% 2[h]: Detection at 88% 3[h]: Detection at 94%

The Initial value for CSVLV and CSHLV are "0[h]", so suppress is not activated. When only one side is activated, the suppress amount is as indicated in the tables above. However, note that when suppress is set for both sides at the same time, if the luminance and V aperture correction are both detected at the same time while CSVLV and CSHLV are set to combination of "1[h]" and "2[h]", the suppress level becomes "100%”.

10.4. Variable Gamma Function

10.4.1. Gamma Curve Types

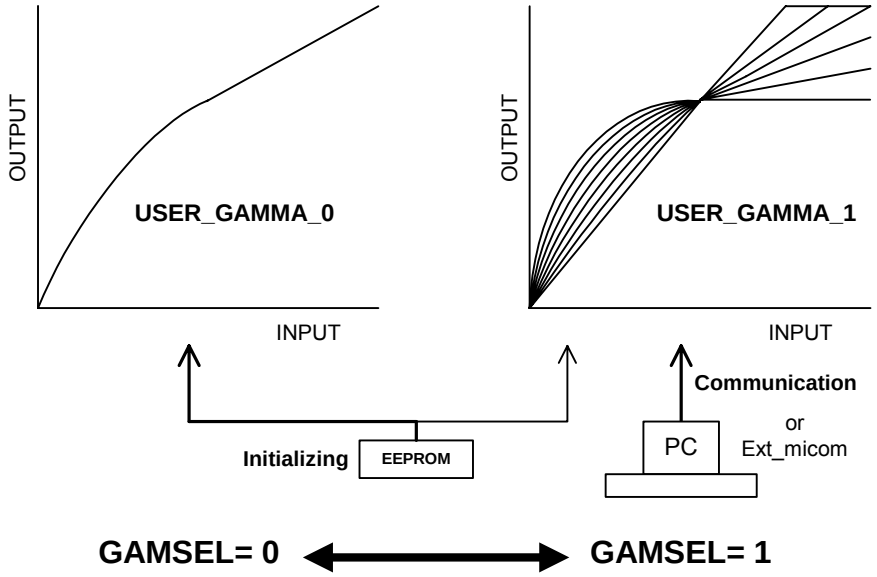


Fig 10.4-1 Gamma Curve Selection

The SS-HQ1 system's DSP (CXD3172AR) has an internal gamma correction circuit. The parameter GAMSEL (CAT12_Byte7_bit0) can be used to switch between User Gamma 0, which is saved to EEPROM for use, and User Gamma 1, which can be changed at immediately through serial communication. Use either of these two values according to the particular application.

Table 10.4-1 Gamma Curve Selection Parameter

Parameter Name	Description	Setting Value	Applications
GAMSEL (CAT12_Byte7_bit0)	Gamma curve selection	0[h] : User Gamma 0 (value saved in EEPROM)	A fixed, such as a factory default setting. The category 2 parameter is saved to EEPROM for use.
		1[h] : User Gamma 1 (value set through serial communication)	A temporary curve change, used for applications such as camera installation adjustment (portable monitor) or matching to a user-provided monitor. The value set in the category 13 parameter can be changed simply through serial communication.
Note Under the default setting (initial setting with no EEPROM), GAMSEL is set to input through port P11 (pin 79).			

To change the gamma curve, select the setting parameter in **Table 10.4-2** “Gamma curve parameters (luminance signal)” and set the gamma area (nonlinear) and knee (KNEE) area (linear). Details on each parameter are discussed later.

Table 10.4-2 Gamma Curve Parameter (Luminance Signal)

Type	Address	Parameter Name	Description	Setting Value
Parameters for User Gamma 0, which is enabled when GAMSEL=0[h] Saved to EEPROM for use.	CAT2_Byte7_bit2-4	YGAMSEL	Y (luminance signal) variable gamma selection	0[h] to 7[h]
	CAT2_Byte7_bit5-7	YKNEESEL	Y (luminance signal) variable knee selection	0[h] to 7[h]
	CAT2_Byte6_bit7	YGAMSON	Y gamma curve correction compression function for low luminance areas	0[h]: OFF 1[h]: ON
	CAT2_Byte7_bit0	YGAMSLV	Y gamma curve correction compression level selection for low luminance areas	0[h]: Strong 1[h]: Weak
Parameters for User Gamma 1, which is enabled when GAMSEL=1[h] Can be updated immediately through serial communication. (Can also be saved to EEPROM.)	CAT13_Byte52_bit2-4	UYGAMSEL	Y (luminance signal) variable gamma selection	0[h] to 7[h]
	CAT13_Byte52_bit5-7	UYKNEESEL	Y (luminance signal) variable knee selection	0[h] to 7[h]
	CAT13_Byte54_bit1	UYGAMSON	Y gamma curve correction compression function for low luminance areas	0[h]: OFF 1[h]: ON
	CAT13_Byte52_bit0	UYGAMSLV	Y gamma curve correction compression level selection for low luminance areas	0[h]: Strong 1[h]: Weak

Details on each setting value are discussed later.

10.4.2. Y Variable Gamma

Any of the curves shown in **Fig 10.4-2** “Y variable gamma” can be selected through combinations of YGAMSEL and YKNEESEL (when GAMSEL=0[h]), or UYGAMSEL and UYKNEESEL (when GAMSEL=1[h]).

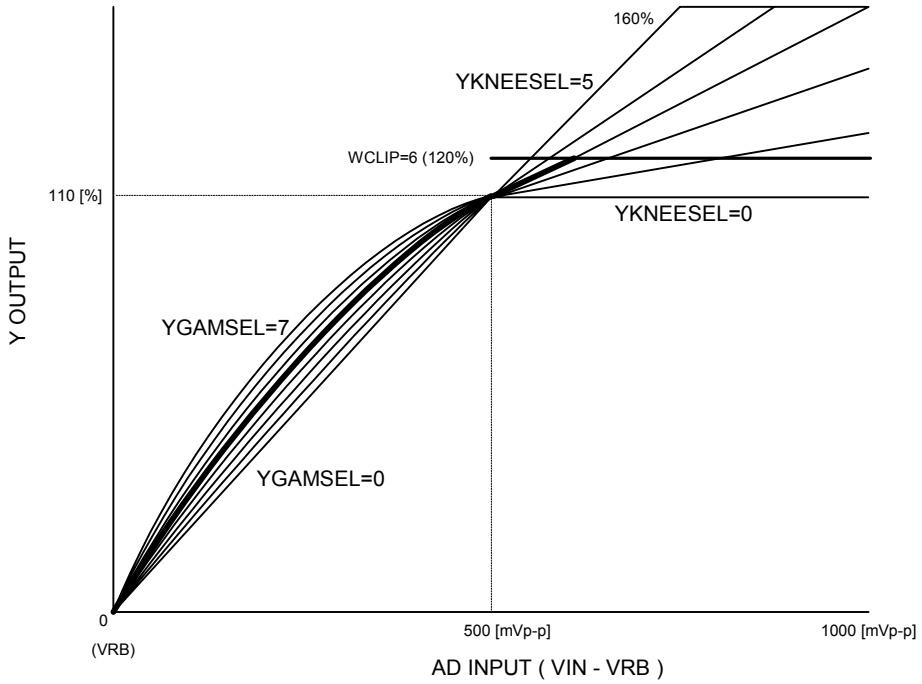


Fig 10.4-2 Y Variable Gamma

Note: The curves in **Fig 10.4-2** “Y variable gamma” were created through software and do not represent actual measurements.

When YKNEESEL (or UYKNEESEL) is selected with a value of 0[h] to 5[h], you can select from 48 different curves. These curves represent a combination of eight different nonlinear areas, which are selected by setting YGAMSEL (or UYGAMSEL) to a value in the range of 0[h] to 7[h], for the area up to AD input 500[mVp-p] (125[%] of standard input); together with six different linear areas based on YKNEESEL (or UYKNEESEL) for higher than AD input 500[mVp-p].

When YGAMSEL (or UYGAMSEL) is set to 4[h] or when YKNEESEL (or UYKNEESEL) is set to 3[h], the gamma comes closes to 0.45 (inverse of standard CRT gamma value of 2.2), and the Y output is 100[%] (equivalent to 100[IRE] for NTSC) with respect to AD input 400[mVp-p] (100[%] of standard input). With many LCD monitors, the light emitting characteristics are such that gamma is greater than 1.0, but this is not a standard value. Select the appropriate gamma curve for the monitor you will be using.

The maximum gamma output value is 160[%], but in the high luminance areas a white clipping process (WCLIP, CAT2_Byte9_bit4-6) is applied in the last stage. (See the WCLIP=6[h] line in **Fig 10.4-2** “Y variable gamma”.)

-Reference information-

The Y variable gamma curve characteristics can be checked using the PG function built into the DSP (CXD3172AR) of the SS-HQ1 system. Output a Raster Horizontal Ramp (see **Fig 12.5-2**), referring to 12.5 “Pattern Generator (PG)”. The curve characteristics can be checked as changes in the horizontal direction luminance signal level through monitoring using an oscilloscope or waveform monitor.

10.4.3. Y Gamma OFF

You can select one of the lines in **Fig 10.4-3** “Y gamma OFF” in order to make the camera-side output linear, such as for image data processing using digital output, or in cases where the receiving monitor has a gamma correction function.

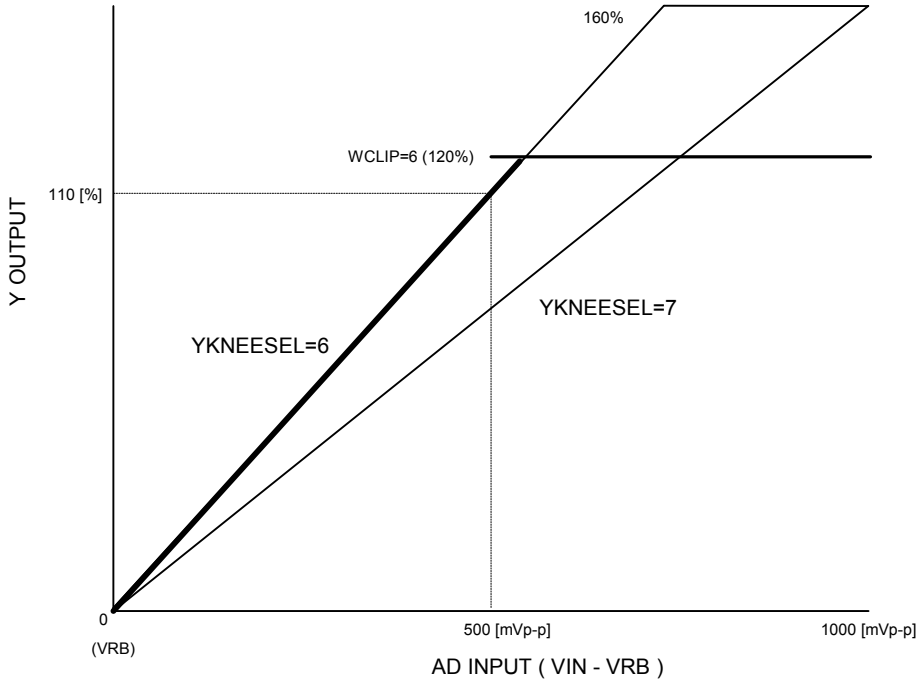


Fig 10.4-3 Y Gamma OFF

When YKNEESEL (or UYKNEESEL) is set to 6[h] or 7[h], the curve becomes a “Y gamma OFF”.

The line created by setting YGAMSEL (or UYGAMSEL) to 0[h] and setting YKNEESEL (or UYKNEESEL) to 5[h] will be the same as the line created by setting YKNEESEL (or UYKNEESEL) to 6[h].

10.4.4. Y Gamma Curve Compression in Low Luminance Areas (S Gamma)

The closer the AD input is to 0 (black level), the stronger the elongation will be. As a result, changes in luminance near the black level seem to be very large. The DSP (CXD3172AR) in the SS-HQ1 system also has a function for compressing the low areas of the gamma curve.

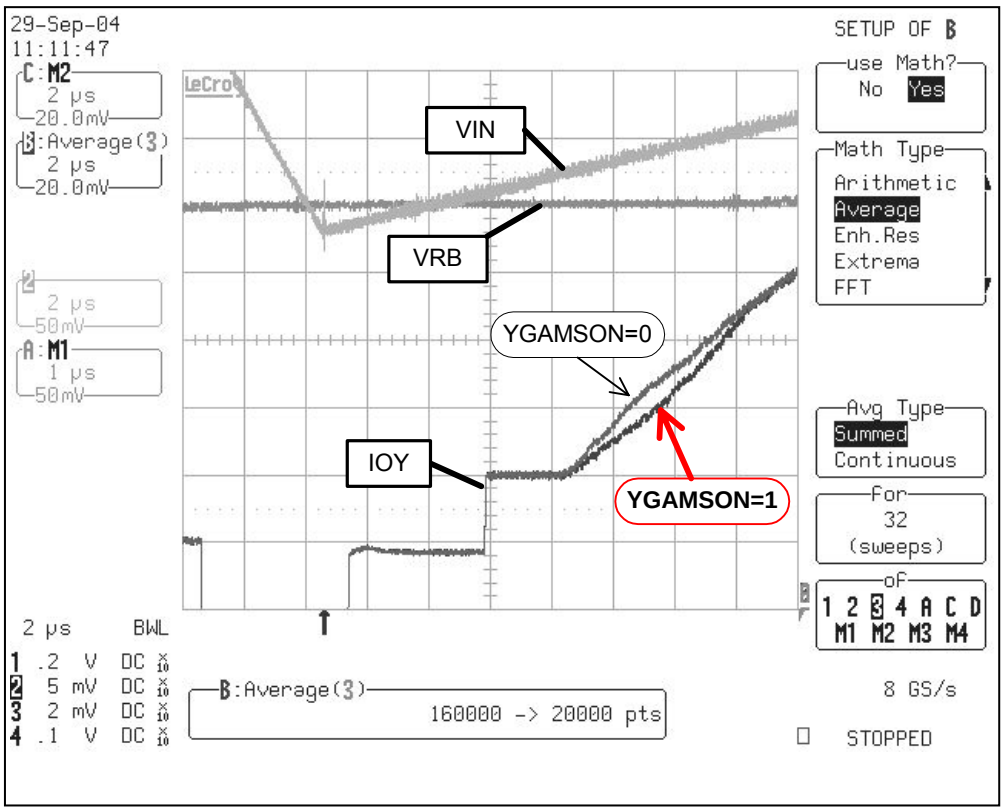


Fig 10.4-4 Gamma Curve Compression in Low Luminance Areas (S Gamma)

When YGAMSON (or UYGAMSON) is set to 1[h], the low luminance areas of the Y gamma curve are compressed. The compression characteristics vary depending on the selected gamma curve (YGAMSEL or UYGAMSEL).

Note that the compression level can be selected using the following parameters.

YGAMSLV (or UYGAMSLV) = 0[h]: Strong 1[h]: Weak

10.4.5. Chroma Variable Gamma

The following table summarizes the chroma signal gamma curve parameters.

Table 10.4-3 Gamma Curve Parameters (Chroma Signal)

Type	Address	Parameter Name	Description	Setting Value
Parameters for User Gamma 0, which is enabled when GAMSEL=0[h] Saved to EEPROM for use.	CAT2_Byte30_bit0-2	CGAMMA	Chroma signal variable gamma selection	0[h] to 7[h]
	CAT2_Byte30_bit5-7	CKNEE	Chroma signal variable knee selection	0[h] to 7[h]
	CAT2_Byte29_bit6	CKNEE2	Chroma knee high region correction (CKNEE=3[h] only)	0[h]: OFF 1[h]: ON
	CAT2_Byte30_bit3,4	CKNCLIP	Chroma knee high region clipping process	0[h] to 3[h]
Parameters for User Gamma 1, which is enabled when GAMSEL=1[h] Can be updated immediately through serial communication. (Can also be saved to EEPROM.)	CAT13_Byte53_bit0-2	UCGAMMA	Chroma signal variable gamma selection	0[h] to 7[h]
	CAT13_Byte53_bit5-7	UCKNEE	Chroma signal variable knee selection	0[h] to 7[h]
	CAT13_Byte54_bit0	UCKNEE2	Chroma knee high region correction (CKNEE=3[h] only)	0[h]: OFF 1[h]: ON
	CAT13_Byte53_bit3,4	UCKNCLIP	Chroma knee high region clipping process	0[h] to 3[h]

Details on the set values are presented below.

The gamma curve may be selected from the curves shown in “**Fig 10.4-5** Chroma variable gamma”, through a combination of CGAMMA and CKNEE (when GAMSEL=0[h]) or UCGAMMA and UCKNEE (when GAMSEL=1[h]).

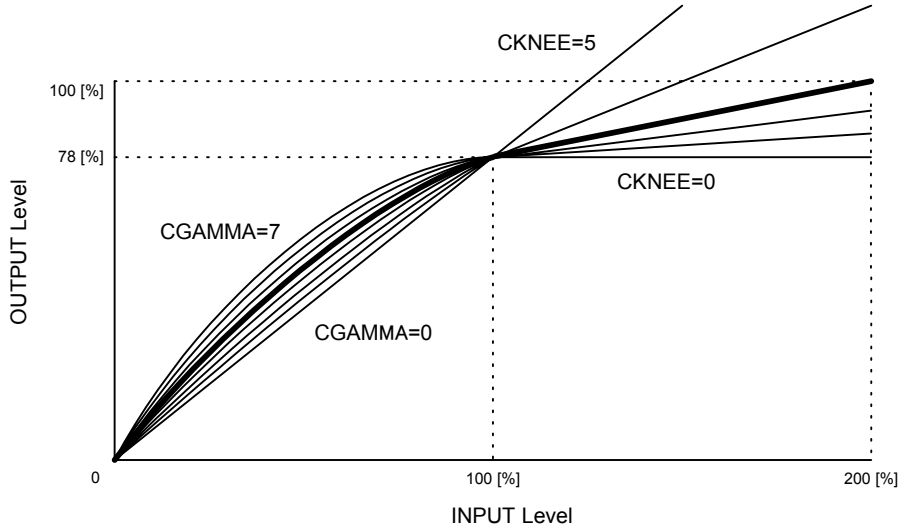


Fig 10.4-5 Chroma Variable Gamma

Note: The curves shown in "**Fig 10.4-5** Chroma variable gamma", are model curves. They do not represent actual measurements.

If CKNEE (or UCKNEE) = 0[h]~5[h] is selected, 48 different curves may be selected, through a combination of eight different nonlinear regions selected by setting CGAMMA (or UCGAMMA) to 0[h]~7[h] for input levels up to 100% (1024[d] converted to digital), and six different linear regions based on CKNEE (or UCKNEE) for higher levels.

If CGAMMA (or UCGAMMA) is set to 4[h] and CKNEE (or UCKNEE) is set to 3[h], then the result will be the closest to gamma = 0.45 (the inverse of standard CRT gamma = 2.2), and the output level for 100% input level will be 78% (400/511[d]).

Note that the input signals for the chroma variable gamma circuit are equivalent to the following:

Input signal inside DSP (CXD3172AR): RGB signal after white balance correction

Output signal: RGB signal before R-Y and B-Y color difference conversion

Note that neither of these signals can be measured directly.

Also note that chroma variable gamma output at high input levels may overflow in the R-Y and B-Y color difference conversion process in a later step, and may be clipped or suppressed at specific levels.

10.4.6. Chroma Gamma OFF

Like Y gamma OFF, chroma gamma OFF can be used to select a line shown in "**Fig 10.4-6** Chroma gamma OFF", if you want to make the chroma output level linear.

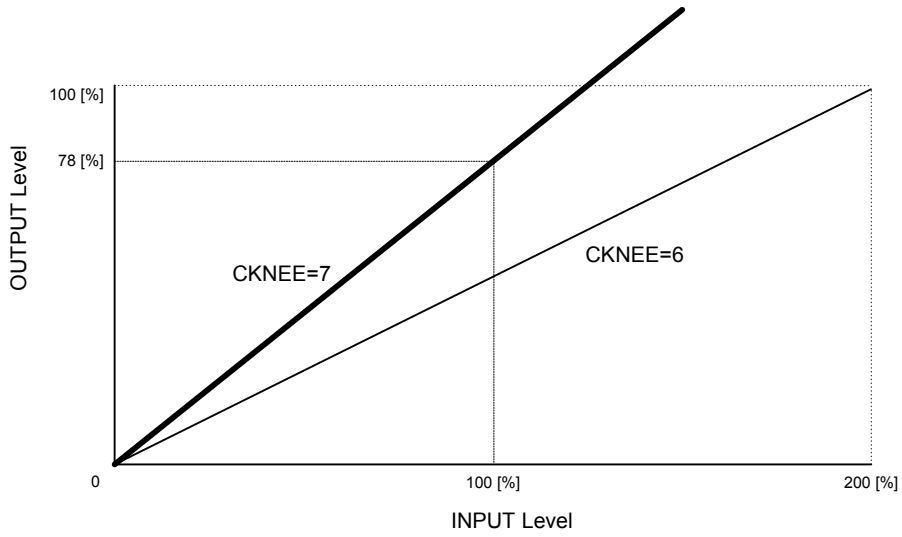


Fig 10.4-6 Chroma Gamma OFF

If CKNEE (or UCKNEE) is set to 6[h] or 7[h], chroma gamma OFF is set.
In such cases, CGAMMA (or UCGAMMA) is disabled.
The line formed by CGAMMA (or UCGAMMA) = 0[h] and CKNEE (or UCKNEE) = 5[h] is identical to the line formed by CKNEE (or UCKNEE) = 7[h].

10.4.7. Chroma Knee High Region Correction

When CKNEE (or UCKNEE) is set to 3[h] and CKNEE2 (or UCKNEE2) is set to 1[h], the knee area at 150% input level and higher is bent as shown in the following graph.

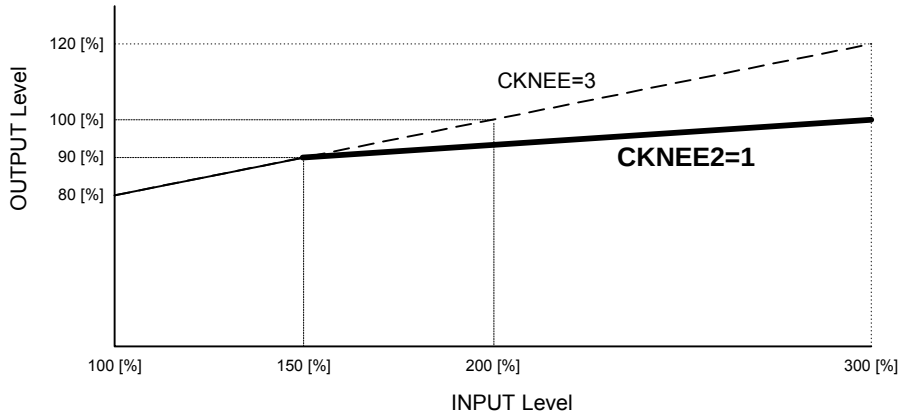


Fig 10.4-7 Chroma Knee High Region Correction

10.4.8. Chroma Signal Knee Clipping Process

In cases where the chroma variable gamma circuit input level exceeds 200%, the knee output can be clipped to a constant level.

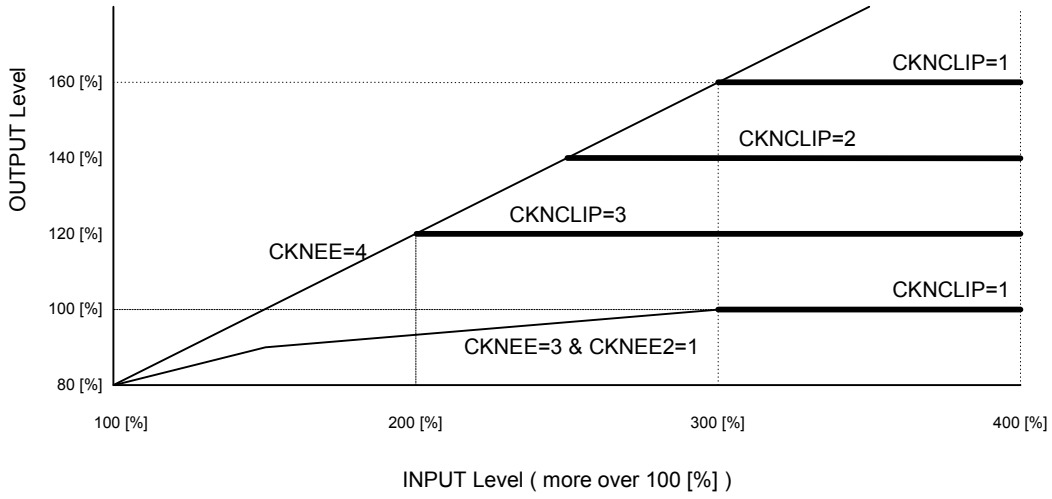


Fig 10.4-8 Chroma Signal Knee Clipping Process

Table 10.4-4 CKNCLIP (or UCKNCLIP) Function Explanation

Parameter	Setting value	Description	Remarks
CKNCLIP CAT2_Byte30_bit3,4 UCKNCLIP CAT13_Byte53_bit3,4	0[h]	No chroma knee output clipping	Depends on output level =CKNEE (UCKNEE). Also linked to CKNEE2=1[h] (UCKNEE2=1[h]).
	1[h]	Clips chroma knee output at 300% input and higher	
	2[h]	Clips chroma knee output at 250% input and higher	
	3[h]	Clips chroma knee output at 200% input and higher	

The output level depends on the CKNEE (UCKNEE) setting.

Examples:

CKNCLIP=1[h] & (CKNEE=3[h] & CKNEE2=1[h]) -> Output is clipped to 100% chroma knee output at 300% input and higher.

CKNCLIP=1[h] & CKNEE=4[h] -> Output is clipped to 160% chroma knee output at 300% input and higher.

CKNCLIP=3[h] & CKNEE=4[h] -> Output is clipped to 120% chroma knee output at 200% input and higher.

<Note>

These output characteristics are based on the use of a chroma variable gamma circuit. If overflowing occurs (e.g., if R-Y and B-Y color difference conversion processes or YC-Mix processes are used in a later step), clipping or suppression (drop in output level with high input) may occur in the output chroma signal at low levels.

10.5. OPD Window Setting and Display

10.5.1. Detection Window Setting Method

The CXD3172AR's OPD (detection integrating circuit) has an AE/AWB common detection window generation circuit. It also has a function for displaying the detection window on the screen.

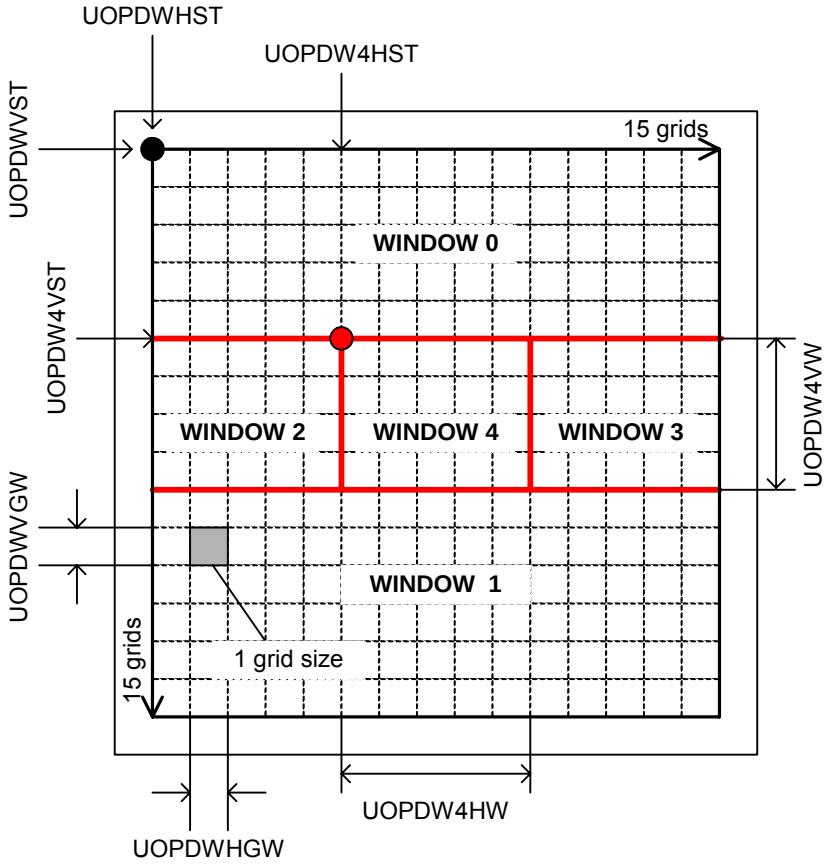


Fig 10.5-1 SS-HQ1 Detection Window

The entire detection window screen consists of a 15x15 grid extending in the horizontal and vertical directions. The overall area is determined by setting the window starting position and the size of a single grid. It is divided into five areas: WINDOW0, WINDOW1, WINDOW2, WINDOW3 and WINDOW4. Different weightings can be set for each area.

When the WINDOW4 starting grid and grid length are setting, the positions and sizes of WINDOW0, WINDOW1, WINDOW2 and WINDOW3 are set automatically.

Table 10.5-1 Detection Window Setting Parameters

Parameter name	Description	Setting unit
UOPDWHST (CAT16_Byte1_bit0-7)	(Normal) Detection window horizontal start position	4 pixels
UOPDWHSTM (CAT16_Byte2_bit0-7)	(Mirror) Detection window horizontal start position	4 pixels
UOPDWVST (CAT16_Byte3_bit0-7)	(Common) Detection window vertical start position	2line / FLD
UOPDWHGW (CAT16_Byte4_bit0-3)	(Common) Detection window horizontal grid width	4 pixels
UOPDWVGW (CAT16_Byte4_bit4-7)	(Common) Detection window vertical grid width	2line / FLD
UOPDW4HST CAT16_Byte5_bit0-3)	(Normal) WINDOW4 horizontal start position	grid
UOPDW4VST (CAT16_Byte5_bit4-7)	(Normal) WINDOW4 vertical start position	grid
UOPDW4HSTM (CAT16_Byte6_bit0-3)	(Mirror) WINDOW4 horizontal start position	grid
UOPDW4VSTM (CAT16_Byte6_bit4-7)	(Mirror) WINDOW4 vertical start position	grid
UOPDW4HW (CAT16_Byte7_bit0-3)	(Common) WINDOW4 horizontal grid width	grid
UOPDW4VW (CAT16_Byte7_bit4-7)	(Common) WINDOW4 vertical grid width	grid

When the mirror function is used, the detection window is set with respect to the horizontally flipped video signal. The window starting position is in the upper left corner after the flip. Adjust the horizontal position of the detection window using the mirror horizontal start position parameters UOPDWHSTM and UOPDW4HSTM in order to link the mirror function and detection window. (CAT1_Byte1_bit4) The horizontal starting position automatically switches to UOPDWHSTM and UOPDW4HSTM in conjunction with the MIRROR=1 setting. For UOPDW4VSTM (mirror WINDOW4 vertical starting position), set the same value as for UOPDW4VST (normal WINDOW4 vertical starting position).

The size varies depending on the CCD type (510H/760H, NTSC/PAL). Set the OPD window within the effective video period.

Table 10.5-2 Detection WINDOW Setting Condition (effective video period)

CCD Type	Setting Condition
510H / NTSC	4 * (UOPDWHST+15*UOPDWHGW) < 501[d] 2 * (UOPDWVST+15*UOPDWVGW) < 241[d]
510H / PAL	4 * (UOPDWHST+15*UOPDWHGW) < 489[d] 2 * (UOPDWVST+15*UOPDWVGW) < 287[d]
760H/NTSC	4 * (UOPDWHST+15*UOPDWHGW) < 753[d] 2 * (UOPDWVST+15*UOPDWVGW) < 241[d]
760H/PAL	4 * (UOPDWHST+15*UOPDWHGW) < 739[d] 2 * (UOPDWVST+15*UOPDWVGW) < 287[d]

10.5.2. Detection Window Screen Display

We recommend displaying markers on the screen when adjusting the detection window.

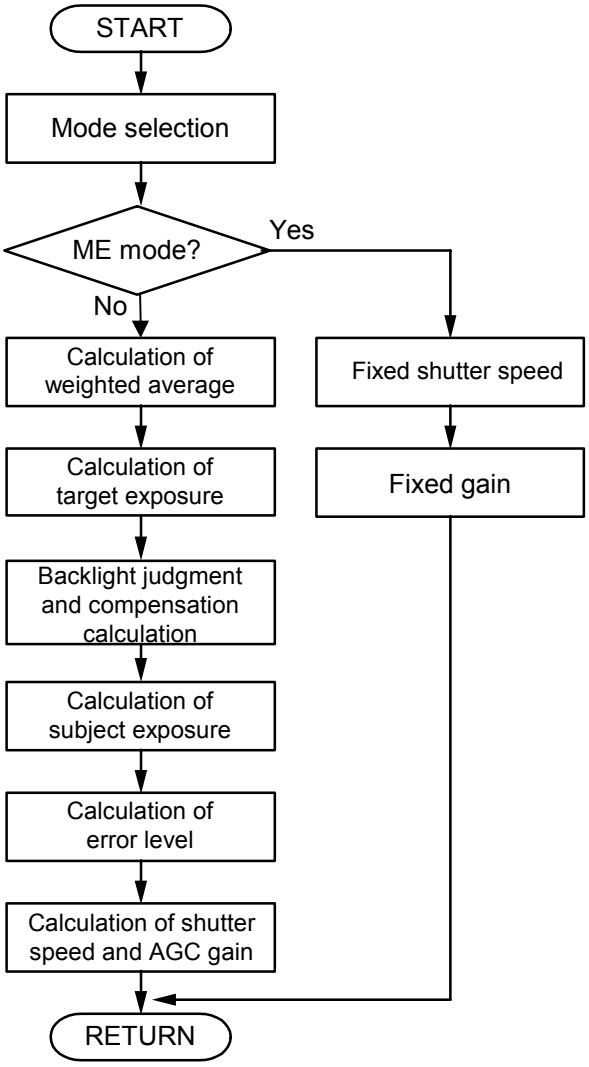
Table 10.5-3 Detection Window Display Parameters

Parameter name	Description	Note
UOPDWMK (CAT16_Byte8_bit0)	Displays detection window on monitor when set to “1[h]”	
UOPDDISP (CAT16_Byte8_bit1-4)	Selects detection window to be displayed on monitor 1[h]: WINDOW 0 2[h]: WINDOW 1 3[h]: WINDOW 2 4[h]: WINDOW 3 5[h]: WINDOW 4	7-9h: AWB integration area display 0,6, A-F[h]: NONE
UWINDOUT (CAT16_Byte8_bit7)	When set to “1[h]”, outputs “High” from P4 (pin 96) for the WINDOW period set in UOPDDISP.	Port 4 driver control is turned off for the duration of UWINDOUT=1[h].

Detection window display (UOPDDISP) also permits the display of integration area windows other than weighted windows (WINDOW0 through WINDOW4).
UOPDDISP=7, 8, 9[h]: AWB integration target display ----------See” 10.7 WB operation”.

10.6. AE operation

10.6.1. Sequence of Operation



Processing is branched in modes accepting from DIP switches or serial communication input.

In ME mode, fixed shutter speed and fixed gain are selected before sending to TG and AGC.

A judgment regarding backlight conditions is made based on the data from OPD, and compensation for it is calculated.

In AE mode, the subject exposure is calculated from the integral value of each OPD window.

Shutter speed and AGC gain are obtained from the subject exposure.

Fig 10.6-1 AE Flowchart

10.6.2. Mode

Switching among BLCOFF, AEREF, FLC[0], AGCMAX, AEME, and AESHUT enables selection of the operating mode as well as activation and deactivation of additional functions. As for the switching method, in some cases switching is done by means of DIP switches and in others, by serial communication.

1. For DIP switches, switching is done with BLCOFF, AEREF, FLC[0], AGCMAX (CXD3172AR Pins 96 to 99), AEME (CXD3172AR Pin 76), and AESHUT (CXD3172AR Pin 77).
2. For serial communication, switching is done by setting PDRHOLD = 1[h] and using the parameters in the table "Parameters and DIP Switches."

These settings combinations are equivalent: DIP setting = Low/Serial setting = 0[h] and DIP setting = High/Serial setting = 1[h]. (The parameters are explained in the next section.)

Table 10.6-1 Parameters and DIP Switches

Parameter	DIP SW NAME
BLCOFF(CAT14_Byte1_bit2)	BLCOFF(P4)
AEREF(CAT14_Byte1_bit3)	AEREF(P5)
NORMFLC(CAT14_Byte2_bit0)	FLC[0](P6)
AGCMAX(CAT14_Byte1_bit4)	AGCMAX(P7)
AEME(CAT14_Byte1_bit0)	AEME(P8)
AESHUT(CAT14_Byte1_bit6)	AESHUT(P9)

AE Mode

AE mode can be activated by setting AEME (CAT CAT14_Byte1_bit0) to 0[h]. This mode offers AE operation through AGC and electronic iris control. AE here essentially controls exposure by means of the electronic iris with AGC at the minimum required gain. If there is insufficient exposure even at the maximum exposure time, AGC controls AE with the shutter speed still set for longest exposure time. If exposure is excessive, first the AGC gain is lowered. If there is too much exposure even at minimum gain, the electronic iris is operated.
AE mode has the following related parameters.

Table 10.6-2 AE Mode Parameters

Parameter	Description	Settings range
BLCOFF(CAT14_Byte1_bit2)	Deactivates backlight compensation.	1[h]: No backlight compensation.
AEREF(CAT14_Byte1_bit3)	Enables switching and setting the AE convergence level. At 1[h], the setting value of AEUSR (CAT14_Byte13_bit0 to 7) is applied.	0[h]:100[IRE] 1[h]: AEUSR setting
AGCMAX(CAT14_Byte1_bit4)	Enables switching two types of AGC maximum gain.	0[h]:AGCMAXL 1[h]:AGCMAXH
AESPEED(CAT14_Byte12_bit0-7)	Enables adjustment of the AE response speed. The smaller the value, the faster the response; the larger the value, the slower the response.	0[h] to FF[h]
AGCMIN(CAT19_Byte1_bit0-7)	Enables the AGC minimum gain to be set. This refers to the AGC gain when electronic iris control and AGC gain control are in transition.	0[h] to FF[h]

* For information on AEUSR, see "Detailed Description (Relationship of Modes and Parameters)."

AESHUT Mode

AESHUT mode can be activated in AE mode by setting AESHUT (CAT14_Byte1_bit6) to 1[h].
At this time, the shutter speed can be set with SHUTMAX, SHUTMIN, SHTSEL, and LLFLC. (See the table "Setting the Shutter Speed.") The electronic shutter speed is selected in SHTSEL. Under these conditions, the electronic shutter speed can be selected by means of the SHTSEL value from eight scale values equally dispersed between SHUTMAX and SHUTMIN.

Table 10.6-3 Electronic Shutter Speed Setting Parameters

Parameter	Description	Settings range
AESHUT(CAT14_Byte1_bit6)	AE shutter mode ON/OFF	0[h]:OFF 1[h]:ON
SHUTMAX(CAT14_Byte17_bit0-7)	Electronic shutter speed maximum value	0[h] to FF[h]
SHUTMIN(CAT14_Byte18_bit0-7)	Electronic shutter speed minimum value	0[h] to FF[h]
SHTSEL(CAT14_Byte3_bit2-4)	Electronic shutter speed selector	0[h] to 7[h]
LLFLC(CAT14_Byte2_bit1)	Low-speed shutter limiter flickerless	0[h]:OFF 1[h]:ON

Table 10.6-4 Example of Setting the Shutter Speed (NTSC)

LLFLC	SHUTMAX	SHUTMIN	SHTSEL	Shutter Speed [sec]
0	FF	0	0	1/60
1	FF	0	0	1/100
0	AC	0	2	1/250
0	AA	0	3	1/500
1	95	0	4	1/1,000
0	A9	0	5	1/2,000
0	A9	0	6	1/4,000
1	AA	0	7	1/10,000
0	FF	0	7	1/100,000

Table 10.6-5 Example of Setting the Shutter Speed (PAL)

LLFLC	SHUTMAX	SHUTMIN	SHTSEL	Shutter Speed [sec]
0	FF	0	0	1/50
1	FF	0	0	1/120
0	BD	0	2	1/250
0	B4	0	3	1/500
0	B0	0	4	1/1,000
1	BB	0	4	1/2,000
0	CE	0	5	1/4,000
1	A8	0	7	1/10,000
0	FF	0	7	1/100,000

10.6.3. Backlight Compensation

The SS-HQ1 system offers a backlight compensation function. This backlight compensation mode can be switched ON and OFF in BLCOFF (CAT14_Byte1_Bit2).
As for the compensation method, it can be set to weighted average mode or compensation gain fixed mode by switching BLCSEL (CAT13_Byte4_Bit0).

Weighted average mode

The screen is divided into five detection windows. Each window's integral value for exposure is multiplied by the weighting value for backlight compensation based on the weighted average. It is suitable for when the main subject remains motionless on screen. (See “Fig 10.6-2 AE Detection Windows of OPD”.)
For windows 0 to 4, the weighting to be applied can be assigned separately. The range is 0[h] to 0F [h]. Each window's weighting value is specified in the parameters shown in the "Table 10.6-6 Detection Windows Weighting Values." For details on how to specify OPD detection windows, see "10.5 OPD Window Setting and Display."

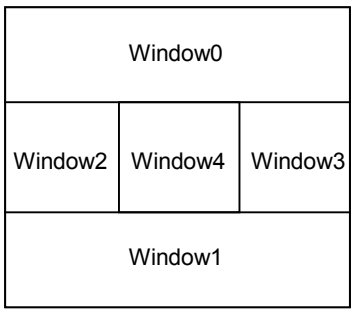


Fig 10.6-2 AE Detection Windows of OPD

Note

If set so that the size of window 4 is extremely small and the weighting of windows 0 to 3 is 0, it will cause rounding errors from the internal calculation. Care should be taken because this worsens the accuracy of AE operation, resulting in an effect like oscillation.

Table 10.6-6 Detection Windows Weighting Values

(CAT14_AE2)

Parameter	Description	Settings range
AEW0 (Byte6_bit0-3)	Window 0 weighting value	00[h] to 0F[h] (0 to 1x)
AEW1 (Byte6_bit4-7)	Window 1 weighting value	00[h] to 0F[h] (0 to 1x)
AEW2 (Byte7_bit0-3)	Window 2 weighting value	00[h] to 0F[h] (0 to 1x)
AEW3 (Byte7_bit4-7)	Window 3 weighting value	00[h] to 0F[h](0 to 1x)
AEW4 (Byte8_bit0-3)	Window 4 weighting value	00[h] to 0F[h] (0 to 1x)

Compensation Gain Fixed Mode

Compensation gain fixed mode can be accessed by making BLCSEL = 1[h].
Backlight compensation is performed in compensation gain fixed mode by reducing the luminance integral average value only by the compensation gain (fixed value) specified in the parameter FBLCGAIN (CAT14_Byte5). In this mode, the supported gain range for compensation by means of FBLCGAIN follows FBLCGAINSEL (CAT14_Byte4_bit1), determined as shown in the "Table 10.6-7 FBLCGAIN and FBLCGAINSEL."

Table 10.6-7 FBLCGAIN and FBLCGAINSEL

FBLCGAINSEL	FBLCGAIN
0	x0.0 to x4.0
1	x1.0 to 1024.0

10.6.4. Flickerless Function

A flickerless function is available with the SS-HQ1 system. Flickerless mode is explained in the "Table 10.6-8 Flickerless Mode."
Modes are selected through the parameters for NORMFLC, LLFLC, and FIXSHTFLC as indicated in the table. When multiple modes are set to be ON, the mode with the smaller value for the priority ranking value is selected.

Table 10.6-8 Flickerless Mode

(CAT14_AE2)

Parameter	Description	Settings range	Priority
NORMFLC(Byte2_bit0)	Electronic shutter, AGC gain modulation method	0[h]:OFF 1[h]:ON	3
LLFLC(Byte2_bit1)	Low-speed shutter limiter method	0[h]:OFF 1[h]:ON	2
FIXSHTFLC(Byte2_bit2)	Electronic shutter fixed method NTSC:1/100[sec] PAL:1/120[sec]	0[h]:OFF 1[h]:ON	1

NORMFLC Mode

In NORMFLC mode, when NORMFLC (CAT14_Byte2_bit0) = 1[h] and AGCOFF (CAT14_Byte1_Bit7), SHUTFLOF (CAT14_Byte2_Bit4), and AGCFLOF (CAT14_Byte2_Bit3) are all 0[h], the general range around the speed selected for the electronic shutter fixed method (NTSC:1/100[sec], PAL:1/120[sec]) is a reference point. For shutter control faster than this, compensation control is performed through shutter speed modulation flickerless function. Control at lower speeds is performed through AGC gain modulation flickerless control.

LLFLC Mode

LLFLC mode is a low-speed shutter limiter flickerless mode. In this mode, the electronic shutter is controlled and the longest exposure time is set at 1/100[sec] for NTSC and 1/120[sec] for PAL. When the subject is dark, the electronic shutter fixed method is used, and when bright, the electronic shutter and AGC gain modulation method is used.

FIXSHTFLC Mode

FIXSHTFLC mode is an electronic shutter fixed flickerless mode. In this mode, the shutter speed is fixed at 1/100[sec] for NTSC and 1/120[sec] for PAL. This is a mode to control flicker by making the shutter speed match the emission cycle for the fluorescent light, which is the cause of flicker in each TV mode.

10.6.5. AE Hysteresis Function

AE hysteresis function is available with the SS-HQ1 system. Using this function can enhance AE stability, even in moments when the luminance level changes, such as when objects momentarily cross in front of the screen.

Table 10.6-9 AESTAB

AESTAB	AE STABility
Category	CAT14_Byte9_bit0-7 (8bit)
Outline	The threshold value at which AE control stops can be set.
Conditions	AEHYST>0, AEWAIT>0, AEHYST>AESTAB
Available settings range	00[h] to FF[h] 8bit
Initial value	0[h]
Description	This setting specifies the threshold value for AE operation to stop after it is in effect. 0[h] (none) to FF[h] (maximum)
Notes	

Table 10.6-10 AEHYST

AEHYST	AE HYSTeresis
Category	CAT14_Byte10_bit0-7 (8bit)
Outline	The threshold value at which AE control starts can be set.
Conditions	AEHYST>0, AEWAIT>0, AEHYST>AESTAB
Available settings range	00[h] to FF[h] 8bit
Initial value	0[h]
Description	Specifies the dead zone relevant to fluctuations in subject luminance. 0[h] (no dead zone) to FF[h] (dead zone maximum) If the setting value is too small, AE tracks even minimal fluctuations in the luminance, and the hysteresis function is less effective. Excessive values, on the other hand, make differences in the luminance level obvious when AE reaches convergence.
Notes	When AEHYST = 0[h], the AE hysteresis function is deactivated.

Table 10.6-11 AEWAIT

AEWAIT	AE WAIT time
Category	CAT14_Byte11_bit0-7 (8bit)
Outline	The hysteresis counter can be set.
Conditions	AEHYST>0, AEWAIT>0, AEHYST>AESTAB
Available settings range	00[h] to FF[h] 8bit
Initial value	0[h]
Description	The greater the value, the less responsive AE is with respect to momentary fluctuations of the subject's luminance level. The smaller the value, the more responsive the reaction.
Notes	

10.6.6. AE Mechanical Iris Mode

This is an example of a lens with an automatic iris which operates using a power supply and video signal.
In AE mode, if MIRIS (CAT14_Byte1_bit1) is set to 1[h], then Mechanical Iris Mode is set.
In this mode, the shutter speed is always 1/60 sec for NTSC and 1/50 sec for PAL, and the backlight compensation amount is output and supplied as a voltage to an external circuit using the CXD3172AR's internal EVR1. The AE operation is performed using AGC control based on the microcontroller's AE, and the mechanical iris inside the external lens.

Example configuration of mechanical iris using IRISVCNT

The CCDLEVEL signal of CXA2096N is used as the video signal. The amplitude of this signal can be controlled by VCA, which is controlled by the IRISVCNT voltage after level adjustment by a pre-amp circuit. This makes it possible to perform backlight compensation using the lens iris.

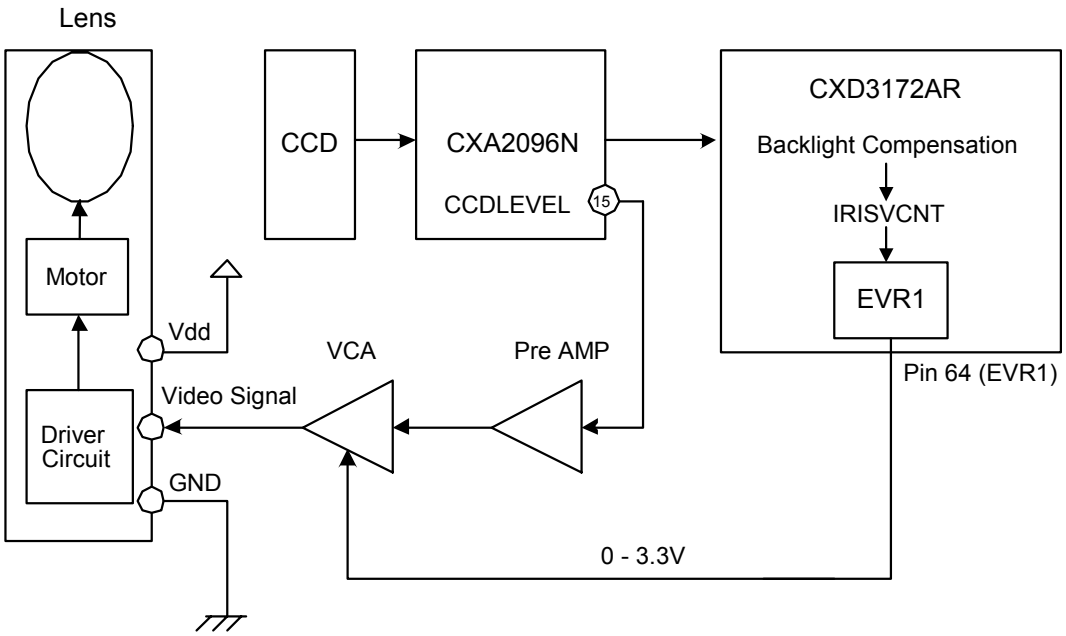


Fig 10.6-3 Example configuration of video servo mechanical iris

Parameters for setting VCA characteristics for mechanical iris control

The voltage to be output to VCA is set through the following parameters.

The characteristics set through the following parameters are output through EVR1 (IRISVCNT). (See **Fig 10.6-4** “Example VCA settings (control range: -12dB to 0dB)”.)

Table 10.6-12 Parameters for setting VCA characteristics for mechanical iris control

Parameter	Description	Settings range
VCAM12(CAT14_Byte21)	EVR value when mechanical iris backlight compensation is -12dB	0[h]-FF[h]
VCAM6(CAT14_Byte22)	EVR value when mechanical iris backlight compensation is -6dB	0[h]-FF[h]
VCA0(CAT14_Byte23)	EVR value when mechanical iris backlight compensation is 0dB	0[h]-FF[h]
VCAP6(CAT14_Byte24)	EVR value when mechanical iris backlight compensation is 6dB	0[h]-FF[h]
VCAP12(CAT14_Byte25)	EVR value when mechanical iris backlight compensation is 12dB	0[h]-FF[h]

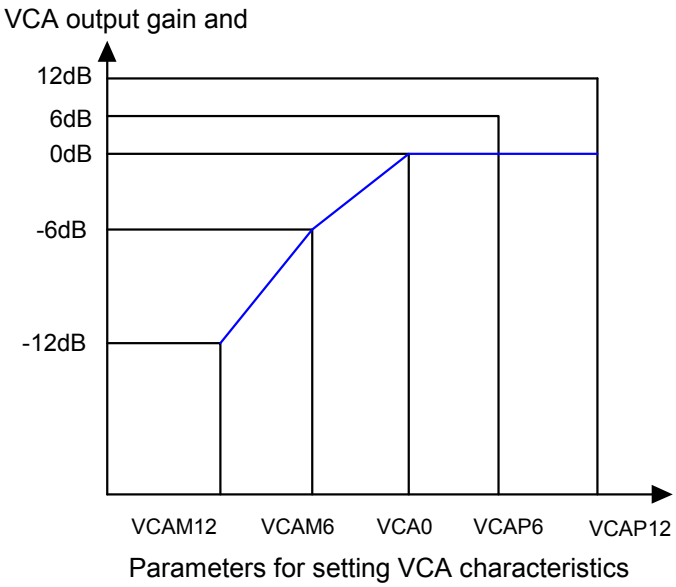


Fig 10.6-4 Example VCA settings (control range: -12dB to 0dB)

* Note

Fig 10.6-4 is an example in which a Rohm BA7655AF is used as the VCA, and a control range of -12dB to 0dB is used when there is backlight. The maximum value is 0dB, with VCA0=VCAP6=VCAP12.

Sony has only evaluated controls (with backlight) in the range of VCA -12dB to 0dB.

10.6.7. ME Shutter Speed and AGC Gain Setting

ME mode can be activated by setting AEME (CAT CAT14_Byte1_bit0) to 1[h]. In ME mode (short for "manual exposure" mode), the shutter speed can be set with SHUTMAX, SHUTMIN, SHTSEL, and LLFLC. (See the table "Setting the Shutter Speed.") The method for selecting the electronic shutter speed is the same as for AESHUT mode, as described above.

Additionally, the gain for AGC can be set with AEREF and BLCOFF. (See the "Table 10.6-13 AGC Gain in ME Mode.") The gain can be selected with AGCMAXL as selected in AGCMAX or from four scale values equally dispersed between AGCMAXH and AGCMIN.

Table 10.6-13 AGC Gain in ME Mode

Parameter	Combinations of BLCOFF and AEREF			
BLCOFF(CAT14_Byte1_bit2)	0	1	0	1
AEREF(CAT14_Byte1_bit3)	0	0	1	1
AGC gain (dB)	Approx. 5	Approx. 13	Approx. 22	Approx. 30

The AGC gain values of the above "Table 10.6-13 AGC Gain in ME Mode" are values when AGCMAX = FF[h] and AGCMIN = 28[h].

10.6.8. Detailed Description (Relationship of Modes and Parameters)

Table 10.6-14 AGCMAXL

AGCMAXL	ae AGC MAXimum gain Low
Category	CAT14_Byte15_bit0-7 (8bit)
Outline	Enables the AGC maximum gain to be set.
Conditions	AGCMAX=0[h] setting
Available settings range	00[h] to FF[h] 8bit
Initial value	C0[h]
Description	The maximum value limiter of AGC gain when AGCMAX is 0[h] can be set as shown in the figure "Correspondence of AGCMIN, AGCMAXL, AGCMAXH, and AGC Gain."
Notes	Valid when AGCMAX is 0[h]. Set it at or above the value of AGCMIN.

Table 10.6-15 AGCMAXH

AGCMAXH	ae AGC MAXimum gain High
Category	CAT14_Byte16_bit0-7 (8bit)
Outline	Enables the AGC maximum gain to be set.
Conditions	AGCMAX=1[h] setting
Available settings range	00[h] to FF[h] 8bit
Initial value	FF[h]
Description	The maximum value limiter of AGC gain when AGCMAX is 1[h] can be set as shown in the figure "Correspondence of AGCMIN, AGCMAXL, AGCMAXH, and AGC Gain."
Notes	Valid when AGCMAX is 1[h]. Set it at or above the value of AGCMIN.

Table 10.6-16 AGCMIN

AGCMIN	ae AGC MINimum gain
Category	CAT19_Byte1_bit0-7 (8bit)
Outline	Enables the AGC minimum gain to be set.
Conditions	
Available settings range	00[h] to FF[h] 8bit
Initial value	28[h]
Description	The minimum value limiter of AGC can be set as shown in the figure "Correspondence of AGCMIN, AGCMAXL, AGCMAXH, and AGC Gain."
Notes	

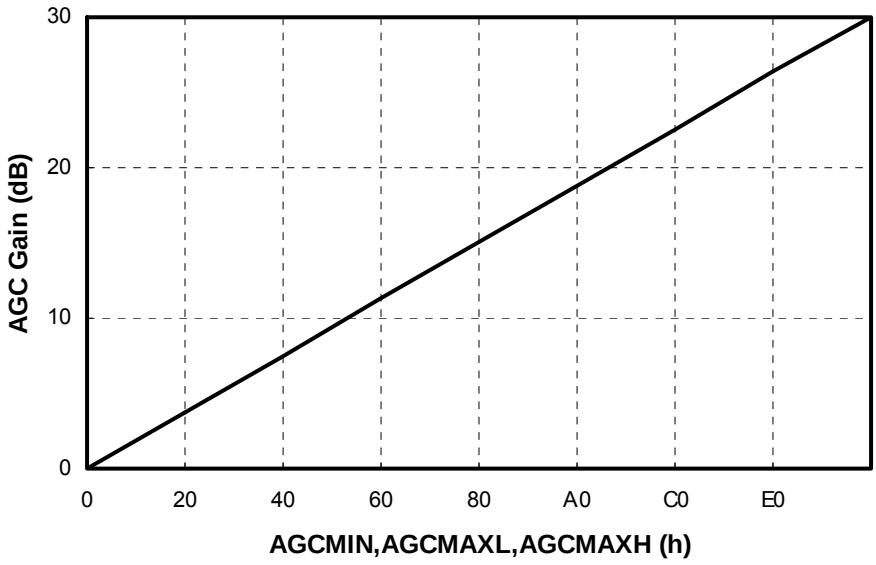


Fig 10.6-5 Correspondence of AGCMIN, AGCMAXL, AGCMAXH, and AGC Gain

Table 10.6-17 AEUSR

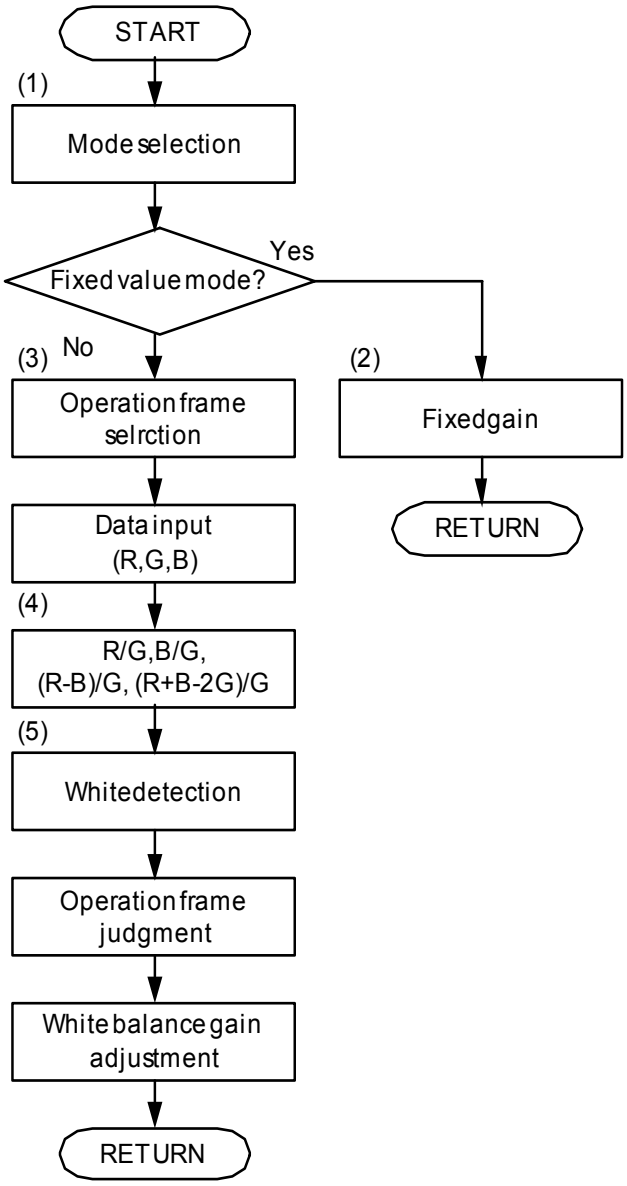
AEUSR	AE USR setting level
Category	CAT14_Byte13_bit0-7 (8bit)
Outline	The AE convergence exposure (AE reference) can be set.
Conditions	AEREF=1[h] (USR)
Available settings range	00[h] to FF[h] 8bit
Initial value	0[h] 60IRE
Description	The white video level when shooting a test chart can be set as shown in the table "AEUSR and AE Convergence Values."
Notes	

Table 10.6-18 AEUSR and AE Convergence Values

AEUSR	IRE
00[h]	Approx. 60
01	65
02	70
03	75
04	80
05	85
06	90
07	95
08	100
09	105
0A	110
0B	115
0C	120
0D	400mV adjustment reference for AGCMIN
0E or higher	100

10.7. WB operation

10.7.1. Sequence of Operation



(1) Processing branches according to the mode input by the DIP switches or serial input.

(2) In fixed value mode, the fixed gain is selected, the signal is sent to the WB gain amplifier.

(3) In ATW mode, the operation frame is selected. Next, operations are performed using the data from the OPD.

(4) The detection data from the OPD is converted to R/G, B/G and (R-B)/G, (R+B-2G)/G format.

(5) In ATW mode, after performing white detection, the operation frame is judged and operation shifts to convergence processing.

Fig 10.7-1 AWB Flow Chart

10.7.2. WB Operation

The modes shown in “WB Modes” can be selected by switching AWBMODE(CAT15_Byte1_bit0-3).

Table 10.7-1 WB Modes

MODE	AWB1	AWB2	AWB3	AWBMODE
ATW	0	0	0	0
Manual White Balance	0	0	1	4
Push	0	1	0	2
Hold	0	1	1	6
User fixed value 1	1	0	0	1
User fixed value 2	1	0	1	5
User fixed value 3	1	1	0	3
User fixed value 4	1	1	1	7

ATW

ATW is the Auto Trace White balance mode.

ATW is a feedforward system that automatically aligns the white balance by detecting the R,G and B before WB amplifire.

Please be sure to carry out pre white balance adjustment before using ATW. See "Pre-WB adjustment mode" under "11. Description of Operation of Each Mode" for the pre white balance adjustment method.

Push

Push mode has no operation frame or other limitations, and performs correction so that the R:G:B evaluation value is always 1:1:1.

In addition, the convergence speed can be adjusted by ALLSTEP (CAT15_Byte 32_bit 0-7). Reducing this parameter value increases the convergence speed.

Note that luminance specific integration is not performed in this mode.

Table 10.7-2 Push Related Parameters

Parameter	Description	Settings range
ALLSTEP(CAT15_Byte32_bit0-7)	Push convergence speed adjustment parameter	0[h]:Maximum speed FF[h]:Minimum speed

MWB (Manual white balance)

When adjusting the R gain, the B gain is also adjusted following the black body radiation curve.
SFTUP and SFTDWN in **Table 10.7-3** are respectively set to port drivers to perform adjustments through key operations.
The up-key (SFTUP) shifts toward the high color temperature side and the down-key (SFTDWN) shifts toward the low color temperature side. The adjustable color temperature range is low color temperature (approximately 2500K) to high color temperature (approximately 9500K) saved at the time of pre-white balance adjustment.

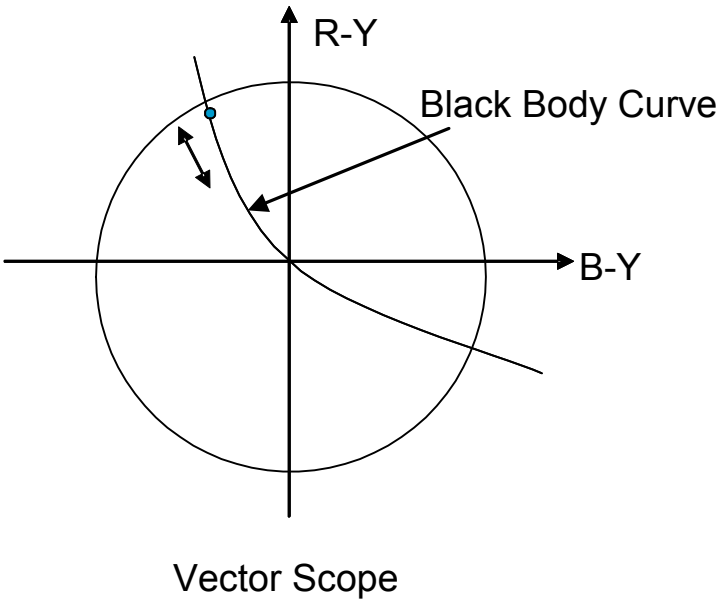


Fig 10.7-2 Trace Curve for Manual White Balance (image)

In MWB mode, the parameters controlled through key operations (SFTUP/SFTDWN) are WBR and WBB in **Table 10.7-4**. When the key is released (or set to “0[h]”) after making adjustments using the SFTUP or SFTDWN key, the gain at that time is saved to a parameter in **Table 10.7-5** and saved to EEPROM. To start up using the gain value written to EEPROM, perform a reset start while in MWB mode.
If both SFTUP and SFTDWN are set to 1[h], the preset values which are set in advance (MWBPRESETR and MWBPRESETB in **Table 10.7-6**) will be applied to WBR or WBB.

Table 10.7-3 MWB Related Parameters

Parameter	Description	Settings range
SFTUP(CAT17_Byte18_bit0)	UP key	1[h]:R gain UP (B gain linked)
SFTDWN(CAT17_Byte18_bit1)	DOWN key	1[h]:R gain DOWN (B gain linked)

Table 10.7-4 Parameters controlled through keys

Parameter	Description
WBR(CAT4_Byte1)	White balance gain R
WBB(CAT4_Byte3)	White balance gain B

Table 10.7-5 Parameter for saving WBR/WBB adjustment value

Parameter	Description
PLRGAIN(CAT15_Byte33)	Push lock R gain Parameter for saving WBR adjustment value when key is released
PLBGAIN(CAT15_Byte34)	Push lock B gain Parameter for saving WBB adjustment value when key is released

Table 10.7-6 WB gain parameters when using presets

Parameter	Description
MWBPRESETR(CAT19_Byte10)	WBR setting for presets
MWBPRESETB(CAT19_Byte11)	WBB setting for presets

Hold

When operation shifts to hold mode, white balance control is stopped and the gain value is held in the condition before the mode transition. Also, when shifting to hold mode from push mode, the gain value at that time is stored in the EEPROM, so push lock mode can be realized by using hold mode in combination with push mode.
In addition, conventional push lock mode and trigger system push lock mode can be switched by switching the parameter AWBTRG (CAT15_Byte2_bit1).

1. Conventional push lock mode (AWBTRG=0[h])
   Operation is performed in push mode while the button is pressed and shifts to hold mode when the button is released, allowing the white balance gain at that point to be written to the EEPROM.

2. Trigger system push lock mode (AWBTRG=1[h])
   Operation shifts to push mode when the button is pressed and convergence operation continues even if the button is released. When convergence is automatically judged to be completed, the white balance gain at that point is written to the EEPROM.
   To start up using the gain value written to EEPROM, perform a reset start while in HOLD mode.

User fixed value

In this mode, the white balance gain is set to a preset value. Four different patterns of setting values can be stored. The default values are as shown in the "Table 10.7-7　User fixed value".

Table 10.7-7　User fixed value

Parameter	Description	Settings range
WBUSRR1(CAT15_Byte35_bit0-7)	User R gain 1(4700K)	00[h]-FF[h]
WBUSRB1(CAT15_Byte36_bit0-7)	User B gain 1(4700K)	00[h]-FF[h]
WBUSRR2(CAT15_Byte37_bit0-7)	User R gain 2(3200K)	00[h]-FF[h]
WBUSRB2(CAT15_Byte38_bit0-7)	User B gain 2(3200K)	00[h]-FF[h]
WBUSRR3(CAT15_Byte39_bit0-7)	User R gain 3(4200K)	00[h]-FF[h]
WBUSRB3(CAT15_Byte40_bit0-7)	User B gain 3(4200K)	00[h]-FF[h]
WBUSRR4(CAT15_Byte41_bit0-7)	User R gain 4(6300K)	00[h]-FF[h]
WBUSRB4(CAT15_Byte42_bit0-7)	User B gain 4(6300K)	00[h]-FF[h]

AWB monitor mode

This mode outputs the white balance gain value during AWB operation on AWBOUT1 to 3. See "AWB Monitor Mode " of “11.1Adjustment Operation Mode” for a detailed description.

AWB coprocessor mode

This mode outputs the AWB control OPD evaluation value on AWBOUT1 to 4. See "AWB Co-process Mode " of “11.1Adjustment Operation Mode” for a detailed description.

10.7.3. ATW Operation Range

ATW sets an operation frame that follows the black body radiation curve.

The operation color temperature range (R-B axis direction) for the standard operation frame is from approximately 2500 K to approximately 9500 K.

The operation color temperature ranges for each operation frame are as shown in the table below.

The frame is selected by operation frame parameter described. In addition three kinds of operation frame can be set up, and ON/OFF is possible respectively. Please refer to the ”Table 10.7-9 Operation frame setting parameters” about the parameter.

Table 10.7-8 Operation Color Temperature Ranges for Different Operation Frame

Frame	Minimum operation color temperature	Maximum operation color temperature
Standard frame	approximately 2500 K	approximately 9500 K
Large frame	approximately 2400 K	approximately 11000 K
frame canceled	less than approximately 2000 K	more than approximately 18000 K

Table 10.7-9 Operation frame setting parameters

Parameter	Description	Settings range
ATWFRAMOF(CAT15_Byte3_bit0)	ON/OFF setting for ATW operation frames (all frames 1 to 3).	0[h] : ON 1[h] : All Cancel
ATWFRM1OF(CAT15_Byte3_bit1)	ON/OFF setting for ATW operation frame type 1.	0[h] : ON 1[h] : Cancel
ATWFRM2OF(CAT15_Byte3_bit2)	ON/OFF setting for ATW operation frame type 2.	0[h] : ON 1[h] : Cancel
ATWFRM3OF(CAT15_Byte3_bit3)	ON/OFF setting for ATW operation frame type 3.	0[h] : ON 1[h] : Cancel
ATWLARGFRM(CAT15_Byte3_bit4)	ON/OFF setting for ATW operation frame enlargement (all frames 1 to 3).	0[h] : OFF 1[h] : ON

During push mode, this frame is canceled. In addition, the frame is also canceled during ATW operation if ATWFRAMOF is set to 1[h].

When the frame is canceled, convergence operation is performed for any subject. However, push and white balance may differ for some subjects. This is due to a difference in the algorithms for ATW and push.

Note that the convergence accuracy during ATW and push modes is approximately 4% with respect to the size of the burst flag.

10.7.4. ATW Related Parameters

Luminance specific integration

Table 10.7-10 AWBSEPOF

AWBSEPOF	AWB SPEcific OFf
Category	CAT15_Byte2_bit0 (1bit)
Outline	ON/OFF setting for luminance specific integration.
Conditions	AWBMODE=0[h]
Available settings range	0[h],1[h] 1bit
Initial value	0[h]
Description	0[h]:Luminance specific integration ON 1[h]:OFF
Notes	This parameter affects both the ATW response characteristics and the convergence speed.

Table 10.7-11 UWBYREFL

UWBYREFL	
Category	CAT15_Byte28_bit0-7 (8bit)
Outline	Sets the minimum value on the medium luminance side of the integral range for luminance specific integration.
Conditions	AWBMODE=0[h]
Available settings range	0[h]-FF[h] 8bit
Initial value	4[h]
Description	When AWBSEPOF = 0[h]: The integral range is fixed to UWBYREFL to UWBYREFH. When AWBSEPOF = 1[h]: Detection is performed on the medium luminance region UWBYREFL to INTSLICE and the high luminance region INTSLICE to UWBYREFH, and the optimum region is selected for ATW control.
Notes	Please set value like UWBYREF < INTSLICE < UWBYREFH

Table 10.7-12 INTSLICE

INTSLICE	
Category	CAT15_Byte29_bit0-7 (8bit)
Outline	Sets the maximum value on the medium luminance side of the integral range for luminance specific integration.
Conditions	AWBMODE=0[h], AWBSEPOF=1[h]
Available settings range	0[h]-FF[h] 8bit
Initial value	80[h]
Description	When AWBSEPOF = 1[h]: Detection is performed on the medium luminance region UWBYREF to INTSLICE and the high luminance region INTSLICE to UWBYREFH, and the optimum region is selected for ATW control.
Notes	Please set value like UWBYREF < INTSLICE < UWBYREFH

Table 10.7-13 UWBYREFH

UWBYREFH	
Category	CAT15_Byte30_bit0-7 (8bit)
Outline	Sets the maximum value on the high luminance side of the integral range for luminance specific integration.
Conditions	AWBMODE=0[h]
Available settings range	0[h]-FF[h] 8bit
Initial value	0[h]
Description	When AWBSEPOF = 0[h]: The integral range is fixed to UWBYREFL to UWBYREFH. When AWBSEPOF = 1[h]: Detection is performed on the medium luminance region UWBYREF to INTSLICE and the high luminance region INTSLICE to UWBYREFH, and the optimum region is selected for ATW control.
Notes	Please set value like UWBYREF < INTSLICE < UWBYREFH

Table 10.7-14 HLCUT

HLCUT	
Category	CAT15_Byte31_bit0-7 (8bit)
Outline	Sets the high luminance side selection threshold value for luminance specific integration.
Conditions	AWBMODE=0[h], AWBSEPOF=1[h]
Available settings range	0[h]-FF[h] 8bit
Initial value	80[h]
Description	Reducing this parameter makes easier to use high luminance portions.
Notes	

Adjustment of ATW control speed

Table 10.7-15 AWBSPED

AWBSPED	AWB SPEeD
Category	CAT15_Byte5_bit0-7 (8bit)
Outline	Sets the ATW control speed.
Conditions	
Available settings range	0[h]-FF[h] 8bit
Initial value	2[h]
Description	0[h]:Maximum speed FF[h]:Minimum speed
Notes	This parameter affects both the ATW response characteristics and the convergence speed.

Table 10.7-16 WBDLY

WBDLY	White Balance DeLaY
Category	CAT15_Byte6_bit0-7 (8bit)
Outline	Sets the ATW response speed.
Conditions	
Available settings range	0[h]-FF[h] 8bit
Initial value	10[h]
Description	0[h]:Maximum speed FF[h]:Minimum speed This parameter sets the WAIT time until convergence operation starts.
Notes	

Table 10.7-17 ATWSTEP

ATWSTEP	
Category	CAT15_Byte7_bit0-7 (8bit)
Outline	Sets the ATW convergence speed.
Conditions	
Available settings range	0[h]-FF[h] 8bit
Initial value	8[h]
Description	0[h]:Maximum speed FF[h]:Minimum speed This parameter sets the time from when convergence operation starts until convergence operation ends.
Notes	

Convergence point shift

The SS-HQ1 has a function for shifting the convergence point. This system has the two convergence point shift modes of auto discrimination mode and select 1 point mode. Auto discrimination mode automatically discriminates the convergence point position and controls the gain. In this mode the convergence point shift can be set in four directions. In addition, select 1 point mode shifts the convergence point to an optional preset point.
The convergence point shift mode is switched by AWBSFT (CAT15_Byte 2_bit 2).

Table 10.7-18 AWBSFT

AWBSFT	AWB ShiFT
Category	CAT15_Byte2_bit2 (1bit)
Outline	Switches the ATW convergence point shift mode
Conditions	
Available settings range	0[h],1[h] 1bit
Initial value	1[h]
Description	0[h]:Automatic discrimination 1[h]:Select 1 point
Notes	This parameter is only valid in ATW mode.

Table 10.7-19 ATWGSFT1 / ATWRSFT1 / ATWBSFT1 / ATWMSFT1

ATWGSFT 1 / ATWRSFT1 / ATWBSFT1 / ATWMSFT1	ATW Green ShiFT1 / ATW Red ShiFT1 ATW Blue ShiFT1 / ATW Magenta ShiFT1
Category	CAT15_Byte8,9,10,11_bit0-7 (8 bits each)
Outline	ATW convergence point shift 1 Sets the convergence range frame in the G, R, B and Mg directions.
Conditions	AWBSFT=0[h]
Available settings range	0[h]-FF[h] 8bit
Initial value	2[h]/ 2[h]/ 2[h]/ 2[h]
Description	When AWBSFT is "0[h]" (Auto discrimination mode), the G, R, B and Mg convergence points can be shifted in an optional direction.
Notes	When this value is too large, convergence operation is not performed. This parameter is only valid in ATW mode.

Table 10.7-20 ATWRSFT2 / ATWBSFT2

ATWRSFT2 / ATWBSFT2	ATW Red ShiFT2 / ATW Blue ShiFT2
Category	CAT15_Byte8,9,10,11_bit0-7 (8 bits each)
Outline	ATW convergence point shift 2 Sets the shift amount in the R and B directions.
Conditions	AWBSFT=1[h]
Available settings range	0[h]-FF[h] 8bit
Initial value	2[h]/2[h]
Description	When AWBSFT is "1[h]" (Select 1 point mode), a single point can be selected as the convergence point.
Notes	When this value is too large, convergence operation is not performed. This parameter is only valid in ATW mode.

Dead band adjustment

Table 10.7-21 WBDBAND

WBDBAND	White Balance DeadBAND
Category	CAT15_Byte14_bit0-7 (8bit)
Outline	Sets the dead band width for the convergence point complete judgment.
Conditions	
Available settings range	0[h]-FF[h] 8bit
Initial value	10[h]
Description	Setting a large WBDBAND value is effective for stabilizing operation.
Notes	

Table 10.7-22 DBANDR / DBANDB / DBANDM / DBANDG

DBANDR / DBANDB / DBANDM / DBANDG	DeadBAND Red / DeadBAND Blue / DeadBAND Magenta / DeadBAND Green
Category	CAT15_Byte15,16,17,18_bit0-7 (8 bits each)
Outline	Sets the dead band width in the R, B, Mg and G directions for the convergence start judgment.
Conditions	
Available settings range	0[h]-FF[h] 8bit
Initial value	12[h]/ 12[h]/ 12[h]/ 12[h]
Description	The dead band can be adjusted in the four directions of R, B, Mg and G. These parameters are the dead band widths used to make the next convergence start judgment after convergence has been performed. The dead band width can be set in four directions, which makes it difficult for convergence operation to start even when the color changes in that direction.
Notes	

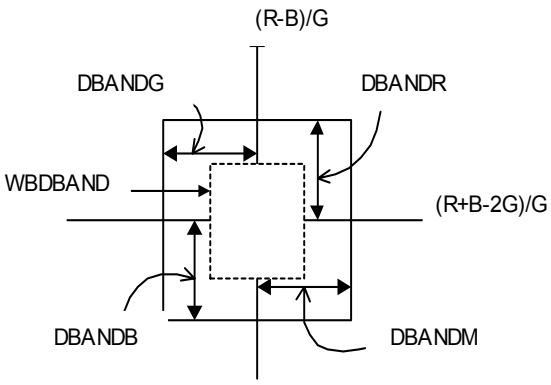


Fig 10.7-3 Dead band of ATW

AWB window

The weighting can be set for each OPD window.
The AWB windows can be displayed on the monitor by setting UOPDWMK (CAT16_Byte8_bit0) = 1[h]. In addition, the detection frames to be displayed on the monitor can be selected by setting AWBWON (CAT4_Byte5_bit2) = 1[h] and setting UOPDDISP (CAT16_Byte8_bit 1-4). (See "10.5 OPD Window Setting and Display" for a detailed description of the OPD windows.)

Table 10.7-23 UAWBW0 / 1 / 2 / 3 / 4

UAWBW0/1/2/3/4	User Auto White Balance Weight window 0/1/2/3/4
Category	CAT16_Byte9, Byte10_bit0-1 (2 bits each)
Outline	The weight of each window of OPD.
Conditions	AWBWON=1[h]
Available settings range	0[h]-3[h] 2bit
Initial value	2[h]/ 2[h]/ 2[h]/ 2[h]/2[h]
Description	0[h]:x0 1[h]:x1/16 2[h]:x1/4 3[h]:x1
Notes	When AWBWON (CAT4_Byte 5_bit 2) = 1[h], windows with a weighting of "x0" are not displayed on the monitor.

Table 10.7-24 Detection frame display parameters

Parameter	Description	Remarks
UOPDDISP(CAT16_Byte8_bit1-4)	Selects the detection frames to be displayed on the monitor. 7[h] : HISTOGRAM WINDOW(OPD_MAX) 8[h] : AWB WINDOW 9[h] : AWB integral pixels (luminance specific integration)	0[h] : NONE 1[h]-5[h] : WINDOW0-4 6[h], A[h]-F[h] : NONE
AWBWON(CAT4_Byte5_bit2)	AWB detection frame selection 0[h] : S_OPDW_MAX 1[h] : AWBW	The weighting values for each detection frame can be set when this is "1[h]".

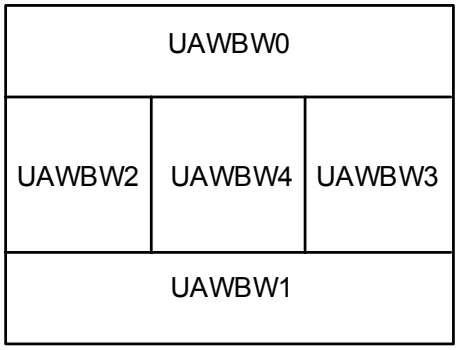


Fig 10.7-4 Weight of each window of OPD

10.7.5. Anti Color-rolling mode

When shooting with a NTSC (59.94 Hz) camera under fluorescent lighting with a 60 [Hz] power supply, cyclic color changes with a long period appear. This is called color-rolling.
Anti-color-rolling mode can be set regardless of the AWBMODE by setting the anti-color-rolling mode to ON (CRLESSON = 1[h]) and color-rollingless AWB to ON (CRLESSAWB = 1[h]).
In addition, in anti-color-rolling mode the following parameters can be controlled independently from ATW.

- Operation frame
- Parameter for adjustment of convergence speed.
- Parameter for adjustment of response speed.
- Dead band width for determination of convergence start.
- Convergence point shift.(Select 1 point only)

Table 10.7-25 CRLESSON

CRLESSON	Color-Rolling LESS ON
Category	CAT12_Byte11_bit0 (1bit)
Outline	ON/OFF setting for anti-color-rolling mode.
Conditions	
Available settings range	0[h],1[h] 1bit
Initial value	0[h]
Description	0[h] : OFF / 1[h] : ON When this is ON, the two anti-color-rolling countermeasures of color-rollingless AWB (CRLESSAWB) and minus gain (U6DBDWN) are controlled together.
Notes	When the port setting has been made, the port has priority.

Table 10.7-26 CRLESSAWB

CRLESSAWB	Color-Rolling LESS AWB
Category	CAT12_Byte11_bit1 (1bit)
Outline	ON/OFF setting for color-rollingless AWB.
Conditions	CRLESSON=1[h]
Available settings range	0[h],1[h] 1bit
Initial value	1[h]
Description	0[h] : OFF / 1[h] : ON
Notes	

Table 10.7-27 U6DBDWN

U6DBDWN	
Category	CAT12_Byte11_bit2 (1bit)
Outline	ON/OFF setting for minus gain.
Conditions	CRLESSON=1[h]
Available settings range	0[h],1[h] 1bit
Initial value	0[h]
Description	0[h] : OFF / 1[h] : ON
Notes	

Color-rollingless AWB mode operation frames

In addition to the ATW operation frames, the SS-HQ1 also has operation frames for color-rollingless AWB mode. Two types of operation frames can be set and turned on and off independently.

Table 10.7-28 CRFRMOFF

CRFRMOFF	anti Color-Rolling FRaMe OFF
Category	CAT15_Byte44_bit0 (1bit)
Outline	ON/OFF setting for color-rollingless AWB operation frames.
Conditions	CRLESSON=1[h]
Available settings range	0[h],1[h] 1bit
Initial value	0[h]
Description	0[h] : ON / 1[h] : All OFF When this is 1[h], frame 1 and frame 2 are both turned off. See "Fig 10.7-5 Operation frame of Color-rollingless" for frame 1 and frame 2.
Notes	

Table 10.7-29 CRFRM1OFF / CRFRM2OFF

CRFRM1OFF / CRFEM2OFF	anti Color-Rolling FRaMe1 OFF / anti Color-Rolling FRaMe2 OFF
Category	CAT15_Byte44_bit0 (1 bit each)
Outline	ON/OFF settings for color-rollingless AWB operation frames.
Conditions	CRLESSON=1[h] CRFRMOFF=0[h]
Available settings range	0[h],1[h] 1bit
Initial value	1[h] / 0[h]
Description	0[h] : ON / 1[h] : OFF Frame 1 is turned off by CRFRM1OFF. Frame 2 is turned off by CRFRM2OFF. See "Fig 10.7-5 Operation frame of Color-rollingless" for frame 1 and frame 2.
Notes	

Table 10.7-30 CRRGMAXL / CRRGMAXH / CRRGMINL / CRRGMINH

CRRGMAXL / CRRGMAXH / CRRGMINL / CRRGMINH	
Category	CAT15_Byte45,46,47,48_bit0-7 (8 bit each)
Outline	Sets the color-rollingless AWB operation frames.
Conditions	CRLESSON=1[h] CRFRMOFF=0[h]
Available settings range	0[h]-FF[h] 8bit
Initial value	0[h] / 15[h] / 0[h] / 07[h]
Description	These parameters set the maximum R/G value (High/Low) and minimum R/G value (High/Low) of the color-rollingless AWB operation frames.
Notes	

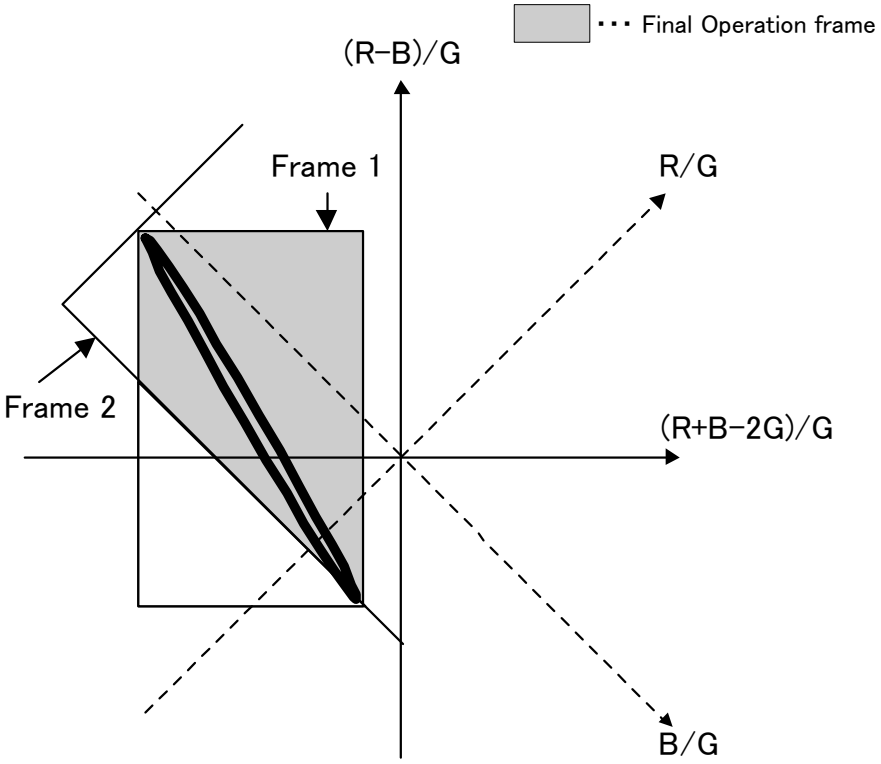


Fig 10.7-5 Operation frame of Color-rollingless

10.8. Suppress

Switches the suppress ON and OFF with the following parameters.
When this parameter is ON, a setup of CSPR(CAT12_Byte6_bit4) and ASPR(CAT12_Byte6_bit3) are reflected.

Table 10.8-1 SPRS

Parameter	Description	Settings range
SPRS(CAT12_Byte6_bit2)	Switches the suppress ON and OFF	0[h]:OFF 1[h]:ON

10.8.1. Chroma Suppress

This suppresses the chroma signal level (RYGAIN and BYGAIN) in accordance with AGC gain.
The settings (start AGCCNT, end AGCCNT, minimum level) are changed by using the following parameters.

CSPRSTA :Chroma suppress start AGCCNT
CSPREND :Chroma suppress end AGCCNT
CSPRMIN :Chroma suppress minimum level

Table 10.8-2 CSPRSTA

CSPRSTA	Chroma SuPpRess STArt level
Category	CAT13_Byte19_bit0-7 (8bit)
Outline	Chroma suppress start AGCCNT
Available setting range	00[h] to FF[h] 8bit
Initial value	A0[h]
Description	
Notes	Don’t set I value larger than CSPREND.

Table 10.8-3 CSPREND

CSPREND	Chroma SuPpRess END level
Category	CAT13_Byte20_ bit0-7 (8bit)
Outline	Chroma suppress end AGCCNT
Available setting range	00[h] to FF[h] 8bit
Initial value	D0[h]
Description	
Notes	Don’t set a value smaller than CSPRSTA.

Table10.8-4 CSPRMIN

CSPRMIN	Chroma SuPpRess MINimum level
Category	CAT13_Byte21_ bit0-7 (8bit)
Outline	Chroma suppress minimum level
Available setting range	00[h] to FF[h] 8bit
Initial value	8A[h]
Description	“00[h]”:Complete suppress, ”FF[h]”:No suppress
Notes	

Table 10.8-5 CSPR

CSPR	Chroma SuPpRess
Category	CAT12_Byte6_bit4 (1bit)
Outline	Switches the chroma suppress ON and OFF
Conditions	SPRS=1[h]
Available setting range	0 [h],1[h] 1bit
Initial value	1[h]
Description	
Notes	Enabled when SPRS=1[h]

10.8.2. Aperture Correction Suppress

This suppresses the aperture correction level in accordance with the AGC gain.
The settings (start AGCCNT, end AGCCNT, minimum level) are changed by using the following parameters.

ASPRSTA :Aperture correction suppress start AGCCNT
ASPREND :Aperture correction suppress end AGCCNT
ASPRMIN :Aperture correction suppress minimum level

Table10.8-6 ASPRSTA

ASPRSTA	Apcon SuPpRess STArt level
Category	CAT13_Byte16_ bit0-7 (8bit)
Outline	Aperture correction suppress start AGCCNT
Available setting range	00[h] to FF[h] 8bit
Initial value	A0[h]
Description	
Notes	Don’t set a value larger than ASPREND.

Table10.8-7 ASPREND

ASPREND	Apcon SuPpRess END level
Category	CAT13_Byte17_ bit0-7 (8bit)
Outline	Aperture correction suppress end AGCCNT
Available setting range	00[h] to FF[h] 8bit
Initial value	D0[h]
Description	
Notes	Don’t set a value smaller than ASPRSTA.

Table10.8-8 ASPRMIN

ASPRMIN	Apcon SuPpRess MINimum level
Category	CAT13_Byte21_ bit0-7 (8bit)
Outline	Aperture correction suppress minimum level
Available setting range	00[h] to FF[h] 8bit
Initial value	8A[h]
Description	“00[h]”:Complete suppress, ”FF[h]”:No suppress
Notes	

Table 10.8-9 ASPR

ASPR	Apcon SuPpRess
Category	CAT12_Byte6_bit3 (1bit)
Outline	Switches the apcon suppress ON and OFF
Conditions	SPRS=1[h]
Available setting range	0 [h],1[h] 1bit
Initial value	1[h]
Description	
Notes	Enabled when SPRS=1[h]

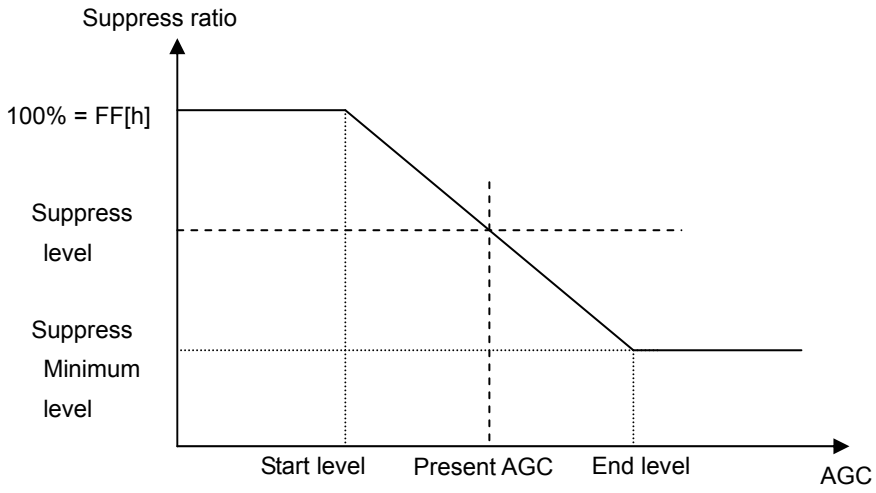


Fig 10.8-1 Suppress Characteristics Diagram

10.9. Mirror Function

The CXD3172AR contains a mirror function.

The video signal which reversed right and left as shown in the following figure can be outputted by using the mirror function.

Notes : It has no top / bottom reversal function.

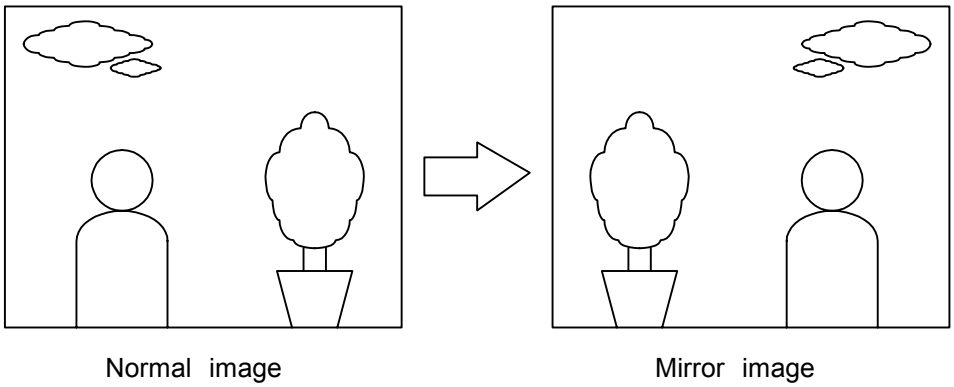


Fig 10.9-1 Outline

The mirror setting procedure is as follows.

MIRROR (CAT1_Byte1_bit4)

0h : Normal image

1h : Mirror image

10.10. Mask Function

10.10.1. Setting Procedure

The CXD3172AR is equipped with a mask function. Eight masks can be produced from the serial communication data settings. The following table presents the parameters related to the mask function settings.

Table 10.10-1 Mask Function Setting Parameters

Parameter		Description
MSK**n**HSET *	CAT9_Byte1-8	Mask horizontal direction start position (1 step = 4 MCK)
MSK**n**HRST *	CAT9_Byte9-16	Mask horizontal direction end position (1 step = 4 MCK)
MSK**n**VSET *	CAT9_Byte17-24	Mask vertical direction start position (1 step = 4 lines)
MSK**n**VRST *	CAT9_Byte25-32	Mask vertical direction end position (1 step = 4 lines)
MSKBYLV	CAT9_Byte33	Color (B-Y) setting
MSKRYLV	CAT9_Byte34	Color (R-Y) setting
MSKYLV	CAT9_Byte35-36	Luminance level
MSKON	CAT9_Byte36_bit2	Show mask: 0: OFF/1: ON
MSKHLD	CAT9_Byte36_bit3	0th hold mode: 0: OFF/1: ON
MSKDLY	CAT9_Byte37	Mask signal Y-side delay adjustment
MSKDLC	CAT9_Byte38	Mask signal CR-side delay adjustment

* Mask number indicated by "n"

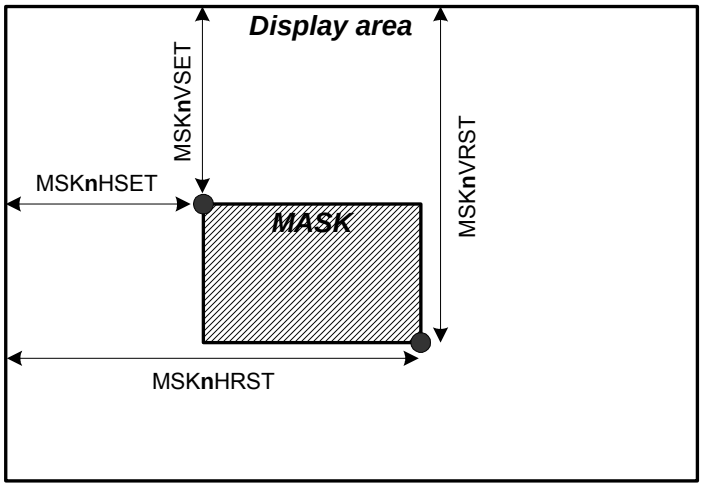


Fig 10.10-1 Mask Function Setting Parameters

The mask setting procedure is as follows.

1. Set MSKON to 1h.
2. Set the mask display positions in MSKnHSET, MSKnHRST, MSKnVSET, and MSKnVRST.
3. Set the brightness in MSKYLV and the colors in MSKBYLV and ASKRYLV.
   (This parameter is invalid when the 0th hold is being used.)

• 0th hold function

To apply the color at the mask start position of MSKnHSET and MSKnVSET to the entire mask, set the 0th hold function MSKHLD (CAT9_Byte36_bit3) to ON (1h). Accordingly, during 0th hold execution, the settings of MSKBYLV, MSKRYLV and MSKYLV are disabled.

Activate 0th hold by setting MSKHLD to 1h.

If there are overlapping masks, the mask with the smaller number is given priority, as shown in the following figure. In this case, the colors of MASK0 and MASK1 are not subject to the hold function. MASK0 "holds" the image color under MASK1.

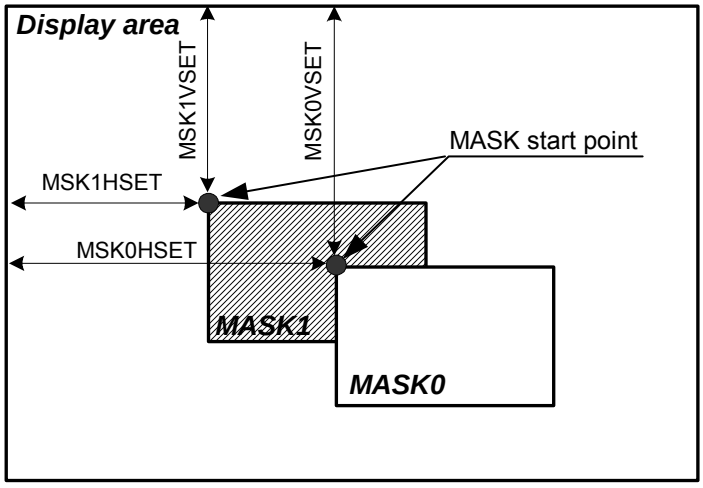


Fig 10.10-2 0-order Hold Function

10.10.2. Important

The following points are important to keep in mind in relation to mask function settings.

1. Eight masks can be simultaneously displayed or stacked on top of each other, but it is not possible to change the brightness signal level and colors separately for each mask. (0th hold does change individual masks.)
2. Masks are not linked to MIRROR.
3. Note that the mask will not be displayed if the MSKnHRST value is smaller than the MSKnHSET value, or if the MSKnVRST value is smaller than the MSKnVSET value.
4. Set MSKnVSET parameter values at 7h or higher. (If they are set under 7h, the mask start position during 0th hold would exceed the period of the effective video signal, so the "held" color would be incorrectly displayed.)
5. Set all MSKnHSET parameter values at 2h or higher. (If they are set under 2h, the mask is not displayed.)
6. With 0th hold, shooting in dark conditions (when the iris is closed, for example) may make the masked areas appear to oscillate. This is caused by random noise, not a problem with the mask function.
7. Under regular mask settings, the mask edges may appear blurred in some cases. This is due to a mismatch of the mask Y and CR delay adjustments. Adjust them by the following parameters.
    - MSKDLY (CAT9_Byte37) Mask signal Y-side delay adjustment
    - MSKDLC (CAT9_Byte38) Mask signal CR-side delay adjustment

11. Functions for Adjustment

11.1. Adjustment Operation Mode

11.1.1. The kind of Modes

It is possible to change in six adjustment operation modes by the setting of serial communication data in CXD3172AR. The selection of each mode is possible to set by ADJMODE (CAT12_Byte2) of the following table.

Table 11.1-1 Parameters of Adjustment Mode

(CAT12_Byte2)

Parameter	DATA	MODE
ADJMODE	00[h]	Normal operation mode
	20[h]	AGCMIN Adjustment mode
	21[h]	Pre-WB Adjustment mode
	22[h]	Static mode of blemish detection
	31[h]	AWB monitor mode
	32[h]	AWB co-process mode

Normal Operation Mode

This is the normal camera operation mode.

AGCMIN Automatic Adjustment Mode

This system is designed to set the video output to the equivalent of 100[IRE] when the A/D input is 400[mVp-p] because the D range is 250[%]. At the CCD standard output of 250[mVp-p], the A/D input must be 400[mVp-p], but the actual AGC gain characteristic (CXA2069N) varies in each case.
This adjustment sets the minimum AGC gain required to absorb variations in the AGC gain characteristic (CXA2069N) and set the A/D input to 400[mVp-p] when the CCD output is 250[mVp-p].
The AGCMIN adjustment is set using the following parameters.

Table 11.1-2 AGCMIN Automatic Adjustment Parameters

Parameter		Description
ADJMODE	CAT12_Byte2	Adjustment mode switching
CCDLEV	CAT12_Byte4_bit0	CCD level 250mV manual adjustment end 0[h]: Not completed/1[h]: Completed
AGCMINFIN	CAT12_Byte4_bit5	AGCMIN automatic adjustment end flag
AGCMIN	CAT19_Byte1	AGC minimum value

<Adjustment procedure>

1. Shoot an all-white subject.
2. Set ADJMODE to 20[h] (ADJMODE=20[h]) to set the adjustment mode to AGCMIN adjustment mode.

3. Adjust the exposure level so that the video signal is 250[mVp-p] in the CCD-OUT signal.
   Adjust the exposure level using an ND filter, changing the iris of lens, etc.
4. Set CCDLEV to 1[h] (CCD level adjustment end).
5. If AGCMINFIN is 1[h], then the AGCMIN adjustment has ended.
6. Write AGCMIN to the EEPROM.
7. Set ADJMODE to 00[h] (resets normal mode).
   (CCDLEV and AGCMINFIN are reset to “0”.)

Pre-WB Adjustment Mode

Pre-white balance consists of aligning the operation color temperature rage of the built-in ATW and Manual White Balance with three reference color temperature for each CCD to be used.

The pre-white balance alignment procedures are as follows. (This adjustment is reflected during power-on.)

1. Image a light source of the reference color temperature (approximately 3200K) onto the entire screen.
2. Enter Pre-white balance adjustment mode.
   Set ADJMODE to 21[h].
3. Set PREWBMODE (CAT12_Byte3) to 1[h]. Confirm the convergence.
4. After setting PREWBMODE (CAT12_Byte3) to 2[h], apply a color temperature conversion filter to the light source (approximately 3200K) to obtain a color temperature of approximately 2500K.
   Confirm the convergence
5. After setting PREWBMODE (CAT12_Byte3) to 3[h], apply a color temperature conversion filter to the light source (approximately 3200K) to obtain a color temperature of approximately 9500K.
   Confirm the convergence.
6. After setting PREWBMODE (CAT12_Byte3) to 0, remove a color temperature conversion filter.
7. Write the value to the EEPROM.

The range of operation of ATW is determined by the above-mentioned adjustment.

Table 11.1-3 Adjustment Items

Parameter		bit width	Description
AWBPRER	CAT19_Byte3	8	R gain in 3200K
AWBPREB	CAT19_Byte6	8	B gain in 3200K
ATWSTARTR	CAT19_Byte8	8	R gain when ATW starts up
ATWSTARTB	CAT19_Byte9	8	B gain when ATW starts up
MWBPRESETR	CAT19_Byte10	8	Preset R gain in MWB
MWBPRESETB	CAT19_Byte11	8	Preset B gain in MWB
PRERDIVG1	CAT19_Byte12-13	16	R/G in high color temperature
PREBDIVG1	CAT19_Byte14-15	16	B/G in high color temperature
PRERDIVG0	CAT19_Byte16-17	16	R/G in low color temperature
PREBDIVG0	CAT19_Byte18-19	16	B/G in low color temperature
PRER1	CAT19_Byte4	8	R gain in high color temperature
PREB1	CAT19_Byte7	8	B gain in high color temperature
PRER0	CAT19_Byte2	8	R gain in low color temperature
PREB0	CAT19_Byte5	8	B gain in low color temperature

Static Blemish Detection Mode

There are two modes, which are manual mode and auto mode, in static blemish detection mode.

• Manual mode

The detected data are written to EEPROM by manual operation, after blemish detection in manual mode.

The parameters shown in the following table are used in blemish detection of manual mode.

• Automatic mode

The detected data are written to EEPROM automatically, after blemish detection in auto mode.

The parameters shown in the following table are also used in blemish detection of auto mode.

The static blemish detection is set by the parameters of the following table.

Table 11.1-4 The setting parameters of static blemish detection

Parameter		Description
ADJMODE	CAT12_Byte2	Switching adjustment modes
BLMDETFIN	CAT12_Byte4_bit6	End flag of the static blemish detection
BLMDETAGC	CAT21_Byte1	The setting value of AGC gain operating the static blemish detection
OPSHBLMDET	CAT21_Byte2_bit1	The automatic static blemish detection 0:OFF 1:ON

The static blemish detection procedure is shown below.

• Manual mode

1. Shade CCD by closing the iris of the lens.
2. The value of the AGC gain under blemish detection is set up by BLMDETAGC.
3. Set OPSHBLMDET to 0[h].
4. Set ADJMODE to 22h and it starts detection.
5. After detection, BLMDETFIN is set to 1[h]. And read the category.
6. Write the data of CAT11 (BLMDET1) to EEPROM
7. Set ADJMODE to 0 and return to the normal operation mode.

• Automatic mode

1. Shade CCD by closing the iris of the lens.
2. The value of the AGC gain under blemish detection is set up by BLMDETAGC.
3. Set OPSHBLMDET to 1[h].
4. Set ADJMODE to 22[h] and it starts detection.
5. After detection, BLMDETFIN is set to 1[h]. And read the category.
6. Set ADJMODE to 0[h] and return to the normal operation mode.

Blemish Detection and Compensation Modes

There are two blemish detection and compensation modes (static detection and compensation functions): normal static detection and compensation mode and one-push static detection and compensation mode. (For further details on the static detection and compensation functions, see “11.2 CCD blemish detection and compensation.”)

1. Normal static detection and compensation mode : Mode for manually writing the detection result to EEPROM
2. One-push static detection and compensation mode : Mode in which detection result is automatically written to EEPROM

Table 11.1-5 Parameters for setting static detection

Parameter		Description
ADJMODE	CAT12_Byte2	Adjustment mode switching
BLMDETFIN	CAT12_Byte4_bit6	Static detection end flag
BLMDETAGC	CAT21_Byte1	AGC gain setting during static detection operation
OPSHBLMDET	CAT21_Byte2_bit0	Static automatic EEPROM writing function ON/OFF 0[h]:OFF/1[h]:ON
DEFON	CAT1_Byte1_bit6	0[h]: Blemish compensation function OFF 1[h]: Blemish compensation function ON
DETREFL	CAT11_Byte5(LSB)	Ordinary blemish threshold level setting
DETREFM	CAT11_Byte9_bit0-1(MSB)	
LARGREFL	CAT11_Byte7(LSB)	Adjustment mode switching
LARGREFM	CAT11_Byte9_bit4-5(MSB)	

Setting procedure

Preparation: Shield the CCD from light, such as by closing the iris of the lens.

1. Normal static detection and compensation mode (OPSHBLMDET=0[h])

1. Set OPSHBLMDET to 0[h] (OPSHBLMDET=0[h]) (sets normal static detection and compensation mode).
2. Set the blemish compensation function to ON. (DEFON=1[h])
3. Set the blemish detection range. (See “11.2 CCD blemish detection and compensation.”)
4. Set the detection threshold levels in DETREFL/M and LARGEREFL/M.
5. In BLMDETAGC, set the AGC gain to be applied during blemish detection.
6. Set ADJMODE to 22[h] (ADJMODE=22[h]) (starts blemish detection and compensation).
7. Read the parameters. If BLMDETFIN is 1[h] (BLMDETFIN=1[h]), detection and compensation have ended.
8. Write the value of CAT11 BLMDET1 Bytes 20-147 (parameters storing detection results) to EEPROM.
9. Set ADJMODE to 0[h] (ADJMODE=0[h]) (resets the normal operation mode).

2. One-push static detection and compensation mode (OPSHBLMDET=1[h])

1. Set OPSHBLMDET to 1[h] (sets one-push static detection and compensation mode).
2. Set the blemish compensation function to ON. (DEFON=1[h])
3. Set the blemish detection range. (See “11.2 CCD blemish detection and compensation.”)
4. Set the detection threshold levels in DETREFL/M and LARGEREFL/M.
5. In BLMDETAGC, set the AGC gain to be applied during blemish detection.
6. Set ADJMODE to 22[h] (ADJMODE=22[h]) (starts blemish detection and compensation).
7. Read the parameters. If BLMDETFIN is 1[h] (BLMDETFIN=1[h]), detection and compensation have ended.
8. Set ADJMODE to 0[h] (ADJMODE=0[h]) (resets the normal operation mode).

* For further details on the parameters, see “11.2 CCD blemish detection and compensation.”

AWB Monitor Mode

Set ADJMODE to 31[h] to enter AWB monitor mode.

In AWB monitor mode, the white balance gain values occurring during the AWB operation are output in AWBOUT1-3. See “Table 11.1-6 Outputs in Monitor Mode” for the gain values which are output in each parameter.

Note that this mode can coexist with all AWBMODE. In addition, AWB functions normally with this mode.

Table 11.1-6 Outputs in Monitor Mode

Parameter	WB gain value
AWBOUT1(CAT23_Byte1)	R gain (WBR(CAT4_Byte1))
AWBOUT2(CAT23_Byte2)	G gain (WBG(CAT4_Byte2))
AWBOUT3(CAT23_Byte3)	B gain (WBB (CAT4_Byte3))
AWBOUT4(CAT23_Byte4)	0 Fixed

AWB Co-process Mode

Set ADJMODE to 32[h] to enter AWB co-process mode.

In AWB co-process mode, the OPD evaluation values for AWB controls are output in AWBOUT1-4. See “Table 11.1-7 Outputs in Co-process Mode” for the individual output values.

Table 11.1-7 Outputs in Co-process Mode

Parameter	Output value
AWBOUT1(CAT23_Byte1)	(R-B)/G (lower)
AWBOUT2(CAT23_Byte2)	(R-B)/G (upper)
AWBOUT3(CAT23_Byte3)	(R+B-2G)/G (lower)
AWBOUT4(CAT23_Byte4)	(R+B-2G)/G (upper)

Note

AWB controls other than OPD integration are stopped in this mode, regardless of the AWB mode.

11.2. CCD blemish detection and compensation

Blemish specifications are established for spot blemishes, which are a type of pixel defect. During the production process, Sony CCDs are sorted based on these blemish specifications. However, white blemishes, in which the blemish level varies in proportion to the temperature, may be observed during use, especially at high temperatures, due to external factors and the like. The CCD blemish detection and compensation function automatically detects and corrects such white blemishes, so that high image quality can be maintained.
The SS-HQ1 automatically detects and corrects blemishes in order of blemish level (starting with the highest blemish level). It can detect and correct 32 blemishes.

11.2.1. CCD blemish detection method types

Static blemish detection (Static detection)

A blemish is recognized by static detection, when a target pixel is more than a fixed level to a black level, while the CCD is shielded from light.

Dynamic blemish detection (Dynamic detection)

A blemish is recognized by dynamic detection, when a target pixel is more than a fixed level to the surrounding pixels, during the normal imaging state.
Dynamic detection does not need to shade CCD like Static detection.
However, Since Dynamic detection detects in the normal imaging state, it may incorrect-detect a place without a defect.

Manual detection

The SS-HQ1 detects and corrects blemishes automatically, so manual blemish detection is not supported.

11.2.2. Blemish detection and compensation parameters

Detection Area Setting

These parameters set the blemish detection area. When AREA is set to “1[h]”, the detection area is displayed. The location and size of the displayed box can be changed by setting HSRTL/M, VSRTL/M, HWIDTHL/M, and VWIDTHL/M.

Table 11.2-1 Parameters for setting the detection area

Parameter		Description
AREA	CAT11_Byte1_bit4	0[h]: Hides the blemish detection area 1[h]: Displays the blemish detection area
HSRTL	CAT11_Byte13_bit0-7(LSB)	Used to set the horizontal start position of the blemish detection area
HSRTM	CAT11_Byte17_bit0-1(MSB)	
VSRTL	CAT11_Byte14_bit0-7(LSB)	Used to set the vertical start position of the blemish detection area
VSRTM	CAT11_Byte17_bit2-3(MSB)	
HWIDTHL	CAT11_Byte15_bit0-7(LSB)	Used to set the horizontal width of the blemish detection area
HWIDTHM	CAT11_Byte17_bit4-5(MSB)	
VWIDTHL	CAT11_Byte16_bit0-7(LSB)	Used to set the vertical width of the blemish detection area
VWIDTHM	CAT11_Byte17_bit6-7(MSB)	

* These parameters can be used for both static detection and dynamic detection.

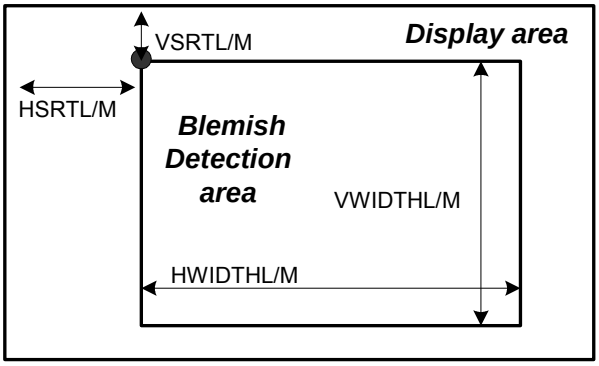


Fig 11.2-1 Detection Area Setting

Displaying blemish markers

This parameter is used to display marks in point where blemishes are detected. Even if a blemish has been corrected and is no longer visible, when it is DEFMK=1[h], the marker will remain displayed. This makes it appear as if the blemish has not been corrected. To check whether blemishes have been corrected, set DEFMK to 0[h].

Table 11.2-2 Parameter for setting marker display

Parameter		Description
DEFMK	CAT11_Byte1_bit1	0[h]: Hides marker 1[h]: Displays marker

11.2.3. Static detection and compensation function

Description of operations

Detection operation

A blemish is recognized by static detection, when a target pixel is more than a fixed level to a black level, while the CCD is shielded from light. The following diagram presents an overview of the static detection operation.

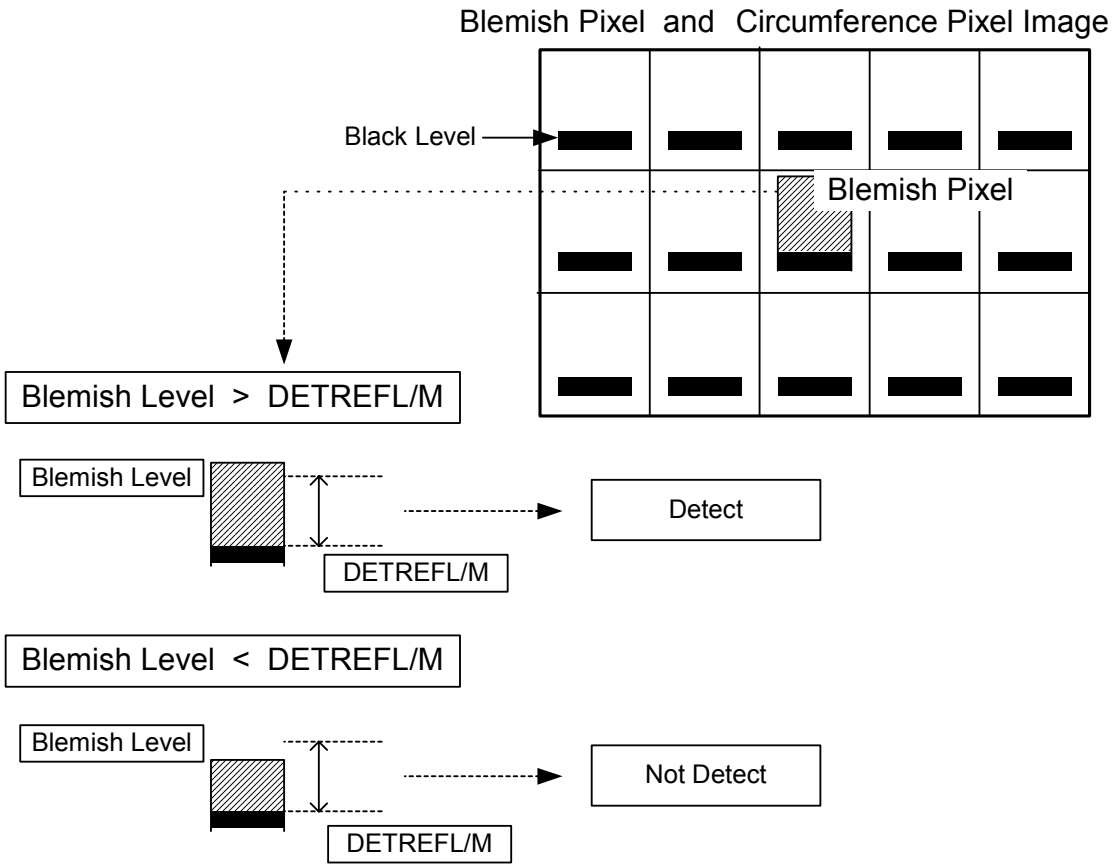


Fig 11.2-2 Static detection operation

Compensation operation

Blemish pixels are corrected by replacing them with the average value of two pixels of the same color filter which are adjacent in the horizontal direction.

* The results of blemish detection and compensation appear in Table 11.2-6 Parameters for storing blemish detection results".

Related Parameters

Blemish compensation function ON/OFF

The following parameter is used to turn the blemish compensation function ON/OFF.

Table 11.2-3 Blemish compensation function ON/OFF parameter

Parameter		Description
DEFON	CAT1_Byte1_bit6	0[h]: Turns blemish compensation function OFF 1[h]: Turns blemish compensation function ON

* These parameters can be used for both static detection and dynamic detection.

Detection mode settings

This parameter is used to switch between normal blemish detection mode and large blemish detection mode. Normal blemish detection mode is detected to one blemish pixel. In large blemish detection mode, a pixel which the blemish more than a certain level adjoined is also detected as a blemish. (The detection and compensation process treats the blemish as a continuous blemish, but the correction place is counted as one place.)

Table 11.2-4 Parameter for switching blemish detection modes

Parameter		Description
LARGEON	CAT11_Byte1_bit3	0[h]: Normal blemish detection mode 1[h]: Large blemish detection mode

* These parameters can be used for both static detection and dynamic detection.

Detection threshold level settings

These parameters are used to set the blemish threshold level and the large blemish threshold level. Pixels exceeding the levels set in these parameters are recognized as being blemish.
Blemishes exceeding the normal blemish threshold level (DETREFL/M) are recognized as being normal blemishes. Blemishes exceeding the large blemish threshold level (LARGREFL/M) are recognized as being large blemishes.

Table 11.2-5 Parameters for setting detection threshold levels

Parameter		Description
DETREFL	CAT11_Byte5_bit0-7(LSB)	Used to set normal blemish threshold level
DETREFM	CAT11_Byte9_bit0-1(MSB)	
LARGREFL	CAT11_Byte7_bit0-7(LSB)	Used to set large blemish threshold level
LARGREFM	CAT11_Byte9_bit4-5(MSB)	

* These parameters can be used for both static detection and dynamic detection.
* When setting LARGREFL/M, be sure to set a value that is greater than the DETREFL/M value (DETREFL/M < LARGREFL/M).

Blemish detection results

The blemish detection results (type, level, address) are written to these parameters. Blemish detection results for a total of 32 blemishes may be written. (If there are fewer than 32 blemishes [e.g., if there are just two blemishes], the other parameters are left at their initial values and are not overwritten.)
Blemish detection results are written in order of blemish level, starting with the highest blemish level. If blemishes are detected through both static detection and dynamic detection, the blemishes found through static detection are written first.

Table 11.2-6 Parameters for storing blemish detection results

Parameter		Description	
SD**n***	CAT11_Byte20-147	Blemish detection type	0[h]: Static detection 1[h]: Dynamic detection
LARGE**n***		Blemish type	0[h]: Normal blemish 1[h]: Large blemish
VCNT**n***		Vertical address of blemish	10bit data
HCNT**n***		Horizontal address of blemish	
DETLV**n***		Blemish level	

*** n:0 - 31**

* These parameters can be used for both static detection and dynamic detection.

Blemish address resetting

This parameter is used to reset the values of parameters storing blemish detection results (all values are set to “00[h]”).
Note that if blemish detection results are written to EEPROM (blemishes detected through static detection), the EEPROM values are not reset. This parameter resets the blemish detection results that have been applied to registers. (To reset EEPROM data, write “00[h]” to EEPROM.)
If this parameter is set to “1[h]” (reset ON), the blemish detection operation will not be performed, so normally it should be set to “0[h]”.

Table 11.2-7 Parameter for resetting blemish address

Parameter		Description
ADDRRST	CAT11_Byte18_bit0	0[h]: Normal blemish detection operation 1[h]: Resets blemish detection results

* These parameters can be used for both static detection and dynamic detection.

* Enabled when DYNDETON=0[h] and DYNDELON=0[h]

Blemish correction count setting

The maximum number of detected blemishes is always 32. However, the number of corrections is set using the following parameter.

Table 11.2-8 Parameter for setting the number of blemish corrections

Parameter		Description
DEFNUM	CAT11_Byte3_bit2-6	Correction count setting 0[h]:1 correction - 1F[h]:32 corrections

* These parameters can be used for both static detection and dynamic detection.

Accumulation time setting

This parameter sets the accumulation time (number of accumulated frames) for static detection. For low-level blemishes, the blemish level will gradually increase as the accumulation time is increased.
When the blemish level exceeds the set threshold level, a blemish is recognized and detected.

Table 11.2-9 Parameter for setting accumulation time

Parameter		Description
DETACCT	CAT11_Byte12_bit2-7	Number of fields accumulated (only non-zero even numbers can be set)

Setting procedure

The SS-HQ1 has two adjustment modes for performing static detection and compensation.

1. Normal static detection and compensation mode : In this mode, detection results are manually written to EEPROM.
2. One-push static detection and compensation mode : In this mode, detection results are automatically written to EEPROM.

Table 11.2-10 Parameters for setting static detection

Parameter		Description
ADJMODE	CAT12_Byte2_bit0-7	Switches the adjustment mode
BLMDETFIN	CAT12_Byte4_bit6	Static detection end flag
BLMDETAGC	CAT21_Byte1_bit0-7	AGC gain setting for static detection operation
OPSHBLMDET	CAT21_Byte2_bit0	Static automatic EEPROM writing function ON/OFF 0[h]:OFF/1[h]:ON

Preparations:
Shield the CCD from light by, for example, closing the lens iris.

1. Normal static detection and compensation mode (OPSHBLMDET=0[h])

1. Set OPSHBLMDET to 0[h]. (Sets normal static detection and compensation mode.) (See Table 11.2-10)
2. Turn ON the blemish compensation function. (DEFON=1[h]) (SeeTable 11.2-3)
3. Set the blemish detection area. (See Table 11.2-1)
4. Use DETREFL/M and LARGEREFL/M to set the detection threshold levels. (See Table 11.2-5)
5. Use BLMDETAGC to set the AGC gain to be applied during blemish detection. (See Table 11.2-10)
6. Set ADJMODE to 22[h] (ADJMODE=22[h]).
   (Starts blemish detection and compensation.) (See Table 11.2-10)
7. Read the parameters. If BLMDETFIN=1[h],detection and compensation are terminated. (See Table 11.2-10)
8. The values of Bytes 20-147 in CAT11 BLMDET1 (parameters for storing detection results) are written to EEPROM.
9. Set ADJMODE to 0[h] (ADJMODE=0[h]). (Resets the normal operation mode.) (See Table 11.2-10)

2. One-push static detection and compensation mode (OPSHBLMDET=1[h])

1. Set OPSHBLMDET to 1[h]. (Sets one-push static detection and compensation mode.) (See Table 11.2-10)
2. Turn ON the blemish compensation function. (DEFON=1[h]) (See Table 11.2-3)
3. Set the blemish detection area. (See Table 11.2-1)
4. Use DETREFL/M and LARGEREFL/M to set the detection threshold levels. (See Table 11.2-5)
5. Use BLMDETAGC to set the AGC gain to be applied during blemish detection. (See Table 11.2-10)
6. Set ADJMODE to 22[h] (ADJMODE=22[h]).
   (Starts blemish detection and compensation.) (See Table 11.2-10)
7. Read the parameters. If BLMDETFIN=1[h],detection and compensation are terminated. (See Table 11.2-10)
8. ADJMODE to 0[h] (ADJMODE=0[h]). (Resets the normal operation mode.) (See Table 11.2-10)

* Note: After executing adjustment mode, be sure to reset the normal operation mode in order to execute adjustment mode again. The above procedure is also described in Adjustment Operation Mode.

CCD blemish threshold levels

The blemish detection threshold level (DETREFL/M) is determined by the following equation:

• DETREFL/M (10bit)
= 1023×DETACCT×BLMDETAGC×(blemish level threshold value mV during accumulation of 1 field) / 1000mV

- DETACCT : Number of fields accumulated in CCD during blemish detection operation
- BLMDETAGC : AGC gain during blemish detection operation

As shown in **Fig 11.2-3**, the accumulation time is determined by applying the electronic shutter control DETACCT (CAT11_Byte12_bit0-7) to the light-shielded CCD. This is because the blemish level and accumulation time are proportionate to each other.

• Accumulation time = 2field × DETACCT / 2 (2-field increments)

Next, in order to transfer the CCD output to the CXD3172AR, the CXA2096N performs sample hold and performs AGC processing.
The output from the CXA2096N is A/D-converted inside the CXD3172AR. In order to perform blemish detection by Z1 block, DETREFL/M (10bit) is compared with the value which pulled the black level (equivalent to the offset voltage) to the 10bit AD (1Vpp input) conversion value. (A blemish is recognized if Det_signal is greater than DETREF).

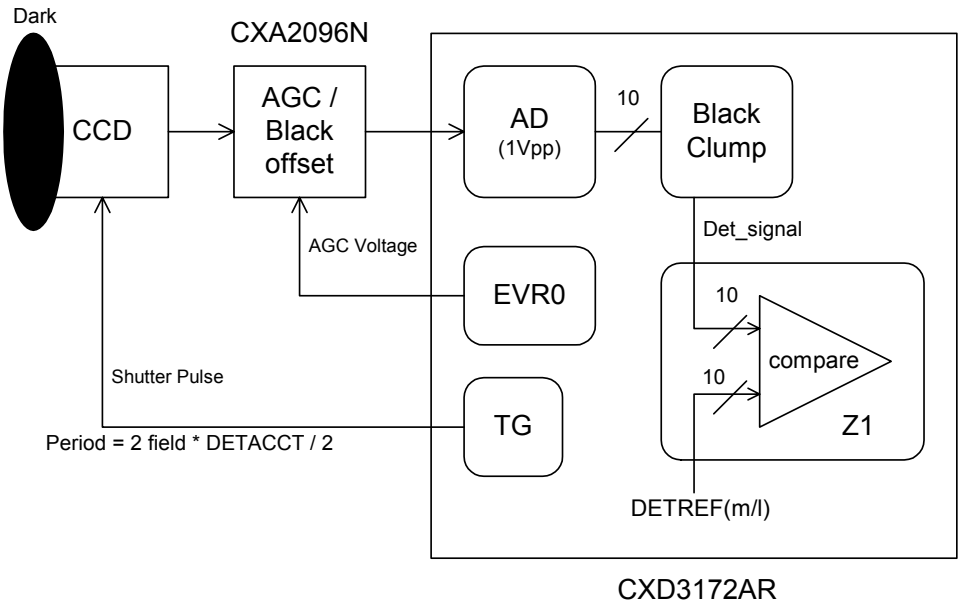


Fig 11.2-3 Blemish detection block diagram

Fig 11.2-4 is a graph illustrating the correlation between the CCD blemish level, accumulation time (DETACCT) and threshold level (DETREFL/M). Because exposure time is less than one field in practice, the CCD blemish level is the Real (1-field) line in the graph. However, blemish detection errors increase at the 100mV/102 gradient. Therefore, the accumulation time (DETACCT) is increased and CCD output is increased to improve detection precision.

For example, if DETACCT = 32 (20h), output equivalent to AGC30dB can be obtained and detection can be performed at the 15.6mV/511 gradient without degrading the S/N ratio. However, please set DETACCT to become Det_Max_value = ((1000[mV] - black offset [mV]) / 1000[mV]) x1023 < 3FF[h].

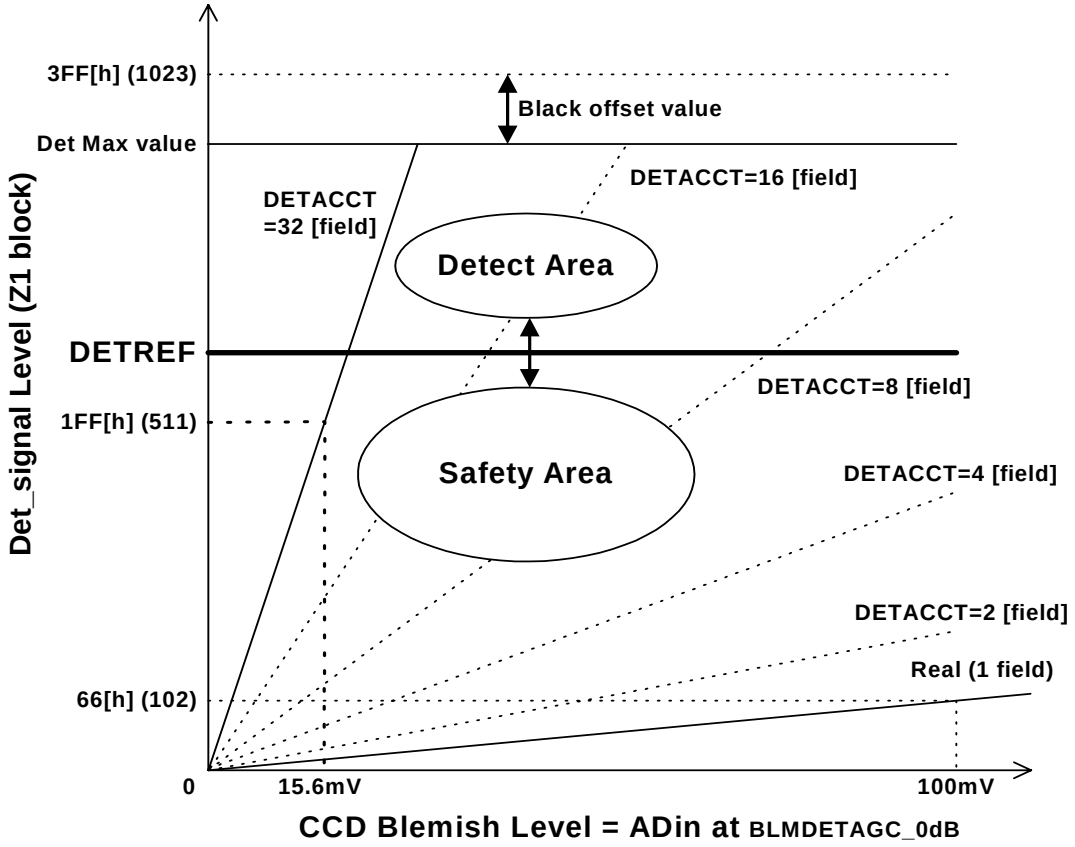


Fig 11.2-4 CCD Blemish level/accumulation time and DETREF

11.2.4. Dynamic detection and compensation function

Description of operations

This function holds a blemish address for each frame. It compares this address against the blemish address from N fields earlier, and if they match, a blemish is recognized. The blemish address held for each frame is an address with the highest blemish level among pixels which are at or above the threshold level when compared to two pixels of the same color filter adjacent in the horizontal direction, while the pixels surrounding the target pixel are at or below the dark level reference value during the normal imaging state. (This excludes blemish addresses that have already been detected.)

Detection performs in the normal imaging state. Thus, false detection may take place in dynamic detection. However, there is also a function for releasing such false blemishes. With this function, false blemishes up to a level set by the user can be released.

The diagram below shows an image of the dynamic detection operation. Determination data are the target pixel's level and the levels of the peripheral (horizontal and vertical) pixels. In reality, CCD performs 2-pixel addition read-out. The process of 1-pixel read-out is omitted from this explanation.

Detection operation (1)

As shown in **Fig 11.2-5**, the peripheral pixel levels are checked to determine whether or not they are at or below the dark level reference value.

Peripheral pixels can be selected using the parameter DETSPEC. The dark level reference value can be set using the parameter DARKREF/M.

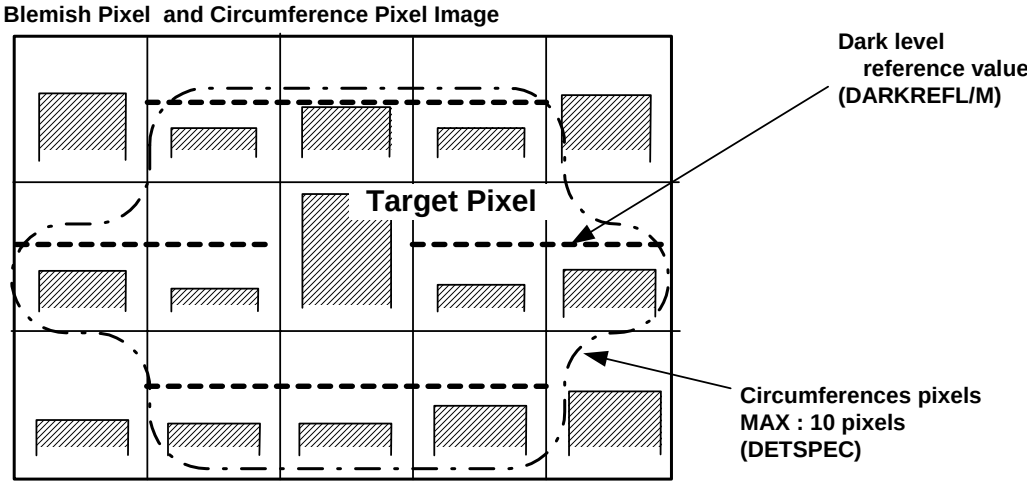


Fig 11.2-5 Dynamic detection overview (1)

Detection operation (2)

The only blemish address which is held is the highest-level blemish address within a frame, when the conditions of detection operation (1) are satisfied, and the target pixel is at or above a level consisting of the threshold level set in the parameter DETREFL/M plus the pixel level of each of two pixels of the same color filter which are adjacent in the horizontal direction.

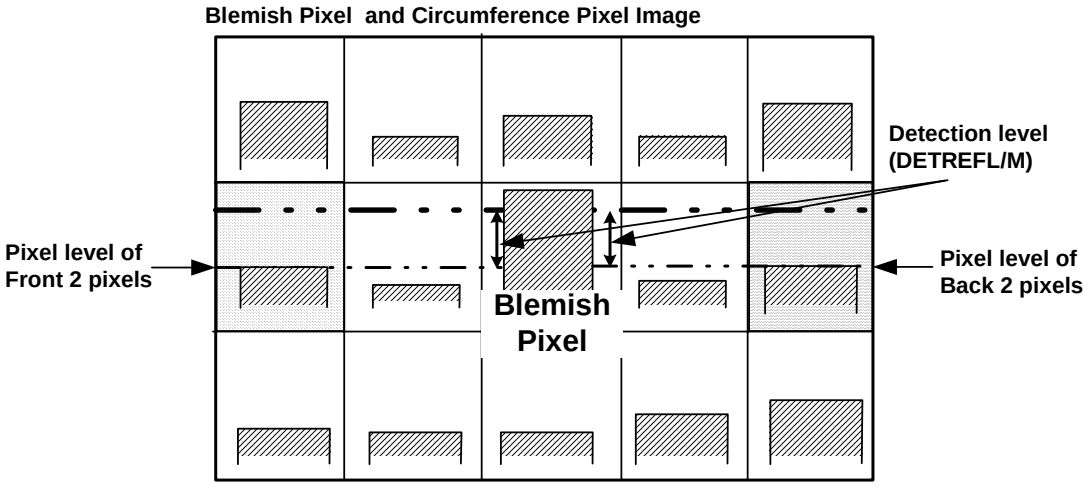


Fig 11.2-6 Dynamic detection overview (2)

Detection operation (3)

If a blemish address held in detection operation (2) matches the address from N fields earlier, then a blemish is recognized. The number of fields N can be set using the parameter FLDWAIT.

Compensation operation

Blemish pixels are corrected by replacing them with the average value of two pixels of the same color filter which are adjacent in the horizontal direction (same as for static detection and compensation).

* The results of blemish detection and compensation appear in “Table 11.2-15 Parameters for storing blemish detection results”.

Related parameters

Blemish compensation function ON/OFF

The following parameter is used to turn the blemish compensation function ON/OFF.

Table 11.2-11 Blemish compensation function ON/OFF parameter

Parameter		Description
DEFON	CAT1_Byte1_bit6	0[h]: Turns blemish compensation function OFF 1[h]: Turns blemish compensation function ON

* These parameters can be used for both static detection and dynamic detection.

Dynamic detection function ON/OFF

The following parameter is used to turn the dynamic detection function ON/OFF.

Table 11.2-12 Dynamic detection function ON/OFF parameter

Parameter		Description
DYNDETON	CAT1_Byte1_bit7	0[h]: Turns dynamic detection function OFF 1[h]: Turns dynamic detection function ON (default)

* Set this parameter to “1[h]” even if you do not plan on using the dynamic detection function.

Detection mode settings

This parameter is used to switch between normal blemish detection mode and large blemish detection mode. Normal blemish detection mode is detected to one blemish pixel. In large blemish detection mode, a pixel which the blemish more than a certain level adjoined is also detected as a blemish. (The detection and compensation process treats the blemish as a continuous blemish, but the correction place is counted as one place.)

Table 11.2-13 Parameter for switching blemish detection modes

Parameter		Description
LARGEON	CAT11_Byte1_bit3	0[h]:Normal Blemish detection mode 1[h]:Large Blemish detection mode

* These parameters can be used for both static detection and dynamic detection.

Detection threshold level settings

These parameters are used to set the blemish threshold level and the large blemish threshold level. Pixels exceeding the levels set in these parameters are recognized as being blemish.
Blemishes exceeding the normal blemish threshold level (DETREFL/M) are recognized as being normal blemishes. Blemishes exceeding the large blemish threshold level (LARGREFL/M) are recognized as being large blemishes.

Table 11.2-14 Parameters for setting detection threshold levels

Parameter		Description
DETREFL	CAT11_Byte5_bit0-7(LSB)	Used to set normal blemish threshold level
DETREFM	CAT11_Byte9_bit0-1(MSB)	
LARGREFL	CAT11_Byte7_bit0-7(LSB)	Used to set large blemish threshold level
LARGREFM	CAT11_Byte9_bit4-5(MSB)	

* These parameters can be used for both static detection and dynamic detection.
* When setting LARGREFL/M, be sure to set a value that is greater than the DETREFL/M value (DETREFL/M < LARGREFL/M).

Blemish detection results

The blemish detection results (type, level, address) are written to these parameters. Blemish detection results for a total of 32 blemishes may be written. (If there are fewer than 32 blemishes [e.g., if there are just two blemishes], the other parameters are left at their initial values and are not overwritten.)
Blemish detection results are written in order of blemish level, starting with the highest blemish level. If blemishes are detected through both static detection and dynamic detection, the blemishes found through static detection are written first.

Table 11.2-15 Parameters for storing blemish detection results

Parameter		Description	
SD**n***	CAT11_Byte20-147	Blemish detection type	0[h]: Static detection 1[h]: Dynamic detection
LARGE**n***		Blemish type	0[h]: Normal blemish 1[h]: Large blemish
VCNT**n***		Vertical address of blemish	10bit data
HCNT**n***		Horizontal address of blemish	
DETLV**n***		Blemish level	

*** n:0 - 31**

* These parameters can be used for both static detection and dynamic detection.

Blemish address resetting

This parameter is used to reset the values of parameters storing blemish detection results (all values are set to "00[h]").
Note that if blemish detection results are written to EEPROM (blemishes detected through static detection), the EEPROM values are not reset. This parameter resets the blemish detection results that have been applied to registers. (To reset EEPROM data, write "00[h]" to EEPROM.)
If this parameter is set to "1[h]" (reset ON), the blemish detection operation will not be performed, so normally it should be set to "0[h]".

Table 11.2-16 Parameter for resetting blemish address

Parameter		Description
ADDRRST	CAT11_Byte18_bit0	0[h]: Normal blemish detection operation 1[h]: Resets blemish detection results

* These parameters can be used for both static detection and dynamic detection.
* Enabled when DYNDETON=0[h] and DYNDELON=0[h]

Blemish correction count setting

The maximum number of detected blemishes is always 32. However, the number of corrections is set using the following parameter.

Table 11.2-17 Parameter for setting the number of blemish corrections

Parameter		Description
DEFNUM	CAT11_Byte3_bit2-6	Correction count setting 0[h]:1 correction - 1F[h]:32 corrections

* These parameters can be used for both static detection and dynamic detection.

Dynamic detection wait field count setting

In dynamic detection mode, the address with the highest-level blemish in a frame is compared with the addresses N fields before and following. It is stored as a blemish only if it matches. This parameter can be used to set the number of fields N.

Table 11.2-18 Parameter for setting dynamic detection wait field count

Parameter		Description
FLDWAIT	CAT11_Byte4_bit0-7	Dynamic detection wait field count (in frame increments, so only even numbers can be set)

Dark level reference value setting

This parameter is used to set the dark level reference value, which serves as a reference during dynamic detection.

Table 11.2-19 Parameter for setting dark level reference value

Parameter		Description
DARKREFL	CAT11_Byte8_bit0-7(LSB)	Dark level reference value setting
DARKREFM	CAT11_Byte9_bit6-7(MSB)	

Setting for number of peripheral pixels during dynamic detection

With dynamic detection, one of the detection conditions is that the pixels surrounding the target pixel be at or below the dark level reference value during the normal imaging state. The following parameter is used to change the number of peripheral pixels for the target pixel (blemish pixel).

Table 11.2-20 Setting for number of peripheral pixels during dynamic detection

Parameter		Description
DETSPEC	CAT11_Byte1_bit5-7	0[h]: All 10 peripheral pixels 1[h]: One of the ten peripheral pixels is not judged 2[h]: Two of the ten peripheral pixels are not judged 3[h]: Three of the ten peripheral pixels are not judged 4[h]: Eight pixels (above, below, left, right) 5[h]: One of the eight pixels (above, below, left, right) is not judged 6[h]: Four pixels (above, below, left, right) 7[h]: Four pixels in horizontal direction

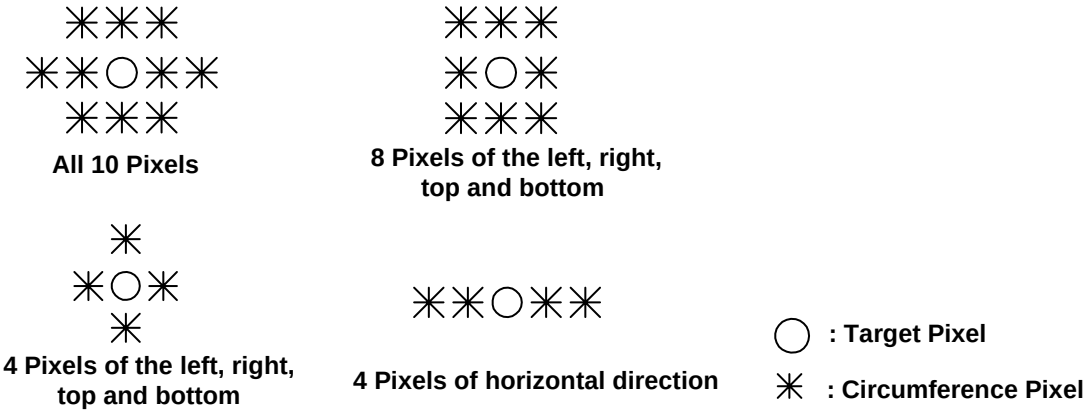


Fig 11.2-7 Layout of target pixel and peripheral pixels

Blemish releasing function ON/OFF

This parameter is used to turn ON/OFF the function for releasing blemishes that have been detected/corrected through dynamic detection.

Table 11.2-21 Blemish releasing function ON/OFF parameter

Parameter		Description
DYNDELON	CAT1_Byte2_bit0	0[h]: Turns blemish releasing function OFF 1[h]: Turns blemish releasing function ON

* Valid when DYNDETON=1[h]

Blemish releasing level setting

This parameter is used to set the releasing level for releasing detections made through dynamic detection.

Table 11.2-22 Parameter for setting releasing level

Parameter		Description
DELREFL	CAT11_Byte6_bit0-7(LSB)	Releasing level setting
DELREFM	CAT11_Byte9_bit2-3(MSB)	

* When the blemish releasing function is used as shown in the diagram below, held blemishes which have once exceeded the threshold level (DETREFL/M) can be released if they fall below the blemish releasing level (DELREFL/M) due to imaging subject conditions.

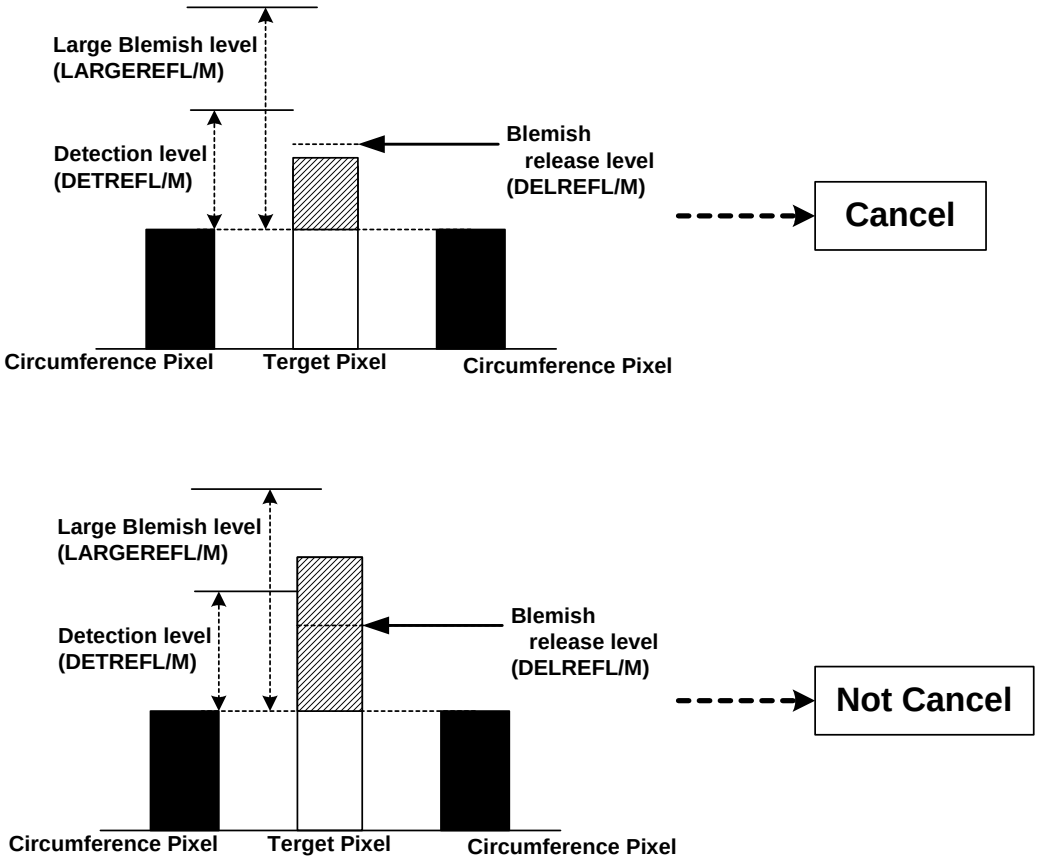


Fig 11.2-8 Overview of blemish releasing function

Setting procedure

Use the following procedure to set up dynamic detection and compensation.

1. Set the dynamic detection function to OFF. (DYNDETON=0[h]) (See Table 11.2-12)
2. Set the blemish detection area. (See Table 11.2-1)
3. Use DETSPEC to set the number of peripheral pixels. (See Table 11.2-20)
4. Set the number of detection-wait fields. (See Table 11.2-18)
5. Set the blemish reference dark level (DARKREFL/M). (See Table 11.2-19)
6. Use DETREFL/M and LARGEREFL/M to set the detection threshold levels. (See Table 11.2-14)
7. Turn the dynamic detection function ON. (DYNDETON=1[h]) (See Table 11.2-12)
8. Turn the blemish compensation function ON. (DEFON=1[h]) (See Table 11.2-11)

* To change the detection conditions, repeat steps 1 through 7.
* Set DYNDETON to 1[h] even if you do not plan to use dynamic detection and compensation.

11.2.5. False blemish generating function

Description of operations

This function generates false blemishes. The blemish level can be set as well, so use this function to check the blemish detection and compensation operations. This function may be used with both static detection and dynamic detection.

Related parameters

False blemish generating function

False blemishes can be detected and corrected just like CCD blemishes. Use this function to check the operations of the blemish detection and correction function.

Table 11.2-23 Parameters false blemishes

Parameter		Description
DEFPG	CAT11_Byte1_bit0	0[h]: No false blemishes 1[h]: Generate false blemish
DEFPGLVL	CAT11_Byte2_bit0-7(LSB)	Set false blemish level
DEFPGLVM	CAT11_Byte3_bit0-1(MSB)	

11.3. Adjustment of TG Phase

You can adjust phase and drive ability of high frequency TG pulse (H1, H2, RG, XSHP, XSHD, XRS). You can acquire a suitable CCD signal by adjusting phase and drive ability, and it can be well sampled. Since these phases may change with the composition of a substrate, or methods of wiring, please adjust a phase if needed.

11.3.1. Adjustment method of phase and drive ability

Adjustment of delay

Delay can be changed by the parameter of **Table 11.3-1**. Moreover, as shown in **Table 11.3-2**, a setting value is changed, and the amount of delay can be adjusted. Please refer to **Fig 11.3-1**about the situation of change.

Table 11.3-1 Adjusting parameter of delay

Parameter		Description
DEH1	CAT6_Byte9_bit0-3	Adjustment of H1delay
DEH2	CAT6_Byte9_bit4-7	Adjustment of H2delay
DERG	CAT6_Byte10_bit0-3	Adjustment of RG delay
DESHP	CAT6_Byte10_bit4-7	Adjustment of XSHP delay
DESHD	CAT6_Byte11_bit0-3	Adjustment of XSHD delay
DERS	CAT6_Byte11_bit4-7	Adjustment of XRS delay

Table 11.3-2 Amount of delay adjustment

Setting Value	Amount of adjustment (ns)
0[h]	0
1[h]	+1
2[h]	+2
3[h]	+3
4[h]	+4
5[h]	+5
6[h]	+6
7[h]	+7
8[h]	-8
9[h]	-7
A[h]	-6
B[h]	-5
C[h]	-4
D[h]	-3
E[h]	-2
F[h]	-1

* The values shown in table are rough data. These values are not guaranteed.

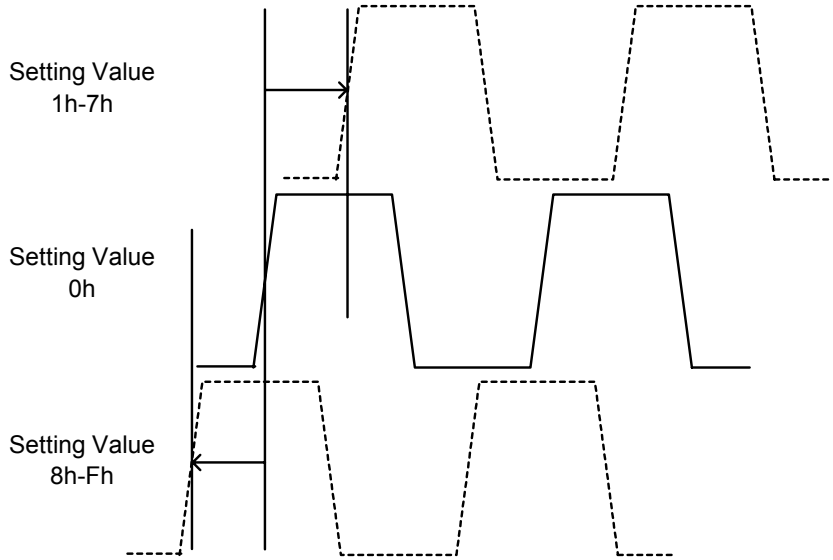


Fig 11.3-1 Adjustment of delay

Adjustment of duty

Duty can be changed by the parameter of **Table 11.3-3**. Moreover, as shown in **Table 11.3-4**, a setting value is changed, and the amount of duty can be adjusted. Please refer to **Fig 11.3-2** about the situation of change.

Table 11.3-3 Adjusting parameter of duty

Parameter		Description
DUH1	CAT6_Byte12_bit0-3	Adjustment of H1duty
DUH2	CAT6_Byte12_bit4-7	Adjustment of H2duty
DURG	CAT6_Byte13_bit0-3	Adjustment of RG duty
DUSHP	CAT6_Byte13_bit4-7	Adjustment of XSHP duty
DUSHD	CAT6_Byte14_bit0-3	Adjustment of XSHD duty
DURS	CAT6_Byte14_bit4-7	Adjustment of XRS duty

Table 11.3-4 Amount of duty adjustment

Setting Value	Amount of adjustment(ns)	Changing point
0[h]	0	-
1[h]	+1	Falling edge
2[h]	+2	
3[h]	+3	
4[h]	+4	
5[h]	+5	
6[h]	+6	
7[h]	+7	
8[h]	0	-
9[h]	+1	Rising edge
A[h]	+2	
B[h]	+3	
C[h]	+4	
D[h]	+5	
E[h]	+6	
F[h]	+7	

* The values shown in table are rough data. These values are not guaranteed.

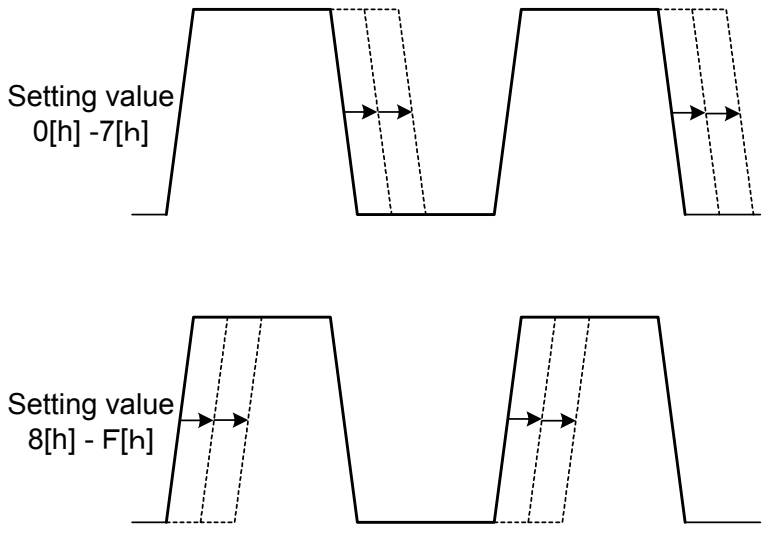


Fig 11.3-2 Adjustment of duty

Adjustment of drive ability

Drive ability can be changed by the parameters shown in **Table 11.3-5**.
“0[h]” is the maximum of drive ability and “6[h]” is the minimum of drive ability. (Common to each TG waveform)
When drive ability is set to "7[h]", each TG output terminal becomes high impedance. Therefore the pulse is not outputted. As an example, when DRBH1 is changed, H1 waveform measured on a Sony evaluation board is shown in **Fig 11.3-3**.
When drive ability is high, depending on substrate composition, the overshoot and the undershoot may appears in TG waveform. Please adjust drive ability if you need.

Table 11.3-5 Drive ability adjustment parameter

Parameter		Description
DRBH1	CAT6_Byte15_bit4-6	Adjustment of H1 drive ability
DRBH2	CAT6_Byte16_bit0-2	Adjustment of H2 drive ability
DRBRG	CAT6_Byte16_bit3-5	Adjustment of RG drive ability
DRBSHP	CAT6_Byte17_bit0-2	Adjustment of XSHP drive ability
DRBSHD	CAT6_Byte17_bit3-5	Adjustment of XSHD drive ability
DRBXRS	CAT6_Byte18_bit0-2	Adjustment of XRS drive ability

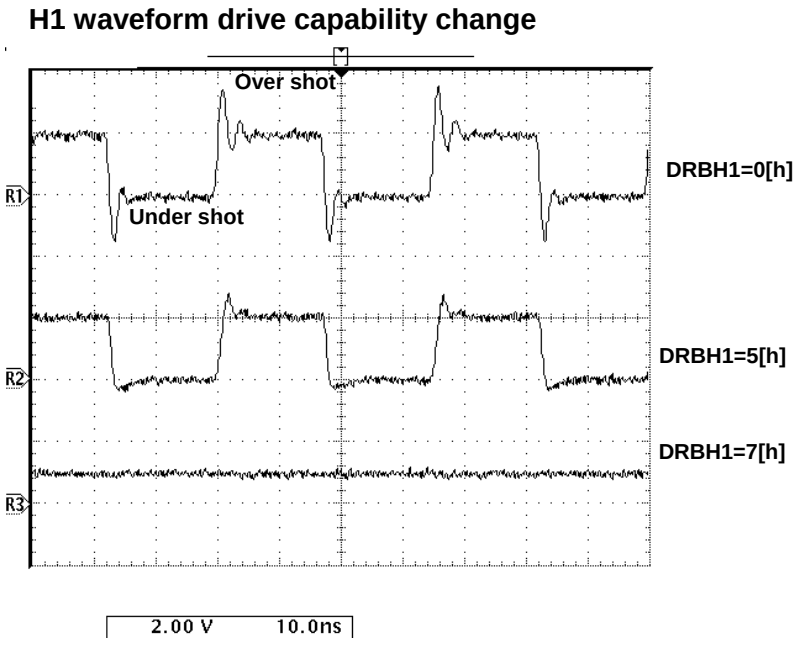


Fig 11.3-3 Drive ability adjustment

* This waveform was measured on a Sony evaluation board.
This waveform changes by circuit composition etc.

Phase relation of each signal

About the phase relation of each signal, please confirm the specifications of CCD to be used and the specifications of CXD3172AR.
These phases affect quality of image. Therefore, it is careful of the phase relation shown in **Fig 11.3-4** , and we recommend you to confirm by the picture finally.

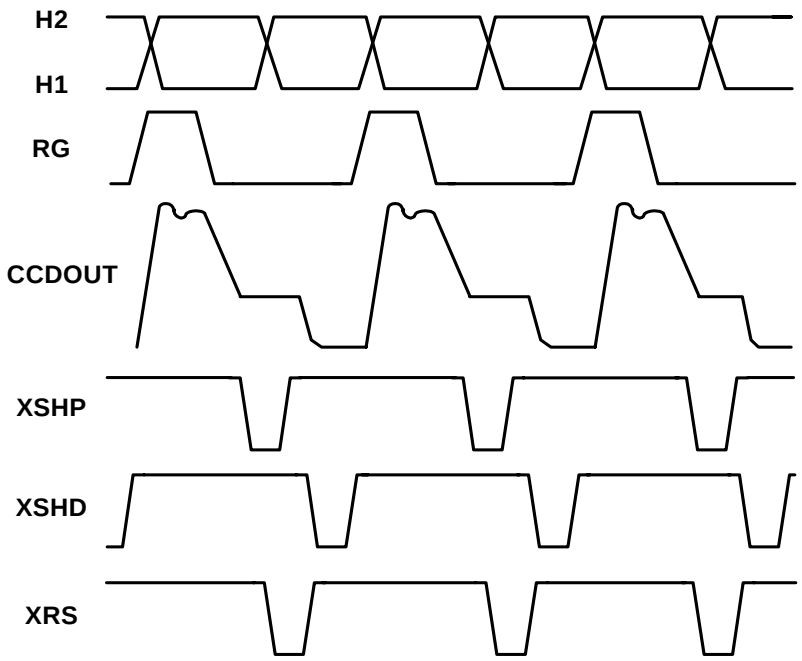


Fig 11.3-4 CCDOUT and TG waveform timing image

* This figure is an image. Please refer to this figure when you adjust the phase of TG.

12. Supporting Functions for applications

12.1. Using Digital Output

12.1.1. Operation Modes with Digital Output

The operation modes (MODESEL) available when digital output is used with the SS-HQ1 are limited.
See Appendix “13.2 Operation Mode Control during Digital Output” for details.

12.1.2. Digital Output Format

Two digital output formats are supported for output from the CXD3172AR: ITU-REC601-compliant output and ITU-REC656-compliant output.

• ITU-REC601-compliant output

Chroma signal	The pre-modulation signal is output as 8 bits from the Port 0-7 pins (CXD3172AR pins 91–94 and 96–99). The modulated signal cannot be output.
Luminance signal	This signal is output as 8 bits from the Port 8-15 pins (CXD3172AR pins 76-80 and 82-84). Sync is not added.
Output rate	Output at 1/2 the encoder clock (ECK) rate. (13.5MHz output is not supported.)
Sync signal	The horizontal sync signal DHD is output through the S0 pin (CXD3172AR pin 44). The vertical sync signal DVD is output through the S1 pin (CXD3172AR pin 46). The RYBY judgment signal (NRYBY) is output through the S3 pin (CXD3172AR pin 48).

• ITU-REC656-compliant output

The chroma signal, luminance signal, blanking signal, and TRC are multiplexed and output as 8 bits through the Port 8-15 pins (CXD3172AR pins 76-80 and 82-84).
The output rate is that of the encoder clock (ECK). (27MHz output is not supported.)

12.1.3. Digital Output Gain Setting

The digital output gain can be set independently of analog output, using the following parameters. For details, see 8. “Level Diagram”.

Table 12.1-1 Digital Gain Adjustment Parameters

Parameter		Description
RECYGAIN	CAT10_Byte8_bit0-7	Digital Y gain setting Setting range: 0-1.99x
RECRYGAIN	CAT10_Byte9_bit0-7	Digital R-Y gain Setting range: 0-3.99x
RECBYGAIN	CAT10_Byte10_bit0-7	Digital B-Y gain Setting range: 0-3.99x

12.1.4. Ways to Use Digital Output

There are two types of digital output: straight output and ITU-REC output. Each piece of output data is output at the rising edge of the clock output from the DCK pin (CXD3172AR pin 90). The DCK clock can be reversed and its delay adjusted through parameter settings (see **Table 12.1-3**).
Table 12.1-2 summarizes the parameters used for digital output settings.

Table 12.1-2 Parameters for Setting Digital Output

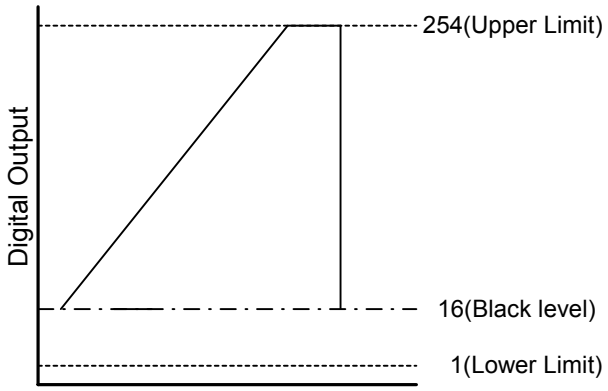
Parameter		Description
DIFON	CAT10_Byte14_bit7	DCK output ON/OFF control and digital signal processing operation 0[h]:OFF 1[h]:ON
RECOUT	CAT10_Byte1_bit0	Digital output level switching 0[h]:Straight output 1[h]:ITU-REC output
DIFOUT	CAT10_Byte1_bit2	Digital output format switching 0[h]:ITU-REC601-compliant output 1[h]:ITU-REC656-compliant output
YDSEL	CAT1_Byte7_bit4	Port 8-15 pin setting switching 0[h]:Port driver 1[h]:YUV digital signal output
CDSEL	CAT1_Byte7_bit5	Port 0-7 pin setting switching 0[h]:Port driver 1[h]:C digital signal output
S0IN	CAT1_Byte7_bit6	S0 pin I/O switching (*1) 0[h]:DHD output 1[h]:VRI input
S1IN	CAT1_Byte7_bit7	S1 pin I/O switching (*1) 0[h]:DVD output 1[h]:HRI input
S3SEL	CAT8_Byte8_bit3-5	S3 pin I/O switching (*1) 0[h]:DHD 1[h]:DVD 2[h]:HD 3[h]:VD 4[h]:NRYBY (color judgment signal) 5[h]:TEST signal 6[h]:FLD 7[h]:Analog shift FSC input
BLCKLV	CAT10_Byte1_bit3-7	Variable black level setting (valid when RECOUT=1[h]) Variable range:0[h]-1F[h]

(*1) The settings for the individual parameters are controlled by firmware. For information on how to change the settings, see 12.6 “Sync Signal Output Setting Method”.

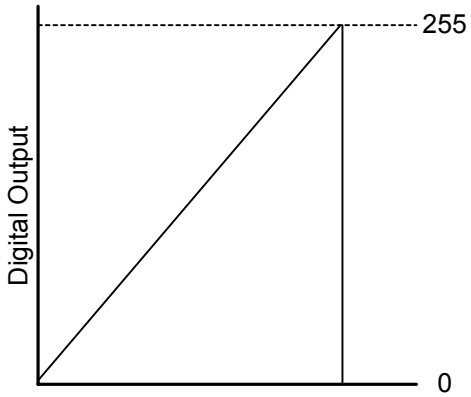
Table 12.1-3 DCK Adjustment Parameters

Parameter		Description
DCKINV	CAT10_Byte14_bit4	DCK output reversal 0[h]: Normal 1[h]: Reverse
DCKDL	CAT10_Byte14_bit5-6	DCK output delay adjustment 0[h]:0ns 1[h]:5ns 2[h]:10ns 3[h]:15ns
DIFCKSEL	CAT1_Byte4_bit6-7	DCK clock selector 0[h]:ECK/2 1[h]:ECK 2[h]:MCK/2 3[h]:MCK

* DIFCKSEL is controlled by firmware based on the MODESEL (CAT12_Byte1_bit0-3) setting. Note, however, that it is only controlled during the initial operation, after which it is open to the user.



ITU-Rec Luminance Output
RECOUT=1[h]



Straight Luminance Output
RECOUT=0[h]

Fig 12.1-1 Differences in Luminance Setting in Each Output Type (with ramp signal input)

* The black level of luminance output can be varied in the range of 0[h] to 1F[h] using BLCKLV. Note that the Y signal high luminance direction range also changes together with the black level. The recommended setting is 10[h].

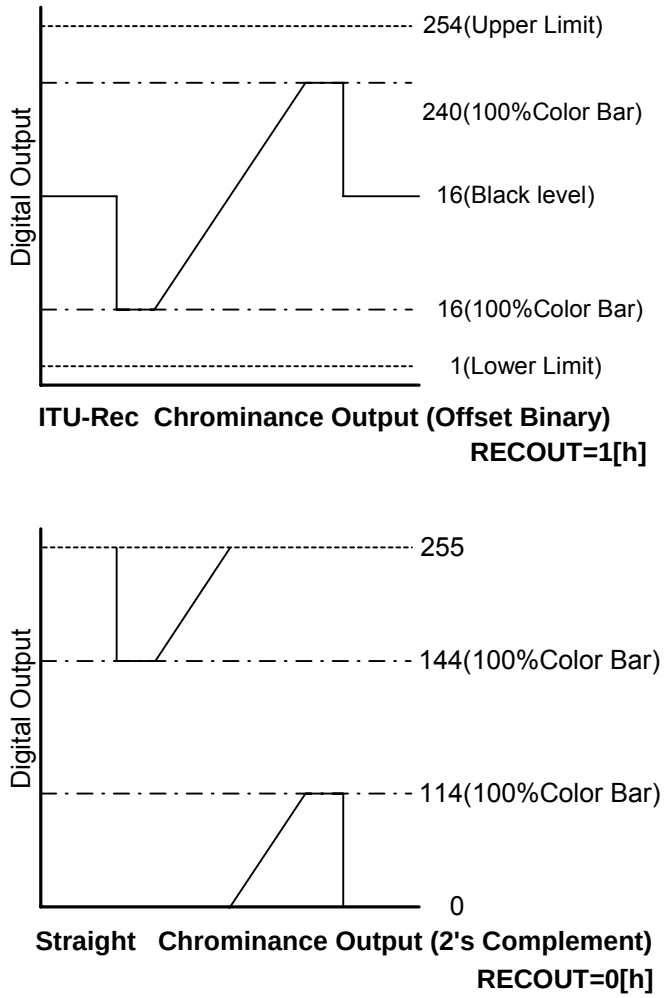


Fig 12.1-2 Differences in Chroma Signal in ach Output Type (with ramp signal input, including plus/minus sign)

12.1.5. Parameter Settings for Each Output Type

Table 12.1-4 summarizes the main parameter settings for each output type.

Table 12.1-4 Parameter Settings for Each Output Type

Parameter		Setting Value			
		Straight output		ITU-REC	
		REC601	REC656	REC601	REC656
DIFON	CAT10_Byte14_bit7	1[h]	1[h]	1[h]	1[h]
RECOUT	CAT10_Byte1_bit0	0[h]	0[h]	1[h]	1[h]
DIFOUT	CAT10_Byte1_bit2	0[h]	1[h]	0[h]	1[h]
YDSEL	CAT1_Byte7_bit4	1[h]	1[h]	1[h]	1[h]
CDSEL	CAT1_Byte7_bit5	1[h]	0[h]	1[h]	0[h]
BLKCKLV	CAT1_Byte1_bit3-7	-	-	10[h]*	10[h]*

* The BLKCKLV shown is the recommended value.

12.1.6. ITU-REC656

TRC settings

When ITU-REC656-compliant output is set, a timing reference code (TRC) indicating the horizontal and vertical blanking periods is multiplexed and output with the Y/Cr/Cb data.
The SS-HQ1 uses the following ITU-REC-compliant codes as codes for the TRC fourth word.

Table 12.1-5 ITU-REC656 TRC(Fourth word)

7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit	HEX
1fixed	F	V	H	P3	P2	P1	P0	
1	0	0	0	0	0	0	0	80[h]
1	0	0	1	1	1	0	1	9D[h]
1	0	1	0	1	0	1	1	AB[h]
1	0	1	1	0	1	1	0	B6[h]
1	1	0	0	0	1	1	1	C7[h]
1	1	0	1	1	0	1	0	DA[h]
1	1	1	0	1	1	0	0	EC[h]
1	1	1	1	0	0	0	1	F1[h]

F=0 Field 1 period F=1 Field 2 period
V=0 Active video period V=1 Vertical blanking period
H=0 SAV(Start of Active Video) H=1 EAV(End of Active Video)
P0-P3: Error correction bits

The following table summarizes the serial settings related to TRC settings.

Table 12.1-6 Serial Settings Related to TRC Output

Parameter		Description
EAVSTAL	CAT10_Byte2_bit0-7(LSB)	Variable EAV start position setting Variable value:1[h] = 1dck
EAVSTAM	CAT10_Byte3_bit0-2(MSB)	
SAVSTAL	CAT10_Byte4_bit0-7(LSB)	Variable SAV start position setting Variable value:1[h] = 1dck
SAVSTAM	CAT10_Byte5_bit0-2(MSB)	
FLD1FSTA	CAT10_Byte6_bit0-2	Field 1 valid video period start position setting Variable value:1[h] = 1DHD
FLD1VSTA	CAT10_Byte6_bit3-7	Field 1 vertical blanking period start position setting Variable value:1[h] = 1DHD
FLD2FSTA	CAT10_Byte7_bit0-2	Field 2 valid video period start position setting Variable value:1[h] = 1DHD
FLD2VSTA	CAT10_Byte7_bit3-7	Field 2 vertical blanking period start position setting Variable value:1[h] = 1DHD

Horizontal timing

Fig 12.1-3 summarizes the relationships between DCK, DHD, and the output data (DOUT).

During horizontal synchronization, DHD falling is detected and the counter is reset.

The counter maximum value is determined from each mode's clock frequency and the TV system's horizontal period.

Therefore, set the SAV and EAV start position settings (EAVSTAL/M and SAVSTAL/M) so that they are less than the maximum setting (see **Table 12.1-7**). If they are not set to less than the maximum setting (see **Table 12.1-7**), video will not be output.

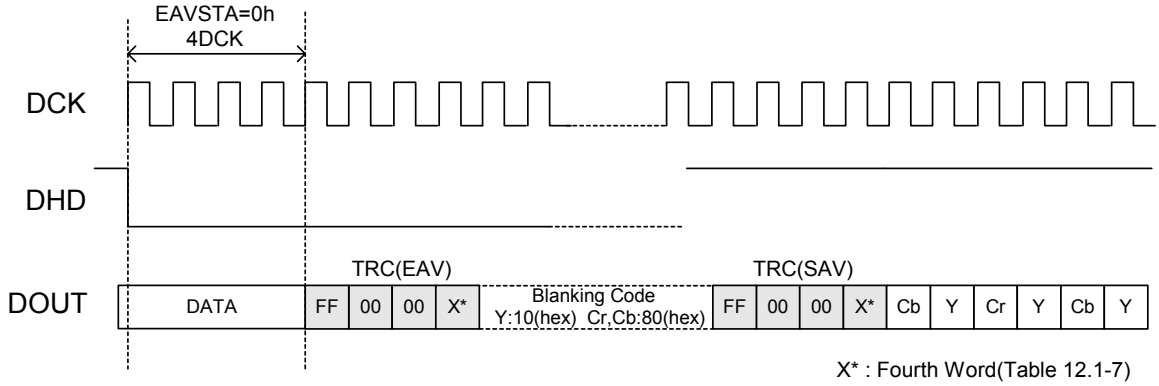


Fig 12.1-3 ITU-REC656 Relationships Between DCK, DHD and Output Data

• **SAV and EAV maximum values and recommended settings for each operation mode**

Table 12.1-7 SAV and EAV maximum values and recommended settings for each operation mod

TV system	CCD Type	Operation mode MODESEL	Maximum setting	Recommended value	
				EAVSTAL/M	SAVSTAL/M
NTSC	510H	0[h]	4BB[h]	0[h]	CF[h]
	760H	6[h]	71B[h]	0[h]	118[h]
PAL	510H	3[h]	4BB[h]	0[h]	117[h]
	760H	9[h]	717[h]	0[h]	133[h]

* Due to the circuit configuration, SAV and EAV are output following the actual setting plus 4DCK.

* Set the values so that the maximum value is greater than SAVSTAL/M minus EAVSTAL/M.

Vertical timing

During vertical synchronization, as in horizontal synchronization, the counter is reset when DVD falls and incremented when HD falls (see **Fig 12.1-4** and **Fig 12.1-5**).

Set the Field 1 and Field 2 blanking periods separately for each TV system in the blanking start parameters in **Table 12.1-6**.

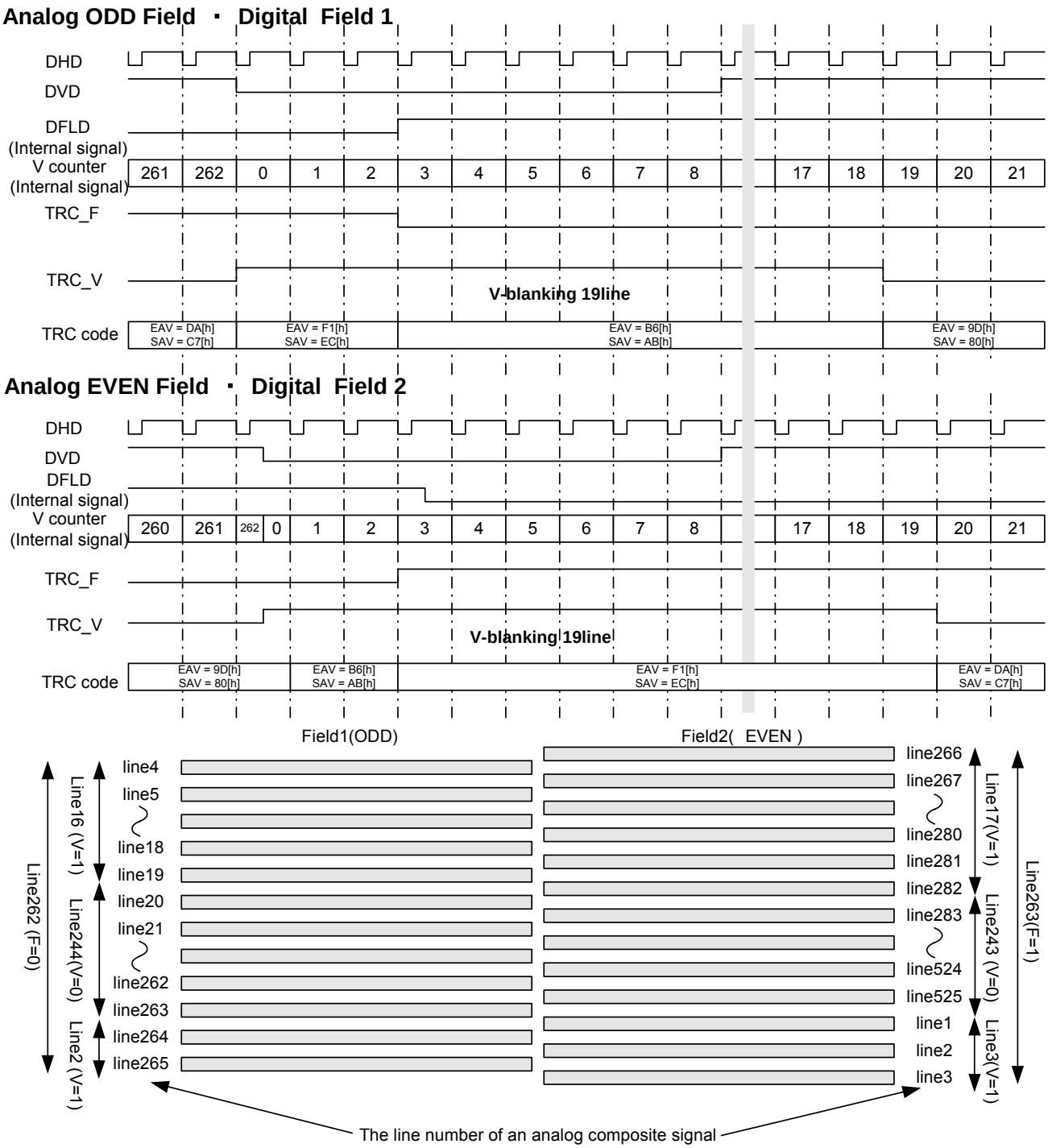


Fig 12.1-4 Vertical Direction Timing NTSC

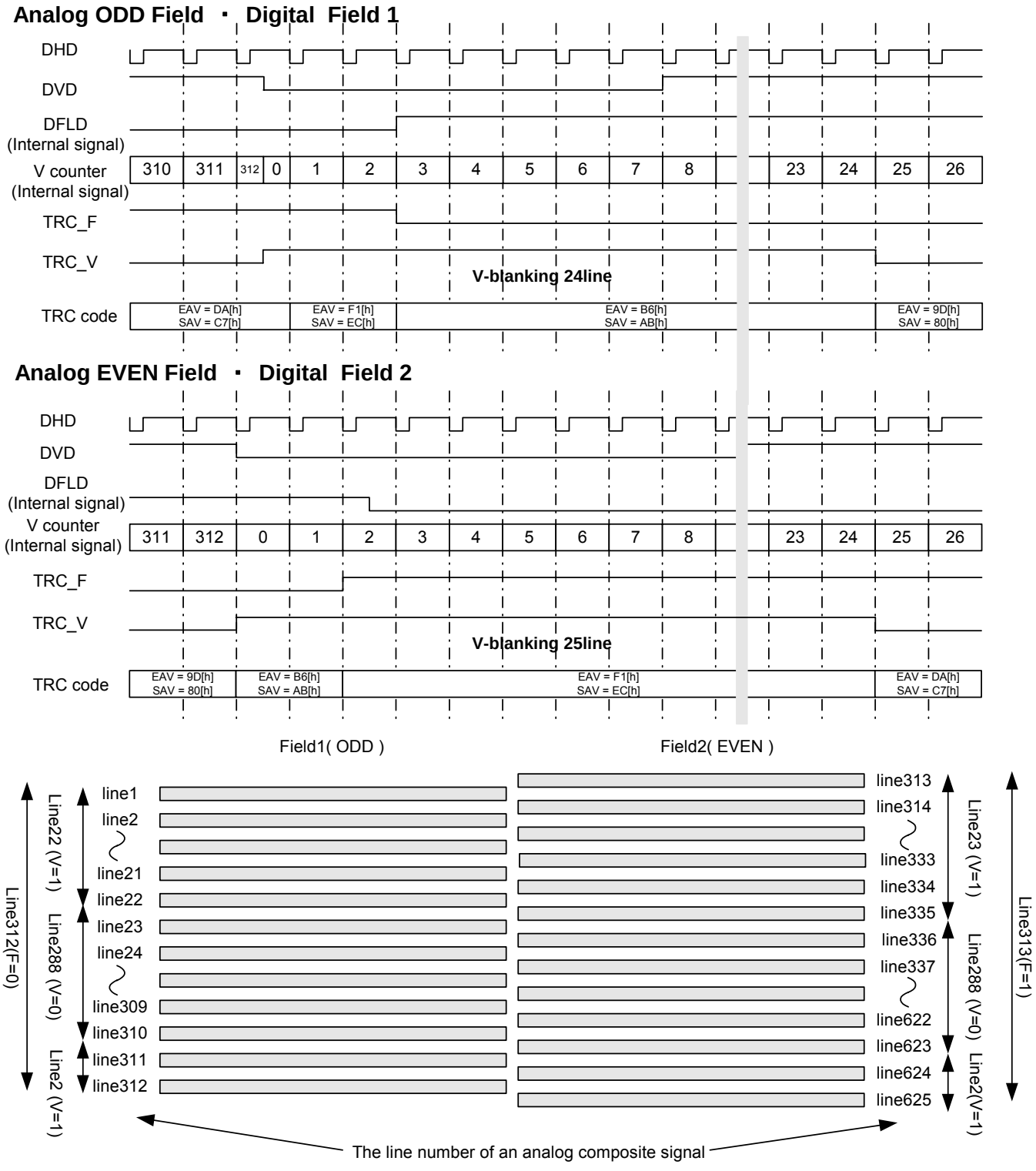


Fig 12.1-5 Vertical Direction Timing PAL

Table 12.1-8 Blanking Parameter Recommended Values

Parameter		Recommended value	
		NTSC	PAL
FLD1FSTA	CAT10_Byte6_bit0-2	3[h]	3[h]
FLD1VSTA	CAT10_Byte6_bit3-7	12[h]	18[h]
FLD2FSTA	CAT10_Byte7_bit0-2	3[h]	2[h]
FLD2VSTA	CAT10_Byte7_bit3-7	13[h]	18[h]

12.2. Using external synchronization

12.2.1. Synchronization for the SS-HQ1 system

The SS-HQ1 system supports line lock, VS lock, VBS lock, V reset H reset, and other external synchronization systems.

Internal mode (INT)

In this mode, external synchronization is not applied.

Line lock mode (LL)

In this mode, the camera's vertical phase is synchronized to the AC power supply. The power supply frequency is 60Hz for NTSC and 50Hz for PAL.

VS lock mode (VSL)

There are three different VS lock mode types as detailed below. They are categorized based on the synchronization signal and operation.

- **VSL**
  In this mode, the camera's vertical and horizontal phases are synchronized to an external video signal. The reset operation is performed in the vertical direction, and the PLL operation is performed in the horizontal direction.
- **VSL-S**
  In this mode, the camera's vertical and horizontal phases are synchronized to an external VD/HD signal. The reset operation is performed in the vertical direction, and the PLL operation is performed in the horizontal direction.
- **VSL-D**
  In this mode, the camera's vertical and horizontal phases are synchronized to an external digital sync signal. The reset operation is performed in the vertical direction, and the PLL operation is performed in the horizontal direction.

VBS lock mode (VBSL)

In this mode, the camera's vertical, horizontal, and subcarrier phases are synchronized to an external video signal. There are two different VBS lock mode types as detailed below. They are categorized based on the synchronization operation.

- **VBSLHP**
  In this mode, the camera's vertical, horizontal, and subcarrier phases are synchronized to an external video signal. The reset operation is performed in the vertical direction, and the PLL operation is performed on the subcarrier. In addition, the PLL operation is performed in the horizontal direction.
- **VBSLHR**
  In this mode, the reset operation is performed in the vertical direction, and the PLL operation is performed on the subcarrier. In addition, the reset operation is performed in the horizontal direction.

V reset H reset mode (VRHR)

In this mode, the camera's vertical, horizontal, and LALT (PAL) phases are synchronized to an external VD/HD/LALT (PAL) reset signal.

12.2.2. Parameters used to set external synchronization

The following two parameters are used to set external synchronization modes.

- **ATMODEON (CAT17_Byte17_bit5)**
- **SGMODE (CAT17_Byte17_bit0-3)**

With ATMODEON, the external input signal is recognized and the external synchronization mode is switched automatically based on that signal. With SGMODE, the external synchronization mode is switched based on a value set by the user.

* When ATMODEON is set to 1[h] (ATMODEON=1[h]), the ATMODEON operation is given priority, so the value set for SGMODE is not updated. To use SGMODE, set ATMODEON to 0[h] (ATMODEON=0[h]).

Auto mode (ATMODEON)

When ATMODEON is set to 1[h] (ATMODEON=1[h]), an external signal is detected. Based on this, the external synchronization mode is determined and switched automatically. Auto mode is turned ON/OFF using the following parameter.

Table 12.2-1 ATMODEON Parameter

Parameter		Description
ATMODEON	CAT17_Byte17_bit5	0[h] : Auto mode OFF 1[h] : Auto mode ON

Auto mode detection parameter

The parameters (detection flags) in **Table 12.2-2** change when an external signal is input through the designated pin. Based on this result, the external synchronization mode is switched automatically (see **Table 12.2-3**). In addition, if the parameters set in **Table 12.2-4** are set, then detection will be disabled, even if an external signal is input to the designated pin.

Table 12.2-2 Detection flag parameters

Input pin	Parameter		Description
S1(46pin)	EXHDET	CAT22_Byte1_bit0	EXT-HD input detection flag
S0(44pin)	EXVDET	CAT22_Byte1_bit1	EXT-VD input detection flag
EXVIDEOY(57pin)	EXSDET	CAT22_Byte1_bit2	EXT-SYNC input detection flag
EXVIDEO(58pin)	EXBDET	CAT22_Byte1_bit3	EXT-BURST input detection flag

* When the designated external signal is input, each parameter is set to “1[h]”. Otherwise, they are set to “0[h]”.

Table 12.2-3 Correspondence between detection flag parameters and external synchronization modes

EXHDET	EXVDET	EXSDET	EXBDET	External synchronization mode	Controlled parameter
0[h]	0[h]	0[h]	0[h]	INT	SGMODE = 0[h] equivalent
0[h]	1[h]	0[h]	0[h]	LL	SGMODE = 1[h] equivalent
0[h]	0[h]	1[h]	0[h]	VSL	SGMODE = 2[h] equivalent
0[h]	0[h]	1[h]	1[h]	VBSLHP	SGMODE = 3[h] equivalent
1[h]	1[h]	0[h]	0[h]	VRHR	SGMODE = 5[h] equivalent

* Set SGMODE (CAT17_Byte17_bit0-3) to use an external synchronization mode other than the above.

* For information on the controlled parameters,see **Table 12.2-6**, **Table 12.2-7**, **Table 12.2-8**,and **Table 12.2-9**.

Table 12.2-4 Detection disabling parameters

Parameter		Description
HDETOFF	CAT7_Byte2_bit0	EXT-HD input detection 0[h]: Enable 1[h]: Disable
VDETOFF	CAT7_Byte2_bit1	EXT-VD input detection 0[h]: Enable 1[h]: Disable
SDETOFF	CAT7_Byte2_bit2	EXT-SYNC input detection 0[h]: Enable 1[h]: Disable
BDETOFF	CAT7_Byte2_bit3	EXT-BURST input detection 0[h]: Enable 1[h]: Disable

SGMODE

SGMODE is used to switch the external synchronization mode based on a value set by the user. The relationships between SGMODE and the various external synchronization modes are shown in **Table 12.2-5**.

Table 12.2-5 SGMODE and external synchronization modes

SGMODE	External synchronization mode	Remarks
0[h]	Internal mode (INT)	Enabled when ATMODEON=0[h]
1[h]	Line lock mode (LL)	
2[h]	VS lock mode (VSL)	
3[h]	VBS lock mode (VBSLHP)	
4[h]	VBS lock mode (VBSLHR)	
5[h]	V reset H reset mode (VRHR)	
A[h]	VS lock mode (VSL-S)	
F[h]	VS lock mode (VSL-D)	

SGMODE controlled parameters

The values of some parameters are controlled automatically based on SGMODE through F/W control in order to facilitate external synchronization mode switching.

The following table shows the relationships between the SGMODE-controlled parameters and values. The parameters in **Table 12.2-6** set the synchronization signal I/O pins which are F/W-controlled based on SGMODE. The relationships between these parameters and SGMODE are shown in **Table 12.2-7**.

Table 12.2-6 SGMODE control pins (parameters setting synchronization signal I/O pins)

Pin name (pin No)	Parameter		Description		
			0[h]	1[h]	7[h]
S0(44pin)	S0IN	CAT1_Byte7_bit6	DHD output	VRI input	-
S1(46pin)	S1IN	CAT1_Byte7_bit7	DVD output	HRI input	-
S2(47pin)	S2SEL	CAT1_Byte8_bit0-2	FSC comparison output	DHD output	LALT IN
S3(48pin)	S3SEL	CAT1_Byte8_bit3-5	DHD output	DVD output	Analog shift FSC input
S4(49pin)	S4SEL	CAT1_Byte8_bit6-7	External EVR chip select output	FSC output	VD output

* For information on other settings, see “12.6 Sync Signal Output Setting Method”.

Table 12.2-7 SGMODE controlled parameter values (parameters setting synchronization signal I/O pins)

SGMODE	controlled parameters				
	S0IN	S1IN	S2SEL	S3SEL	S4SEL
0[h]	-	-	-	-	-
1[h]	1[h]	-	-	-	-
2[h]	-	-	-	-	-
3[h]	-	-	0[h]	7[h]	1[h]
4[h]	-	-	0[h]	7[h]	1[h]
5[h]	1[h]	1[h]	-	-	-
A[h]	1[h]	1[h]	-	-	-
F[h]	-	1[h]	-	-	-

* Hyphens ("-") denote cases where the setting can be changed as desired.
  For information on the settings, see "12.6 Sync Signal Output Setting Method".
* The CXD3172AR default (when there are no valid data in EEPROM) is S0IN=1[h]; otherwise, 0[h] is set.

The parameters shown in **Table 12.2-8** are related to external synchronization which is F/W-controlled based on SGMODE. **Table 12.2-9** shows the relationships between these parameters and SGMODE.

Table 12.2-8 SGMODE controlled parameters (parameters related to external synchronization)

Parameter		Description
INTEXT	CAT7_Byte1_bit0	-
HVPLL	CAT7_Byte1_bit1	1[h] : V-PLL (EXSTAT signal equivalent)
SYNCEX	CAT7_Byte1_bit2	-
VRSTON	CAT7_Byte1_bit3	-
HRSTON	CAT7_Byte1_bit4	-
BCMPON	CAT7_Byte1_bit7	-
SSEPEXT	CAT7_Byte11_bit1	-

* These parameters should not be arbitrarily changed by the user.

Table 12.2-9 SGMODE controlled parameter values (parameters related to external synchronization)

SGMODE	controlled parameters						
	INTEXT	HVPLL	SYNCEX	VRSTON	HRSTON	BCMPON	SSEPEXT
0[h]	0[h]	0[h]	0[h]	0[h]	0[h]	0[h]	0[h]
1[h]	1[h]	1[h]	1[h]	0[h]	0[h]	0[h]	0[h]
2[h]	1[h]	0[h]	0[h]	1[h]	0[h]	0[h]	0[h]
3[h]	1[h]	0[h]	0[h]	1[h]	0[h]	1[h]	0[h]
4[h]	0[h]	0[h]	0[h]	1[h]	1[h]	1[h]	0[h]
5[h]	0[h]	0[h]	1[h]	1[h]	1[h]	0[h]	0[h]
A[h]	1[h]	0[h]	1[h]	1[h]	0[h]	0[h]	0[h]
F[h]	1[h]	0[h]	0[h]	1[h]	0[h]	0[h]	1[h]

12.2.3. Internal mode (INT)

In this mode, external synchronization is not applied.
There are two different system configurations: a 1-clock/digital encoder system, and an ECK master–MCK PLL system. The SGMODE set value is 0[h] (see **Table 12.2-5**).

1-clock/digital encoder system configuration

In this system, the DSP is operated using just one clock. The encoding clock (ECK) is supplied to also generate the system driving clock inside the DSP.
Typically X'tal oscillation is used to generate the encoding clock (ECK). **Fig 12.2-1** shows the system block diagram. **Table 12.2-10** presents the external input signals.

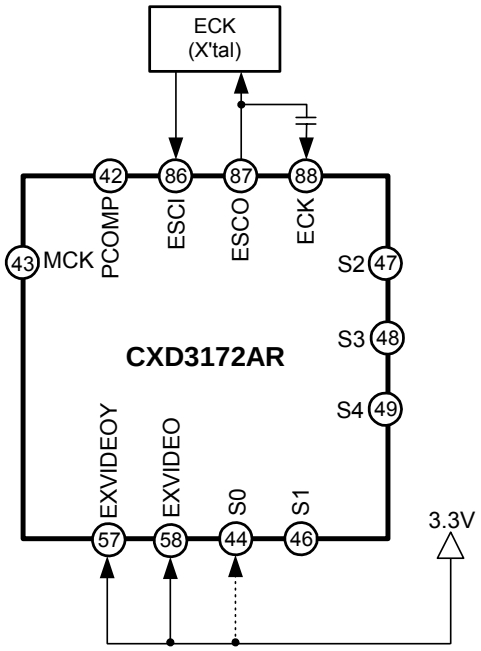


Fig 12.2-1 Internal mode (1-clock/digital encoding)

Table 12.2-10 External input signals (1-clock/digital encoding)

Pin Name	Pin No	Input Signal
S0	44pin	Connected to 3.3V
EXVIDEOY	57pin	
EXVIDEO	58pin	

* In INT mode S0 (pin 44) is not controlled by SGMODE, so any I/O setting can be set. However, under the CXD3172AR default values, S0 is set to input. Therefore, to set input, pull it up to 3.3V in accordance with the system you are using.

2-clock/ECK master–MCK PLL system configuration

This system comprises two clocks, with the encoding clock (ECK) serving as the master, and with PLL applied to the system driving clock (MCK). The master signal is the encoding clock (ECK). Typically X'tal oscillation is used as the MCK VCXO. **Fig 12.2-2** shows the system configuration. **Table 12.2-11** presents the external input signals.

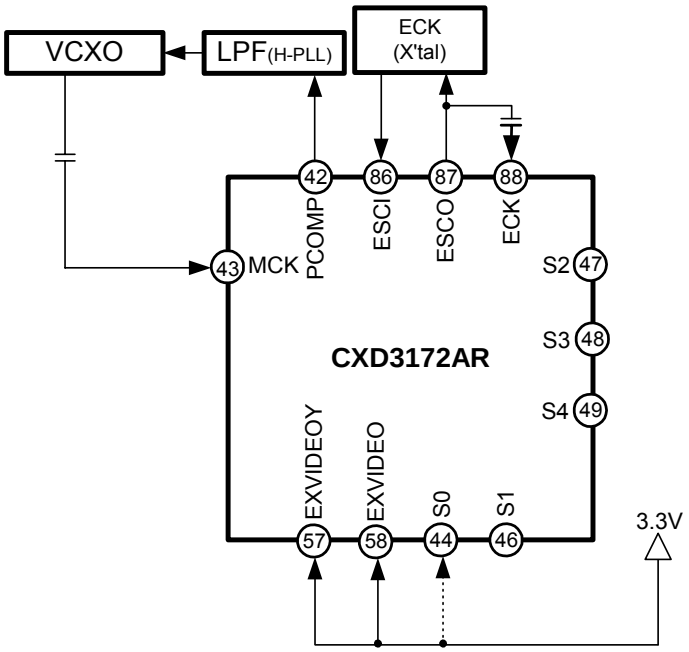


Fig 12.2-2 Internal mode (2-clock MCK-PLL)

Table 12.2-11 External input signal (2-clock MCK-PLL)

Pin Name	Pin No	Input Signal
S0	44pin	Connected to 3.3V
EXVIDEOY	57pin	
EXVIDEO	58pin	

* In INT mode S0 (pin 44) is not controlled by SGMODE, so any I/O setting can be set. However, under the CXD3172AR default values, S0 is set to input. Therefore, to set input, pull it up to 3.3V in accordance with the system you are using.

Internal phase comparison

The CXD3172AR internally compares the phases of the ECK-DHD signal with the frequency-divided encoding clock (ECK), against the MCK-HD signal with the frequency-divided MCK. The phase comparison result is output through PCOMP (pin 42). The PCOMP signal should be applied to LPF (H-PLL) and fed back to the MCK (pin 43) VCO. The PCOMP signal can be polarity-inverted by PCMPINV (CAT7_Byte2_bit4).
In addition, it is possible to select either active filtering or passive filtering in accordance with the external LPF specifications. However, active filtering is recommended since it provides higher performance.
Fig 12.2-3 shows the PCOMP output waveform when a lock is applied. **Fig 12.2-4** shows the PCOMP output waveform without a lock. (From measurements using our evaluation board.) Apply a trigger to the ECK-DHD signal output from S2 (pin 47) and view the PCOMP output waveform to check whether a lock has been applied.

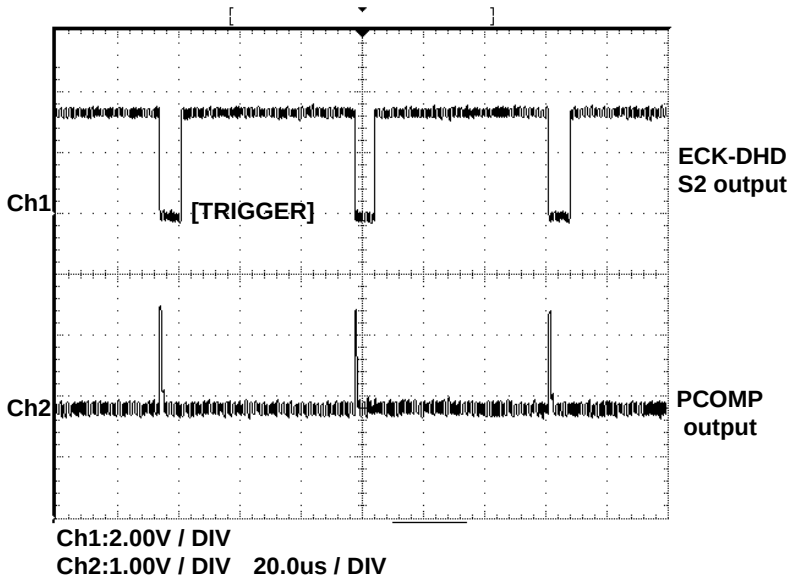


Fig 12.2-3 PCOMP output waveform (locked)

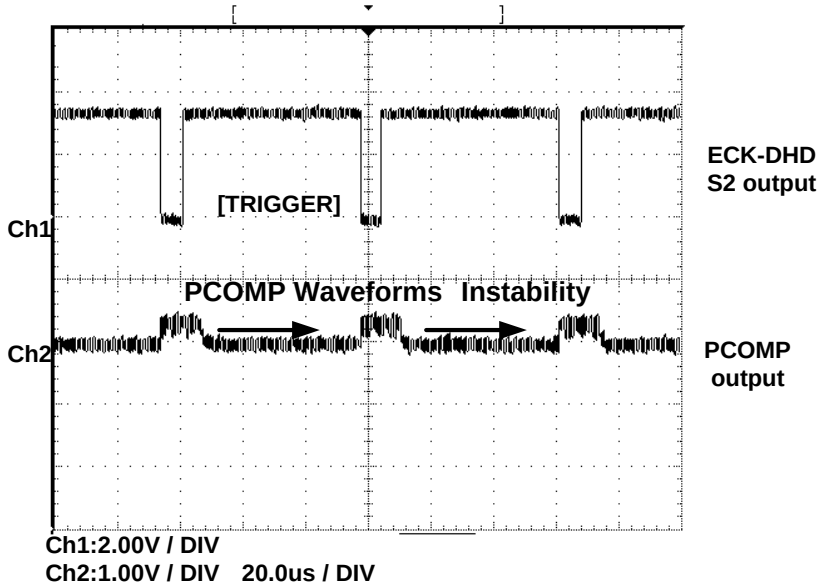


Fig 12.2-4 PCOMP output waveform (unlocked)

12.2.4. Line lock mode (LL)

Line lock mode is a type of external synchronization in which the camera's vertical phase is synchronized to the AC power supply. The power supply frequency is 60Hz for NTSC and 50Hz for PAL.
The SGMODE setting is 1[h] (see **Table 12.2-5**).
The SGMODE LSB is set as a port driver function to P10 (pin 78) under the CXD3172AR initial settings. Therefore, to set line lock mode under the CXD3172AR initial conditions (when there are no valid data in the EEPROM), set the CXD3172AR's P10 (pin 78) to High.

Table 12.2-12 TV systems and supply frequencies

TV system	Line lock supply frequency
NTSC	60Hz
PAL	50Hz

System configuration

The line lock mode master signal is the power supply square wave. A power supply square wave (3.3V amplitude/digital signal), obtained by waveform-rectifying the AC power supply, is input to S0 (pin 44).
In addition, in line lock mode, a 27.000MHz clock is used as the input to ECK (pin 88). The MODESEL (operation mode setting) settings in this case are shown in **Table 12.2-13**. Typically LC oscillation is used as the MCK VCO. The subcarrier is free-run.

* When the 760H CCD is used to run line lock mode, the following MODESEL settings are removed from the specifications.
  MODESEL=6[h],7[h] : NTSC
  MODESEL=9[h] : PAL

Table 12.2-13 MODESEL settings (ECK-27.000MHz)

MODESEL (CAT12_Byte1_bit0-3)	TV system	CCD Type
8[h]	NTSC	760H
B[h]	PAL	

* Note that with the above MODESEL settings, the subcarrier is free-run even in internal mode (INT).

The system configuration is shown in **Fig 12.2-5**. **Table 12.2-14** presents the external input signals.

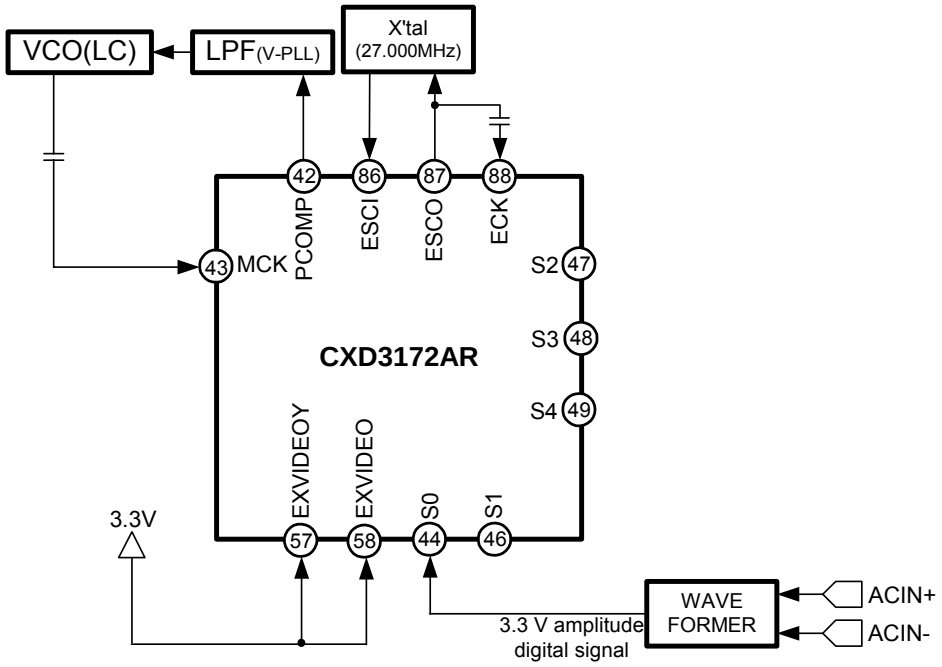


Fig 12.2-5 Line lock mode

Table 12.2-14 External input signals (Line lock mode)

Pin Name	Pin No	Input Signal
S0	44pin	3.3V oscillating/digital signal
EXVIDEOY	57pin	Connected to 3.3V
EXVIDEO	58pin	

Internal phase comparison

The CXD3172AR internally compares the phases of the external power supply square wave signal (S0 pin 44 input), and the VD (MCK-VD) signal obtained by frequency-dividing the MCK (pin 43). The phase comparison result is output through PCOMP (pin 42).
The PCOMP signal is applied to LPF (V-PLL) and fed back to the MCK VCO circuit to form the vertical direction PLL. The PCOMP signal's polarity can be switched through PCMPINV (CAT7_Byte2_bit4).
In addition, it is possible to select either active filter or passive filter in accordance with the external LPF specifications. However, active filter is recommended since it provides higher performance.
Fig 12.2-6 shows the PCOMP output waveform when a lock is applied. **Fig 12.2-7** shows the PCOMP output waveform without a lock. (From measurements using our evaluation board.) Apply a trigger to the external power supply square wave (S0 pin 44 input) and view the PCOMP output waveform to check whether a lock has been applied.

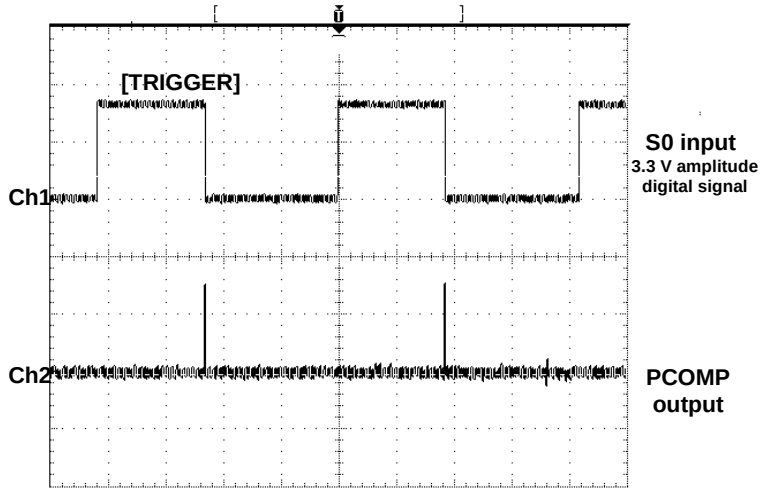


Fig 12.2-6 PCOMP output waveform (locked)

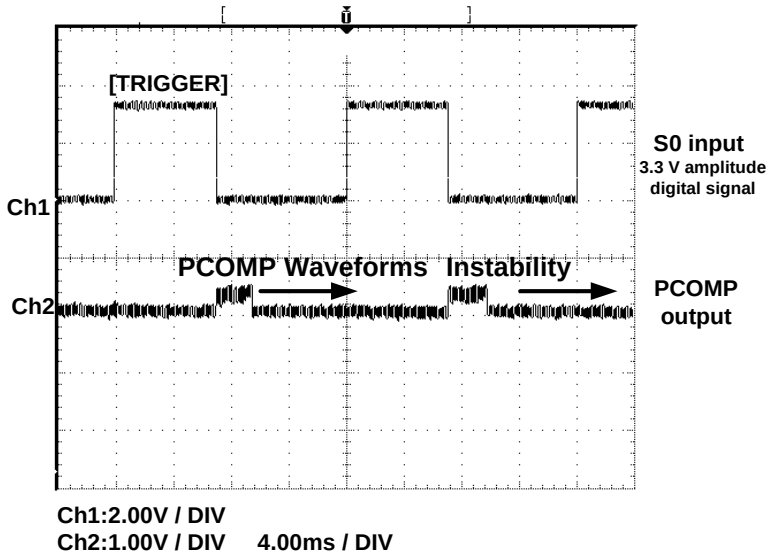


Fig 12.2-7 PCOMP output waveform (unlocked)

Application circuit example

Following is an example application involving an external rectangular wave pulse forming circuit (WAVE FORMER), LPF (V-PLL), and VCO circuit, which are required to configure external synchronization (line lock) with the SS-HQ1 system.

<Note>

Although the operations of these circuits have been checked on our evaluation board, we cannot guarantee circuit operations because PLL stability and lock range vary significantly depending on board layout as well as the electrical characteristics and temperature characteristics of the components used.

If you want to use these circuits in your own set, please be sure to check PLL stability (jitter), supply voltage fluctuations, and temperature fluctuations.

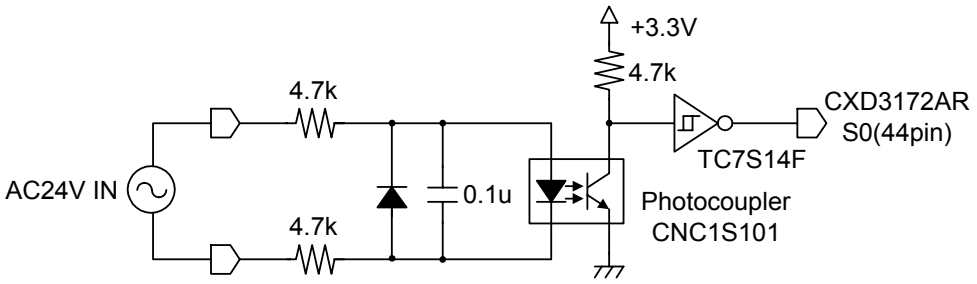


Fig 12.2-8 WAVE FORMER

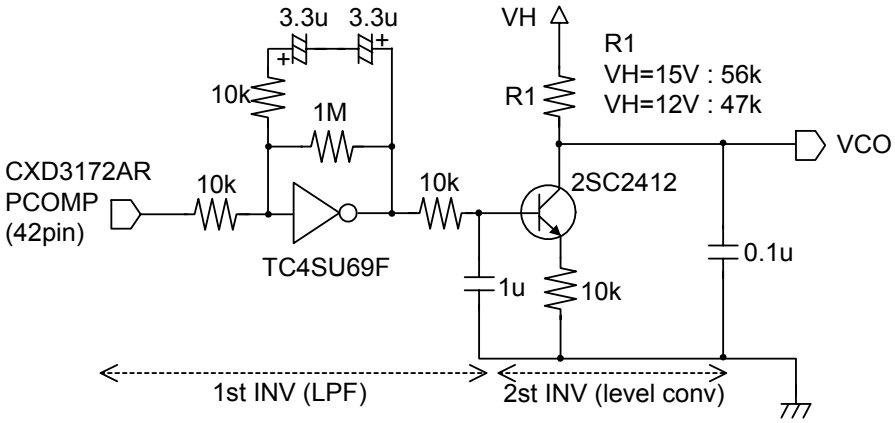


Fig 12.2-9 LPF(V-PLL)

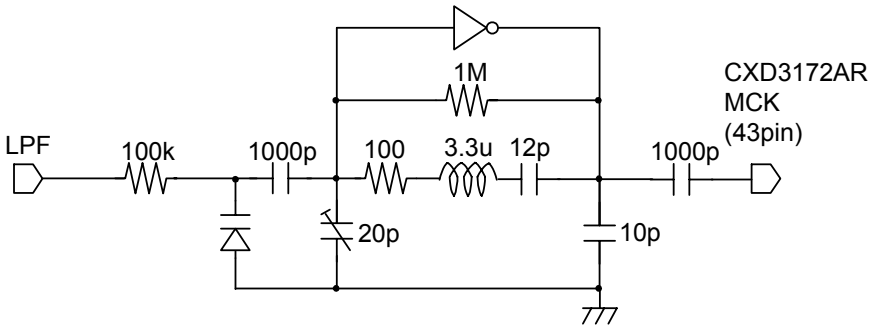


Fig 12.2-10 VCO (using 760H CCD)

LC oscillation is typically used in the MCK VCO circuit with line lock mode.

12.2.5. Combined Use of INT and LL Modes in a Single System

To switch between INT (internal) and LL (line lock) in a single set, we recommend the three switching systems presented below. The main differences between these switching systems are summarized in **Table 12.2-15**.

- **ECK-27MHz INT / ECK-27MHz LL switching system (set automatically; no external circuit)**
  This system uses the internal detector for automatic recognition (auto mode) in order to switch between INT and LL. With this system, ECK input is always operated at 27MHz, regardless of whether INT or LL is used.

- **ECK-28MHz INT / ECK-27MHz LL switching system (set manually; DIP switch change)**
  This system switches (manually) between LL and INT depending on whether a DIP switch is set to "High" or "Low". ECK input must be switched in each mode (INT/LL). (We provide the block diagram of this system by Ver1.2.0.)

- **ECK-28MHz INT / ECK-27MHz LL switching system (set automatically; external circuit required)**
  This system uses an external circuit to automatically detect whether there is an external VD input and automatically switches between LL and INT. ECK input must be switched in each mode (INT/LL). (We provide the block diagram of this system by Ver1.2.0.)

Table 12.2-15 Main Differences Between Switching Systems

System / Difference	ECK-27MHz INT / ECK-27MHz LL Switching system (set automatically)	ECK-28MHz INT / ECK-27MHz LL Switching system (set manually)	ECK-28MHz INT / ECK-27MHz LL Switching system (set automatically)
ECK X'tal	Always 27MHz	27MHz/28MHz Switching required	27MHz/28MHz Switching required
Sub-carrier in INT mode	Free-run	Locked	Locked
PLL in INT mode	Required (X'tal oscillation)	Not required	Not required
RESET operation each time system is switched	Not required	Required	Required
External VD detection circuit	Not required	Not required	Required
Use of Auto mode	Possible (required)	Not possible	Not possible

System Switching Parameters

With the “ECK-28MHz INT / ECK-27MHz LL Switching System (automatic/manual setting system)”, the CXD3172AR’s operation mode (MODESEL) must also be switched to match the input ECK frequency.
In addition, with the “ECK-28MHz INT / ECK-27MHz LL Switching System (automatic/manual setting system)”, auto mode cannot be used. Therefore, because external synchronization mode is switched in SGMODE, SGMODE must also be switched to match the INT/LL switch setting.
This function provides parameters for detecting the switching flag when ECK-28MHz INT and ECK-27MHz LL switch, and simultaneously switching the MODESEL and SGMODE values based on the detection results.
Fig 12.2-11 presents an explanation of the parameters based on the numbers in the flow chart.

・MODESEL/SGMODE control flow

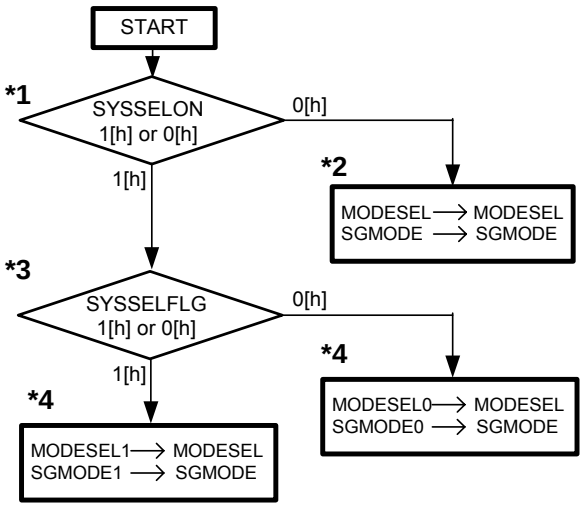


Fig 12.2-11 System Switching Control Flow

*1. SYSSELON
SYSSELON is a parameter for turning system switching control ON/OFF.

Table 12.2-16 SYSSELON Parameter

Parameter		Description
SYSSELON	CAT12_Byte13_bit1	0[h]: System configuration switching function OFF 1[h]: System configuration switching function ON

*2. When SYSSELON is set to OFF (SYSSELON=0[h]), the MODESEL and SGMODE values do not switch. The values originally set for SGMODE and MODESEL are applied.

Table 12.2-17 Parameters Subject to System Switching Control

Parameter		Description
MODESEL	CAT12_Byte1_bit0-3	DSP operation mode setting parameter
SGMODE	CAT17_Byte17_bit0-3	External synchronization mode setting parameter

*3. SYSSELFLG

SYSSELFLG is a detection flag used when the system is switched. The MODESEL and SGMODE values are switched based on the value in this parameter.

SYSSELFLG is assigned to a port driver in order to use this parameter. The parameter value changes according to whether the port input signal from the exterior is “High” or “Low”.

Table 12.2-18 SYSSELFLG Parameter

Parameter		Description
SYSSELFLG	CAT12_Byte13_bit2	System selection flag

*4. MODESEL0/1 and SGMODE0/1

These parameters preset the values to be applied to MODESEL and SGMODE based on the SYSSELFLG value.

- If SYSSELFLG=0[h]
  The MODESEL0 setting is applied to MODESEL, and the SGMODE0 setting is applied to SGMODE.
- If SYSSELFLG=1[h]
  The MODESEL1 setting is applied to MODESEL, and the SGMODE1 setting is applied to SGMODE.

Table 12.2-19 MODESEL and SGMODE setting parameters

Parameter		Description	Notes
MODESEL0	CAT12_Byte16_bit0-7	MODESEL when SYSSELFLG=0[h] (valid only when SYSSELON=1[h])	When using this function, do not assign SGMODE to a port. Also, do not change the SGMODE setting through serial communication.
MODESEL1	CAT12_Byte17_bit0-7	MODESEL when SYSSELFLG=1[h] (valid only when SYSSELON=1[h])	
SGMODE0	CAT12_Byte18_bit0-7	SGMODE when SYSSELFLG=0[h] (valid only when SYSSELON=1[h])	
SGMODE1	CAT12_Byte19_bit0-7	SGMODE when SYSSELFLG=1[h] (valid only when SYSSELON=1[h])	

Example system switching control parameter settings (for 760H NTSC)

In this example, the ECK-28MHz (MODESEL=6[h]) INT (SGMODE=0[h]) and ECK-27MHz (MODESEL=8[h]) LL (SGMODE=1[h]) systems are switched.

1. The MODESEL and SGMODE values assigned to port drivers are removed by the DSP initial signal.
2. SYSSELFLG is assigned to a port driver. (See **Table 12.2-18**.)
3. ECK-28MHz INT settings: MODESEL0 is set to ”6[h]” and SGMODE0 is set to ”0[h]”. (See **Table 12.2-19**.)
4. ECK-27MHz LL settings: MODESEL1 is set to ”8[h]” and SGMODE1 is set to ”1[h]”. (See **Table 12.2-19**.)
5. SYSSELON is set to ”1[h]”. (See **Table 12.2-16**.)
6. The system switches according to whether the input to the port driver where SYSSELFLG is assigned is “High” or “Low”.If the port input is “High”, then LL mode is switched. If it is “Low”, then INT is switched.

* For information on port driver settings, see 10.1 “Port Driver Function”.
* This function performs a RESET operation each time the system is switched. Therefore, the settings must be saved to EEPROM.

YDLY switching control parameters

With the “ECK-28MHz INT / ECK-27MHz LL Switching System (automatic/manual setting system)”, ECK is switched. For this reason, there is a possibility that the Y delay for ECK-28MHz will be different from the Y delay for ECK-27MHz in YC separate output (DACMODE=1[h]). Therefore, with this function, the YDLY parameter can be switched based on the YDACCKSEL value. **Fig 12.2-12** presents an explanation of the parameters based on the numbers in the flow chart.

・YDLY control flow

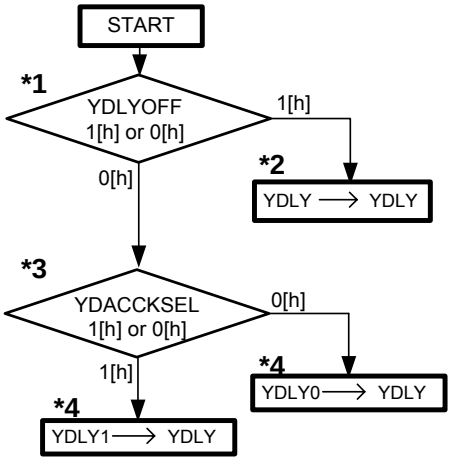


Fig 12.2-12 YDLY switching control flow

*1. YDLYOFF

YDLYOFF is a parameter for turning YDLY switching control ON/OFF.

Table 12.2-20 YDLYOFF Parameter

Parameter		Description
YDLYOFF	CAT12_Byte13_bit0	0[h]:YDLY switching function ON 1[h]:YDLY switching function OFF

*2. When YDLYOFF is set to OFF (YDLYOFF=1[h]), the YDLY value does not change. The value originally set for YDLY is applied.

Table 12.2-21 Parameter Subject to YDLY Switching Control

Parameter		Description
YDLY	CAT2_Byte11_bit1-4	Parameter for adjusting Y-line system delay

*3. YDACCKSEL

YDACCKSEL is a parameter for switching Y-DAC and the encoder clock (ECK/MCK). The YDLY value is switched based on the value of this parameter.

Table 12.2-22 YDACCKSEL Parameter

Parameter		Description
YDACCKSEL	CAT1_Byte12_bit2	0[h]:ECK(default) 1[h]:MCK

*4. YDLY0/1

These parameters preset the values to be applied to YDLY based on the YDACCKSEL value.

- If YDACCKSEL=0[h]
  The YDLY0 setting is applied to YDLY.
- If YDACCKSEL=1[h]
  The YDLY1 setting is applied to YDLY.

Table 12.2-23 YDLY0/1 Parameter

Parameter		Description
YDLY0	CAT12_Byte14_bit0-3	YDLY value when YDACCKSEL=0[h] (valid only when YDLYOFF=0[h])
YDLY1	CAT12_Byte15_bit0-3	YDLY value when YDACCKSEL=1[h] (valid only when YDLYOFF=0[h])

Example YDLY switching control parameter settings
(for 760H NTSC system configured using Sony evaluation board)

The following procedure is used for YDLY switching (assumes DACMODE=1[h]) using the ECK-28MHz (MODESEL=6[h] and ECK-27MHz (MODESEL=8[h]) systems respectively, on the Sony evaluation board.

1. Set YDLY0 to “1[h]” as the ECK-28MHz setting. (See **Table 12.2-23**.)
2. Set YDLY1 to “2[h]” as the ECK-27MHz setting. (See **Table 12.2-23**.)
3. Set YDLYOFF to “0[h]”. (See **Table 12.2-20**.)
4. When YDLY is combined with system switching, the YDLY value changes to the appropriate value. For ECK-28MHz INT, this value is YDLY=1[h]. For ECK-27MHz LL, the value is YDLY=2[h].

* The Y delay varies depending on the product set. Set a value which is appropriate on your set board.

ECK-27MHz INT / ECK-27MHz LL Switching System (automatic setting)

With this system, ECK input is always operated at 27MHz, regardless of whether INT or LL is used. A block diagram of this system is shown in **Fig 12.2-13**. ATMODEON is set to 1[h] in advance (see **Table 12.2-1**). In addition, HVPLL (see **Table 12.2-8**) is assigned to a port (Pn1 in the diagram), and the port driver is set so that the HVPLL signal is output from port Pn1.

The following operations are performed to switch from INT to LL.

- When there is external VD input to S0 (pin 44), the internal system is automatically switched to LL mode.
- VCO is switched to LC oscillation by the HVPLL signal output from Pn1 in the diagram.

The following operations are performed to switch from LL to INT.

- When there is not external VD input to S0 (pin 44), the internal system is automatically switched to INT mode.
- VCO is switched to X'tal oscillation by the HVPLL signal output from Pn1 in the diagram.

<Note>
When the VCO is switched, please terminate VCO oscillation on the unused side in order to prevent noise.
For details, see the applied schematic titled "Circuit Figure of Internal & Line Lock".

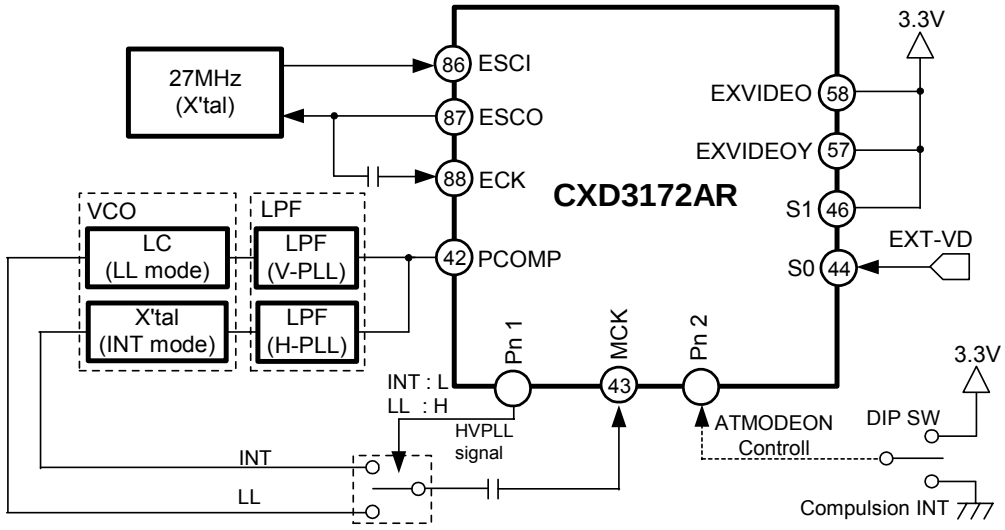


Fig 12.2-13 ECK-27MHz INT/ECK-27MHz LL Switching System Block Diagram

* If you want to force the system to change to INT mode while external VD is being input, assign ATMODEON to port Pn2 and connect a DIP switch, as shown in **Fig 12.2-13**. If the connected DIP switch is set to "Low", the mode is force-changed to INT mode. Note that in such cases, SGMODE must be set to 0[h].

ECK-28MHz INT / ECK-27MHz LL Switching System (manual setting)

This system switches between LL and INT depending on whether the DIP switch is set to “High” or “Low”.
INT mode operates with 28MHz ECK input. LL mode uses 27MHz ECK input.
After the DIP switch position is changed, the RESET operation must be performed, both when changing from INT to LL, and when changing from LL to INT.
Therefore, when switching between INT and LL, first turn off the power, then change the DIP switch position, and then turn the power back on.

A block diagram of the system is shown in **Fig 12.2-14**.
SYSSELFLG is assigned to a port in advance. See **Table 12.2-16**, **Table 12.2-17**, **Table 12.2-18**, and **Table 12.2-19** for information on SYSSELFLG and the parameter settings that are switched according to the SYSSELFLG value.

When switching from INT to LL (when the DIP switch is set to the “High” position), the following operations are performed.

- SYSSELFLG, which is assigned to a specified port, is set to 1[h] to switch MODESEL/SGMODE to the LL setting.
- The MCK switching circuit is switched to the VCO position (MCK clock supply).
- The ECK switching circuit is switched to the 27MHz position (ECK 27MHz clock supply).

When switching from LL to INT (when the DIP switch is set to the “Low” position), the following operations are performed.

- SYSSELFLG, which is assigned to a specified port, is set to 0[h] to switch MODESEL/SGMODE to the INT setting.
- The MCK switching circuit is switched to the GND position (MCK clock supply stopped).
- The ECK switching circuit is switched to the 28MHz position (ECK 28MHz clock supply).

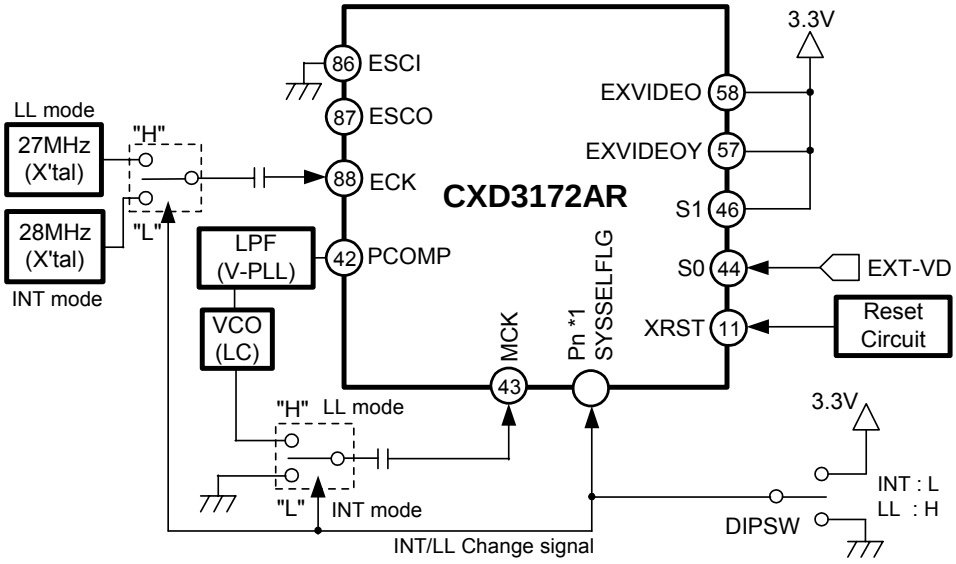


Fig 12.2-14 ECK-28MHz INT/ECK-27MHz LL Switching System Block Diagram

* Do not assign SGMODE to a port.

ECK-28MHz INT / ECK-27MHz LL Switching System (automatic setting)

This system uses an external circuit to detect the presence or absence of external VD input, and switches between LL and INT automatically. INT mode operates with 28MHz ECK input. LL mode uses 27MHz ECK input. Switching between INT and LL is handled automatically by an external VD detection circuit.

A block diagram of the system is shown in **Fig 12.2-15**.
SYSSELFLG is assigned to a port in advance. See **Table 12.2-16**, **Table 12.2-17**, **Table 12.2-18**, and **Table 12.2-19** for information on SYSSELFLG and the parameter settings that are switched according to the SYSSELFLG value.

When switching from INT to LL (when there is external VD input), the following operations are performed.

- SYSSELFLG, which is assigned to a specified port, is set to 1[h] to switch MODESEL/SGMODE to the LL setting.
- The MCK switching circuit is switched to the VCO position (MCK clock supply).
- The ECK switching circuit is switched to the 27MHz position (ECK 27MHz clock supply).

When switching from LL to INT (when there is no more external VD input), the following operations are performed.

- SYSSELFLG, which is assigned to a specified port, is set to 0[h] to switch MODESEL/SGMODE to the INT setting.
- The MCK switching circuit is switched to the GND position (MCK clock supply stopped).
- The ECK switching circuit is switched to the 28MHz position (ECK 28MHz clock supply).

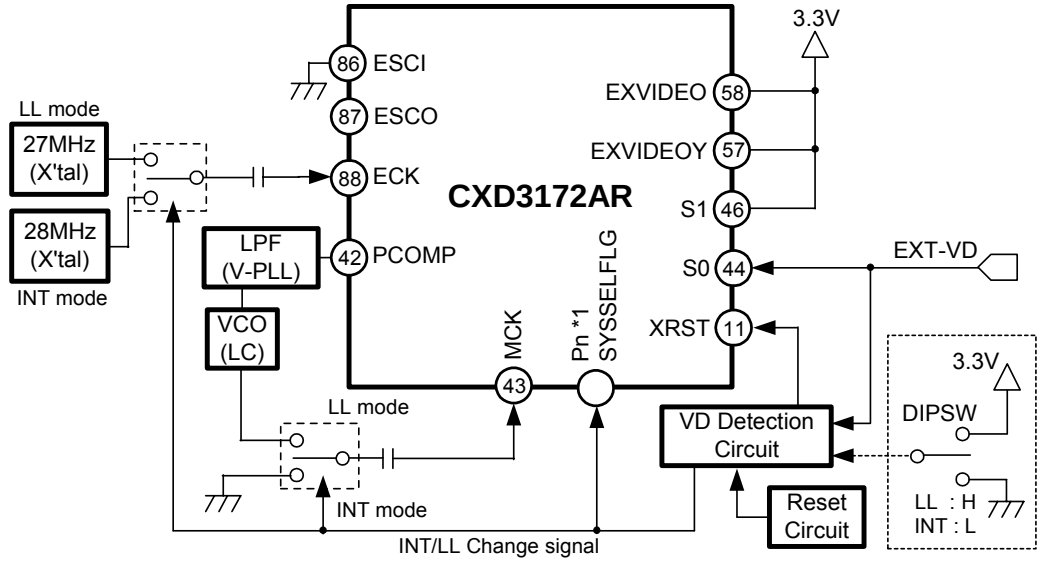


Fig 12.2-15 ECK-28MHz INT/ECK-27MHz LL Switching System (automatic setting) Block Diagram

* The DIP switch is used to force-switch the system to INT mode. If it is normally left in the “H” position, switching will be handled automatically according to whether or not there is VD input.
* Do not assign SGMODE to a port.

• VD Detection Circuit

There is no particular external VD detection circuit which is recommended by Sony.

Build a detection circuit based on the system switching timings shown below.

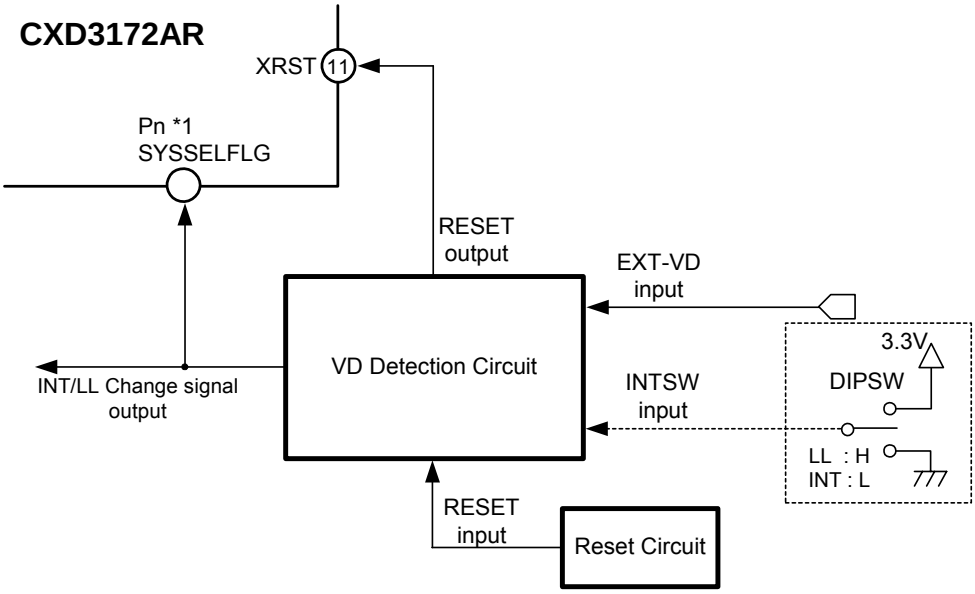


Fig 12.2-16 VD Detection Circuit Block Diagram

1. Timing for switch from INT to LL when external VD input is detected (INTSW input =High)

For a fixed period of time (1VD period or longer), Ext-VD presence/absence detection is performed. If Ext-VD presence is detected, “RESET output” is switched from High to Low and the CXD3172AR is reset. In addition, for the period where “RESET output”=Low, “INT/LL Change signal output” is switched from Low to High. (The “INTSW input” at this time is always High.)

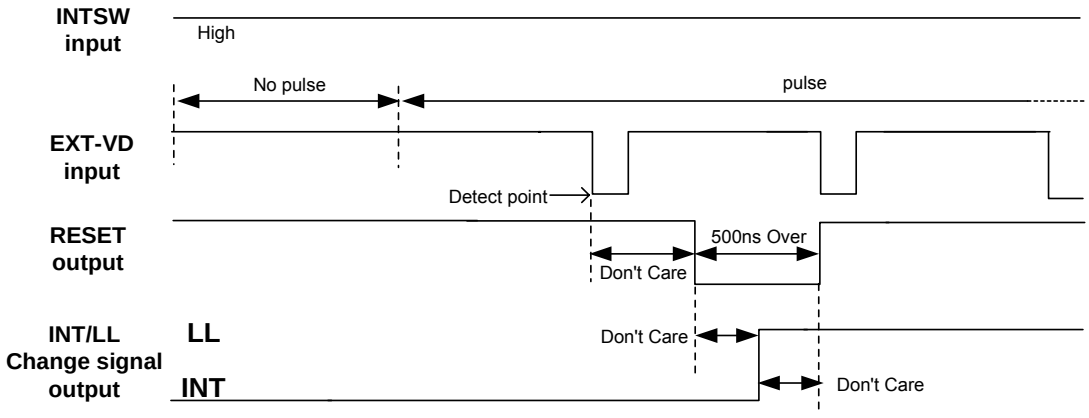


Fig 12.2-17 Timing for switch from INT to LL based on external VD input (INTSW input =High)

2. Timing for switch from LL to INT when external VD input is no longer detected (INTSW input =High)

For a fixed period of time (1VD period or longer), Ext-VD presence/absence detection is performed. If Ext-VD absence is detected, “RESET output” is switched from High to Low and the CXD3172AR is reset. In addition, for the period where “RESET output”=Low, “INT/LL Change signal output” is switched from High to Low. (The “INTSW input” at this time is always High.)

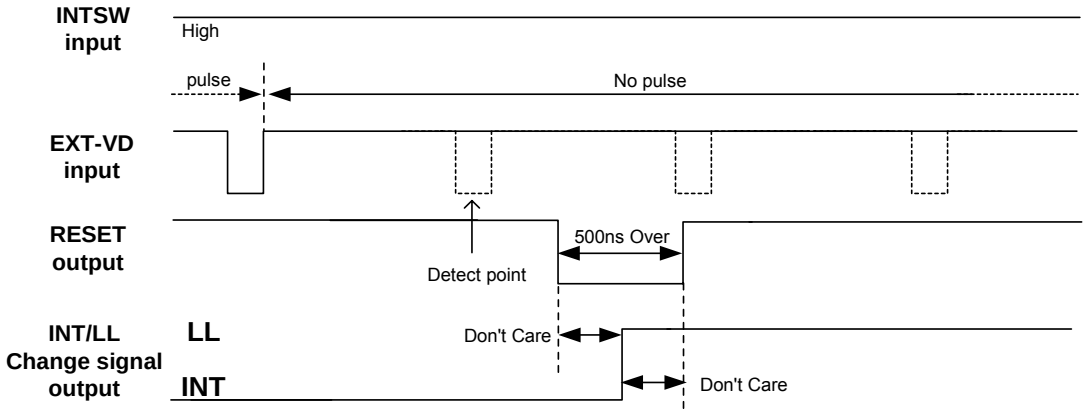


Fig 12.2-18 Timing for switch from LL to INT based on external VD input (INTSW input =High)

3. Timing for switch from INT to LL with external VD input (INTSW input : Low => High)

While “INTSW=Low”, “INT/LL Change signal output” is output at Low, regardless of whether Ext-VD is present or absent. After “INTSW input” switches from Low to High, Ext-VD presence/absence detection begins. If Ext-VD presence is detected, then “RESET output” is switched from High to Low and the CXD3172AR is reset. In addition, for the period where “RESET output”=Low, “INT/LL Change signal output” is switched from Low to High. (External VD remains input during this time.)

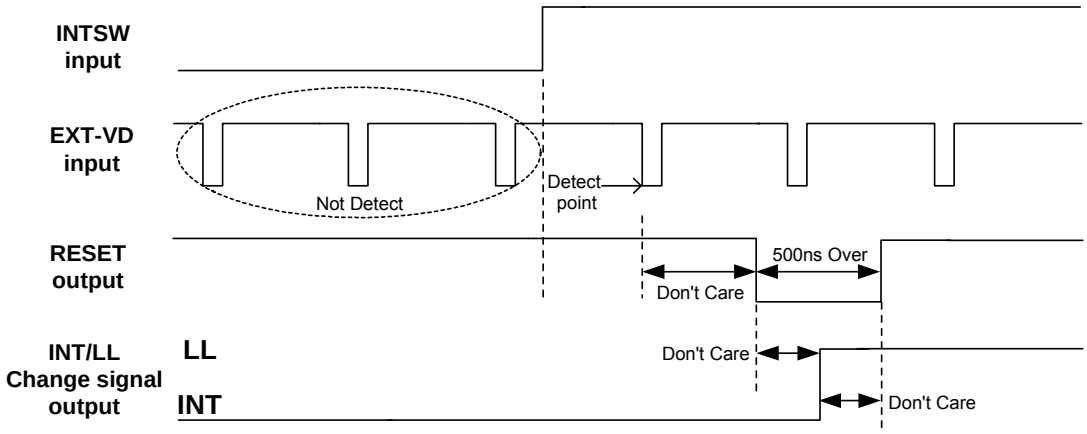


Fig 12.2-19 Timing for switch from INT to LL based on INTSW input

4. Timing for switch from LL to INT with external VD input (INTSW input : High => Low)

When “INTSW input” switches from High to Low, “RESET output” is switched from High to Low and the CXD3172AR is reset regardless of whether Ext-VD is present or absent. In addition, for the period where “RESET output”=Low, “INT/LL Change signal output” is switched from High to Low. (While “INTSW=Low”, “INT/LL Change signal output=Low” is maintained regardless of whether Ext-VD is present or absent.)

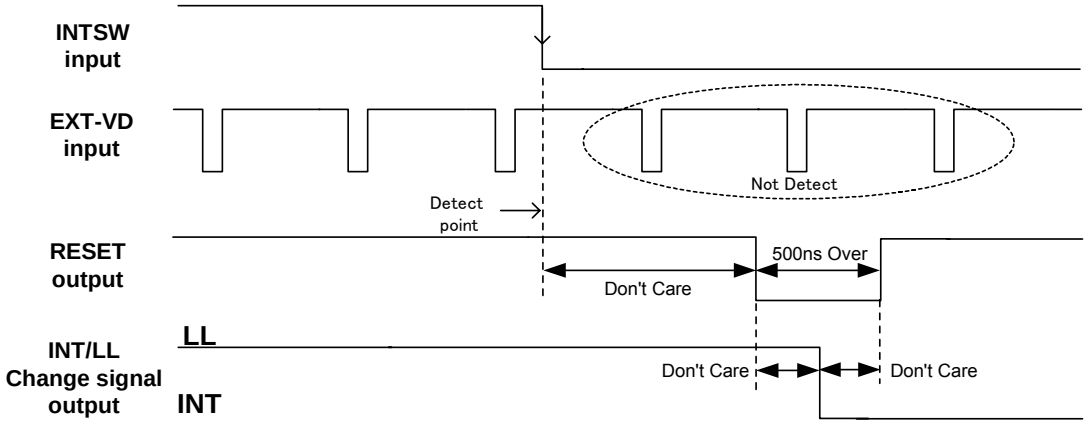


Fig 12.2-20 Timing for switch from LL to INT based on INTSW input

5. RESET output timing when there is an external RESET signal

When a RESET signal is received from the exterior, the CXD3172AR is force-reset, so “RESET output” is output. It does not matter whether or not the external VD detection circuit itself is reset.

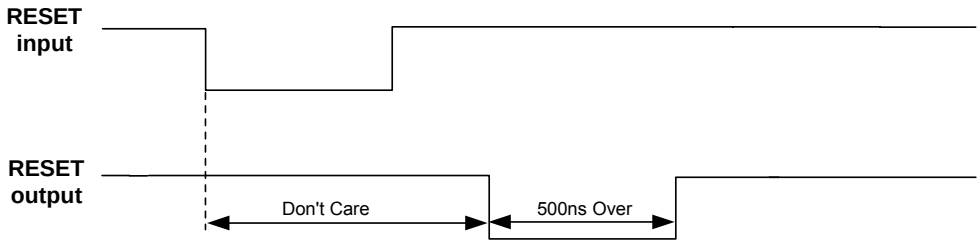


Fig 12.2-21 Operations based on external RESET

12.2.6. VS Lock Mode (VSL)

In this mode, the camera's vertical and horizontal phases are synchronized to an external video signal.
The reset operation is performed in the vertical direction, and the PLL operation is performed in the horizontal direction. SGMODE is set to 2[h]. (See **Table 12.2-5**.)

System Configuration

The VS Lock Mode master signal is the external video signal (EXT-VIDEO). The 1Vpp external video luminance signal (EXT-VIDEO-Y), which has passed through an external LPF and had its subcarrier component removed, is input to the EXVIDEOY (pin 57) pin.
Inside the CXD3172AR, the input EXT-VIDEO-Y signal is divided between a vertical signal (EXT-VD) and a horizontal signal (EXT-HD). EXT-VD resets the vertical counter inside the CXD3172AR. The EXT-HD signal is phase-compared against the MCK-frequency-divided HD (MCK-HD) signal inside the CXD3172AR.
In addition, in VS Lock Mode (VSL), the 27.000MHz clock is used for input to ECK (pin 88). In this case, the MODESEL (operation mode) setting is as shown in **Table 12.2-13**. We recommend using X'tal oscillation for the VCXO on the MCK side.
A system block diagram is shown in **Fig 12.2-22**. The external input signal is presented in **Table 12.2-24**.

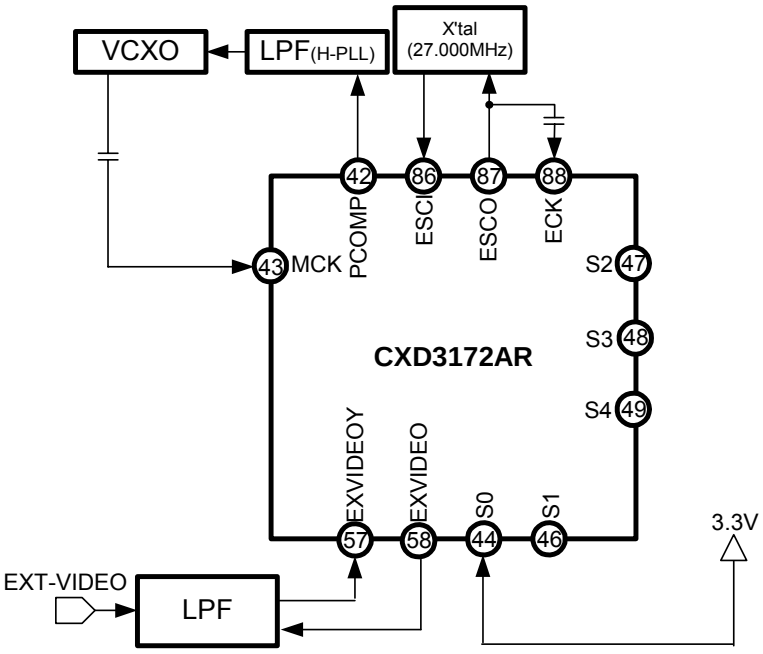


Fig 12.2-22 VS Lock (VSL) mode

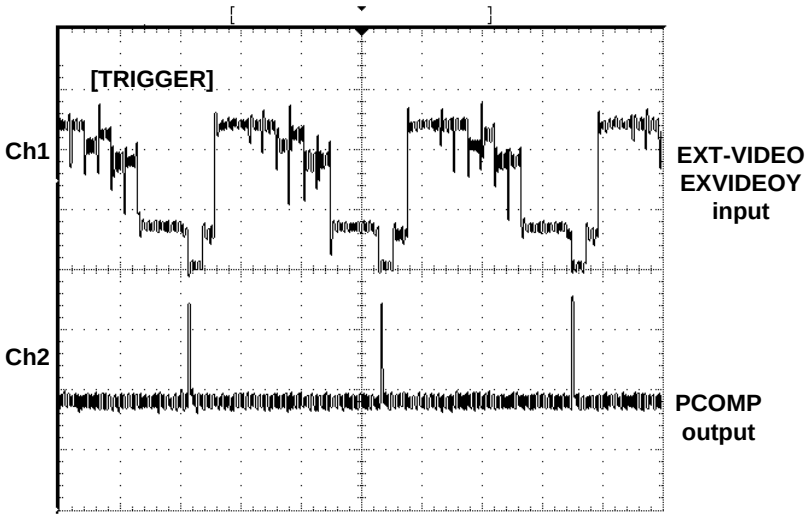
Table 12.2-24 External I/O signals (VS Lock (VSL) Mode)

Pin Name(Pin No)	I/O	I/O signals
S0(44pin)	IN	3.3V connection
EXVIDEOY(57pin)	IN	EXT-VIDEO-Y (1Vpp: analog signal)
EXVIDEO(58pin)	OUT	DC bias supply to EXVIDEOY (pin 57)

* EXT-VIDEO should be passed through an LPF before being input to EXVIDEOY (pin 57). This serves to remove the subcarrier component, and is a countermeasure against noise in cases where no external video signal is input.

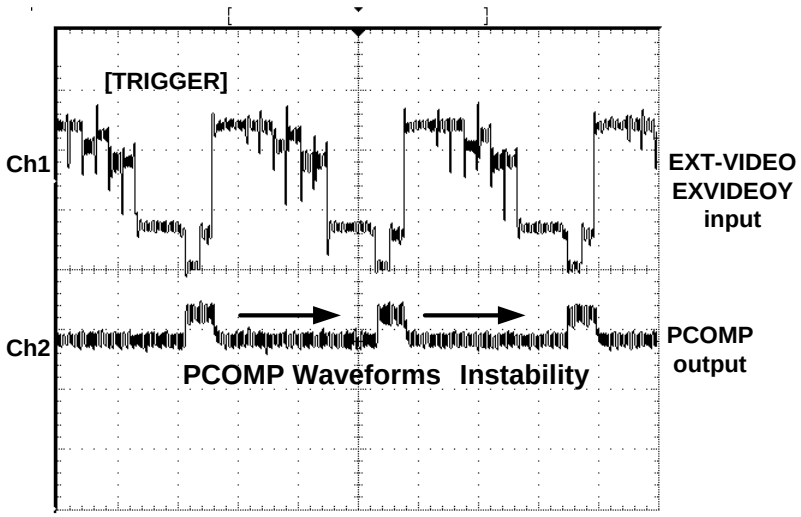
Internal phase comparison

The separated horizontal direction signal (EXT-HD) and the MCK-frequency-divided HD (MCK-HD) signal are phase-compared inside the CXD3172AR, and the result of the comparison is output through PCOMP (pin 42). The PCOMP signal is applied to the LPF (H-PLL) and fed back to the VCXO circuit on the MCK side to form the horizontal direction PLL. The polarity of the PCOMP signal may be switched using PCMPINV (CAT7_Byte2_bit4).
An active or passive filter can be selected, to match the specifications of the external LPF. Note that we recommend an active filter since active filters have better performance.
Fig 12.2-23 shows the PCOMP output waveform when the lock is on. **Fig 12.2-24** shows the PCOMP output waveform when the lock is off. (These waveforms are the results of measurements made using our evaluation board.) Apply a trigger to the external video signal and look at the PCOMP output waveform to check whether the lock is on.



Ch1:500mV / DIV
Ch2:1.00V / DIV 20.0us / DIV

Fig 12.2-23 PCOMP output waveform (locked)



Ch1:500mV / DIV
Ch2:1.00V / DIV 20.0us / DIV

Fig 12.2-24 PCOMP output waveform (unlocked)

Applied circuit example

The figure shows an example of an LPF applied circuit. Also refer to the figure below for the DC bias supply from EXVIDEO (pin 58) to EXVIDEOY (pin 57). The constant is a value used on our evaluation board. Treat it as a reference value.

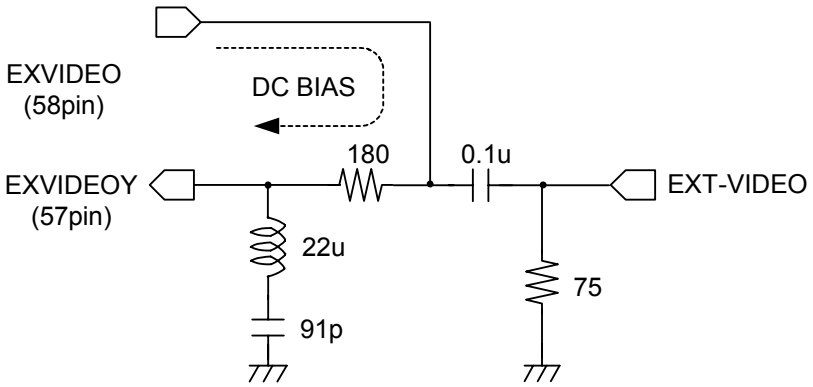


Fig 12.2-25 Example LPF circuit

12.2.7. Using the Internal SYNCSEP

Internal SYNCSEP divides the SYNC of the external video luminance signal (signal which has passed through LPF) input to EXVIDEOY (pin 57) between VD and HD when using VS lock or VBS lock.
The internal SYNCSEP power pins are AVD5 (pin 56) and AVS5 (pin 59).
DC bias is supplied from EXVIDEO (pin 58) to EXVIDEOY (pin 57). In VBS Lock Mode, EXVIDEO (pin 58) also serves as external burst input. In VS Lock Mode, the external burst input is disabled.

12.2.8. VS Lock Mode (VSL-S)

VS Lock (VSL-S) synchronizes the camera vertical and horizontal phases to the external VD/HD signal.
A reset operation is performed in the vertical direction, and a PLL operation is performed in the horizontal direction. The SGMODE setting is A[h]. (See **Table 12.2-5**.)
This is not supported in auto mode (ATMODEON=1[h]).

System Configuration

The master signal is external VD/HD (EXT-VID/EXT-HD).
EXT-VD resets the CXD3172AR's internal vertical direction counter.
The EXT-HD signal and MCK-frequency-divided HD (MCK-HD) signal are phase-compared inside the CXD3172AR. In addition, the 27.000MHz clock is used for input to ECK (pin 88). In this case, the MODESEL (operation mode) setting is as shown in **Table 12.2-13**. We recommend using X'tal oscillation for the VCXO on the MCK side. A system block diagram is shown in **Fig 12.2-26**. The external input signal is presented in **Table 12.2-25**.

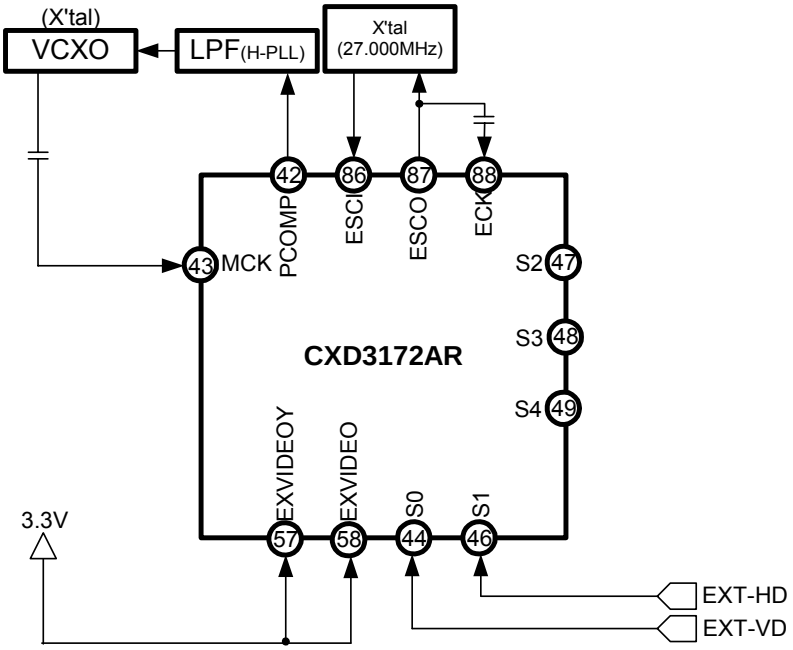


Fig 12.2-26 VS(VSL-S) mode

Table 12.2-25 External Input Signal (VS Lock (VSL-S) mode)

Pin Name(Pin No)	I/O signals
S0(44pin)	EXT-VD(3.3Vpp: digital signal)
S1(46pin)	EXT-HD(3.3Vpp: digital signal)
EXVIDEOY(57pin)	3.3V connection
EXVIDEO(58pin)	

Internal phase comparison

The EXT-HD signal and the MCK-frequency-divided HD (MCK-HD) signal are phase-compared inside the CXD3172AR, and the result of the comparison is output through PCOMP (pin 42). The PCOMP signal is applied to the LPF (H-PLL) and fed back to the VCXO circuit on the MCK side to form the horizontal direction PLL. The polarity of the PCOMP signal may be switched using PCMPINV (CAT7_Byte2_bit4).

An active or passive filter can be selected, to match the specifications of the external LPF. Note that we recommend an active filter since active filters have better performance.

Fig 12.2-27 shows the PCOMP output waveform when the lock is on. **Fig 12.2-28** shows the PCOMP output waveform when the lock is off. (These waveforms are the results of measurements made using our evaluation board.) Apply a trigger to EXT-HD and look at the PCOMP output waveform to check whether the lock is on.

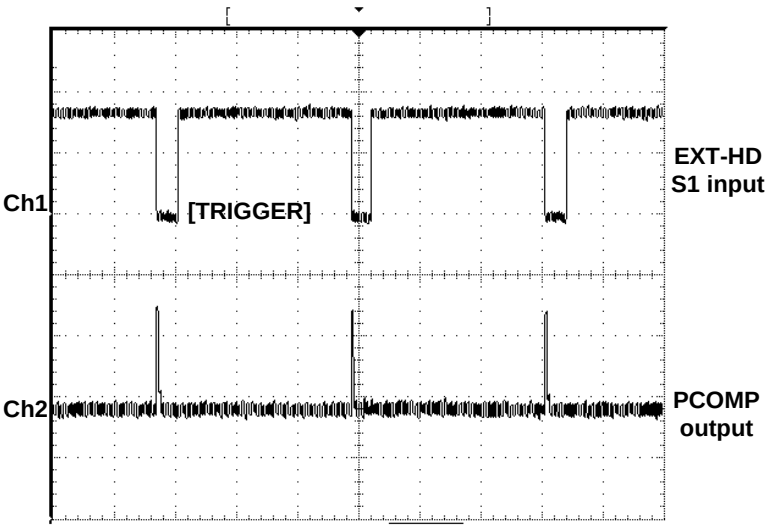


Fig 12.2-27 PCOMP output waveform (locked)

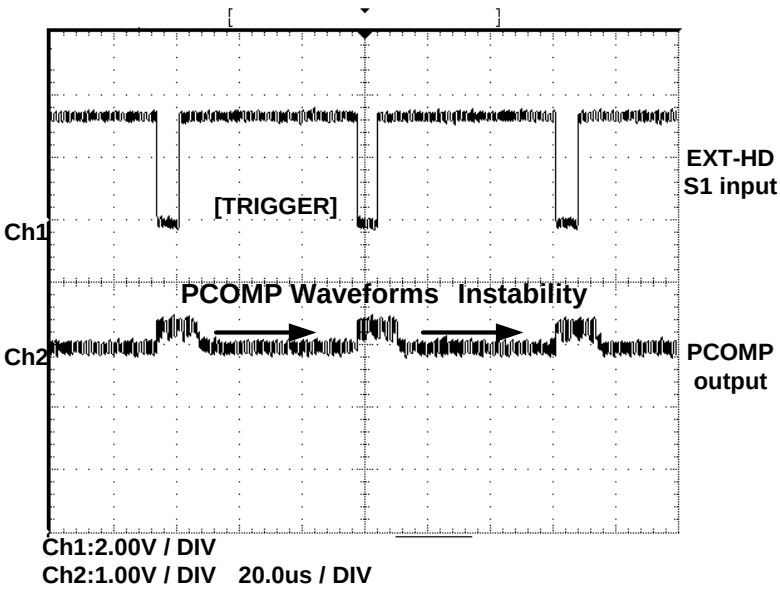


Fig 12.2-28 PCOMP output waveform (unlocked)

12.2.9. VS Lock Mode (VSL-D)

VS Lock (VSL-D) synchronizes the camera vertical and horizontal phases to the external digital sync signal.
A reset operation is performed in the vertical direction, and a PLL operation is performed in the horizontal direction. The SGMODE setting is F[h]. (See **Table 12.2-5**.)
This is not supported in auto mode (ATMODEON=1[h]).

System Configuration

The master signal is external digital sync (D SYNC). D SYNC is divided inside the CXD3172AR between a vertical direction signal (EXT-VD) and horizontal direction signal (EXT-HD).
EXT-VD resets the CXD3172AR's internal vertical direction counter.
The EXT-HD signal and MCK-frequency-divided HD (MCK-HD) signal are phase-compared inside the CXD3172AR.
In addition, the 27.000MHz clock is used for input to ECK (pin 88). In this case, the MODESEL (operation mode) setting is as shown in **Table 12.2-13**. We recommend using X'tal oscillation for the VCXO on the MCK side.
A system block diagram is shown in **Fig 12.2-29**. The external input signal is presented in **Table 12.2-26**.

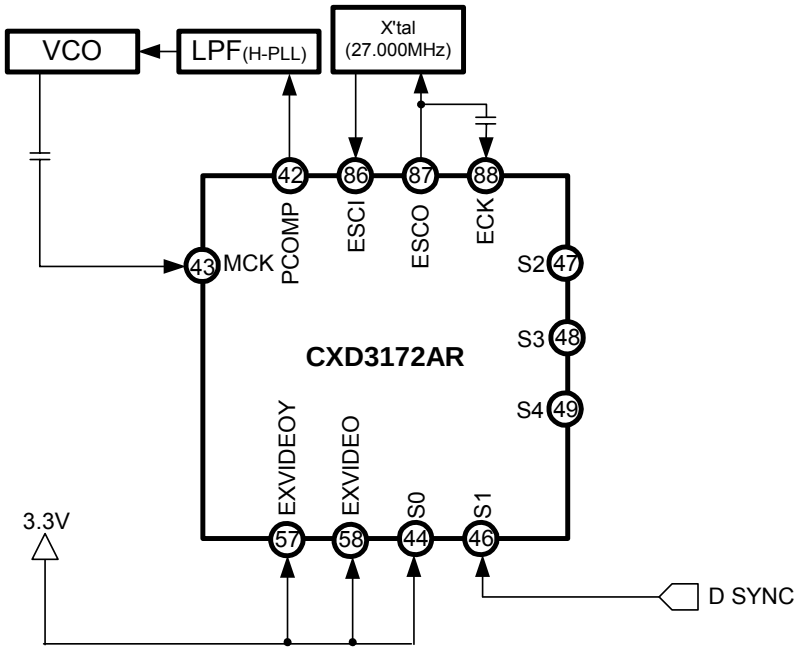


Fig 12.2-29 VS Lock (VSL-D) mode

Table 12.2-26 External I/O signal (VS Lock (VSL-D) Mode)

Pin Name(Pin No)	I/O signals
S1(46pin)	D SYNC(3.3Vpp: digital signal)
S0(44pin)	3.3V connection
EXVIDEOY(57pin)	
EXVIDEO(58pin)	

Internal phase comparison

The result of the phase comparison is output through PCOMP (pin 42). The PCOMP signal is applied to the LPF (H-PLL) and fed back to the VCXO circuit on the MCK side to form the horizontal direction PLL. The polarity of the PCOMP signal may be switched using PCMPINV (CAT7_Byte2_bit4).

An active or passive filter can be selected, to match the specifications of the external LPF. Note that we recommend an active filter since active filters have better performance.

Fig 12.2-30 shows the PCOMP output waveform when the lock is on. **Fig 12.2-31** shows the PCOMP output waveform when the lock is off. (These waveforms are the results of measurements made using our evaluation board.) Apply a trigger to D SYNC and look at the PCOMP output waveform to check whether the lock is on.

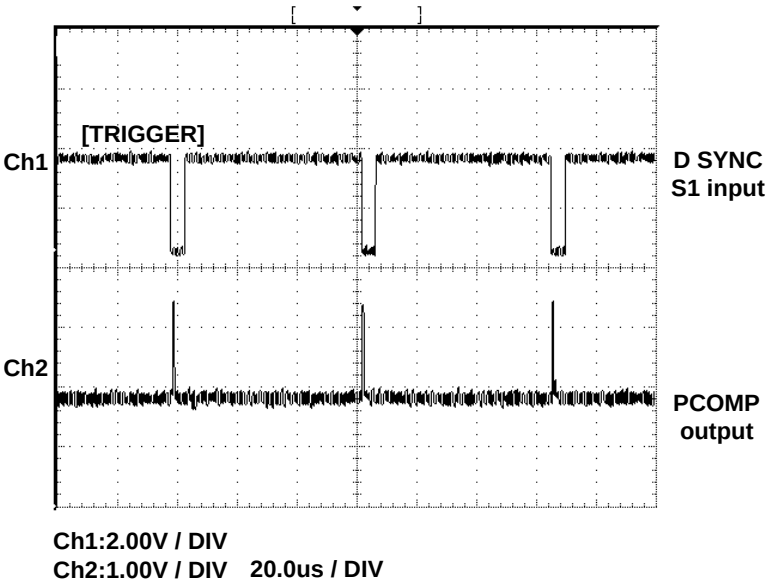


Fig 12.2-30 PCOMP output waveform (locked)

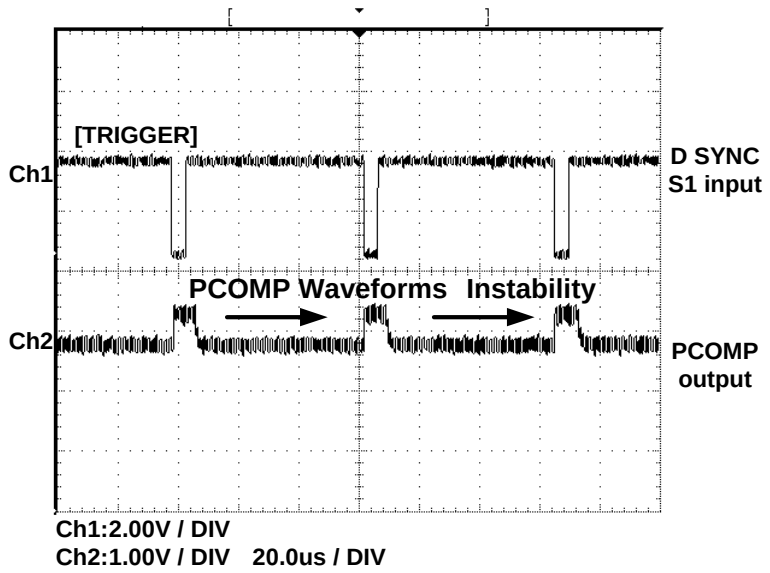


Fig 12.2-31 PCOMP output waveform (unlocked)

12.2.10. VBS Lock Mode (VBSLHP)

VBS Lock (VBSLHP) synchronizes the camera vertical, horizontal, and subcarrier phases to the external video signal.

A reset operation is performed in the vertical direction, and a PLL operation is performed in the horizontal direction and on the subcarrier.

The SGMODE setting is 3[h]. (See **Table 12.2-5**.)

Only a limited number of operation modes can be used with VBSLHP. For details, see appendix 13.1 ("External Synchronization Evaluation Results").

System Configuration

The master signal is an external video signal (EXT-VIDEO). A 1Vpp video signal (analog) is input to EXVIDEOY (pin 57) and EXVIDEO (pin 58). The external video luminance signal (EXT-VIDEO-Y) input to EXVIDEOY (pin 57) is divided inside the CXD3172AR between a vertical direction signal (EXT-VD) and horizontal direction signal (EXT-HD). EXT-VD resets the CXD3172AR's internal vertical direction counter. The EXT-HD signal and MCK-frequency-divided HD (MCK-HD) signal are phase-compared inside the CXD3172AR. The burst component extracted inside the CXD3172AR from EXT-VIDEO (input to EXVIDEO (pin 58)) is amplified and digitized, and the resulting signal is phase-compared against the FSC signal.

X'tal oscillation is used for the VCXO on the ECK side. We recommend using X'tal oscillation for the VCXO on the MCK side.

A system block diagram is shown in **Fig 12.2-32**. The external input signal is presented in **Table 12.2-27**.

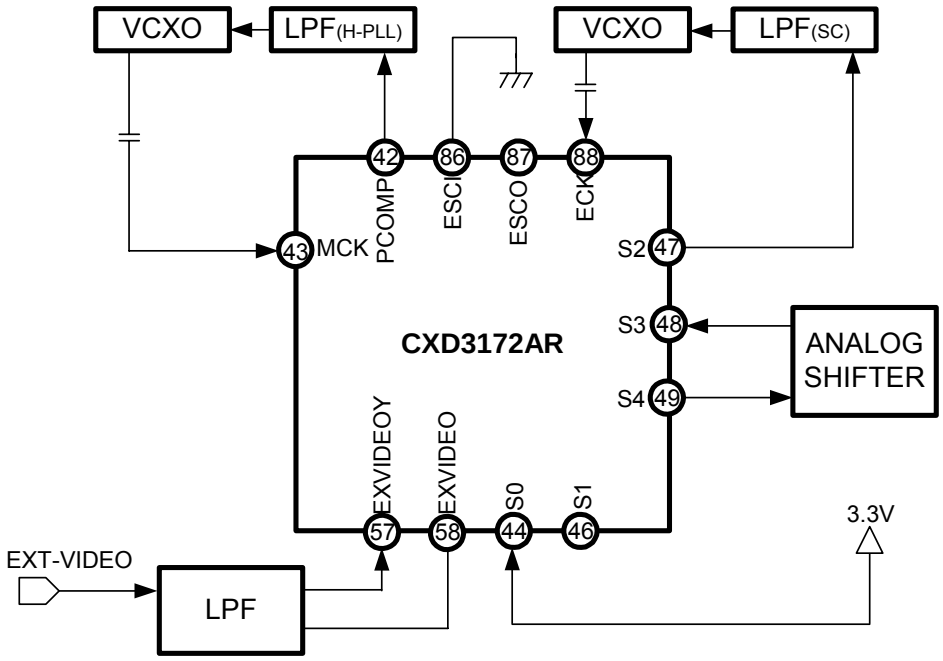


Fig 12.2-32 VBS Lock (VBSLHP) mode

Table 12.2-27 External Input Signal (VBS Lock (VBSLHP) Mode)

Pin Name(Pin No)	I/O signals
S0(44pin)	Connected (3.3V) power supply
S3(48pin)	FSC signal
EXVIDEOY(57pin)	EXT-VIDEO-Y(1Vpp: Analog signal)
EXVIDEO(58pin)	EXT-VIDEO(1Vpp: Analog signal)

The external video signal input to EXVIDEOY should be passed through the LPF to remove the subcarrier component. The phase of the FSC signal output from S4 (pin 49) must be adjusted and the signal must be re-input to S3 (pin 48).

Internal phase comparison

• HD phase comparison

The MCK-frequency-divided HD (MCK-HD) signal and the horizontal signal separated inside the CXD3172AR from the external video signal (luminance signal) input through EXVIDEOY (pin 57) are phase-compared, and the result of the comparison is output through PCOMP (pin 42). The PCOMP signal is applied to the LPF (H-PLL) and fed back to the VCXO circuit on the MCK side to form the horizontal direction PLL. The polarity of the PCOMP signal may be switched using PCMPINV (CAT7_Byte2_bit4).

An active or passive filter can be selected, to match the specifications of the external LPF. Note that we recommend an active filter since active filters have better performance.

Fig 12.2-33 shows the PCOMP output waveform when the lock is on. **Fig 12.2-34** shows the PCOMP output waveform when the lock is off. (These waveforms are the results of measurements made using our evaluation board.) Apply a trigger to the external video signal and look at the PCOMP output waveform to check whether the lock is on.

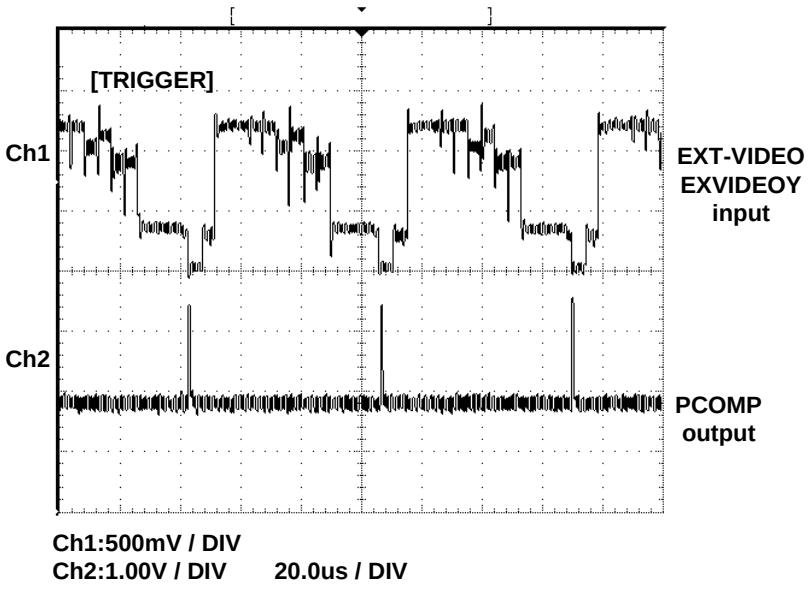


Fig 12.2-33 PCOMP output waveform (locked)

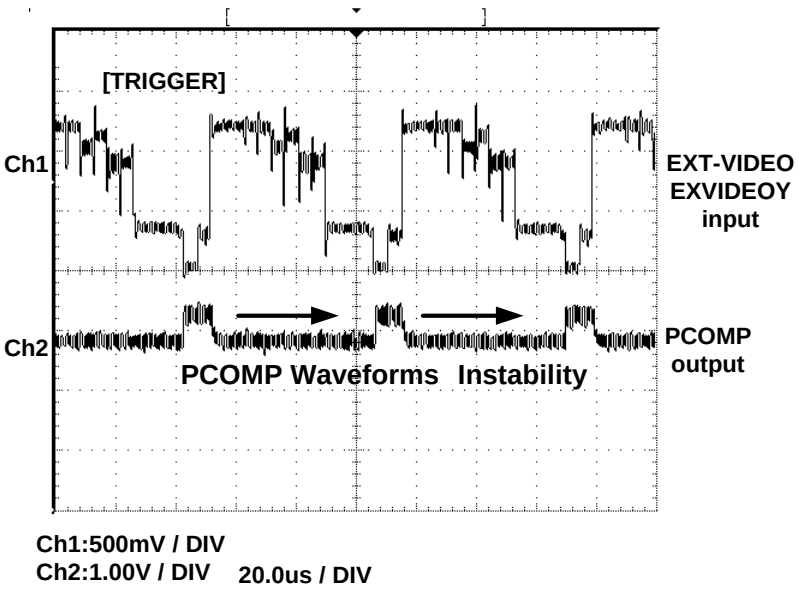


Fig 12.2-34 PCOMP output waveform (unlocked)

• **FSC phase comparison**

The burst component of EXT-VIDEO, which is input to EXTVIDEO (pin 58) from SYNCSEP inside the CXD3172AR, is amplified and digitized, and the resulting signal is phase-compared against the FSC signal. The result of this phase comparison is output through S2 (pin 47) as the FSC comparison output. The FSC comparison output should be applied to an LPF (SC) and fed back to the VCXO on the 8FSC side to form the subcarrier PLL.

12.2.11. VBS Lock Mode (VBSLHR)

VBS Lock (VBSLHR) synchronizes the camera vertical, horizontal, and subcarrier phases to the external video signal. A reset operation is performed in the vertical and horizontal directions, and a PLL operation is performed on the subcarrier.

The SGMODE setting is 4[h]. (See **Table 12.2-5**.)

This is not supported in auto mode (ATMODEON=1[h]).

Only a limited number of operation modes can be used with VBSLHR. For details, see appendix 13.1 ("External Synchronization Evaluation Results").

System Configuration

The master signal is an external video signal (EXT-VIDEO). A 1Vpp video signal (analog) is input to EXVIDEOY (pin 57) and EXVIDEO (pin 58). The external video luminance signal (EXT-VIDEO-Y) input to EXVIDEOY (pin 57) is divided inside the CXD3172AR between a vertical direction signal (EXT-VD) and horizontal direction signal (EXT-HD). EXT-VD resets the CXD3172AR's internal vertical direction counter. The EXT-HD signal resets the CXD3172AR's internal horizontal direction counter.

The burst component extracted inside the CXD3172AR from EXT-VIDEO (input to EXVIDEO (pin 58)) is amplified and digitized, and the resulting signal is phase-compared against the FSC signal.

X'tal oscillation is used for the VCXO on the ECK side. The clock for MCK should be supplied from the VCXO on the ECK side. A system block diagram is shown in **Fig 12.2-35**. The external input signal is presented in **Table 12.2-28**.

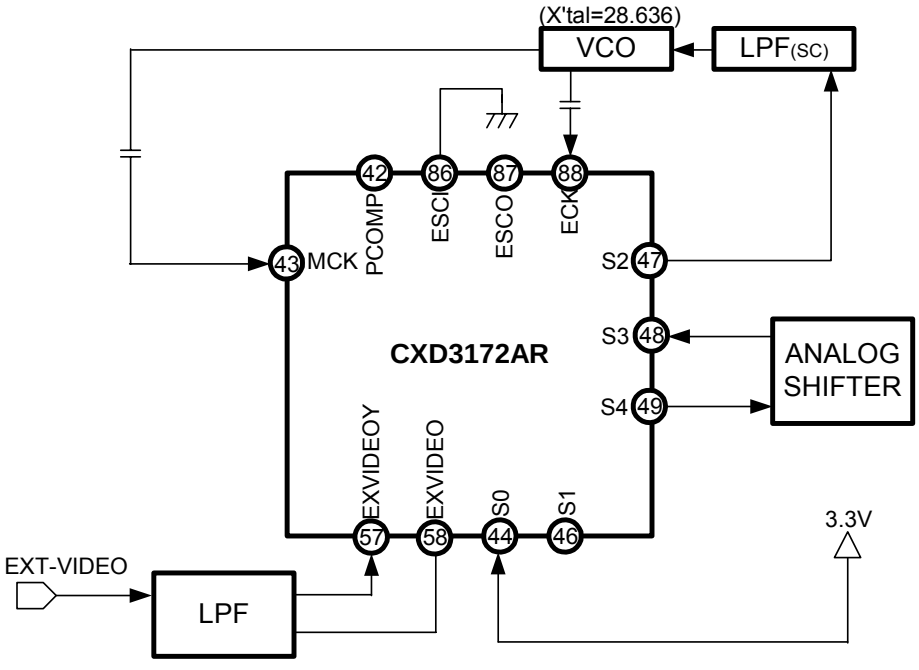


Fig 12.2-35 VBS Lock (VBSLHR) mode

Table 12.2-28 External Input Signal (VBS Lock (VBSLHR) Mode)

Pin Name(Pin No)	I/O signals
S0(44pin)	Connected (3.3V) power supply
S3(48pin)	FSC signal
EXVIDEOY(57pin)	EXT-VIDEO-Y(1Vpp: Analog signal)
EXVIDEO(58pin)	EXT-VIDEO(1Vpp: Analog signal)

The external video signal input to EXVIDEOY should be passed through the LPF. This serves to remove the subcarrier component, and is a countermeasure against noise in cases where no external video signal is input. The phase of the FSC signal output from S4 (pin 49) must be adjusted and the signal must be re-input to S3 (pin 48).

Internal phase comparison

• **FSC phase comparison**

The burst component of EXT-VIDEO, which is input to EXTVIDEO (pin 58) from SYNCSEP inside the CXD3172AR, is amplified and digitized, and the resulting signal is phase-compared against the FSC signal. The result of this phase comparison is output through S2 (pin 47) as the FSC comparison output. The FSC comparison output should be applied to an LPF (SC) and fed back to the VCXO on the 8FSC side to form the subcarrier PLL.

12.2.12. V Reset H Reset Mode (VRHR)

V Reset H Reset Mode synchronizes the camera vertical, horizontal, and LALT (PAL) phases to the external EXT-VD, EXT-HD, and EXT-LALT (PAL) reset signals.
The SGMODE setting is 5[h]. (See **Table 12.2-5**.)

System Configuration

The master signal is the external reset signal.
EXT-VD resets the vertical direction counter inside the CXD3172AR.
EXT-HD resets the horizontal direction counter inside the CXD3172AR.
EXT-LALT resets the LALT counter inside the CXD3172AR.
EXT-CLK, which is synchronized to the external reset signal, must be input to ECK (pin 88) or MCK (pin 43). Note that the configuration in this case is different from that of the 1-clock digital encoder system or 2-clock MCK-PLL system.
A block diagram of the 1-clock digital encoder system is shown in **Fig 12.2-36**. A block diagram of the 2-clock MCK-PLL system is shown in **Fig 12.2-37**. The external input signal is presented in **Table 12.2-29**, and related parameters are shown in **Table 12.2-30**.

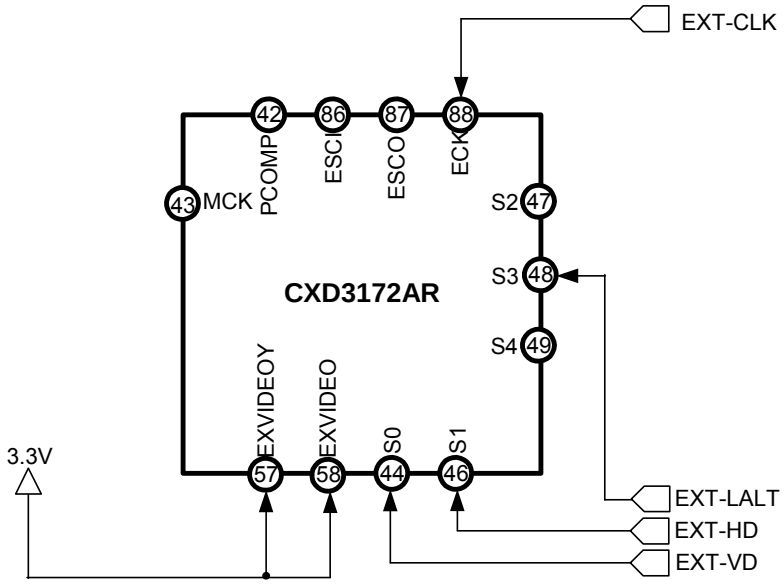


Fig 12.2-36 V Reset H Reset Mode (1-clock digital encoding)

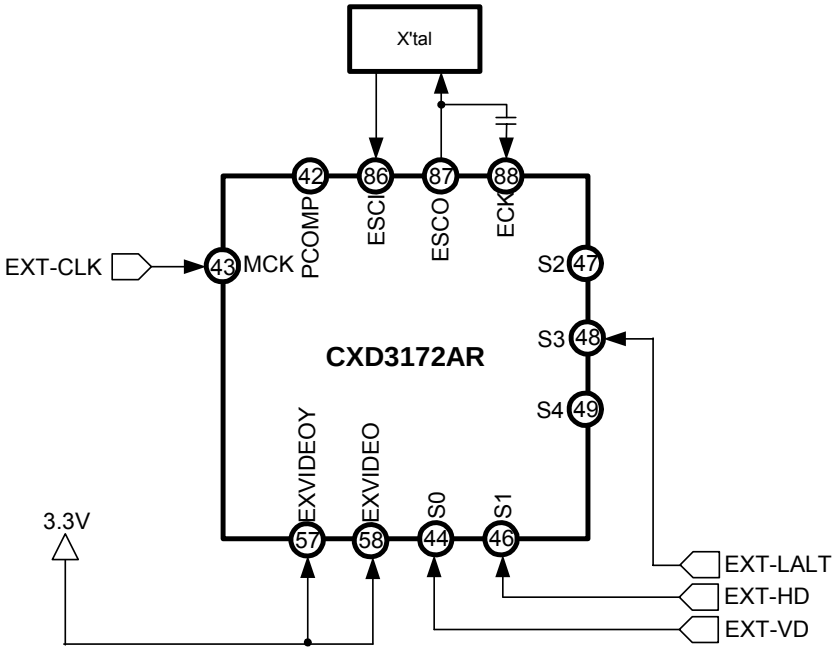


Fig 12.2-37 V Reset H Reset Mode (2-clock MCK-PLL)

Table 12.2-29 External Input Signal (V Reset H Reset Mode)

Pin Name(Pin No)	I/O signals
S0(44pin)	EXT-VD(3.3Vpp: Digital signal)
S1(46pin)	EXT-HD(3.3Vpp: Digital signal)
S3(48pin)*	EXT-LALT(3.3Vpp: Digital signal (PAL)
EXVIDEOY(57pin)	Connected (3.3V) power supply
EXVIDEO(58pin)	

* The EXT-LALT is used with PAL, so S3 (pin 48) may be left OPEN or set as desired in NTSC systems.

Table 12.2-30 Related parameters

Parameter		Description
DZHWID	CAT7_Byte6_bit0-3	Horizontal direction reset dead-band width adjustment (0-±15 Pixel)
DZVWID	CAT7_Byte6_bit4-7	Vertical direction reset dead-band width adjustment (0-±15 H)
PALSEQ	CAT1_Byte7_bit3	Change LALT control field for PAL

12.2.13. I/O pin initial settings and preventive measures

CXD3172AR pins S0-S3 (pins 44, 46, 47, and 48) are parameter-controlled I/O pins (Bi-Directional pins). In external synchronization mode, these pins are used for external synchronization input. However, during initialization (XRST removed -> parameter application), they are force-set to output mode. Therefore, in order to prevent short-circuiting during initialization, insert a resistor with approximately 10k ohm resistance.

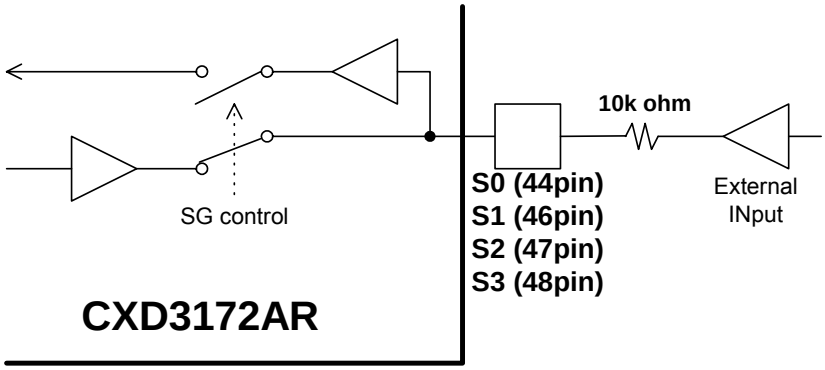


Fig 12.2-38 Measure to prevent shorting of CXD3172AR I/O pins

If the pins are not being used as input pins (e.g., in INT mode), then they can be left open under the output mode setting.

Table 12.2-31 CXD3172AR I/O pins and input mode settings

Pin Name	Pin No	Setting Parameters CAT1_Byte7,8	Initial value	Input setting	Remarks
S0	44	S0IN	0	1	Controlled by SG Output under other settings
S1	46	S1IN	0	1	
S2	47	S2SEL	0	7	
S3	48	S3SEL	0	7	

12.2.14. Phase Adjustment Using the Shifter

SFTV and SFTH in **Table 12.2-32** are parameters which are controlled using the keys (SFTUP, SFTDWN) for phase adjustment.

The particular parameters which can be controlled differ depending on the external synchronization mode.

* For information on key operations (SFTUP, SFTDWN), see 12.3 (“Key Operations (Shifter)”).

Table 12.2-32 Parameters Controlled by Key Operations

Parameter		Description
SFTHL	CAT7_Byte3_bit0-7	Horizontal direction phase adjustment value(LSB)
SFTHM	CAT7_Byte5_bit0-1	Horizontal direction phase adjustment value(MSB)
SFTVL	CAT7_Byte4_bit0-7	Vertical direction phase adjustment value(LSB)
SFTVM	CAT7_Byte5_bit2-3	Vertical direction phase adjustment value(MSB)

Parameters controlled by keys

Table 12.2-33 shows the SFTV and SFTH parameters which are controlled by keys in the various external synchronization modes.

Values which are adjusted through key operations are saved to the parameters in **Table 12.2-34**. Saved values (written to EEPROM when a key is released) are applied to SFTV/SFTH during initialization and when the external synchronization mode is switched.

Table 12.2-33 Parameters Controlled by Keys in Each External Synchronization Mode

External Synchronization Mode	SGMODE (CAT17_Byte17_bit0-3)	Parameters Controlled by Keys
INT	0[h]	-
LL	1[h]	SFTVL/M
VSL	2[h]	SFTHL/M
VBSLHP	3[h]	SFTHL/M
VBSLHR	4[h]	SFTHL/M
VRHR	5[h]	-
VSL-S	A[h]	SFTHL/M
VSL-D	F[h]	SFTHL/M

Table 12.2-34 Parameters for Saving SFTV/SFTH Adjustment Values

Parameter		Description
CTRLSFTHL	CAT17_Byte1_bit0-7	Parameter for saving SFTH adjustment value when key is released (LSB)
CTRLSFTHM	CAT17_Byte2_bit0-1	Parameter for saving SFTH adjustment value when key is released (MSB)
CTRLSFTVL	CAT17_Byte3_bit0-7	Parameter for saving SFTV adjustment value when key is released (LSB)
CTRLSFTVM	CAT17_Byte4_bit0-1	Parameter for saving SFTV adjustment value when key is released (MSB)

Parameters not controlled by keys

Table 12.2-35 shows the SFTV and SFTH parameters which are not controlled by keys in the various synchronization modes.

To change SFTV and SFTH that are not controlled by keys, set the parameters in **Table 12.2-36**.

If the external synchronization mode is VRHR (SGMODE=5[h]), keys cannot be used to change SFTV and SFTH. In such cases, use the parameters in **Table 12.2-37** to change SFTV and SFTH.

Table 12.2-35 Parameters Not Controlled by Keys in Each External Synchronization Mode

External Synchronization Mode	SGMODE (CAT17_Byte17_bit0-3)	Parameters Not Controlled by Keys
INT	0[h]	-
LL	1[h]	SFTHL/M
VSL	2[h]	SFTVL/M
VBSLHP	3[h]	SFTVL/M
VBSLHR	4[h]	SFTVL/M
VRHR	5[h]	SFTVL/M SFTHL/M
VSL-S	A[h]	SFTVL/M
VSL-D	F[h]	SFTVL/M

Table 12.2-36 SFTV and SFTH Adjustment Parameters Which are Not Key-Controlled

Parameter		Description
FIXPHL	CAT17_Byte9_bit0-7	Parameter for setting SFTH not Controlled by Keys(LSB)
FIXPHM	CAT17_Byte10_bit0-1	Parameter for setting SFTH not Controlled by Keys(MSB)
FIXPVL	CAT17_Byte11_bit0-7	Parameter for setting SFTV not Controlled by Keys(LSB)
FIXPVM	CAT17_Byte12_bit2-3	Parameter for setting SFTV not Controlled by Keys(MSB)

Table 12.2-37 SFTV and SFTH Adjustment Parameters Which do Not Support Key Processing in VRHR Mode

Parameter		Description
FIXRSTHL	CAT17_Byte5_bit0-7	Parameter for setting SFTH in VRHR mode (LSB)
FIXRSTHM	CAT17_Byte6_bit0-1	Parameter for setting SFTH in VRHR mode (MSB)
FIXRSTVL	CAT17_Byte7_bit0-7	Parameter for setting SFTV in VRHR mode (LSB)
FIXRSTVM	CAT17_Byte8_bit0-1	Parameter for setting SFTV in VRHR mode (MSB)

12.3. Key Operations (Shifter)

SS-HQ1 key operations (shifter) are used for both manual WB gain adjustment (MWB) in the WB function, and phase adjustment (SG shifter) in external synchronization.
Key operations are used through external switches in combination with the port driver function.

The following explanation of key operations assumes the use of external switches.

12.3.1. AWB MODE and SFTUP/SFTDWN assignments

The SS-HQ1 assigns SFTUP and SFTDWN operations based on the AWB MODE setting, as detailed below.

Table 12.3-1 SFTUP and SFTDWN operation assignments

AWB1	AWB2	AWB3	AWBMODE	MODE	SFTUP/SFTDWN operation assignments
0	0	0	0	ATW	SG shifter
0	0	1	4	MWB	MWB (color temperature)
0	1	0	2	Push	SG Shifter
0	1	1	6	Hold	SG Shifter
1	0	0	1	User fixed value 1	SG Shifter
1	0	1	5	user fixed value 2	SG Shifter
1	1	0	3	user fixed value 3	SG Shifter
1	1	1	7	user fixed value 4	SG Shifter

12.3.2. Key Operations

Key operation procedures

Manual WB gain adjustment for the WB function and external synchronization phase adjustment both use the following parameters as keys.

- **SFTUP (CAT17_Byte18_bit0)**
- **SFTDWN (CAT17_Byte18_bit1)**

The controlled register is controlled by changing the SFTUP/SFTDWN parameter value as shown in **Table 12.3-2**.

Table 12.3-2 SFTUP/SFTDWN Control Procedures

SFTUP	SFTDWN	Control Specifications	Remarks
0[h]	0[h]		
1[h]	0[h]	Increment of the controlled value	Write adjustment value to EEPROM at 01 -> 00
0[h]	1[h]	Decrement of the controlled value	Write adjustment value to EEPROM at 10 -> 00
1[h]	1[h]	PRESET	*

* With the PRESET (1,1), PRSTSFTH, PRSTSFTV, MWBPRESETR, and MWBPRESETB are applied.

SFTUP/SFTDWN key arrangement

Key operations can be arranged using the parameters in **Table 12.3-3**. This key operation provides two periods with different processing intervals. The period immediately after key release is called the initial period. The other period is called the continuous period. (See **Fig 12.3-1**.)

Table 12.3-3 Parameters for setting key arrangement

Parameter		Description	Notes
KEYINFLD	CAT17_Byte19_bit0-7	Sets the key processing interval for the initial period	Common
KEYINCNT	CAT17_Byte20_bit0-1	Sets the key processing count for the initial period	Common
KEYRPFLD	CAT17_Byte21_bit0-7	Sets the key processing interval for the continuous period	Only valid for WB processing
SFTSTEP	CAT17_Byte22_bit0-4	Shifter operation speed setting (STEP width)	Common

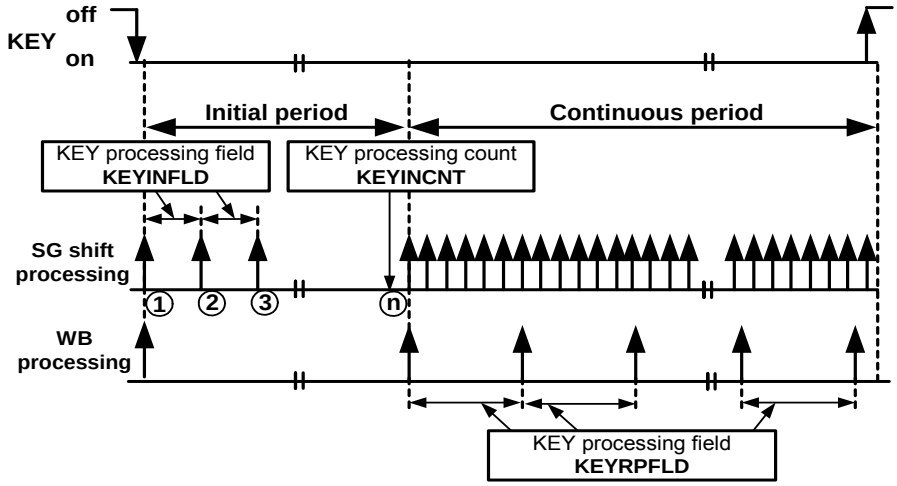


Fig 12.3-1 SFTUP/SFTDWN key arrangement

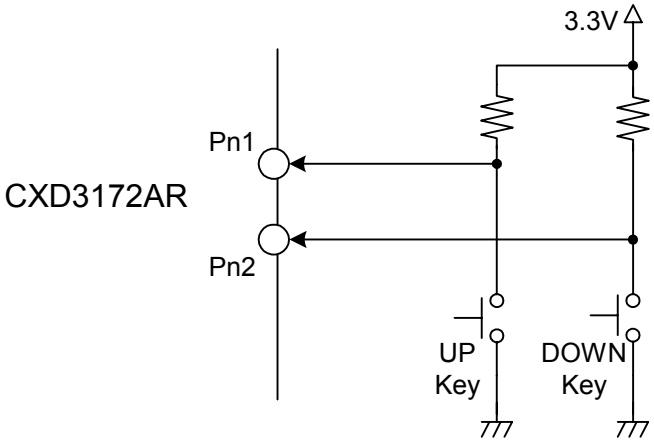


Fig 12.3-2 SFTUP/SFTDWN key assignments

SFTUP and SFTDWN are assigned to ports (Pn1 and Pn2 in the diagram), and the port driver is set so that SFTUP can be controlled through the Pn1 port and SFTDWN through the Pn2 port.

12.3.3. External Synchronization Phase Adjustment through Key Operations

External synchronization phase adjustment can be performed through key operations.

Parameters controlled through keys

During external synchronization phase adjustment, the parameters controlled through key operations (SFTUP/SFTDWN) are SFTV and SFTH in “Table 12.2-32 Parameters Controlled by Key Operations“.
The SFTV/SFTH values adjusted through key operations are saved to the parameters in **Table 12.2-34**. The saved values (written to EEPROM when the keys are released) are applied to SFTV/SFTH during initialization.

Table 12.3-4 Parameters Controlled through Keys

Parameter		Description
SFTHL	CAT7_Byte3_bit0-7	Horizontal direction phase adjustment value (LSB)
SFTHM	CAT7_Byte5_bit0-1	Horizontal direction phase adjustment value (MSB)
SFTVL	CAT7_Byte4_bit0-7	Vertical direction phase adjustment value (LSB)
SFTVM	CAT7_Byte5_bit2-3	Vertical direction phase adjustment value (MSB)

Table 12.3-5 Parameters for saving SFTV/SFTH adjustment values

Parameter		Description
CTRLSFTHL	CAT17_Byte1_bit0-7	Parameter for saving SFTH adjustment value at key release (LSB)
CTRLSFTHM	CAT17_Byte2_bit0-1	Parameter for saving SFTH adjustment value at key release (MSB)
CTRLSFTVL	CAT17_Byte3_bit0-7	Parameter for saving SFTV adjustment value at key release (LSB)
CTRLSFTVM	CAT17_Byte4_bit0-1	Parameter for saving SFTV adjustment value at key release (MSB)

Phase adjustment parameters when using presets

Presets are applied when both SFTUP and SFTDWN are set to “1[h]”.
When presets are applied, the values set in the parameters of **Table 12.3-6** (PRSTSFTH and PRSTSFTV) are applied to SFTH or SFTV.

Table 12.3-6 Phase adjustment parameters when using presets

Parameter		Description
PRSTSFTHL	CAT17_Byte13_bit0-7	SFTH setting for presets (LSB)
PRSTSFTHM	CAT17_Byte14_bit0-1	SFTH setting for presets (MSB)
PRSTSFTVL	CAT17_Byte15_bit0-7	SFTV setting for presets (LSB)
PRSTSFTVM	CAT17_Byte16_bit0-1	SFTV setting for presets (MSB)

* See 12.2 “Using external synchronization” for information on the phase adjustment parameters that are not controlled through keys.

12.3.4. WB Gain Adjustment through Key Operations

The manual white balance (MWB) gain can be adjusted through key operations.

Parameters controlled through keys

In MWB mode, the parameters controlled through key operations (SFTUP/SFTDWN) are WBR and WBB in **Table 12.3-7**. The WBR/WBB values adjusted through key operations are saved to the parameters in **Table 12.3-8**. The saved values (written to EEPROM when the keys are released) are applied to WBR/WBB during initialization.

Table 12.3-7 Parameters controlled through keys

Parameter		Description
WBR	CAT4_Byte1	White balance gain R
WBB	CAT4_Byte3	White balance gain B

Table 12.3-8 Parameter for saving WBR/WBB adjustment value

Parameter		Description
PLRGAIN	CAT15_Byte33	Push lock R gain / Parameter for saving WBR adjustment value when key is released
PLBGAIN	CAT15_Byte34	Push lock B gain / Parameter for saving WBB adjustment value when key is released

WB gain parameters when using presets

Presets are applied when both SFTUP and SFTDWN are set to “1[h]”.

When presets are applied, the values set in the parameters of **Table 12.3-9** (MWBPRESETR and MWBPRESETB) are applied to WBR or WBB.

Table 12.3-9 WB gain parameters when using presets

Parameter		Description
MWBPRESETR	CAT19_Byte10_bit0-7	WBR setting for presets (LSB)
MWBPRESETB	CAT19_Byte11_bit0-1	WBB setting for presets (MSB)

12.4. When Using the External Microcomputer

12.4.1. External Microcomputer-SS-HQ1 System Interface

System Composition

(Connection of External Microcomputer, DSP, and EEPROM)

Even if EEPROM is available for use with an external microcomputer, it cannot be used for reading and writing in DSP (CXD3172AR) parameters via serial communication with the external microcomputer.
Be sure to include the DSP EEPROM in the serial communication line.

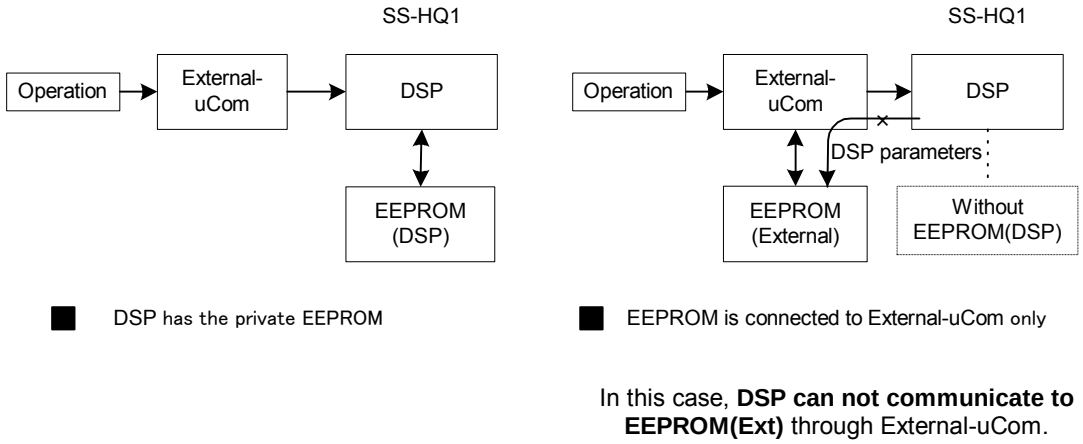


Fig 12.4-1 External Microcomputer-DSP EEPROM Interface

Connection Method

The wiring for each pin is given in the table below.

Table 12.4-1 CXD3172AR Wiring with a Microcomputer

Pin name	Pin Number	Description
SIFSEL	13	Low
XCS	15	Chip selection input
SI	16	Serial settings input
SO	17	Serial data output
SCK	18	Serial clock input
VD	Auxiliary signal (for communication timing control) Output from S3 (Pin 48 S3SEL=3) or S4 (Pin 49 S4SEL=3)	

Note

"L" and "H" of SIFSEL are recognized only during initial operation.
If they are changed, be sure to reset the system.

12.4.2. Communication Protocol with External Microcomputers

Communication Speed

Keep the transfer rate at 400 kbps or less (1SCK > 2.5[us]).
The required transfer rate is such that 32-byte transmissions are less than [1 field - communication prohibited period].

Communication Timing

The CXD3172AR loads data in 8-bit units at the rising edge of SCK when XCS is low. The serial output is sent at the falling edge of SCK in synchronization with the serial input. You must leave at least SCK 1 clock division between byte data. The communication data is LSB first. Additionally, make SCK "H" (or pull-up) before making XCS low.

For details on data strings, see the following sections on command specifications and the communication format.

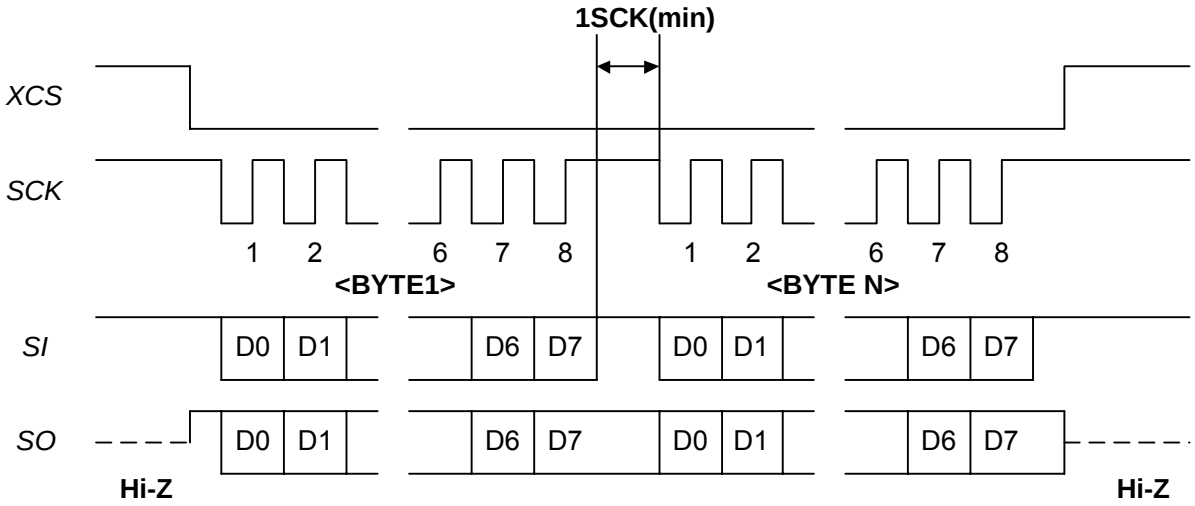


Fig 12.4-2 Communication Timing (External Microcomputers)

Transmission Command Specification (External Microcomputer -> DSP)

Table 12.4-2 Transmission Command Specification for Communication with External Microcomputers

Function	Communication format (in bytes)					
	1	2	3	4	5	6-32
Specify and read register category	05h	01h	CAT	STBN	BYTEn 01h-1Fh	
Specify and write register category	BYTEn+4	02h	CAT	STBN	Write data (28 bytes max.)	
Specify and read EEPROM category	05h	03h	CAT	STBN	BYTEn 01h-1Fh	
Specify and write EEPROM category	05h	04h	CAT	STBN	BYTEn 01h-FFh	
Specify and read actual EEPROM address	05h	05h	EEPROM ADDRESS MSB	EEPROM ADDRESS LSB	BYTEn 01h-1Fh	
Specify and write actual EEPROM address	BYTEn+4	06h	EEPROM ADDRESS MSB	EEPROM ADDRESS LSB	Write data (28 bytes max.)	
Write all to EEPROM	05h	07h	00h	01h	02h	
Dummy (packets for receipt only)	00h	Sends as many 00h as the number of bytes received				

<Explanation of Command Transmission Specification>

Data of first byte Total number of valid bytes in a packet; if 00h, judged a dummy

Data of second byte Command code

CAT Write/read category number

STBN Write/read start byte number

BYTEn Number of bytes to write/read (if CAT is specified, only in the same category)

EEPROM ADDRESS MSB/LSB Actual address in EEPROM : 0000h~02FFhh

Note

CAT can be designated in a range of 01h-18h. However, for CAT 5, 22, and 23, there is no writing to EEPROM. Thus, 05h, 16h, and 17h cannot be designated when specifying the EEPROM category in write/read commands.

For category-specific commands (codes 01h, 02h, 03h, and 04h), errors will occur from instructions for a numbers of bytes exceeding the same category.

The CXD3172AR returns echo backs in response to write commands, so for the following commands, send dummy data that conforms to the reception specification.

Reception Command Specification (DSP -> External Microcomputer)

Table 12.4-3 Reception Command Specification for Communication with External Microcomputers

Function	Communication format (in bytes)			
	1	2	3	4-32
Specify and read register category	BYTEn+1	Read data (the specified amount)		
Specify and write register category	BYTEn+1	Write data (the specified amount)		
Specify and read EEPROM category	BYTEn+1	Read data (the specified amount)		
Specify and write EEPROM category	02h	01h		
Specify and read actual EEPROM address	BYTEn+1	Read data (the specified amount)		
Specify and write actual EEPROM address	02h	01h		
Write all to EEPROM	02h	01h		

<Explanation of Command Reception Specification>

Data of first byte Total number of valid bytes in a packet; otherwise, an error code (Fnh)

Data of second byte Dummy (01h), read data, or echo back (write data)

BYTEn Number of bytes to write/read

<Error codes>

FCH Communication error (overrun or other protocol violation)

F0H Error in number of valid bytes for transmission

F1H Command code error

F2H Category number error

F3H Byte number error

F4H Illegal access (communication data out of range, etc.)

F5H EEPROM busy

If an error code is sent, no bytes after the second byte are sent.

Communication format

The communication format supports packets up to 32 bytes. (The size varies depending on the command.) The CXD3172AR receives a packet of data, analyzes it, and then performs control by executing a command. Until this command is executed, no other commands may be received. For details regarding the command processing time, see "Table 12.4-4 Communication Prohibited Period (Other Than for EEPROM Write)" and ”Table 12.4-5 Communication Prohibited Period of EEPROM Write”.

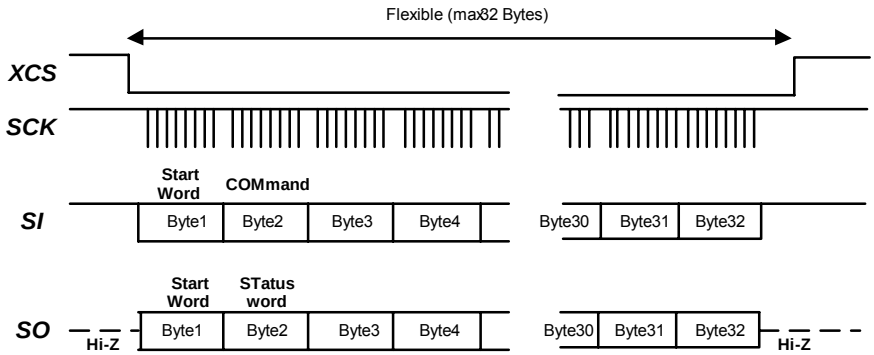


Fig 12.4-3 Microcomputer Communication Format

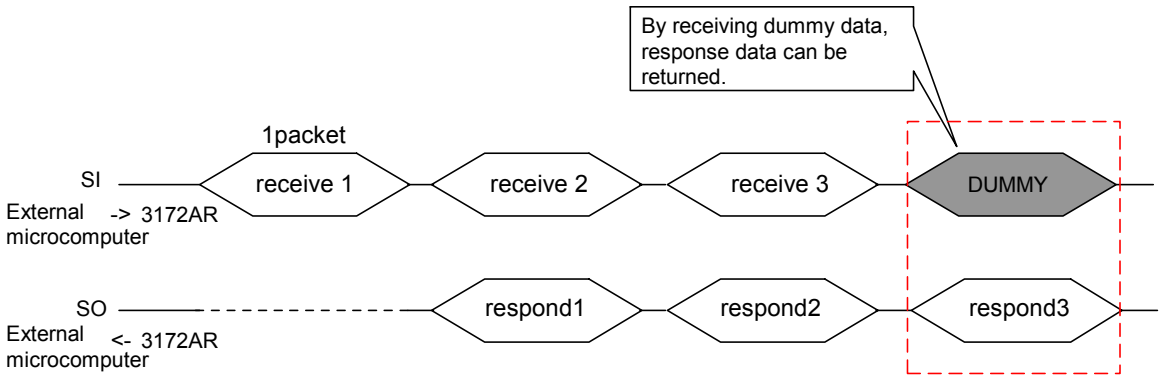


Fig 12.4-4 DSP Response Timing

After the DSP receives a packet, it responds when it receives the next.

Serial Data Latch and Incorporation of Data

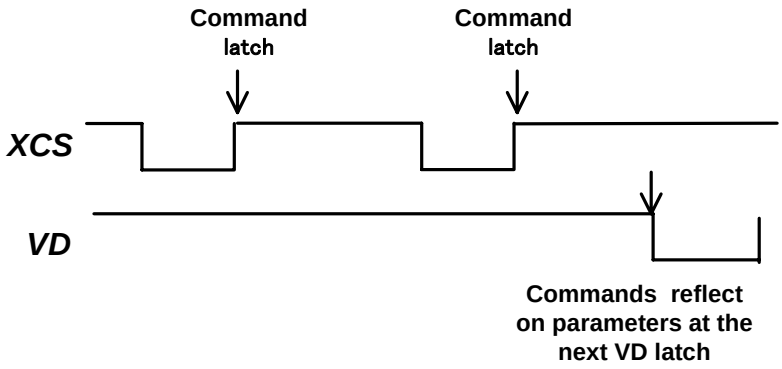


Fig 12.4-5 Serial Data Latch and Parameter Incorporate Timing

Commands are latched and executed after packets are complete (XCS="H"). However, parameter updates from register WRITE commands occur after VD latching of the next field. All latching is performed during the communication prohibited period.

Serial Communication Prohibited Period (Power on/DSP initialization)

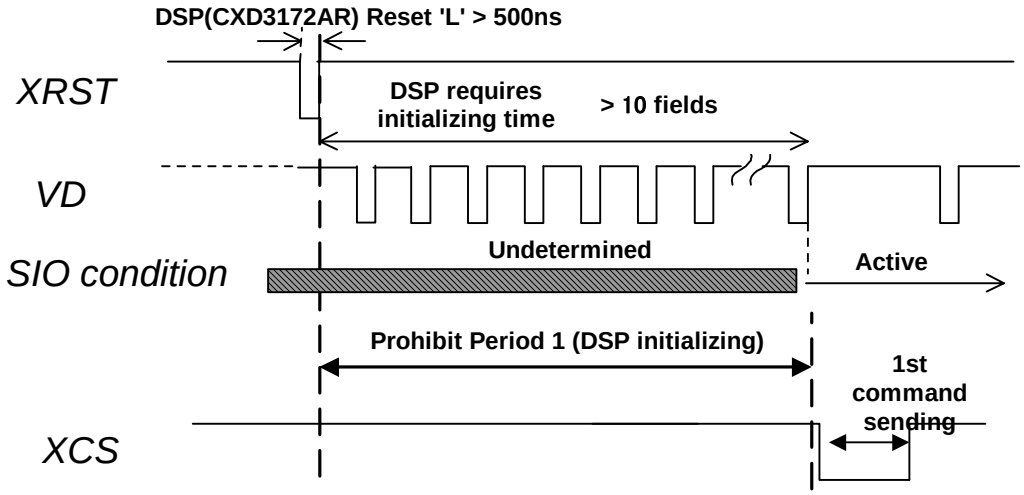


Fig 12.4-6 Communication Prohibited Period during CXD3172AR Initialization

Serial communication cannot be received in the initial period (from reset to 10 fields).
Monitor the VD pulse, for example, and wait until the initial period is over.

Serial Communication Prohibited Period (Register Read/Write, EEPROM Read)

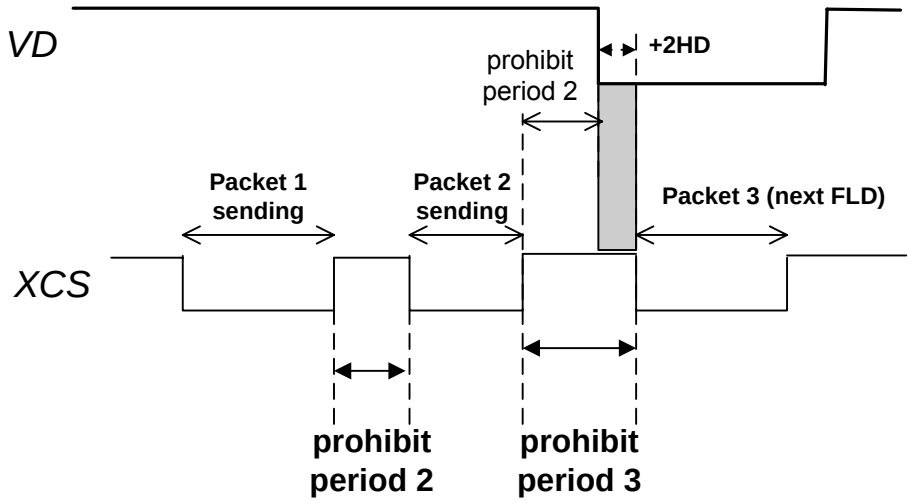


Fig 12.4-7 Communication Prohibited Period during Register Read/Write or EEPROM Read Commands

After a packet is sent, there must be a communication prohibited period (prohibit_period_2) for command processing.

Table 12.4-4 Communication Prohibited Period (Other Than for EEPROM Write)

Command	prohibit_period_2	prohibit_period_3
Register READ	500 [us]	If it depends on the VD falling edge, communication is also prohibited for +2HD.
Register WRITE		
EEPROM category READ	3.0 [ms]	
Specify and Read EEPROM direct address		

To allow for firmware processing for each field, ensure a prohibit_period_3 including a 2HD period after the VD falling edge.

Serial Communication Prohibited Period (EEPROM Write)

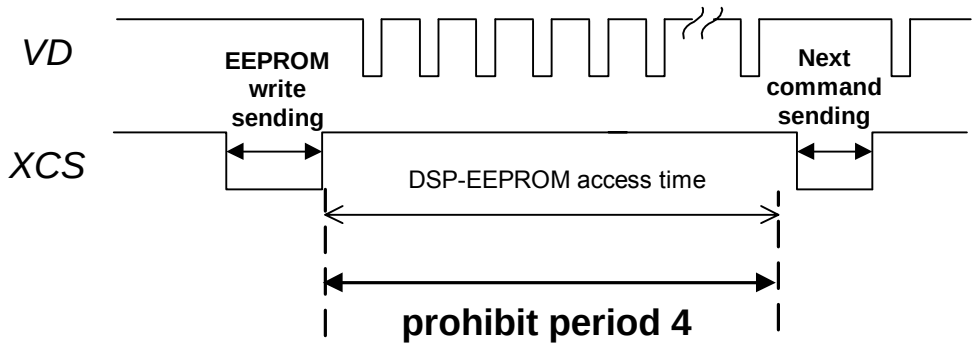


Fig 12.4-8 Communication Prohibited Period of EEPROM Write Commands

When EEPROM write command is received, the next command cannot be received more than 18 fields until the EEPROM write is complete.

Table 12.4-5 Communication Prohibited Period of EEPROM Write

Command	prohibit_period_4
Specify and Write EEPROM direct address	18 field
Specify and Write EEPROM category	
Write all EEPROM categories	360 field

When not using communication with the External Microcomputer

If RS-232C communication is used, set SIFSEL to high and follow the RS-232C communication settings.
Also set XCS and SCK to high if there is no communication with an external microcomputer (or via serial interface and when SIFSEL=low). Keep SI fixed at low or high. Additionally, leave output pin SO open.

12.5. Pattern Generator (PG)

12.5.1. Pattern generator (PG) Usage Method

The CXD3172AR incorporates a pattern generator (PG) for applications which allows various types of patterns to be output based on the serial data settings.

• PG parameter settings

Before using the PG, set the parameters as shown in **Table 12.5-1**.

* Before making these settings, first set **CPUHOLD (CAT12_Byte5_bit0) to 1[h].**

Table 12.5-1 PG parameter settings

Parameter		Setting Value
RMATY	CAT2_Byte31_bit0-7	40[h]
RMATC	CAT2_Byte32_bit0-7	C0[h]
BMATY	CAT2_Byte33_bit0-7	40[h]
BMATC	CAT2_Byte34_bit0-7	C0[h]
GMATCR	CAT2_Byte35_bit0-7	80[h]
GMATCB	CAT2_Byte36_bit0-7	80[h]
RYGAIN1	CAT2_Byte37_bit0-7	26[h]
BYGAIN1	CAT2_Byte38_bit0-7	1B[h]
RYHUE1	CAT2_Byte39_bit0-7	D5[h]
BYHUE1	CAT2_Byte40_bit0-7	E9[h]
BLACKS1	CAT2_Byte55_bit0-7	00[h]
BLACKS2	CAT2_Byte56_bit0-7	00[h]
WBR	CAT4_Byte1_bit0-7	40[h]
WBG	CAT4_Byte2_bit0-7	40[h]
WBB	CAT4_Byte3_bit0-7	20[h]

• PG display ON/OFF

The following parameter is used to turn the PG display ON/OFF.

Table 12.5-2 PGON parameter

Parameter		Setting Value	Description
PGON	CAT9_Byte36_bit3	0[h]	PG display OFF
		1[h]	PG display ON

• PG gain settings

The following parameter can be used to adjust the PG gain.

Table 12.5-3 PGGAIN parameter

Parameter		Setting Value	Description
PGGAIN	CAT9_Byte36_bit6-7	0[h]	Sets PG data gain value to 0X
		1[h]	Sets PG data gain value to 1X
		2[h]	Sets PG data gain value to 2X
		3[h]	Sets PG data gain value to 4X

12.5.2. Pattern settings

• Pattern settings

The following table summarizes the patterns that can be output by the PG. The color settings for monochrome raster are shown in **Table 12.5-5**.

Table 12.5-4 Pattern types (Pattern settings)

Parameter		Setting Value	Pattern
PGPAT	CAT9_Byte37_bit0-1	0[h]	Color bar
		1[h]	Monochrome raster
		2[h]	Impulse
		3[h]	Serial setting (see **Table 12.5-9** for information on how to make this setting)

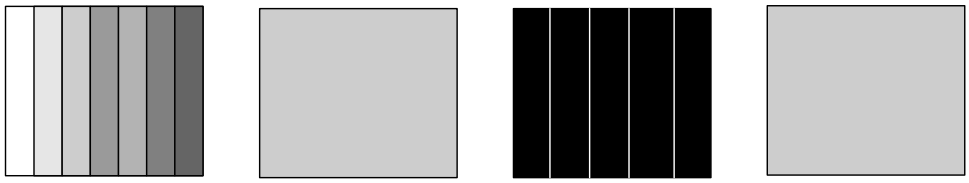


Fig 12.5-1 Pattern types (Pattern settings)

* Note that the images shown above are for reference purposes only.
The patterns that are actually output by the PG will differ slightly from them.

Table 12.5-5 Raster color settings

Parameter		Setting Value	Description
PGCOLOR	CAT9_Byte37_bit5-7	0[h]	Sets raster color to W
		1[h]	Sets raster color to Ye
		2[h]	Sets raster color to Cy
		3[h]	Sets raster color to G
		4[h]	Sets raster color to Mg
		5[h]	Sets raster color to R
		6[h]	Sets raster color to B
		7[h]	Sets horizontal simple ramp (high setting priority)

• Ramp addition

PGRION add a ramp to the selected PG pattern.

Table 12.5-6 Pattern settings (with ramp added)

Parameter		Setting Value	Pattern
PGRION	CAT9_Byte37_bit3	0[h]	Displays the PG selected by PGPAT
		1[h]	Adds a ramp to and displays the PG selected by PGPAT (if impulse is set, then the display is reversed)

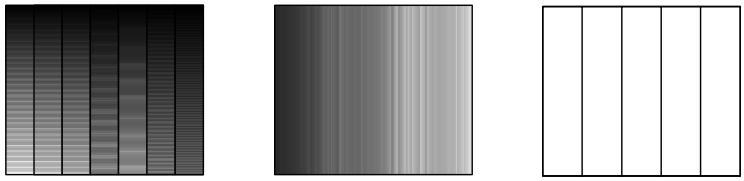


Fig 12.5-2 Pattern types (with ramp added)

* Note that the images shown above are for reference purposes only. The patterns that are actually output by the PG will differ slightly from them.
* It is not possible to add a ramp under serial settings.

• H/V settings

PGHV can switch the selected PG pattern display between the horizontal and vertical directions.

Table 12.5-7 Pattern settings (H/V settings)

Parameter		Setting Value	Pattern
PGHV	CAT9_Byte37_bit2	0[h]	Displays the PG selected by PGPAT in the horizontal direction
		1[h]	Displays the PG selected by PGPAT in the vertical direction

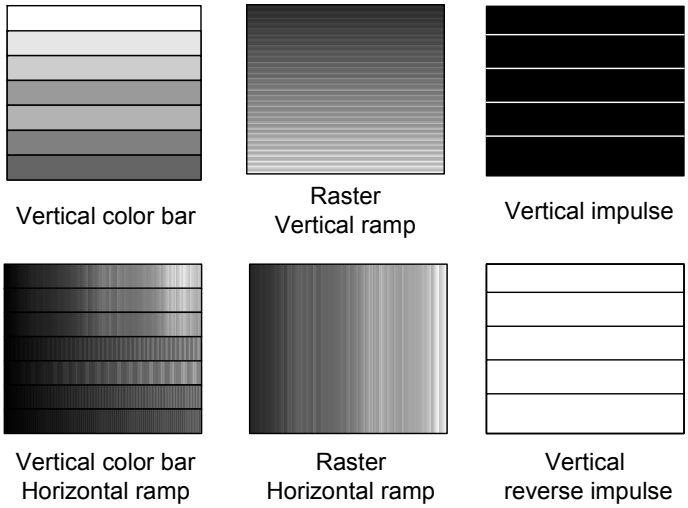


Fig 12.5-3 Pattern types (H/Vsettings)

* Note that the images shown above are for reference purposes only. The patterns that are actually output by the PG will differ slightly from them.
* The PG and ramp are linked together, so if the PG is changed between horizontal and vertical, the ramp will also change between vertical and horizontal. Therefore, it is not possible to display combinations in which a horizontal ramp is added to a horizontal color bar, or a vertical ramp is added to a vertical color bar.

• PGRAWMIX settings

PGRAWMIX can divide the display between a PG area and an imaging area, as shown below.

Table 12.5-8 Pattern settings (PGRAWMIX settings)

Parameter		Setting value	Pattern
PGRAWMIX	CAT9_Byte37_bit4	0[h]	No imaging area (only PG is output)
		1[h]	Imaging area included (PG and MIX are output)

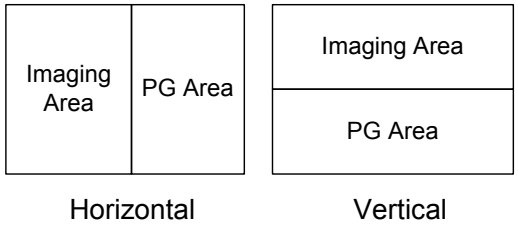


Fig 12.5-4 Pattern types (PGRAWMIX settings)

• Serial settings

With the CXD3172AR, it is possible to set CR line and CB line information through serial communication. Use the parameters in **Table 12.5-9** to make these settings. **Table 12.5-10** shows color reproduction settings which are nearly ideal.

Table 12.5-9 Parameters for setting CR and CB line information

Parameter		Setting Value	Description
PGSDCRS2	CAT9_Byte39_bit0-7	00[h]-FF[h]	CR_S2 serial setting (Ye+Mg)
PGSDCRS1	CAT9_Byte40_bit0-7	00[h]-FF[h]	CR_S1 serial setting (Cy+G)
PGSDCBS2	CAT9_Byte41_bit0-7	00[h]-FF[h]	CB_S2 serial setting (Ye+G)
PGSDCBS1	CAT9_Byte42_bit0-7	00[h]-FF[h]	CB_S1 serial setting (Cy+Mg)

Table 12.5-10 Ideal color bar levels

Parameter	Setting Value						
	W	Ye	Cy	Mg	G	R	B
PGSDCRS2	80[h]	60[h]	40[h]	60[h]	20[h]	40[h]	20[h]
PGSDCRS1	60[h]	40[h]	60[h]	20[h]	40[h]	00[h]	20[h]
PGSDCBS2	60[h]	60[h]	40[h]	20[h]	40[h]	20[h]	00[h]
PGSDCBS1	80[h]	40[h]	60[h]	60[h]	20[h]	20[h]	40[h]

12.6. Sync Signal Output Setting Method

The tables below describe the parameters related to output switching for the sync signal output pins S0 (CXD3172AR 44pin), S1 (CXD3172AR 46pin), S2 (CXD3172AR 47pin), S3 (CXD3172AR 48pin), S4 (CXD3172AR 49pin).
Since a setup of S0-S4 pins are controlled by SG MODE, the setting method is as follows.

1. Set SSELOFF (CAT12 Byte12 bit5) to ”1”. (S pins control by SG MODE is off)
2. Set up the parameters of each S* pins. (CAT1 Bite7-8)
3. Write CAT1 into EEPROM.
4. Set SSELOFF to ”0” back.

Table 12.6-1 S0IN

S0IN	S0 pin INput
Parameter category	CAT1_Byte7_bit6
Outline	Selects the S0 pin input / output signal
Setting range	0[h], 1[h]
Initial value	1[h]:VRI INPUT
Description	0[h]:DHD OUTPUT 1[h]:VRI INPUT
Note	F/W controls this pin during the external synchronization. *Refer to “12.2 Using external synchronization” for details.

Table 12.6-2 S1IN

S1IN	S1 pin INput
Parameter category	CAT1_Byte7_bit7
Outline	Selects the S1 pin input / output signal
Setting range	0[h] - 3[h]
Initial value	0[h]: DVD OUTPUT
Description	0[h]:DVD OUTPUT 1[h]:HRI INPUT
Note	F/W controls this pin during the external synchronization. *Refer to “12.2 Using external synchronization” for details.

Table 12.6-3 S2SEL

S2SEL	S2 pin SELect
Parameter category	CAT1_Byte8_bit0-2 (3bit)
Outline	Selects the S1 pin output signal
Setting range	0[h] - 7[h]
Initial value	0[h]: FSC comparison output
Description	Each signal is output according to the following settings. 0[h]: FSC comparison output 1[h]:DHD 2[h]:DVD 3[h]:SYNC 4[h]: TG EXP 5[h]:Digital YOUT[6] 6[h]:FLD 7[h]:LALT IN
Note	F/W controls this pin during the external synchronization(VBS Lock).

Table 12.6-4 S3SEL

S3SEL	S3 pin SELect
Parameter category	CAT1_Byte8_bit3-5 (3bit)
Outline	Selects the S3 pin output signal
Setting range	0[h] - 7[h]
Initial value	0[h]: DHD OUTPUT
Description	Each signal is output according to the following settings. 0[h]: DHD 1[h]:DVD 2[h]:HD 3[h]:VD 4[h]: NRYBY 5[h]:Digital YOUT[7] 6[h]:FLD 7[h]:Analog shift FSC input
Note	F/W controls this pin during the external synchronization (VBS Lock).

Table 12.6-5 S4SEL

S4SEL	S4 pin SELect
Parameter category	CAT1_Byte8_bit6-7 (2bit)
Outline	Selects the S4 pin output signal
Setting range	0[h] - 3[h]
Initial value	0[h]: Chip select output for external EVR
Description	Each signal is output according to the following settings. 0[h]: Chip select output for external EVR 1[h]: FSC output 2[h]:HD 3[h]:VD
Note	F/W controls this pin during the external synchronization (VBS Lock). Using this pin output, EVRLDSEL (CAT12 byte10 bit1) setting is necessary when you use the external EVR. *Refer to ”3.5 EVR Connection” for details.

12.7. ADJUST Output

12.7.1. ADJUST Function

The ADJUST function is a function which performs 10-bit digital value sampling immediately after the A/D converter; performs 9-bit digital value sampling after YC processing (immediately before encoder processing); and outputs those values through serial communication. This function can be used to digitally measure signal level characteristics with the camera set in the image pickup state.
As an example application, individual color bar color measurement results can be used in studying dynamic range during evaluations, and in testing for variations among camera sets on mass production lines.

Operations

The SG block generates a sampling pulse (ADJUST pulse), and sampling is performed in the A/D block and Y/C block.
In the A/D block, the value immediately following the A/D converter (AJSTOUT) is sampled.
In the Y block, the value immediately preceding the encoder processing block (YOUT) is sampled. In the C block, the color difference values prior to encoding (R-Y: RYOUT, B-Y: BYOUT) are sampled.
The values of AJSTOUT, YOUT, RYOUT, and BYOUT can be read by transmitting CAT22 (SOUT1) through serial communication.

Settings

Marker position indicators during camera adjustment signal output are set by setting numerical values for MSK0HSET and MSK0VSET. When these are set, the indicators are mixed with the Y signal and makers are displayed on the screen. These set values are the same as the position indicated by the mask 0 starting point address.
The marker display can be turned ON/OFF by using ADJSTMK and DISPMIX. Note that these markers will not be displayed unless the individual parameters are set to ON after first setting ADJUST (CAT8_Byte1_bit6) to 1[h].
Also note that the position displayed by the mask 0 starting point address, as well as the marker positions displayed by ADJSTMK and DISPMIX are different from each other for reasons related to DSP processing. However, the sampled data will correspond to the respective marker positions.

Table 12.7-1 ADJUST Settings

Parameter		Description
ADJUST	CAT8_Byte1_bit6	Camera adjustment signal output
ADJSTMK	CAT8_Byte2_bit4	AD sampling point indicator (output to AJSTOUTL/M)
DISPMIX	CAT8_Byte1_bit7	Y, R-Y and B-Y sampling point indicator (output to YOUTL/M, RYOUTL/M, and BYOUTL/M)
MSK0HSET	CAT9_Byte1_bit0-7	Mask 0 horizontal starting point (4-pixel unit) / Sampling horizontal position
MSK0VSET	CAT9_Byte17_bit0-7	Mask 0 vertical starting point (4-pixel unit) / Sampling vertical position

Table 12.7-2 ADJUST Output Data

Parameter		Description
AJSTOUTL/M	CAT22_Byte2_bit0-7 CAT22_Byte3_bit0-1	AD sampling data output
YOUTL/M	CAT22_Byte54_bit0-7 CAT22_Byte57_bit0	Y sampling data output
RYOUTL/M	CAT22_Byte55_bit0-7 CAT22_Byte57_bit1	R-Y sampling data output
BYOUTL/M	CAT22_Byte56_bit0-7 CAT22_Byte57_bit2	B-Y sampling data output

13. Appendix

13.1. External Synchronization Evaluation Results

The SS-HQ1 may operate outside the Specification or noise may occur depending on the particular combination of operation mode (MODESEL) and external synchronization mode (SGMODE). The following table summarizes the external synchronization mode evaluation results obtained using our evaluation board. Refer to this table in selecting a synchronization mode.

Table 13.1-1 Summary of External Synchronization Evaluation Results

MODESEL / SGMODE	0[h]	1[h]	2[h]	3[h]	4[h]	5[h]	6[h]	7[h]	8[h]	9[h]	A[h]	B[h]
	510H CCD						760H CCD					
	NTSC			PAL			NTSC			PAL		
0[h] : INT	○	○	○	○	▲	○	○	○	○	○	▲	○
1[h] : LL	×	○	○	×	▲	○	×	×	○	×	▲	○
2[h] : VSL	▲	○	○	▲	○	○	×	×	○	×	○	○
3[h] : VBSLHP	-	▲	-	-	▲	-	×	×	-	-	▲	-
4[h] : VBSLHR	-	-	-	-	-	-	○	○	-	-	-	-
5[h] : VRHR	○	○	○	○	▲	○	○	○	○	○	▲	○
A[h] : VSL-S	▲	○	○	▲	○	○	×	×	○	×	○	○
F[h] : VSL-D	▲	○	○	▲	○	○	×	×	○	×	○	○

○ : No noise effects
▲ : Noise appears in AGC area
× : Severe noise effects
- : Outside specified range

* For details on MODESEL settings, see “6.CCD Type Selection.”
For information on noise countermeasures, see “3.6 Noise Countermeasures” in the application.

13.2. Operation Mode Control during Digital Output

Only a limited number of operation mode (MODESEL) and external synchronization mode (SGMODE) settings can be used during digital output from the SS-HQ1. Digital output under settings other than those in the following table is not supported.

Table 13.2-1 Operation Mode Control during Digital Output

MODESEL / SGMODE	0[h]	1[h]	2[h]	3[h]	4[h]	5[h]	6[h]	7[h]	8[h]	9[h]	A[h]	B[h]
	510H CCD						760H CCD					
	NTSC			PAL			NTSC			PAL		
0[h] : INT	○	×	×	○	×	×	○	○	×	○	×	×

○ : Can be used
× : Cannot be used

* External synchronization is not supported during digital output. Therefore, SGMODE must be set to 0[h] (SGMODE=0[h]) during digital output.

13.3. Tables: The parameters controlled by FW

CAT1 SYSTEM

Byte, bit	Parameter	FW control timing	Control methods (Except CPUHOLD=1)
Byte1_bit0	NTPAL	Reset	These parameters are controlled by MODESEL.. Please do not change parameters controlled by FW.
Byte1_bit2	CCDTYPE		
Byte3_bit0,1	ENCMODE		
Byte3_bit4-5	TGCKSEL	Every field	These parameters are controlled by SGMODE.. Please do not change parameters controlled by FW.
Byte3_6-7	INTLCKSEL	Reset	These parameters are controlled by MODESEL.. Please do not change parameters controlled by FW.
Byte4_6-7	DIFCKSEL		
Byte7_bit6	S0IN	Every field	SGHOLD(CAT12_Byte5_bit4)=1[h] or SSELOFF(CAT12_Byte12_bit5)=1[h]
Byte7_bit7	S1IN		
Byte8_bit0-2	S2SEL		
Byte8_bit3-5	S3SEL		
Byte8_bit6,7	S4SEL		
Byte11_bit1	PLLSTB		SGHOLD(CAT12_Byte5_bit4)=1[h]
Byte12_bit2	YDACCKSEL	Every field	These parameters are controlled by SGMODE.. Please do not change parameters controlled by FW.

CAT2 PICT1

Byte, bit	Parameter	FW control timing	Control methods (Except CPUHOLD=1)
Byte4_bit2-5	VHAPG	Every field	VHAPGCTL(CAT12_Byte8_bit0)=1[h]
Byte6_bit7	YGAMSON		GAMCTL(CAT12_Byte9_bit0)=1[h]
Byte7_bit0	YGAMSLV		
Byte7_bit1	YGAMSMTH		
Byte7_bit2-4	YGAMSEL		
Byte7_bit5-7	YKNEESEL		
Byte8	YGAIN		YGAINCTL(CAT12_Byte8_bit3)=1[h]
Byte10_bit0-5	SETUP		SETUPCTL(CAT12_Byte8_bit7)=1[h]
Byte11_bit1-4	YDLY		YDLYOFF(CAT12_Byte13_bit0)=1[h]
Byte29_bit6	CKNEE2		GAMCTL(CAT12_Byte9_bit0)=1[h]
Byte30_bit0-2	CGAMMA		
Byte30_bit3,4	CKNCLIP		
Byte30_bit5-7	CKNEE		
Byte31	RMATY		RGBMATCTL(CAT12_Byte8_bit1)=1[h]
Byte32	RMATC		
Byte33	BMATY		
Byte34	BMATC		
Byte35	GMATCR		
Byte36	GMATCB		
Byte37	RYGAIN1		CRGAINCTL(CAT12_Byte8_bit2)=1[h]
Byte38	BYGAIN1		
Byte39	RYHUE1		HUECTL(CAT12_Byte8_bit4)=1[h]
Byte40	BYHUE1		
Byte41	RYGAIN2		CRGAINCTL(CAT12_Byte8_bit2)=1[h]
Byte42	BYGAIN2		
Byte43	RYHUE2		HUECTL(CAT12_Byte8_bit4)=1[h]
Byte44	BYHUE2		
Byte45	RYGAIN3		CRGAINCTL(CAT12_Byte8_bit2)=1[h]
Byte46	BYGAIN3		
Byte47	RYHUE3		HUECTL(CAT12_Byte8_bit4)=1[h]
Byte48	BYHUE3		

Byte49	RYGAIN4		CRGAINCTL(CAT12_Byte8_bit2)=1[h]
Byte50	BYGAIN4		
Byte51	RYHUE4		HUECTL(CAT12_Byte8_bit4)=1[h]
Byte52	BYHUE4		
Byte54_bit0	6DBDWN		AWBHOLD(CAT12_Byte5_bit1)=1[h] or The setting value of U6DBDWN is reflected, when AWBHOLD is 1[h] and CRLESS_ON(CAT12_Byte11_bit0) is 1[h].
Byte55	BLACKS1		CLMPHOLD(CAT12_Byte5_bit3)=1[h]
Byte56	BLACKS2		
Byte57	LGS1R		LVBGCTL(CAT12_Byte8_bit5)=1[h]
Byte58	LGS2R		
Byte59	LGS1B		
Byte60	LGS2B		
Byte61	YLGS1R		YLBGCTL(CAT12_Byte8_bit6)=1[h]
Byte62	YLGS2R		
Byte63	YLGS1B		
Byte64	YLGS2B		

CAT4 AWB1

Byte, bit	Parameter	FW control timing	Control methods (Except CPUHOLD=1)
Byte1	WBR	Every field	AWBHOLD(CAT12_Byte5_bit1)=1[h]
Byte2	WBG	Reset	AWBHOLD(CAT12_Byte5_bit1) = 1[h] or Set the GGAIN(CAT15_Byte4).
Byte3	WBB	Every field	AWBHOLD(CAT12_Byte5_bit1)=1[h]
Byte6	WBYUP		
Byte7	WBYDWN		

CAT5 OPDWND1

Byte, bit	Parameter	FW control timing	Control methods (CPUHOLD=1 以外)
Byte1-8	Fix	Every field	Please do not change parameters controlled by FW.

CAT6 TG

Byte, bit	Parameter	FW control timing	Control methods (Except CPUHOLD=1)
Byte1_bit1	SHUT	Every field	AEHOLD(CAT12_Byte5_bit2)=1[h]
Byte2_bit0-3	ODSGV		
Byte2_bit4-7	EVSGV		
Byte3_bit0-6	ODSGH		
Byte4_bit0-6	EVSGH		
Byte6	ODSUBVL		
Byte7	EVSUBVL		
Byte8_bit0,1	ODSUBVM		
Byte8_bit2,3	EVSUBVM		

CAT7 EXTSYNC1

Byte, bit	Parameter	FW control timing	Control methods (Except CPUHOLD=1)
Byte1_bit0	INTEXT	Every field	These parameters are controlled by SGMODE.. Please do not change parameters controlled by FW.
Byte1_bit1	HVPLL		
Byte1_bit2	SYNCEX		
Byte1_bit3	HRSTON		

Byte1_bit4	VRSTON		
Byte1_bit5	BCMPON		
Byte1_bit6	INT60		
Byte1_bit7	SG27	Reset	These parameters are controlled by MODESEL. Please do not change parameters controlled by FW.
Byte3	SFTHL	Every field	SGHOLD(CAT12_Byte5_bit4)=1[h]
Byte4	SFTVL		
Byte5_bit0,1	SFTHM		
Byte5_bit2,3	SFTVM		
Byte11_bit0	PCMPSEP	Every field	These parameters are controlled by SGMODE.. Please do not change parameters controlled by FW.
Byte11_bit1	SSEPEXT		

CAT8 FEADJ(EVRI)

Byte, bit	Parameter	FW control timing	Control methods (Except CPUHOLD=1)
Byte3	AGCCNT	Every field	AEHOLD(CAT12_Byte5_bit2)=1[h]
Byte4	IRISVCNT		If you set AEHOLD(CAT12_Byte5_bit2) to 1[h] and MIRIS(CAT14_Byte1_bit1) to 0[h], the setting value can be changed.

CAT10 DIF

Byte, bit	Parameter	FW control timing	Control methods (Except CPUHOLD=1)
Byte1_bit1	DIF27	Reset	These parameters are controlled by SGMODE.. Please do not change parameters controlled by FW.

CAT11 BLMDETS1

Byte, bit	Parameter	FW control timing	Control methods (Except CPUHOLD=1)
Byte10	IBLKS1L	Every field	CLMPHOLD(CAT12_Byte5_bit3)=1[h]
Byte11	IBLKS2L		
Byte12_bit0	IBLKS1M		
Byte12_bit1	IBLKS2M		

SS-HQ1 Application Notes Not for sale

Jan/ 2005 Ver. 1.0.0

Editor and Publisher:
Sony Corporation
Semiconductor Solutions Network Company