STMP35XX Reference Schematics

Revision History

REV. A - 3/3/03

Original Release

REV. B - 8/20/03

Added Switched USB Jack 3500 page

Added 35XX 1-Channel Buck page

Edited boot mode tables.

Updated the Buck mode Play/Pswitch circuit to prevent excessive current being injected into the Pswitch pin.

Added Optional Line-In circuit to Optional Circuits Page.

Removed TEA5757 FM Tuner.

Removed 35XX 144QFP information.

Added Panasonic BTF-03 FM Tuner page.

Removed C115 and C116, optional ESD caps on USB D+ and D-.

Removed R139, NOPOP resistor shorting VDDIO to VDDIO_P.

Changed LED drive to match 3410 Rev. G schematics (and keep the same polarity as 3410 SDK LEDs).

Changed the value of resistors to PSwitch from 47K to 20K.

Added pull-up resistors on MMC socket pins 8 and 9.

Added optional 16-bit NAND support.

Updated Boot Mode tables.

Removed SmartMedia circuit.

Changed default TEA5767 FM Tuner connections as follows:

FM_DATA changed from GPIO_19 to I2C_DATA
FM_CLOCK changed from GPIO_18 to I2C_CLK
SWP1 changed from I2C_CLK to GPIO_33

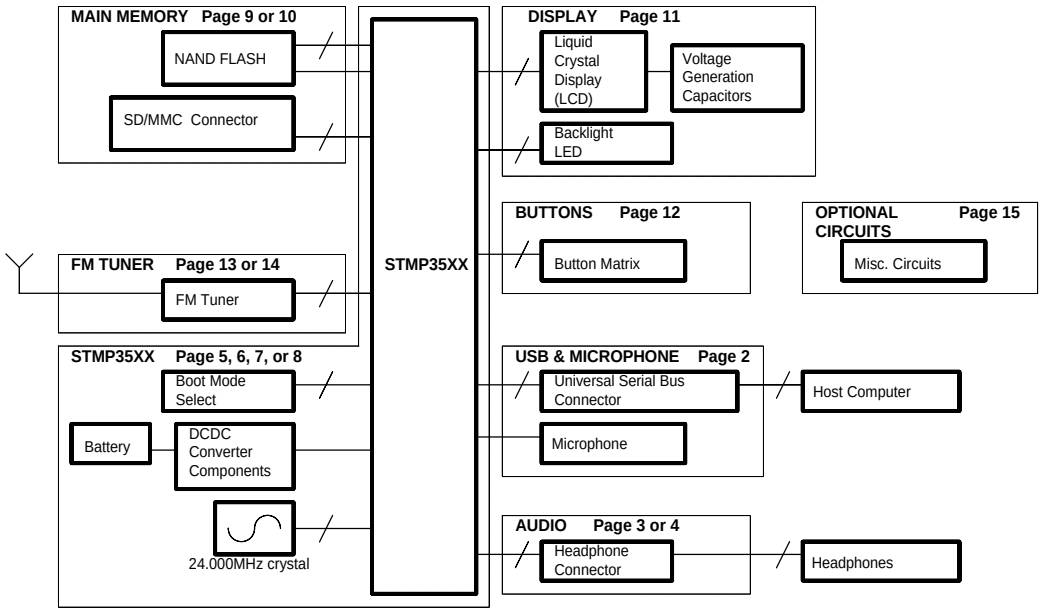
Added SW24 (Reset Button) option to STMP35XX pages.

Removed 1K pull-up to VDDIO on the Hold Switch.

NOTE: These schematics are preliminary and are subject to change.

Block Diagram

Rev. B



To use these schematics to create a design:

1) Select USB and Microphone options on "USB & MICROPHONE" page	
2) Select one of the audio pages:	100QFP STMP35XX Audio Options 144BGA STMP35XX Audio Options
3) Select one of the STMP35XX pages:	STMP35XX 100-TQFP Boost Mode STMP35XX 100-TQFP Single Channel Buck Mode STMP35XX 144-BGA Dual Channel Buck Mode STMP35XX USB Shared Jack Boost Mode
4) Select one of the "Memory" pages:	NAND flash only MMC + NAND flash
5) Select options on the "Display" page as required.	
6) Select options on the "Buttons" page as required.	
7) If required, select one of the "FM Tuner" pages.	
8) If required, select any of the circuits on the "Optional Circuits" page.	

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USB 2.0 Connector

Route USB D+ and D- according to the High Speed USB2.0 Design Guidelines.

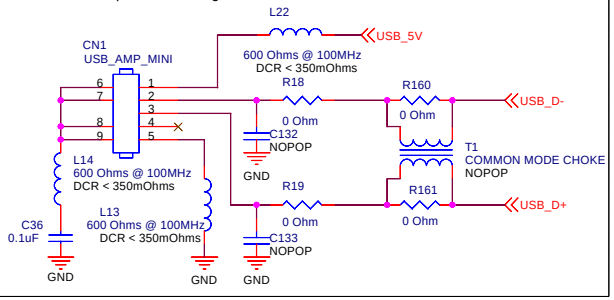
D+ and D- should have a 90 ohm differential trace impedance.

Use 20 mil minimum spacing between D+ and D- and other signal lines.

In order to maximize ESD immunity, the industrial design plastics should expose the USB Connector as little as possible.

L13 and L14 are placeholders for optional ferrites that can be populated for ESD immunity if necessary. If they are not required, populate a 0 ohm resistor.

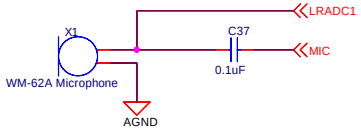
CN1 Pins 6-9 are pins connecting to the USB connector outer shield



Microphone Bias Options

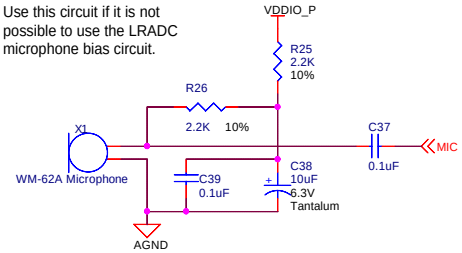
OPTION 1: Microphone using LRADC1 MIC_BIAS

Note: If the LRADC1 line is unavailable, LRADC2 may be used for the Microphone Bias. If both LRADC1 and LRADC2 are unavailable, use OPTION 2.



OPTION 2: Microphone using VDDIO bias

Use this circuit if it is not possible to use the LRADC microphone bias circuit.



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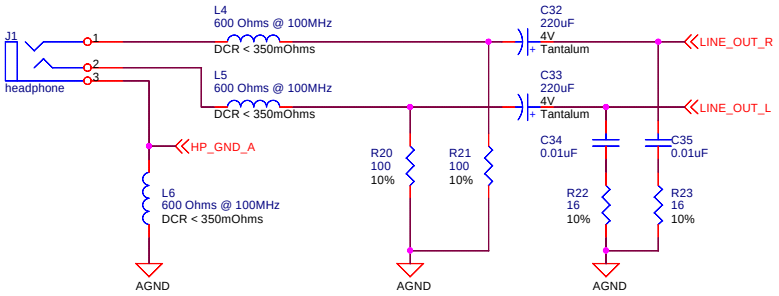
100QFP STMP35XX AUDIO OPTIONS

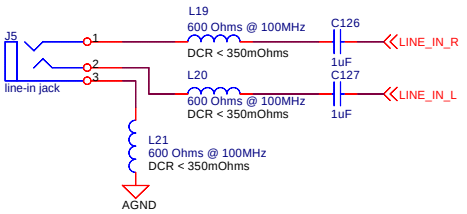
For a design using a 100QFP with an FM Tuner or Line-In Jack:

AC-Coupled Headphone Jack



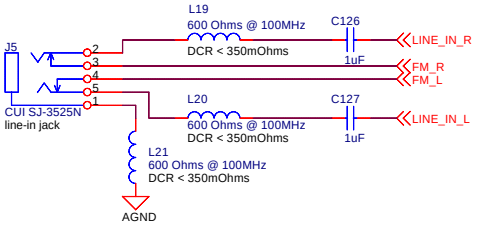
NOTE: HP_GND_A is the antenna for designs with an FM Tuner

OPTION 1: LINE-IN CIRCUIT ONLY



OPTION 3: FM TUNER ONLY

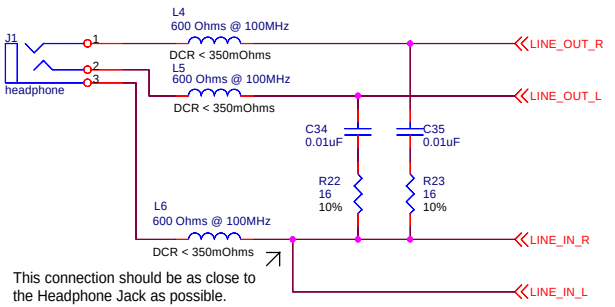
OPTION 2: LINE-IN JACK + FM TUNER



For the 100 Pin QFP package, only one set of LINE IN inputs are available. If a LINE-IN Jack and an FM Tuner are both included in the design, they will need to share the LINE-IN input. This circuit uses a switched audio jack to switch between LINE-IN and FM Tuner. When nothing is plugged into the jack, the FM Tuner is connect to the LINE-IN inputs. When a plug is inserted, the FM Tuner will be disconnect.

For a design using a 100QFP with no FM Tuner or Line-In Jack:

Direct Drive Headphone Jack



This connection should be as close to the Headphone Jack as possible.

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Page: 100QFP AUDIO OPTIONS

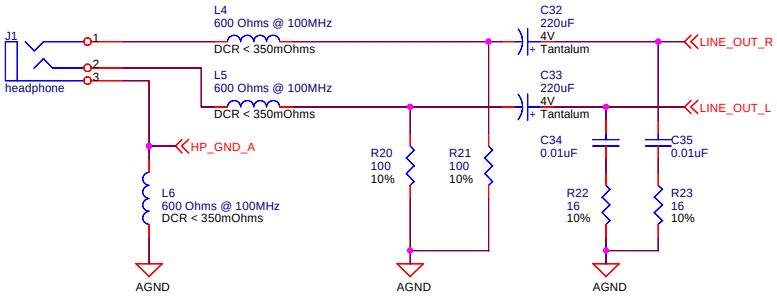
Size B

Rev B

144BGA STMP35XX AUDIO OPTIONS

For a design using a 144BGA with FM TUNER and Line-In Jack :

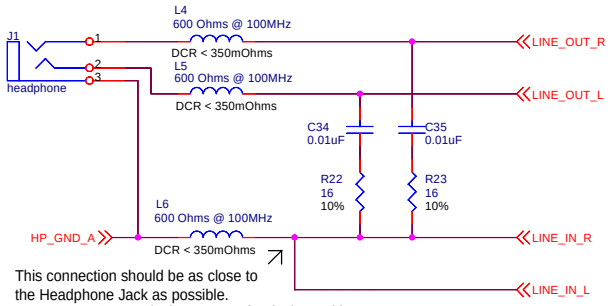
AC-Coupled Headphone Jack



NOTE: HP_GND_A is the antenna for designs with an FM Tuner

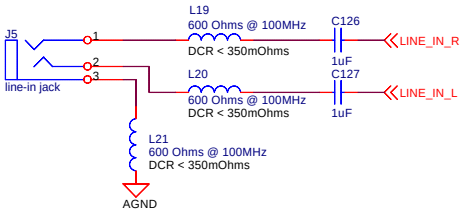
OR

Direct Drive Headphone Jack



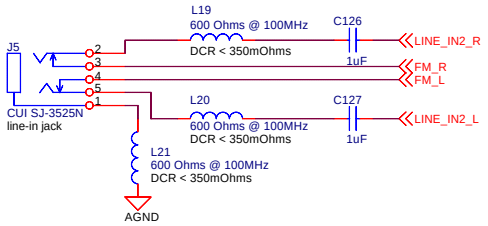
This connection should be as close to the Headphone Jack as possible.
NOTE: HP_GND_A is the antenna for designs with an FM Tuner

LINE-IN CIRCUIT



FM TUNER

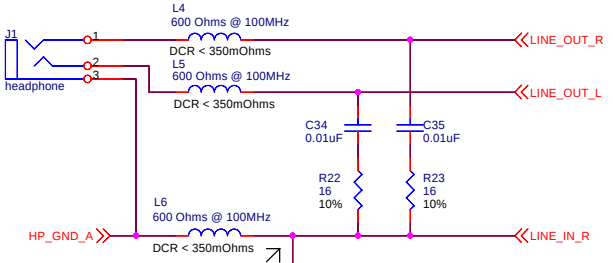
LINE-IN JACK + FM TUNER



If a LINE-IN Jack and an FM Tuner are both included in the design, they will need to share the LINE-IN input. This circuit uses a switched audio jack to switch between LINE-IN and FM Tuner. When nothing is plugged into the jack, the FM Tuner is connect to the LINE-IN inputs. When a plug is inserted, the FM Tuner will be disconnect.

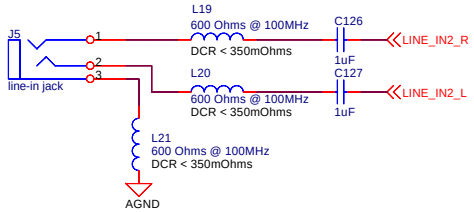
For a design using a 144BGA with FM Tuner or Line-In Jack:

Direct Drive Headphone Jack



This connection should be as close to the Headphone Jack as possible.
NOTE: HP_GND_A is the antenna for designs with an FM Tuner

OPTION 1: LINE-IN CIRCUIT ONLY



OPTION 2: FM TUNER ONLY

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Page: 144BGA AUDIO OPTIONS

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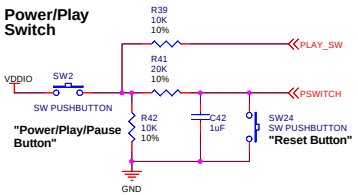
STMP35XX 100-Pin TQFP - BOOST MODE

This circuit shows the STMP35XX in a NiMH or 1.5V Alkaline boost-mode configuration. For the NiMH case, the battery may be charged using USB_5V as a source. The charge current will be delivered through the DCDC_BATT pin. Care must be taken in the design to ensure that the user may not charge an alkaline battery.

Power/Play Switch



Note: For players with a non-removeable battery (i.e. rechargeable), it may be necessary to include switch SW24 (Reset) to allow the user to enter Player Recovery Mode. For players with a removeable battery (i.e. alkaline), this switch is not necessary.

IMPORTANT DESIGN NOTES

The D14 diode may be required for battery charge applications.

The L2 inductor is a critical component - for best battery life, L2 should be a quality, low-ESR inductor. The Panasonic ELL6H inductor or equivalent is recommended for this component.

The industrial design plastics should mechanically prevent a battery accidentally inserted backwards from making contact with the battery terminals.

Route VDD_BAT as a 30mil trace from the positive battery terminal to the L2 inductor, and from the L2 inductor to the STMP35XX DCDC_BATT pin.

Route GND back to the battery negative terminal as either a 30mil trace or as part of a wide digital ground plane

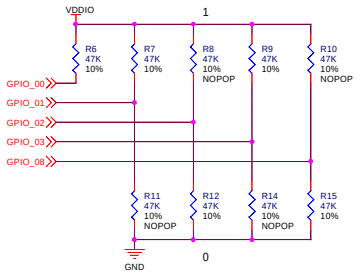
STMP35XX BOOT MODE SELECT

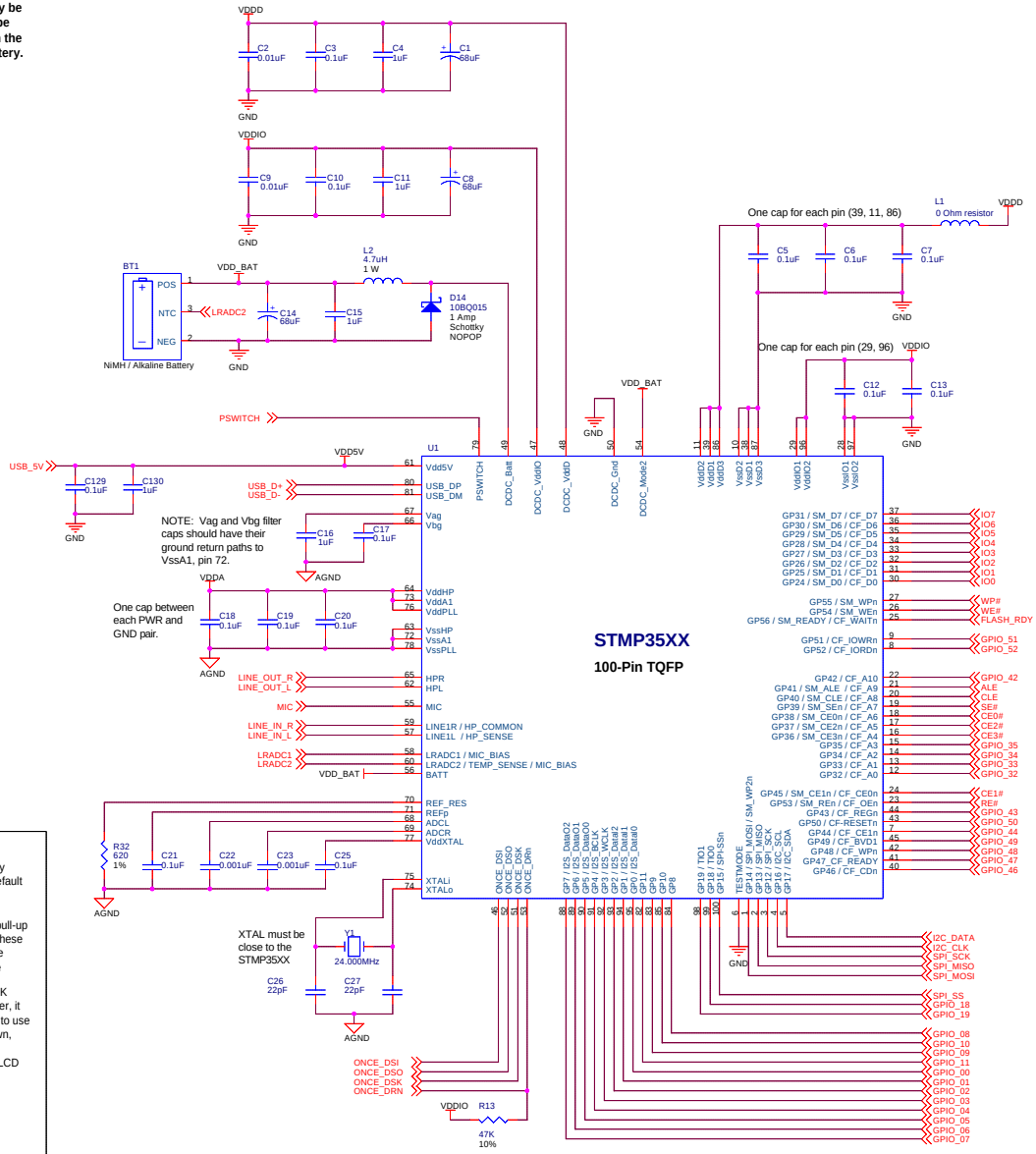
BOOT MODE	GPIO 00	01	02	03	08
3.3V NAND w/Play Recovery	1	1	0	1	0
3.3V NAND w/PSwitch Recovery	1	1	0	1	1
1.8V NAND w/Play Recovery	1	1	0	0	0
1.8V NAND w/PSwitch Recovery	1	1	0	0	1
SPI Master	1	0	1	0	1
SPI Slave	1	0	1	1	1
I2C Master	1	0	1	1	0
I2C Slave	1	0	0	1	1
USB	1	0	0	1	0

3.3V NAND w/ Play Recovery is the Default Boot Mode.

Populate either a pull-up or a pull-down on these GPIOs to select the desired Boot Mode

All resistors are 47K RES0603. However, it may be necessary to use a stronger pull-down, such as a 10K, depending on the LCD used.

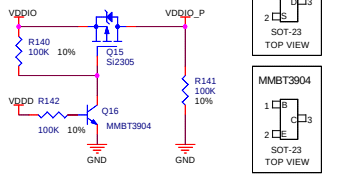




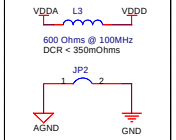
VDDIO_P Power Switch

This circuitry creates a VDDIO_P for peripheral devices. When the player is powered-down, VDDIO_P will drop to GND. This allows peripheral devices to receive a power-on reset, since VDDIO drops to the battery voltage when the player is powered down.

The PFET used in this circuit should have an Rds,on less than 2 ohms when Vgs = -2.8V. A good choice is an Si2305 transistor or equivalent.



GROUNDING & POWER



Tie all grounds together under the IC

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Title: **STMP35XX Reference Schematics**

Page: STMP35XX 100-Pin TQFP - Boost Mode

Size C

Rev B

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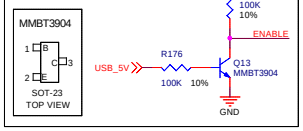
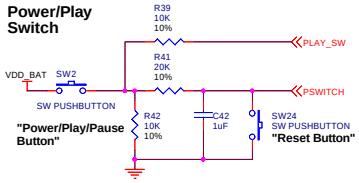
STMP35XX 100-Pin TQFP - 1 CHANNEL BUCK MODE

This circuit shows STMP35XX in a Li-Ion single buck-mode configuration. This schematic assumes a Li-Ion battery voltage of 3.0V to 4.2V. The Li-Ion battery will be recharged using USB_5V as a source, with the constant current charge current being delivered through the BATT pin.

Regulator Enable Circuit



Power/Play Switch



Note: For players with a non-removeable battery (i.e. rechargeable), it may be necessary to include switch SW24 (Reset) to allow the user to enter Player Recovery Mode. For players with a removeable battery (i.e. alkaline), this switch is not necessary.

IMPORTANT DESIGN NOTES

The L2 inductor is a critical component - for best battery life, L2 should be a quality, low-ESR inductor. The Panasonic ELL6H inductor or equivalent is recommended for this component.

The industrial design plastics should mechanically prevent a battery accidentally inserted backwards from making contact with the battery terminals.

Route VDD_BAT as a 30mil trace from the positive battery terminal to the STMP35XX input.

Route GND back to the battery negative terminal as either a 30mil trace or as part of a wide digital ground plane

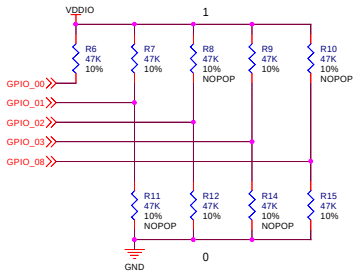
STMP35XX BOOT MODE SELECT

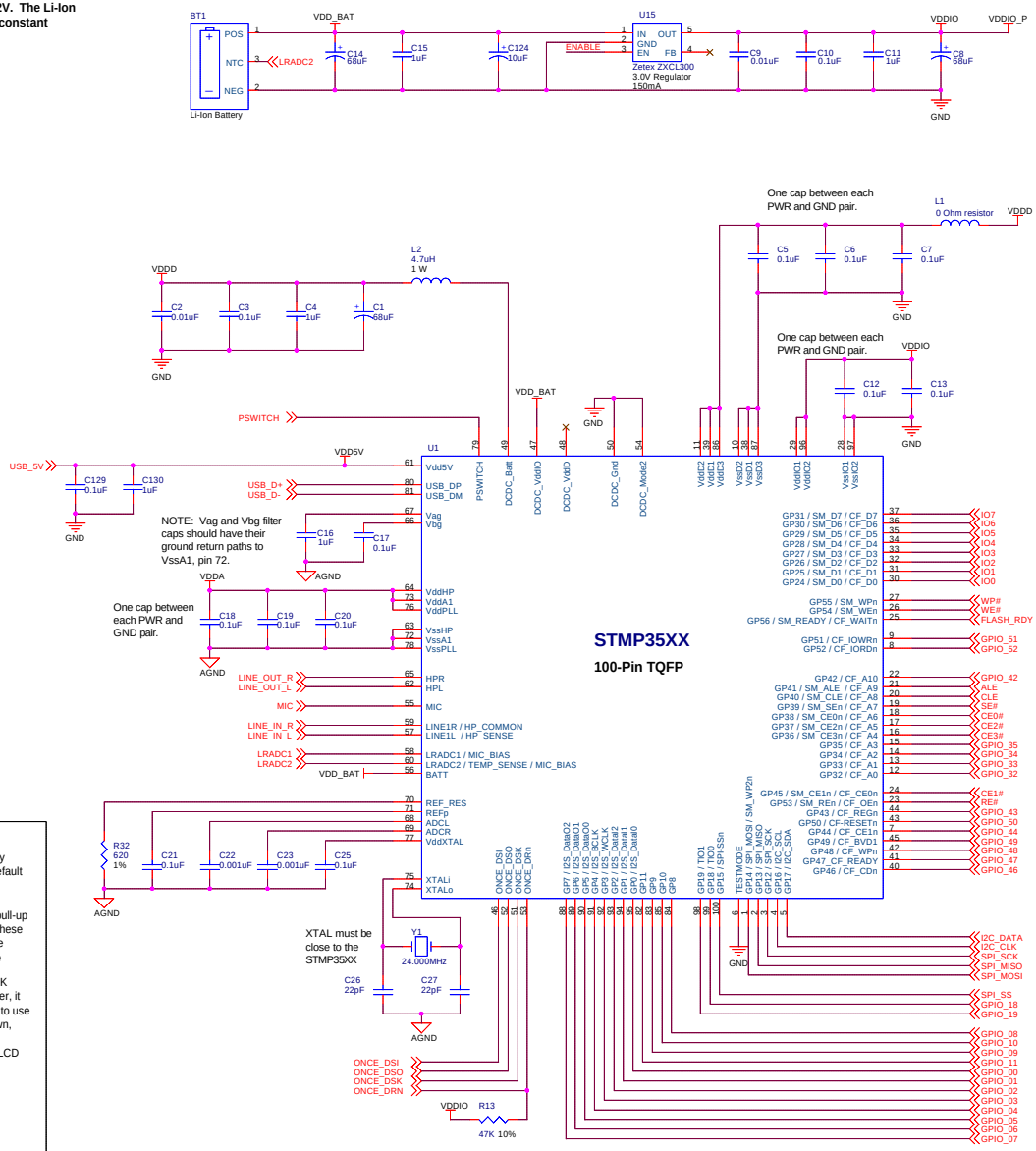
BOOT MODE	GPIO 00	01	02	03	08
3.3V NAND w/Play Recovery	1	1	0	1	0
3.3V NAND w/PSwitch Recovery	1	1	0	1	1
1.8V NAND w/Play Recovery	1	1	0	0	0
1.8V NAND w/PSwitch Recovery	1	1	0	0	1
SPI Master	1	0	1	0	1
SPI Slave	1	0	1	1	1
I2C Master	1	0	1	1	0
I2C Slave	1	0	0	1	1
USB	1	0	0	1	0

3.3V NAND w/ Play Recovery is the Default Boot Mode.

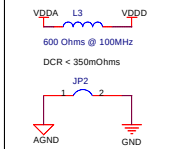
Populate either a pull-up or a pull-down on these GPIOs to select the desired Boot Mode

All resistors are 47K RES0603. However, it may be necessary to use a stronger pull-down, such as a 10K, depending on the LCD used.





GROUNDING & POWER



Tie all grounds together under the IC

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Title	**STMP35XX Reference Schematics**
Page	STMP35XX 100-Pin TQFP - 1 Channel Buck Mode
Size C	This design is the property of SigmaTel, Inc. It is offered on an "as is" basis, and carries no implied warranty. Rev B
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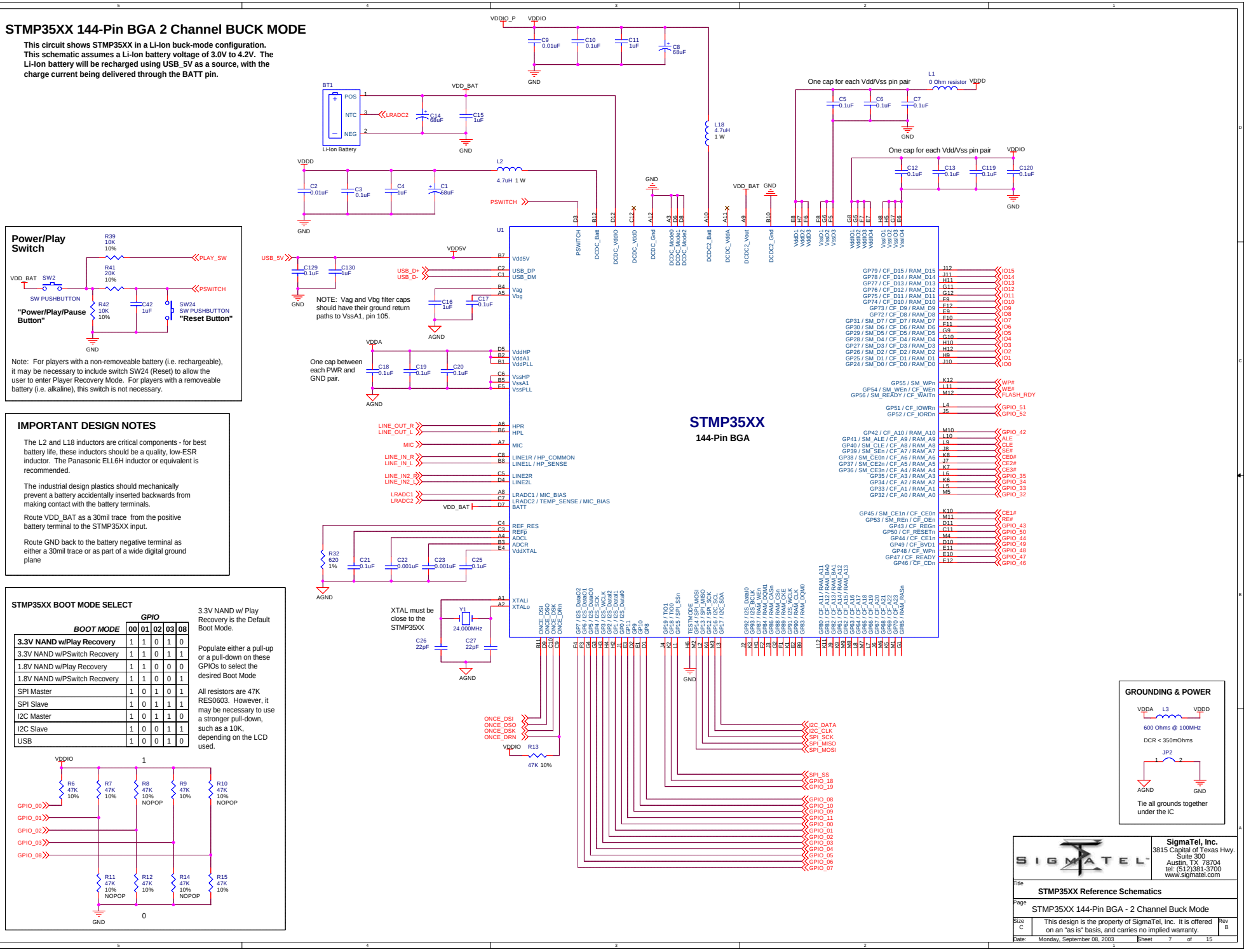
STMP35XX 144-Pin BGA 2 Channel BUCK MODE

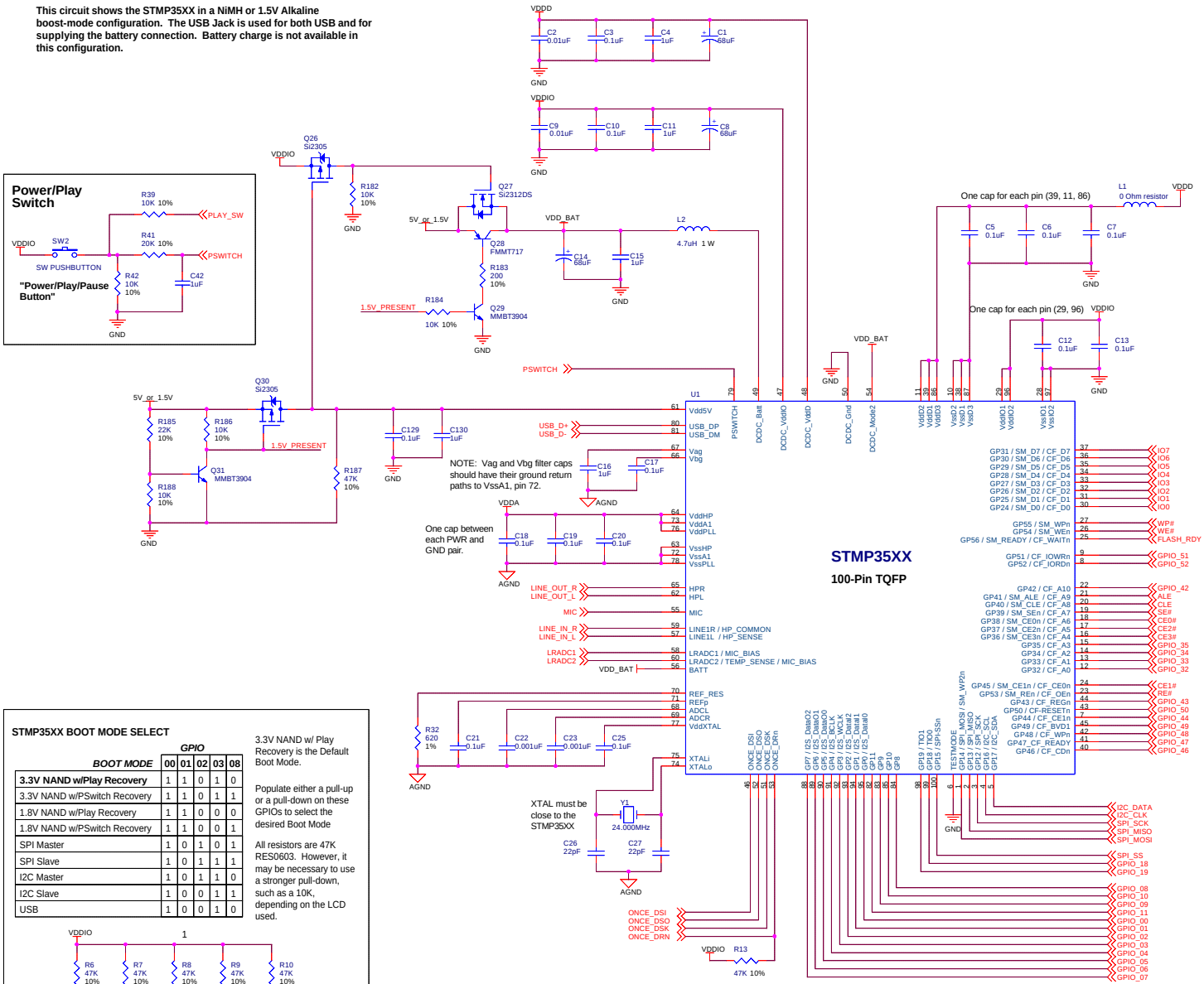
This circuit shows STMP35XX in a Li-Ion buck-mode configuration. This schematic assumes a Li-Ion battery voltage of 3.0V to 4.2V. The Li-Ion battery will be recharged using USB_5V as a source, with the charge current being delivered through the BATT pin.



BOOT MODE	00	01	02	03	08
3.3V NAND w/Play Recovery	1	1	0	1	0
3.3V NAND w/PSwitch Recovery	1	1	0	1	1
1.8V NAND w/Play Recovery	1	1	0	0	0
1.8V NAND w/PSwitch Recovery	1	1	0	0	1
SPI Master	1	0	1	0	1
SPI Slave	1	0	1	1	1
I2C Master	1	0	1	1	0
I2C Slave	1	0	0	1	1
USB	1	0	0	1	0

STMP35XX 100-Pin TQFP - Switched USB Jack - BOOST MODE

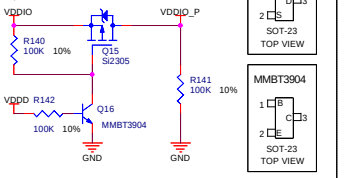
This circuit shows the STMP35XX in a NiMH or 1.5V Alkaline boost-mode configuration. The USB Jack is used for both USB and for supplying the battery connection. Battery charge is not available in this configuration.



VDDIO_P Power Switch

This circuitry creates a VDDIO_P for peripheral devices. When the player is powered-down, VDDIO_P will drop to GND. This allows peripheral devices to receive a power-on reset, since VDDIO drops to the battery voltage when the player is powered down.

The PFET used in this circuit should have an Rds,on less than 2 ohms when Vgs = -2.8V. A good choice is an Si2305 transistor or equivalent.



IMPORTANT DESIGN NOTES

The PFET used Q26 and Q30 in this circuit should have an Rds,on less than 2 ohms when Vgs = -2.8V. A good choice is an Si2305 transistor or equivalent.

The PNP transistor used for Q28 should have low Vce,sat characteristics. When the power button is pressed, the transistor base current will be about 1mA when the 5V_or_1.5V power rail is .9V. At this point, the STMP35XX will begin to start up and VDD_BAT will require about 35mA, which will be the current flowing through the collector of the FMMT717 transistor. Given 35mA of collector current and 1mA base current, the Vce,sat of the FMMT717 transistor will be about 12mV. Because the voltage on the PSWITCH pin must also be > 900mV during startup, the battery voltage required for startup using the FMMT717 transistor will be about 912mV. Similarly, the battery voltage required for startup using a FMMT591A transistor will be about 940mV. If a PNP transistor with higher Vce,sat. characteristics is used, such as the MMBT3906, the startup voltage will be 1.05V or higher. Please consult the transistor datasheet.

The NFET used for Q27 should have characteristics similar to the Si2312DS N-channel mosfet. The minimum gate threshold voltage must be 1.2V or less. The most important characteristic of this mosfet is the Rds,on for a given Vgs. The Rds,on should be 0.06 ohms or less when Vgs = 1.8V. Using a mosfet with higher Rds,on characteristics may decrease battery life.

The L2 inductor is a critical component - for best battery life, L2 should be a quality, low-ESR inductor. The Panasonic ELL6H inductor or equivalent is recommended for this component.

Route VDD_BAT as a 30mil trace from the positive battery terminal to the STMP35XX input.

Route GND back to the battery negative terminal as either a 30mil trace or as part of a wide digital ground plane

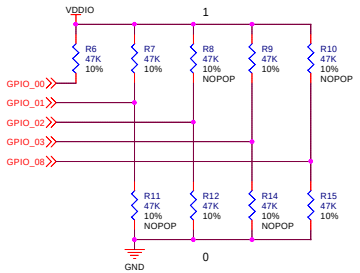
STMP35XX BOOT MODE SELECT

BOOT MODE	GPIO 00	01	02	03	08
3.3V NAND w/Play Recovery	1	1	0	1	0
3.3V NAND w/PSwitch Recovery	1	1	0	1	1
1.8V NAND w/Play Recovery	1	1	0	0	0
1.8V NAND w/PSwitch Recovery	1	1	0	0	1
SPI Master	1	0	1	0	1
SPI Slave	1	0	1	1	1
I2C Master	1	0	1	1	0
I2C Slave	1	0	0	1	1
USB	1	0	0	1	0

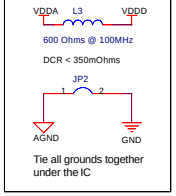
3.3V NAND w/ Play Recovery is the Default Boot Mode.

Populate either a pull-up or a pull-down on these GPIOs to select the desired Boot Mode

All resistors are 47K RES0603. However, it may be necessary to use a stronger pull-down, such as a 10K, depending on the LCD used.



GROUNDING & POWER



Tie all grounds together under the IC

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Title	**STMP35XX Reference Schematics**
Page	STMP35XX 100-Pin TQFP - Boost Mode
Size C	This design is the property of SigmaTel, Inc. It is offered on an "as is" basis, and carries no implied warranty. Rev B
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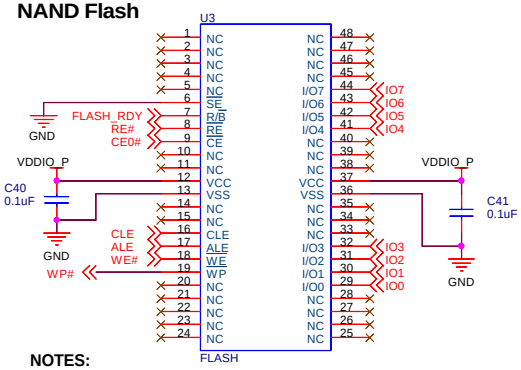
NAND Flash



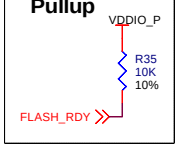
NOTES:

1. The WP# pull-down resistor is required to protect the flash memory from inadvertent writes during power transitions.

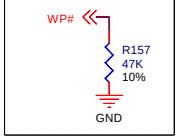
2. The CE# pull-up resistor is required to keep the flash de-selected during power transitions.

3. A pull-up resistor is required on the FLASH_RDY signal because the flash output is open drain.

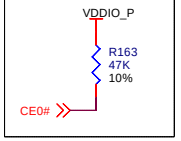
FLASH_RDY Pullup



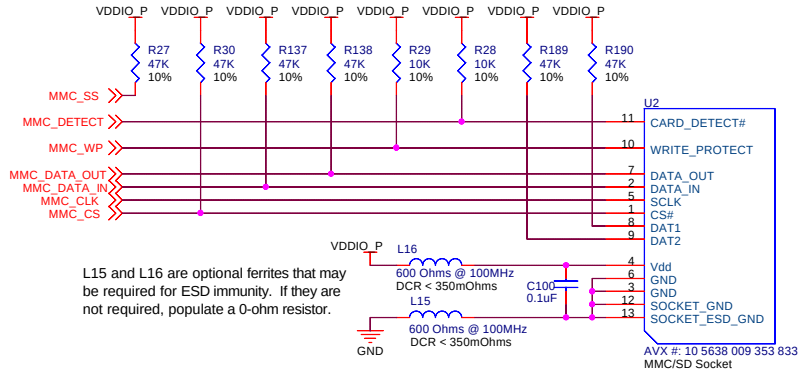
WP# Pulldown



CE0# Pullup

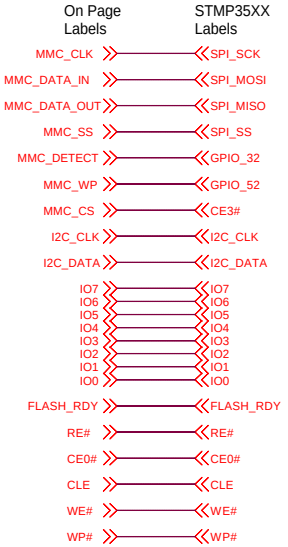


MultiMedia Card Socket

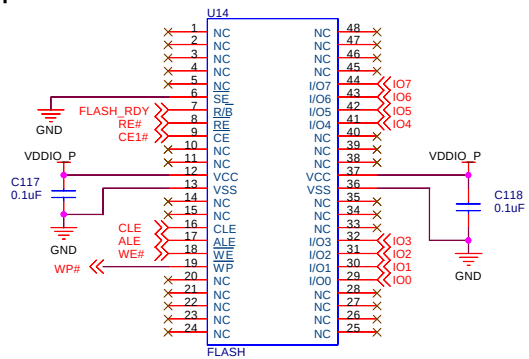


L15 and L16 are optional ferrites that may be required for ESD immunity. If they are not required, populate a 0-ohm resistor.

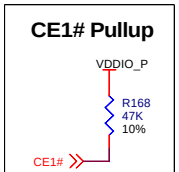
Integration



Optional Second NAND Flash



CE1# Pullup



NOTES:

1. The CE# pull-up resistor is required to keep the flash de-selected during power transitions.

STMP35XX CHIP ENABLE ASSIGNMENT

If using more than one NAND chip, the first chip MUST be attached to CE0#, the second MUST be attached to CE1#, and the third MUST be attached to CE2#. The software requires that the NAND chip enables start at CE0# and be consecutive.

If using a NAND and a MMC Card, it is recommended that the MMC Card use CE3# by default, but this is not required.

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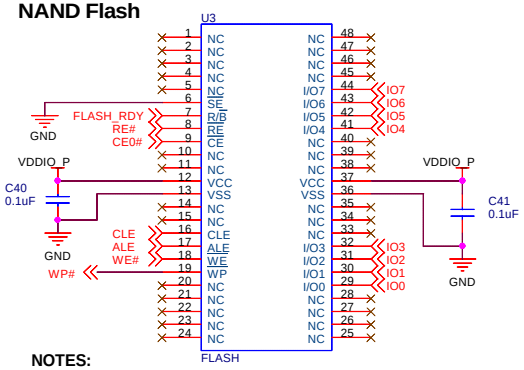
NAND Flash



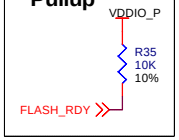
NOTES:

1. **The WP# pull-down resistor is required to protect the flash memory from inadvertent writes during power transitions.**

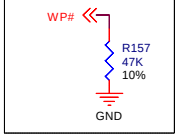
2. **The CE# pull-up resistor is required to keep the flash de-selected during power transitions.**

3. **A pull-up resistor is required on the FLASH_RDY signal because the flash output is open drain.**

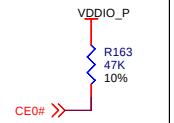
FLASH_RDY Pullup



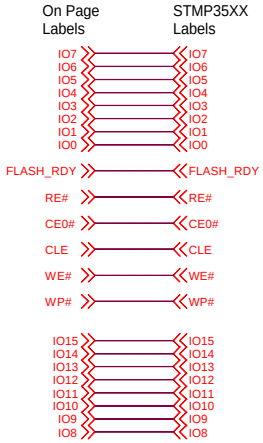
WP# Pulldown



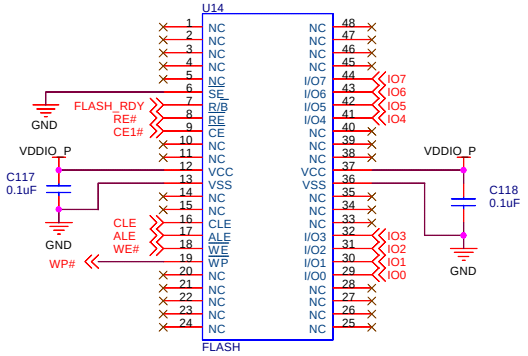
CE0# Pullup



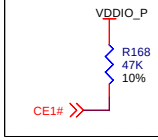
Integration



Optional Second NAND Flash



CE1# Pullup



NOTES:

1. **The CE# pull-up resistor is required to keep the flash de-selected during power transitions.**

STMP35XX CHIP ENABLE ASSIGNMENT

If using more than one NAND chip, the first chip MUST be attached to CE0#, the second MUST be attached to CE1#, and the third MUST be attached to CE2#. The software requires that the NAND chip enables start at CE0# and be consecutive.

If using a NAND and a MMC Card, it is recommended that the MMC Card use CE3# by default, but this is not required.

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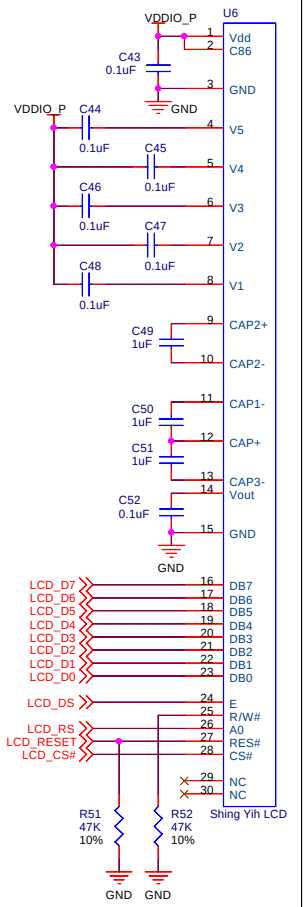
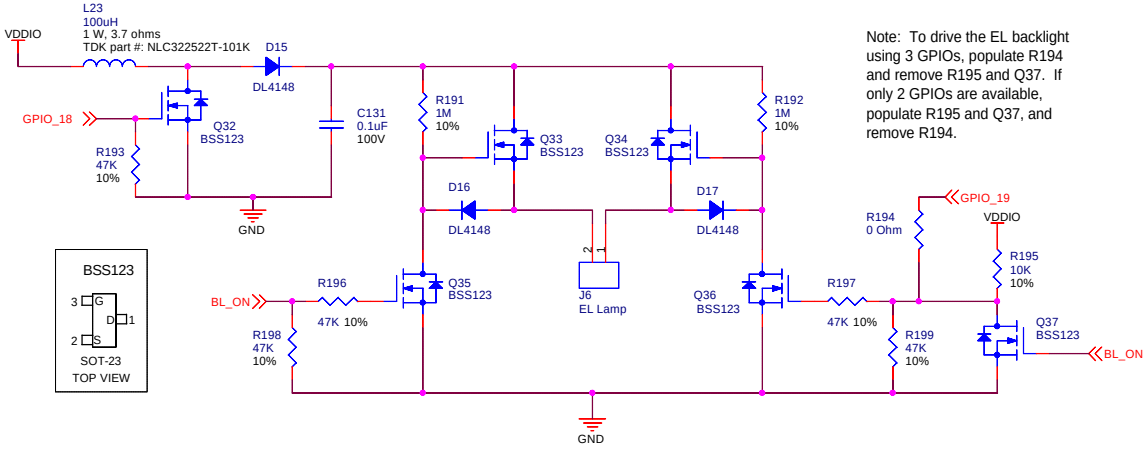
DOT-MATRIX LCD



OPTIONAL PWM EL BACKLIGHT



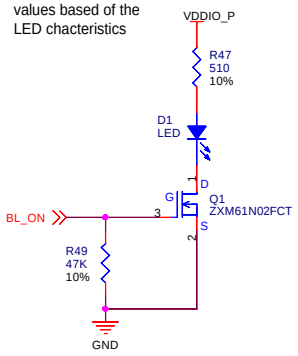
Note: To drive the EL backlight using 3 GPIOs, populate R194 and remove R195 and Q37. If only 2 GPIOs are available, populate R195 and Q37, and remove R194.

Integration

On Page Labels	STMP35XX Labels
LCD_CS#	GPIO_08
LCD_DS	GPIO_10
LCD_RS	GPIO_11
LCD_D0	GPIO_00
LCD_D1	GPIO_01
LCD_D2	GPIO_02
LCD_D3	GPIO_03
LCD_D4	GPIO_04
LCD_D5	GPIO_05
LCD_D6	GPIO_06
LCD_D7	GPIO_07
LCD_RESET	GPIO_44
BL_ON	GPIO_09
GPIO_19	GPIO_19
GPIO_18	GPIO_18

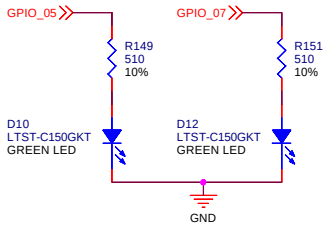
Optional LED Backlight

Size series resistor values based of the LED chacteristics



Optional LEDs

Use for LED-only players.



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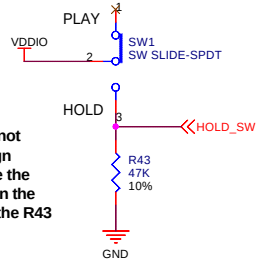
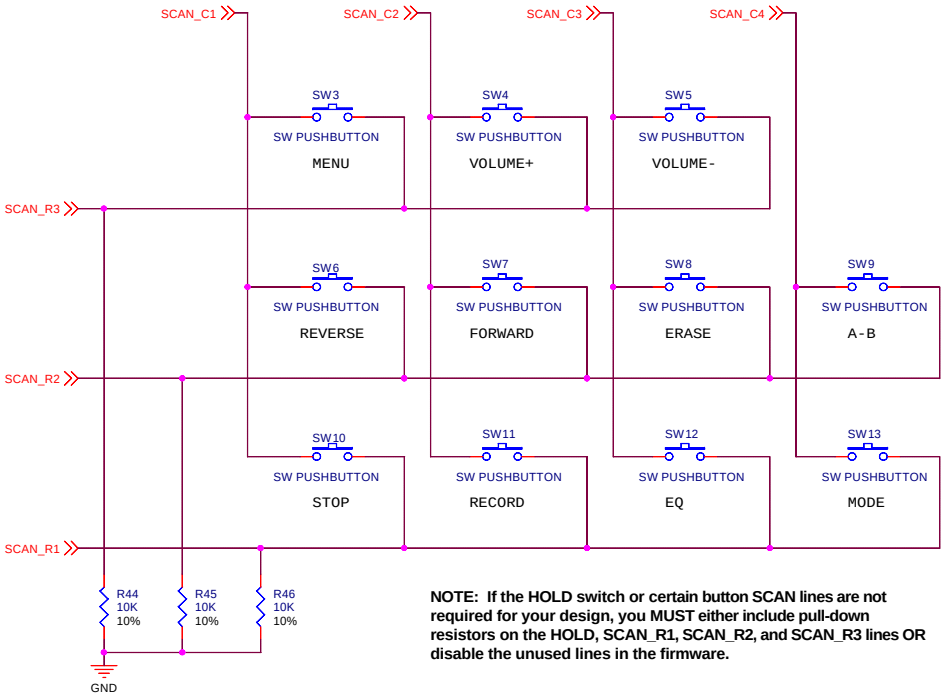
Hold Switch



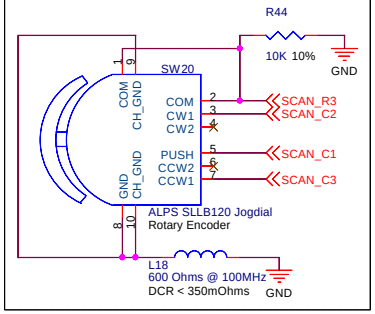
If a HOLD switch is not required, your design MUST either disable the HOLD functionality in the firmware OR leave the R43 pull-down on the HOLD_SW line.

Buttons

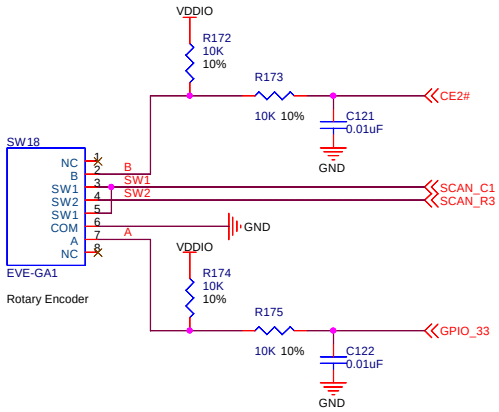


NOTE: If the HOLD switch or certain button SCAN lines are not required for your design, you MUST either include pull-down resistors on the HOLD, SCAN_R1, SCAN_R2, and SCAN_R3 lines OR disable the unused lines in the firmware.

OPTIONAL JOG DIAL



OPTIONAL ROTARY ENCODER



Integration

On Page Labels	STMP35XX Labels
PLAY_SW	GPIO_34
SCAN_C4	GPIO_42
SCAN_C3	GPIO_46
SCAN_C2	GPIO_47
SCAN_C1	GPIO_48
SCAN_R3	GPIO_50
SCAN_R2	GPIO_43
SCAN_R1	GPIO_49
PSWITCH	PSWITCH
HOLD_SW	GPIO_35

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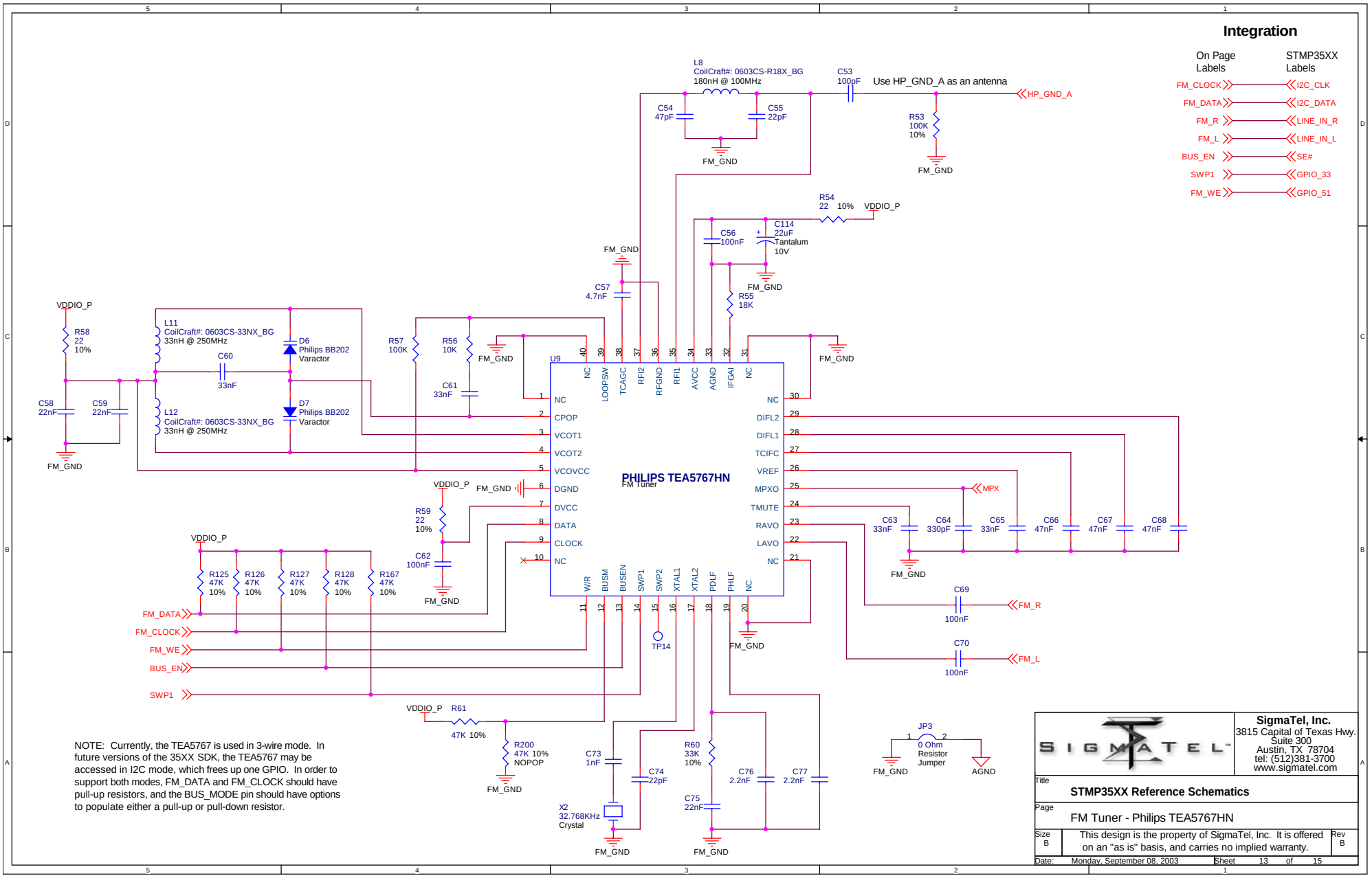
Integration
On Page Labels
STMP35XX Labels
FM_CLOCK
I2C_CLK
FM_DATA
I2C_DATA
FM_R
LINE_IN_R
FM_L
LINE_IN_L
BUS_EN
SE#
SWP1
GPIO_33
FM_WE
GPIO_51
L8
CoilCraft#: 0603CS-R18X_BG
180nH @ 100MHz
C53
100pF
Use HP_GND_A as an antenna
HP_GND_A
C54
47pF
C55
22pF
R53
100K
10%
FM_GND
R54
22
10%
VDDIO_P
C56
100nF
C114
22uF
Tantalum
10V
C57
4.7nF
R55
18K
VDDIO_P
R58
22
10%
L11
CoilCraft#: 0603CS-33NX_BG
33nH @ 250MHz
D6
Philips BB202
Varactor
C60
33nF
L12
CoilCraft#: 0603CS-33NX_BG
33nH @ 250MHz
D7
Philips BB202
Varactor
C58
22nF
C59
22nF
R57
100K
R56
10K
C61
33nF
U9
NC
LOOPSW
TCAGC
RFI2
RFGND
RFI1
AVCC
AGND
IFGAI
NC
1 NC
2 CPOP
3 VCOT1
4 VCOT2
5 VCOVCC
6 DGND
7 DVCC
8 DATA
9 CLOCK
10 NC
30 NC
29 DIFL2
28 DIFL1
27 TCIFC
26 VREF
25 MPXO
24 TMUTE
23 RAVO
22 LAVO
21 NC
11 W/R
12 BUSM
13 BUSEN
14 SWP1
15 SWP2
16 XTAL1
17 XTAL2
18 PDLF
19 PHLF
20 NC
PHILIPS TEA5767HN
FM Tuner
VDDIO_P
R59
22
10%
C62
100nF
R125
47K
10%
R126
47K
10%
R127
47K
10%
R128
47K
10%
R167
47K
10%
FM_DATA
FM_CLOCK
FM_WE
BUS_EN
SWP1
TP14
C63
33nF
C64
330pF
C65
33nF
C66
47nF
C67
47nF
C68
47nF
MPX
C69
100nF
FM_R
C70
100nF
FM_L
VDDIO_P
R61
47K 10%
R200
47K 10%
NOPOP
C73
1nF
C74
22pF
X2
32.768KHz
Crystal
R60
33K
10%
C75
22nF
C76
2.2nF
C77
2.2nF
JP3
0 Ohm
Resistor
Jumper
AGND
NOTE: Currently, the TEA5767 is used in 3-wire mode. In future versions of the 35XX SDK, the TEA5767 may be accessed in I2C mode, which frees up one GPIO. In order to support both modes, FM_DATA and FM_CLOCK should have pull-up resistors, and the BUS_MODE pin should have options to populate either a pull-up or pull-down resistor.
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Title
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FM Tuner - Philips TEA5767HN
Size B
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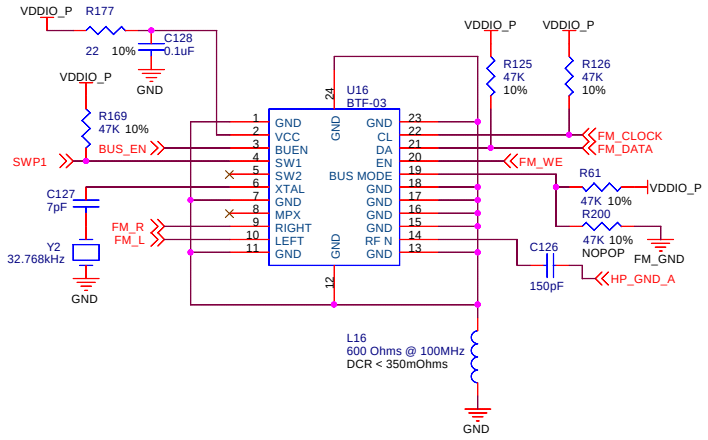
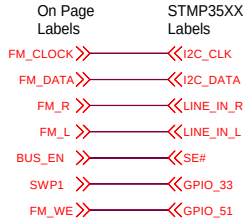
Optional FM Tuner Module

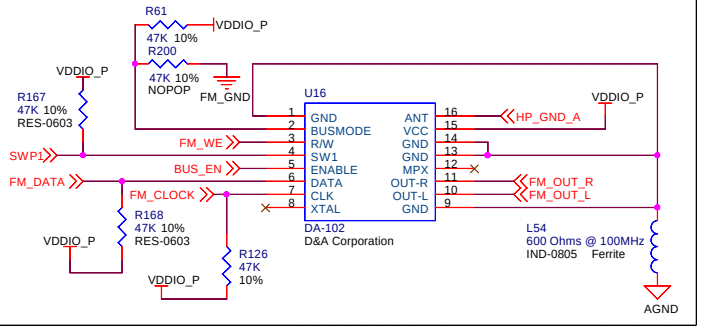
The Panasonic BTF-03 integrates the TEA5767 and most of the discrete components.



Integration



Option 2:
DA-102 (TEA5767)



NOTE: Currently, the TEA5767 is used in 3-wire mode. In future versions of the 35XX SDK, the TEA5767 may be accessed in I2C mode, which frees up one GPIO. In order to support both modes, FM_DATA and FM_CLOCK should have pull-up resistors, and the BUS_MODE pin should have options to populate either a pull-up or pull-down resistor.

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Title: **STMP35XX Reference Schematics**

Page: FM Tuner Modules

Size B

Rev B

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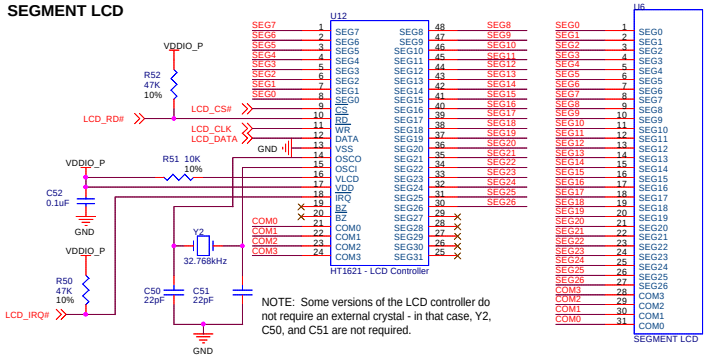
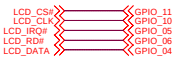
SEGMENT LCD

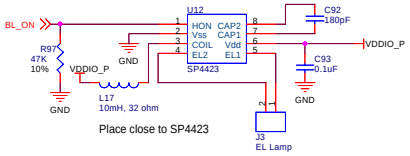


Integration



Optional EL Backlighting

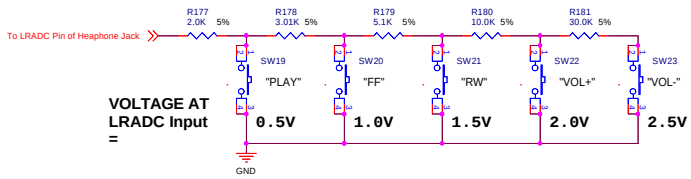
IMPORTANT: The EL Backlight Driver should have a current draw between 5mA and 20mA at 3.0V.



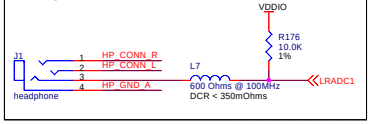
OPTIONAL HEADPHONE REMOTE

This circuitry may be built into the headphone cord to provide remote control functionality.

If using this circuit, use the Headphone Jack + Remote Control circuit.

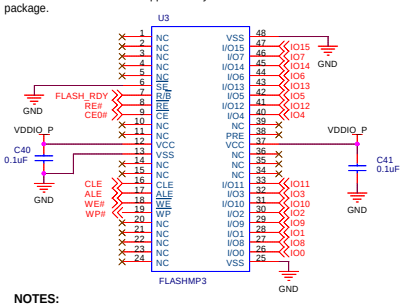


Headphone Jack + Remote Control



OPTIONAL 16-bit NAND Flash

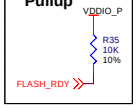
NOTE: 16-bit NAND Flash support is only available on the 144BGA package.



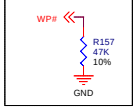
NOTES:

1. **The WP# pull-down resistor is required to protect the flash memory from inadvertent writes during power transitions.**
2. **The CE# pull-up resistor is required to keep the flash de-selected during power transitions.**
3. **A pull-up resistor is required on the FLASH_RDY signal because the flash output is open drain.**

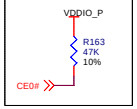
FLASH_RDY Pullup



WP# Pulldown



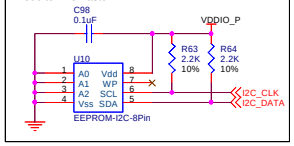
CE0# Pullup



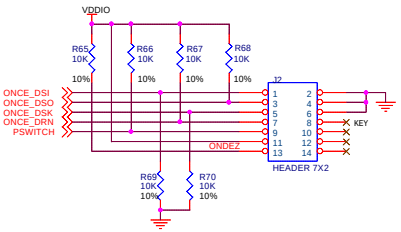
OPTIONAL I2C EEPROM Boot

Use Microchip 24LCxx-I/P or Equivalent

Booting from an EEProm requires setting the Boot Mode to "I2CMaster".



OPTIONAL ONCE PORT

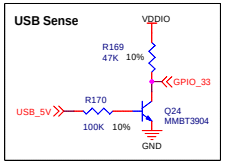


OPTIONAL: Wall Power + USB Power Switch

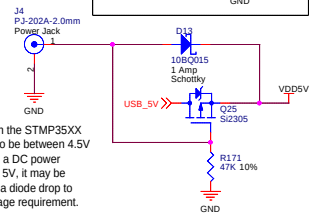
This circuit allows the STMP35XX to power from an external wall power supply. In the case where wall power and USB power are both connected, the STMP35XX will power and/or recharge using the wall power supply.

To implement this circuit, remove the direct USB_5V connection on the STMP35XX VDD5V pin, and connect the USB_5V line through a FET as shown.

USB Sense



5V DC, 1 A, Wall Transformer



Note: the voltage on the STMP35XX VDD5V pin needs to be between 4.5V and 5.25V. If using a DC power supply greater than 5V, it may be necessary to insert a diode drop to meet this input voltage requirement.

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Title: **STMP35XX Reference Schematics**

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