SERVICE MANUAL

COLOR TELEVISION RECEIVER

MODEL: SA-A SERIES

CONTENTS

IMPORTANT SERVICE SAFETY INFORMATION

Operating the receiver outside of its cabinet or with its back removed involves a shock hazard. Work on these models should only be performed by those who are thoroughly familiar with precautions necessary when working on high voltage equipment.

Exercise care when servicing this chassis with power applied. Many B plus and high voltage RF terminals are exposed which, if carelessly contacted, can cause serious shock or result in damage to the chassis. Maintain interconnecting ground lead connections between chassis, escutcheon, picture tube dag and tuner when operating chassis.

These receivers have a “polarized” AC line cord. The AC plug is designed to fit into standard AC outlets in one direction only. The wide blade connects to the “ground side” and the narrow blade connects to the hot “side” of the AC line. This assures that the TV receiver is properly grounded to the house wiring. If an extension cord must be used, make sure it is of the “polarized” type.

Since the chassis of this receive is connected to one side of the AC supply during operation, service should not be attempted by anyone not familiar with the precautions necessary when working on these types of equipment.

When it is necessary to make measurements or tests with AC power applied to the receiver chassis, an Isolation Transformer must be used as a safety precaution and to prevent possible damage to transistors. The Isolation Transformer should be connected between the TV line cord plug and the AC power outlet.

Certain High voltage (HV) maybe cause X-ray radiation. Receivers should not be operated with HV levels exceeding the specified rating for their chassis type. Higher voltage may also increase the possibility of failure in the HV supply.

It is important to maintain specified values of all components in the horizontal and high voltage circuits and anywhere else in the receive that could cause a rise in high voltage, or operating supply voltages. No changes should be made the original design of the receiver.

Components shown in the shaded areas on the schematic diagram and/or identified by in the replacement parts list should be replaced only with exact factory recommended replacement parts. The use of unauthorized substitute parts man creats may create shock, fire, X-ray radiation, or other hazards.

To determine the presence of high voltage, use an accurate high impedance HV meter

connected between the second anode lead and he CRT dag grounding device. When servicing the High Voltage System remove static charges from it by connecting a 10K Ohm resistor in series Wan insulated wire(such as test probe) between the picture tube dag and 2nd anode lead(Have AC line cord disconnected from AC supply).

The picture tube use in this receiver employ integral implosion protection. Replace with a tube of the same type number for continued safety. Do not lift picture tube by the neck. Handle the picture tube only when wearing shatterproof goggles and after discharging the high voltage completely, Keep others without shatter proof goggles away.

Before returning the receiver to the user, perform the following safety checks:

1. Inspect all lead dress to make certain that leads are not pinched or that hardware is not lodged between the chassis and other metal parts in the receiver.

2. Replace all protective devices such as non-metallic control knobs, insulating fish-papers, cabinet backs, adjustment and compartment covers of shields, isolation resistor-capacitor networks, mechanical insulators etc.

3. To be sure that not shock hazard exists, a check for the presence of leakage current should be made at each exposed metal part having a return path to the chassis (antenna, cabinet metal, screw heads knobs and/or shafts, escutcheon, etc.) in the following manner.

Plug the AC line cord directly into a 110V/220V/240V AC receptacle. (Do not use an Isolation Transformer during these checks.) All checks must be repeated with the AC line cord plug connection reversed. (If necessary, a non-polarized adapter plug must be used only for the purpose of completing these checks.)

If available, measure the current using an accurate leakage current tester. Any reading of 0.35mA or more is excessive and indicates a potential shock hazard which must be corrected before returning the receiver to owner.

If a reliable leakage current tester is not available, this alternate method of measurement should be used. Using two clip leads, connect a 1500 Ohm, 10 watt resistor paralleled by a 0.15MF capacitor in series with a known earth ground, such as a water pipe or conduit and the metal part to be checked. Use a VTVM or VOM with 1000 Ohms per Volt, or higher, sensitivity to measure this AC voltage drop across the resistor,. Any reading of 0.35 volt RMS of more is excessive and indicates potential shock hazard which must be corrected before returning he receiver to the owner.

ALIGNMENT PROCEDURES
PLEASE READ BEFORE ATTEMPTING SERVICE

1. Use an Isolation Transformer when performing any service on this chassis.
2. Never disconnect any leads while receiver is in operation.
3. Disconnect all power before attempting an repairs.
4. Do not short any position of the circuit while the power is on.
5. For safety reasons, replacing any components should be according with identical replacement parts.
6. Before testing, warm up the TV for at least 30 minutes and demagnetize the CRT with an external degaussing coil.
7. When removing a PCB or related component, after unfastening or changing a wire, be sure to put the wire back in its original position.
8. Inferior silicon grease can damage IC's and transistors. When replacing IC's and transistors, use only specified silicon grease,. Remove all old silicon when applying new silicon.
9. Before removing the anode cap, discharge drastically because it contains high voltage.

TV SPECIFICATION

1. Ambient Conditions:

1.1 Ambient Temperatures:

a. Operating: -10 ~ +40 ℃

b. Storage: -15 ~ +45 ℃

1.2 Humidity

a. Operation: <80%

b. Storage: <90%

1.3 Air Pressure: 86kpa ~ 106kpa

2. General Specification

2.1 Main IC: Philips UOCIII chip

2.2 System: TV PAL DK / BG / I
SECAM DK / BG
NTSC M
AV PAL
SECAM
NTSC 4.43/3.58

2.3 Channel: VHF-LOW 46.25～140.25MHz
VHF-HIGH 147.25～423.25MHz
UHF 431.25～855.25MHz
CATV 112.25～464.25MHz

2.4 Scanning Lines & Frequencies
525 lines/60Hz or 625 lines/50Hz
15.75KHz/15.625KHz

2.5 Color Sub-Carrier Frequency: 4.433MHz/3.579MHz

2.6 IF: Picture 38.9MHz/38.0MHz/45.75MHz
Sound 4.5MHz/5.5MHz/6.0MHz/6.5MHz

2.7 Power Consumption: 14” and 15” TV 70W
21” TV 75W

29” TV 150W

34” TV 180W

2.8 Power Supply: AC 110/220/240V 50/60 Hz

2.9 Max Audio Output Power (7% THD): 14” and 15” ≥1W X 2

21” ≥2W X 2

29” and 34” ≥4W X 2

2.10 Antenna Impedance: 75 Ω

3. Basic Features of Controller

3.1 Channel Tuning Method: Frequency Synthesizer

3.2 Presettable Program: 256 Programs or 181 Programs

3.3 Tuning for VHF and UHF Bands: Auto Tuning/Manual Tuning

3.4 Picture and Sound Adjustment

Bright, Contrast, Color, Sharpness control and Color Temperature adjustment

TINT control (NTSC only)

Volume, Balance, Bass, Treble control(only for the model with stereo function)

3.5 OSD

General Features (Volume, Balance, Bass, Treble, Brightness, Contrast, Color, Sharpness, Program, Auto Search, Manual Tune, Muting, AV/TV, Child Lock and Sleep Timer)

Multi-Language (including English)

3.6 Sleep Timer: 30、60、90、120 Minutes

3.7 Auto Standby When No Signal in 5 minutes(under the state of blue screen or non-signal saver state)

3.8 Full Function Infrared Remote Control

3.9 Remote Effective Distance: 8m

4. Construction of Front Panel

Main Power Switch

Remote Sensor

Standby Indicator

Menu Select Button

TV/AV Select Button

Program and Volume Up/Down Button

5. TV's Terminals

75 Ω Aerial Terminal

AV Input and AV Output (SA-A Series)

S-Video Input (only for some model)

Y/Cb/Cr Input (only for some model)

6. Other Informations

6.1 Magnetic Field: Bv = 0.3~0.65Gs

6.2 Standard Color Temperature: 9300K (X = 0.284, Y = 0.299)

Service Flow Chart

Power supply

check input voltage —→ check voltage of C910 anode —→ check Pin 4 of N901 —→ check output voltage of T901 secondary coil —→check voltage of N904 Pin 3(5.0v), N903 Pin3 (9.0V) and V951 Emitter—→ check voltage of N103 Pin 8,31,32,35,36,43,55(5v) and Pin11,19(8v)—→ check voltage of N602 Pin 8 (+5V)

Audio circuit

check power supply of audio power amplify circuit —→ check input audio signal of audio power amplify circuit (26V)—→ check waveform of N103 Pin 5—→ check waveform of xs808 Pin 16,17—→ check waveform of N201 Pin 7,10

Horizontal circuit

Check voltage of T402 Pin 3 (110V) —→ check voltage of N103 Pin 19 (+8.0V) —→ check waveform of V401 Base —→ check waveform of V402 Collector —→ check output voltage of T402 coil (PIN 2)—→ check waveform of T402 Pin 8

Vertical circuit:

check voltage of N440 Pin 2 (+25V) and Pin7(+9V)—→ check voltage of N103 pin 19 (+9V) —→ check waveform of N103 Pin 17 —→ check waveform of N440 Pin 1 —→ check waveform of N440 Pin 5

MCU circuit:

check voltage of N103 Pin 31,32(5v) —→ check waveform of N103 Pin 33

TV ADJUSTMENT

Test equipment

1. Oscilloscope
2. Multifunction meter (Internal resistance: DC≥20kΩ/V AC≥5kΩ/V)
3. High voltmeter: 27.5kV
4. Standard Signal Generator
5. Degaussing coil

Factory menu

Some adjustments must be performed in the Factory menu. You can enter the Factory menu in the following way:

1. Press the MENU button on the remote control then press the RECALL button on the remote control three times sequentially.
2. Press P+ or P- button on the remote control to select test item.
3. Press V+ or V- button on the remote control to adjust the value of selected item
4. Press RECALL button again to exit FACTORY MENU.

B+ adjustment

Test Equipment: Multifunction meter

1. Operate the TV set with AC 110/220/240V(50/60Hz).
2. Receive Television broadcast signal, set PICTURE to Normal mode.
2. Connect the multifunction meter + lead to C960 and GND. Adjust the RP950 until the meter reading the proper DC value (More details please refer to the TV's BOM).

High voltage check and filament voltage check

Test Equipment: High voltmeter

1. Make sure AC power supply and +B are within pointed range before calibrating high voltage.
2. Connect high voltmeter to anode (G4) of CRT and GND.

3. Turn on the TV, set the BRIGHTNESS and CONTRAST to the minimum (zero beam current), swap to AV mode (No any signal applied).

4. High voltage please refer to different CRT

5. Filament voltage measured by virtual value meter please see the related model BOM, usually within the range of 6.3±0.2Vrms.

Grid voltage adjustment

1. Set Unit to AV, and set the picture to standard mode.

2. Enter FACTORY MENU 00, press P+ or P- button to choose V-KILL, then press V+ button to display horizontal light line on the screen, adjust SCREEN potentiometer so that the horizontal light line just displays anyone color of R,G and B, press V- button to restore the screen.

RF AGC adjustment

1. Receive signal (VHF channel)

2. Set input field strength to 60dBμV

3. Enter into FACTORY MENU 00, select RF AGC item, press V+ button to adjust RF AGC automatically, and when the adjustment is finished, the screen will display RF AGC value.

Focus adjustment

1. Receive five circles pattern, adjust the pattern to Normal mode.

2. Adjust focus potentiometer (horizontal output transformer) so that the center and four corners of pattern are the best focus.

Horizontal scanning, vertical scanning and geometry correction adjustment (adjust with PAL and NTSC signal separately)

1. Enter into factory menu to call up FAC1

H-PHASE XX Adjust it so that the left half is symmetrical with the right half (H. CENTER correction).

OSD-H-PHASE XX Adjust it so that the OSD is displayed on the middle of the screen (OSD H. CENTER correction).

V-POSITION XX Adjust it so that the pattern midline superposes over CRT geometric center.

V-SIZE XX Adjust it so that the picture vertical reproduction display ratio is more than 92%.

V-SC XX Adjust it so that upper pane and bottom pan of the pattern are the same as the middle pane.

V-LINEARRITY XX Adjust vertical linear.

.

White balance adjustment (PAL or SECAM signal)

1. Enter into menu firstly and set PICTURE to Normal mode. (9300K)
2. Enter into AV mode and receive left black right white signal which with color sync signal.
3. Plug XS600, adjust it automatically with white balance adjustment software.

Standard：Color temperature 9300K （X=0.284 Y=0.299）

Warm color：Color temperature 6500K （X=0.313 Y=0.329）

Cold color：Color temperature 12000K（X=0.272 Y=0.279）

Other factory menu data

Each TV model has different factory menu, more details please refer to the TV's adjustment Engineering Illumination.

IC INFORMATION

1. SANYO USOC CHIP – LA76936/LA76938 (N103)

The SANYO USOC series combines the functions of a Video Signal Processor (VSP) together with a CPU embedded Control/Graphics μ-Controller (TCG μ-Controller) .The delivery specifications of LA76936 or LA76938:

1.1 Case Outline: DIP64S(600mil) Plastic Package;

1.2 Function: IIC Bus Control VIF/SIF/Y/C/Deflection/CbCr IN/Implemented in a Single Chip with CPU

1.3 Applications: PAL/NTSC/SECAM Color Television Sets

1.4 PIN function of LA76936/LA76938

PIN	FUNCTION	VOLTAGE	PIN	FUNCTION	VOLTAGE
1	SIF output	2.45V	33	XT1	1.52V
2	IF AGC Filter	2.55V	34	XT2	2.53V
3	SIF input	3.11V	35	VDD	5.0V
4	FM filter	2.17V	36	POW (I/O)	5.0V
5	FM output/select audio	2.20V	37	FACP/N (I/O)	0.71V
6	Audio output	2.15V	38	APDC	1.12V
7	SND APC filter	2.11V	39	KEY	5.0V
8	IF Vcc	5.0V	40	RESET	5.0V
9	EXT audio input		41	PLL	2.78V
10	ABL	4.19V	42	CPU GND	0
11	RBG Vcc	8.22V	43	CCDVCC	5.0V
12	R output	2.43V	44	FBP input	
13	G output	2.49V	45	Y/C-C input	
14	B output	2.42V	46	N.C	
15	N.C		47	X radial protect	
16	V RAMP OSC.capacitor	2.14V	48	Fast blanking input	2.47V
17	Vertical output	1.93V	49	Cb input	
18	I reference	1.67V	50	4.43MHz crystal	
19	Horizontal/BUS Vcc	5.0V	51	Cr input	
20	FAC filter	2.63V	52	Select video output	
21	Horizontal output	0.78V	53	Chroma APC filter	3.21V
22	Video chroma deflection GND	0	55	Video chroma deflection Vcc	4.89V
23	N.C		54	EXT video input	
24	N.C		56	INT video input	
25	SVHS (I/O)		57	Black stretch filter	2.6V
26	REM (I/O)	5.0V	58	PIF APC filter	2.36V
27	AV2 (I/O)		59	AFT output	
28	AV1 (I/O)		60	Video output	
29	N.C		61	RF AGC output	
30	MUTE (I/O)		62	IF GND	
31	SDA	5.0V	63	VIF AMP INPUT	
32	SCK	5.0V	64	VIF AMP INPUT	

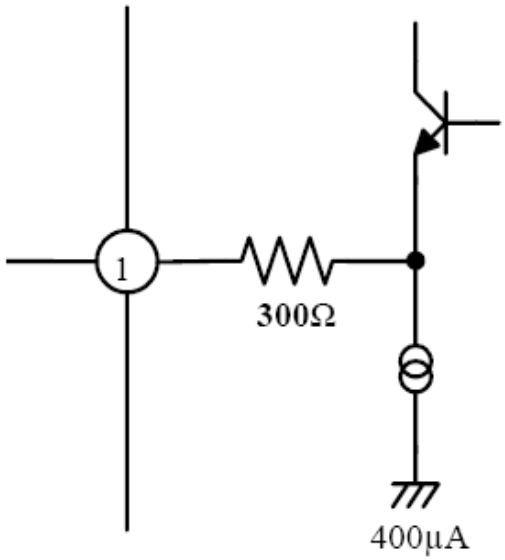
PIN 1 (SIF OUTPUT)

This is a SIF output pin.

The output of this pin can be used as an input for Stereo Decoder IC e.g. NICAM IC.

The output is a follow-emitter and its output impedance is about 350Ω. The DC output is about 2.8V.

When the Picture to Sound carrier ratio input to the IC is 25dB, the sound IF output of this pin is abou 100dBμV(without SAW Filter). When through the SAW filter , the Picture to Sound carrier ratio input t the IC is about 10dB ,the sound IF output of this pin is about 100dBμV.



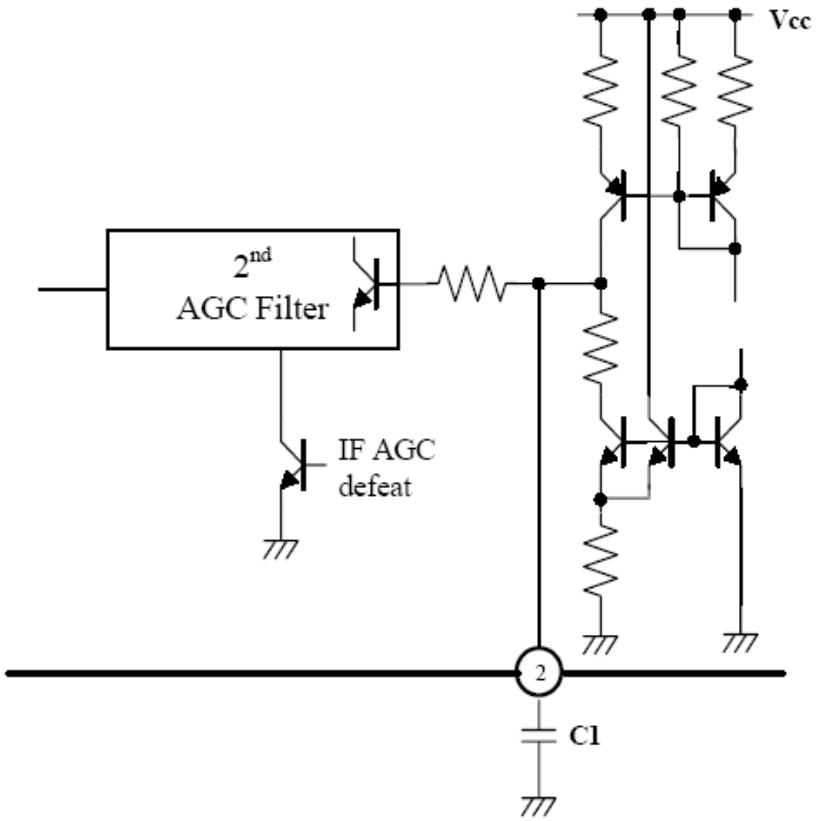
The circumference circuit of pin 1

PIN 2 (IF AGC Filter)

This is 1st AGC filter pin.

The signal, which is peak detected by the AGC detector, is smoothed by the external capacitor C1 and become to AGC voltage. A 2nd AGC filter is also built-in into IC. The value of C1 depends on the speed of AGC, sag etc. The recommended value is about 0.022μF.

If the BUS of IF AGC option is set as '1', the gain of PIF is set to minimum.

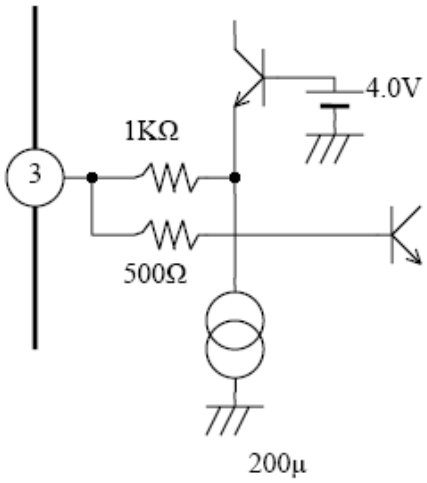


The circumference circuit of pin 2

PIN 3 (SIF INPUT)

This is a SIF input pin.

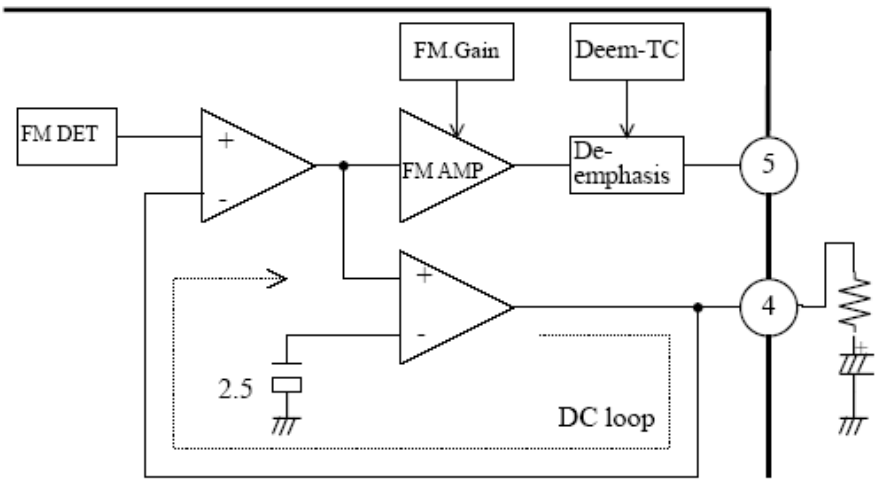
The input impedance is about 1kΩ and the internal DC voltage is biased at about 3.3V. The maximum input for this pin is 96dBμV.(When the output of pin 1 is 100dBuV, because fo capacity 10pF enters between the pin1 and pin3 , sound career decreases and become about 90dBuV at Pin3).



The circumference circuit of pin 3
Recommended application circuit

PIN 4 (FM FILTER)

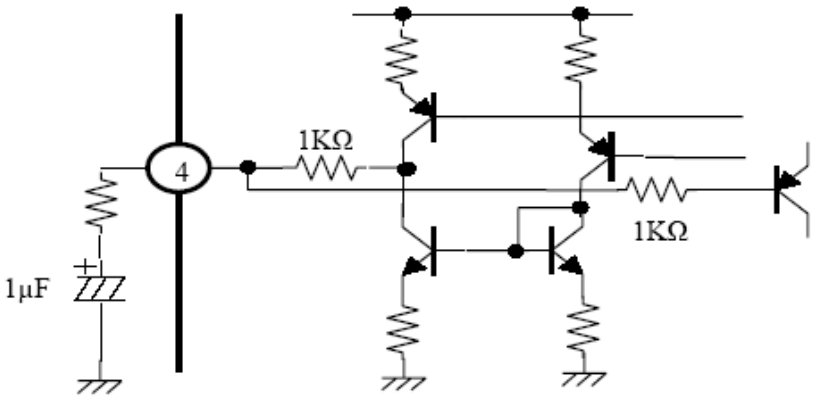
This is the filter pin for the DC loop of FM detector.



Using PLL FM detection will cause DC shift during detecting SIF from 4.5MHz to 6.5MHz. However, this IC is able to detect SIF signal from 4.5MHz to 6.5MHz with good linearity range. The detected signal will pass through an amplifier after the DC output is fixed. In order to keep the DC output constant, feedback loop using operating amplifier is built-in into the IC. It is necessary to feedback a DC component, which is created by the external capacitor of pin 4. The recommend value of this capacitor is 1uF. The low frequency and the respond time characteristic of input signal depend on the value of this capacitor.

It is also possible to decrease the FM detection level by connecting a resistor is series with the capacitor at pin 4. By setting the resistor to 39KΩ, the output level can be controlled by the FM GAIN :

BUS setting for FM Gain	Output level
'0'	500mVrms (± 50KHz)
'1'	500mVrms (± 25KHz)



The circumference circuit of pin 4

Pin 5 (FM Output)

This is an output pin for FM detector.

The output circuit is a voltage follower. The DC voltage is about 2.5V and the dynamic range is 3.5V.

The setting of BUS is depending on the frequency of SIF:

SIF frequency	BUS setting
4.5MHz	'00'
5.5MHz	'01'
6.0MHz	'10'
6.5MHz	'11'

The output level is variable which is controlled by BUS:

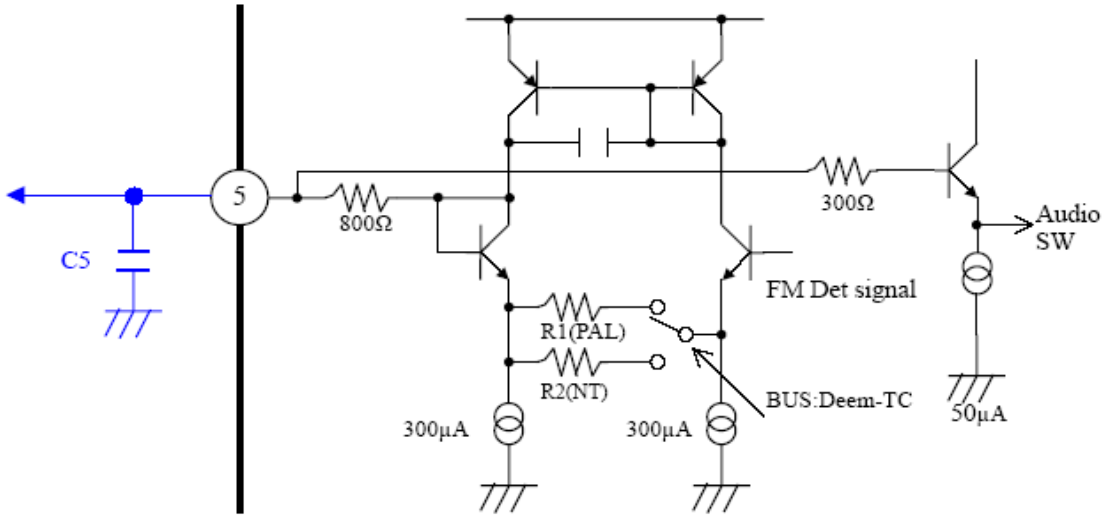
BUS setting for FM Gain	Output level
'0'	500mVrms (±50KHz)
'1'	500mVrms (±25KHz)

The output impedance is variable which is controlled by BUS:

BUS setting for Deem-TC	Output Impedance
'0'	5.0KΩ
'1'	7.5KΩ

The time constant of the de-emphasis is determined by the value of external capacity C5 (0.022uF). It is not necessary to connect an external capacity if a stereo IC is used but the output impedance is very high. This pin can also be used as an audio switch by setting the bus for AMON.SW :

0 = Normal mode (de-emphasis FM-Detector).
1 = SAO mode at External audio input mode.



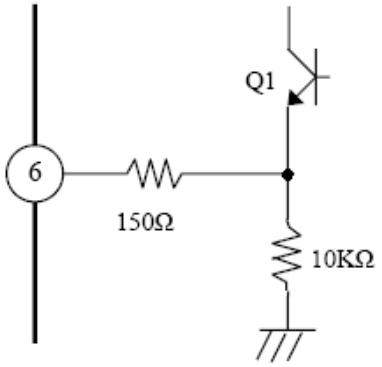
The circumference circuit of pin 5

PIN 6 (Audio Output)

This is an audio output pin.

The output impedance is about 300Ω (Q1 impedance is about 150Ω) and the DC output is about 2.5V. The dynamic range is 3.5Vpp.

There is an attenuator between input (internal audio.: pin 5; external audio: pin 9) and output, whose maximum gain is 0dB. The DAC step is 0.5dB. A LPF (fc = 30Hz) is built in-between D/A circuit and volume circuit to eliminate 'POP' noise problem caused by the volume control.



Circumference circuit of pin 6

PIN 7 (SND APC FILTER)

This is a SND APC FILTER pin.

The phases of chroma frequency signal is compared with the sound IF VCO frequency signal. The discrepancy in phase is transformed into current and output to pin 7. This current is smoothened by the external capacitor of pin 7 and is used to control the Sound IF VCO.

The dividing ratio of Sound IF VCO is varied according to the SIF system selected. The oscillator frequency of Sound IF VCO is locked at a frequency which is 500k away from SIF frequency.

PIN 8 (IF Vcc)

This is DC voltage supply pin for IF circuit. Connect a 5.0Vdc to it.

Connect the grounding of the filtering capacitors to the IF Ground at Pin 62.

PIN 9 (VM OUTPUT or EXT AUDIO INPUT)

This pin can be selected to be Ext Audio Input or VM Output by setting :

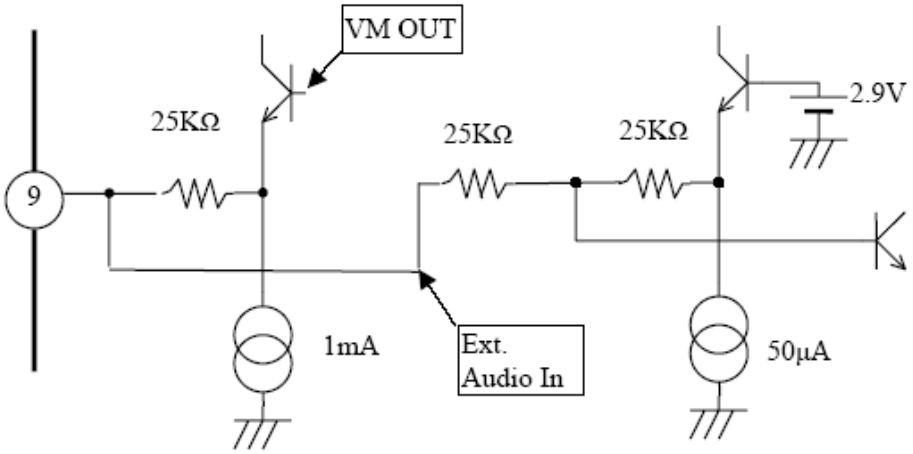
VM/AUDIO SW	=	0	EXT AUDIO IN
	=	1	VM OUT

VM output

Output the differentiated signal.

Functions that can be controlled by BUS.

- VM GAIN Control VM AMP GAIN/with defeat (3 bits)
- VM delay Control VM delay time (2 bits)



EXT Audio Input

This pin can be configured as an external audio signal input.

The input impedance is about 50KΩ and the DC voltage is biased at about 2.9V. There is necessary to use a coupling capacitor at the input.

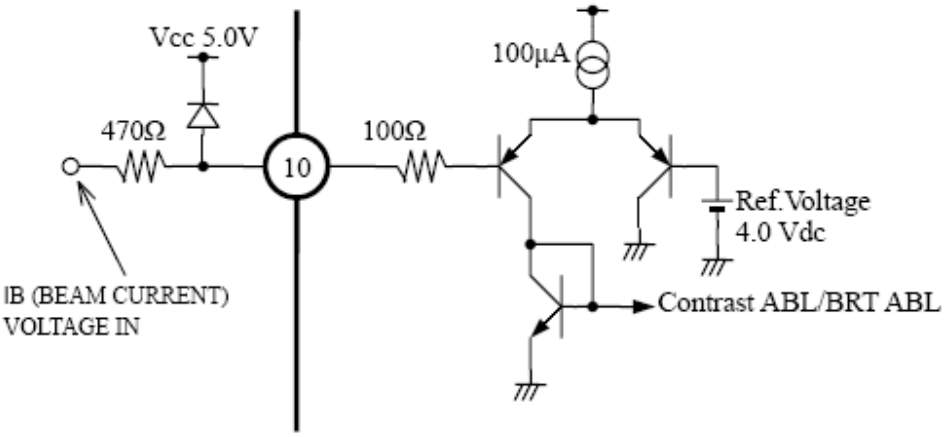
PIN 10 (ABL)

* ABL (Auto Beam Limiter) Function

This is an ABL / ACL input pin.

Please transform beam current into voltage.

Refer data-sheet for more details about the characteristics.



PIN 11 (RGB Vcc)

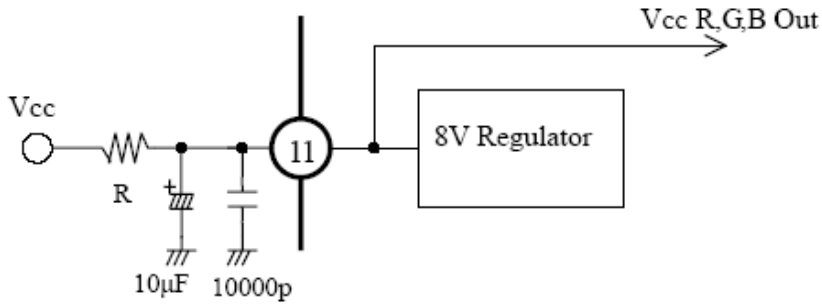
This is a Vcc input pin for RGB output block.

An 8.0V regulator is built-in in the IC. Please supply a current of 18mA to it.

A resistor is needed to connect with this pin from Vcc. The value of the resistor is calculated as below:

R[Ω] = (Vcc - 8.0)/18m

For example: Vcc = 9.0V, then an 51Ω resistor is necessary



PIN 12, PIN 13, PIN 14 (R, G, B OUTPUT)

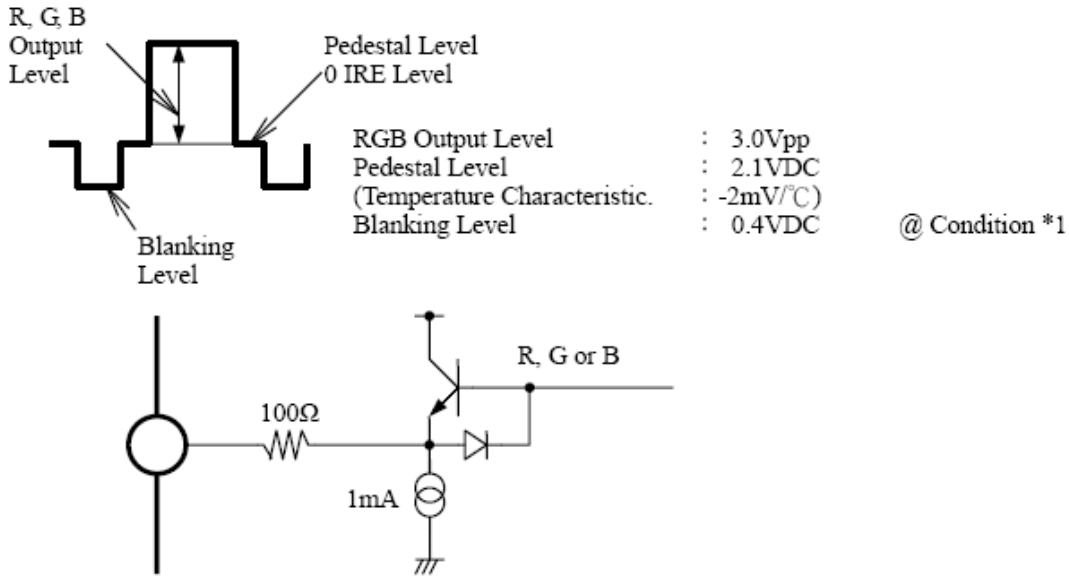
These are the R, G, B signal output pin.

PIN 12 : R OUT,

PIN 13 : G OUT,

PIN 14 : B OUT

Output Signal :



Condition *1 :

- Contrast Control (7 bit) : Max
- Brightness Control (7 bit) : Mid (100000)
- Sub-Brightness Control (7 bit) : Mid
- R, B Drive Control (7 bit each) : Max
- G Drive Control (4 bit) : Min
- R, G, B Bias (Cut-Off) Control (8 bit each) : Min

Each control variable range is show below:

Input signal：1Vpp (Sync Tip to White) = 140 IRE

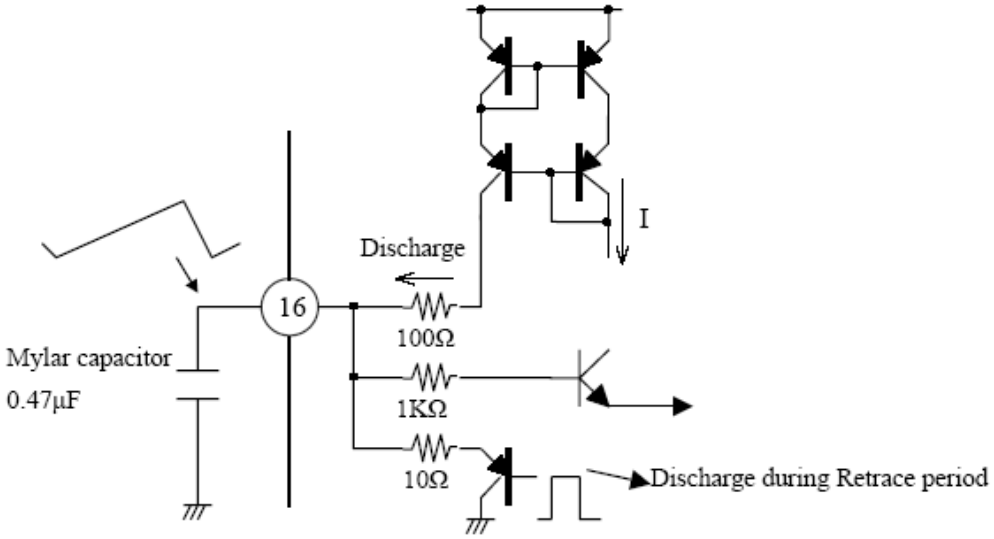
		Min		Typical		Max	
Y Total Gain (Max)		12	dB	14	dB	16	dB
Contrast Control Max/Mid		5	dB	7	dB	9	dB
Contrast Control Range Min/Max	(128-step)	-15	dB	-12	dB	-9	dB
Brightness Control Max/Mid	(64-step)	25	IRE	30	IRE	35	IRE
Brightness Control Min/Mid	(64-step)	-35	IRE	-30	IRE	-25	IRE
Sub-Bias Control Range	(128-step)	700	mV	800	mV	900	mV
Bias Control Range	(256-step)	700	mV	800	mV	900	mV
G Drive Reduction Control Range	(16-steps)			4	dB		
R,B Drive Reduction Control Range	(128-step)	9	dB	11	dB	13	dB

PIN 15 (N.C)

PIN 16 (V RAMP OSC. Capacitor)

This pin is connected to a capacitor, which is used to generate a ramp waveform for the reference of pin 17 (Vertical Output).

Ramp waveform is generated by charging / discharging the capacitor. Please use a 0.47µF Mylar capacitor.



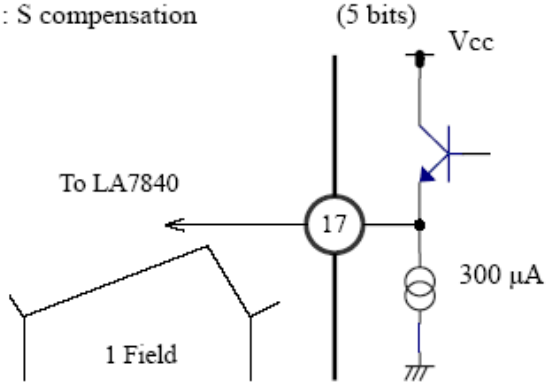
PIN 17 (VERTICAL OUTPUT)

This is an output pin of vertical synchronization ramp signal.

We recommend using together with LA7840 serial.

Below are some functions which can be control by BUS:

- V.DC : position of field (6 bits)
- V. Size : size of field (7 bits)
- V. Linearity : linearity (5 bits)
- V. SC : S compensation (5 bits)

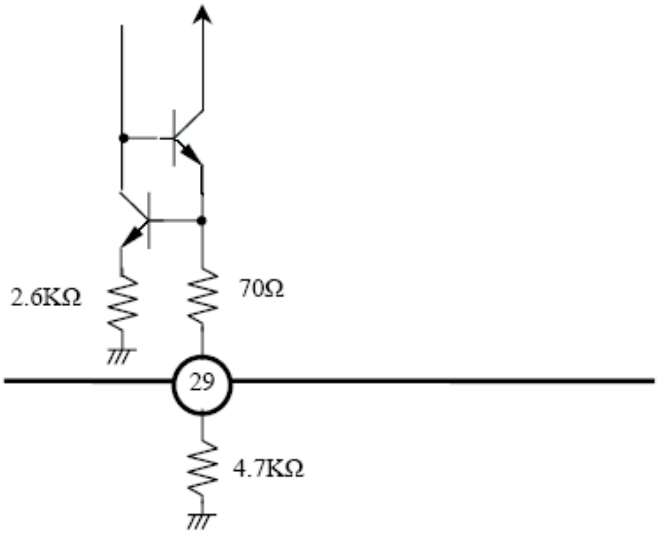


The application of vertical position adjustment circuit is different depending on either using ± dual voltage supply or single voltage supply. Please refer to technical note of LA7840/LA78040 (Vertical output IC).

PIN18 (I reference)

This is a pin for producing the reference current.

Connect a resistor of 4.7KΩ to ground from this pin.



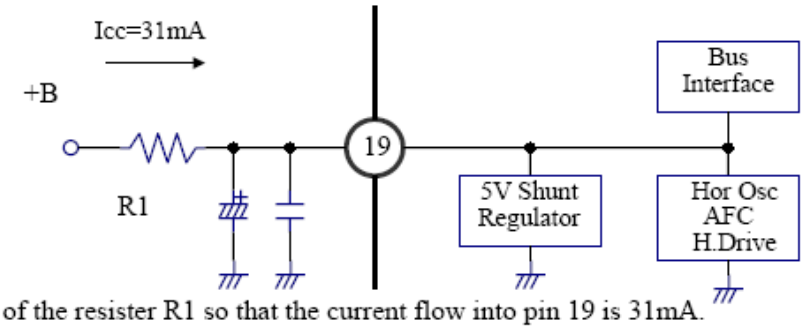
Note :

During the evaluation stage of this IC (engineering sample), bus-control is used to adjust the horizontal frequency (H freq. = 6 bits). No adjustment of horizontal frequency is needed in the mass-production products. Depending on the accurate level of horizontal free-run frequency we need, a low offset external resister is requested.

PIN 19 (HORIZONTAL / BUS Vcc)

This is a Vcc pin for horizontal deflection block and BUS interface block.

There is a 5V regulator built-in the IC.



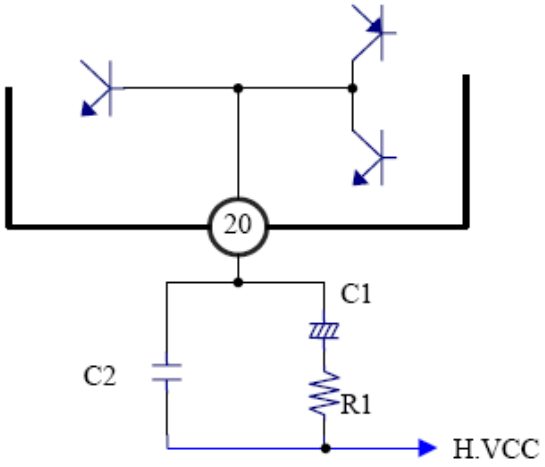
Choose the value of the resister R1 so that the current flow into pin 19 is 31mA.

The value of the resister is decided as below:

R1 = (+B - 5.0V)/31mA

PIN 20 (AFC FILTER)

This is the AFC filter pin of horizontal VCO.

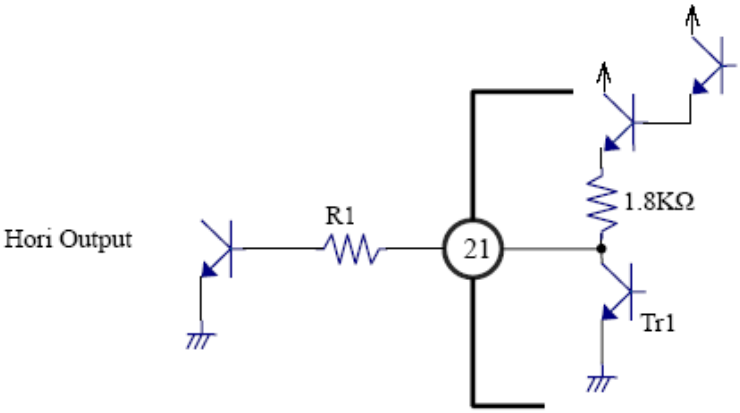


C1 is used for canceling the vertical ripple, while the resister R1 is used for transforming the control current into voltage. C2 is a smoothing capacitor.

Reference value : C1 = 1.0μF
C2 = 0.015μF
R1 = 3.0KΩ

PIN 21 (HORIZONTAL OUTPUT)

This is a horizontal output pin, and its output circuit is push-pull circuit.



The maximum collector current of the Tr1 is 3mA. Usually, R1 is used to reduce the influence of the horizontal output to IF block and is recommended to be set at 100Ω. The level of influence depends on the pattern lay-out of the chassis.

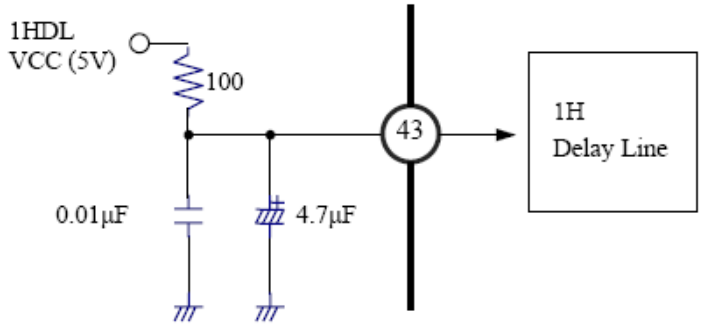
Note : The duty of the horizontal output pulse is designed at 37.6μs in low period.

PIN 22 (Video Chroma Deflection GND)

This is the ground pin of video/ chroma/ deflection block.

PIN 43 (CCD Vcc)

This is a Vcc (5V) pin for 1 H delay-line.



PIN 44 (FBP INPUT)

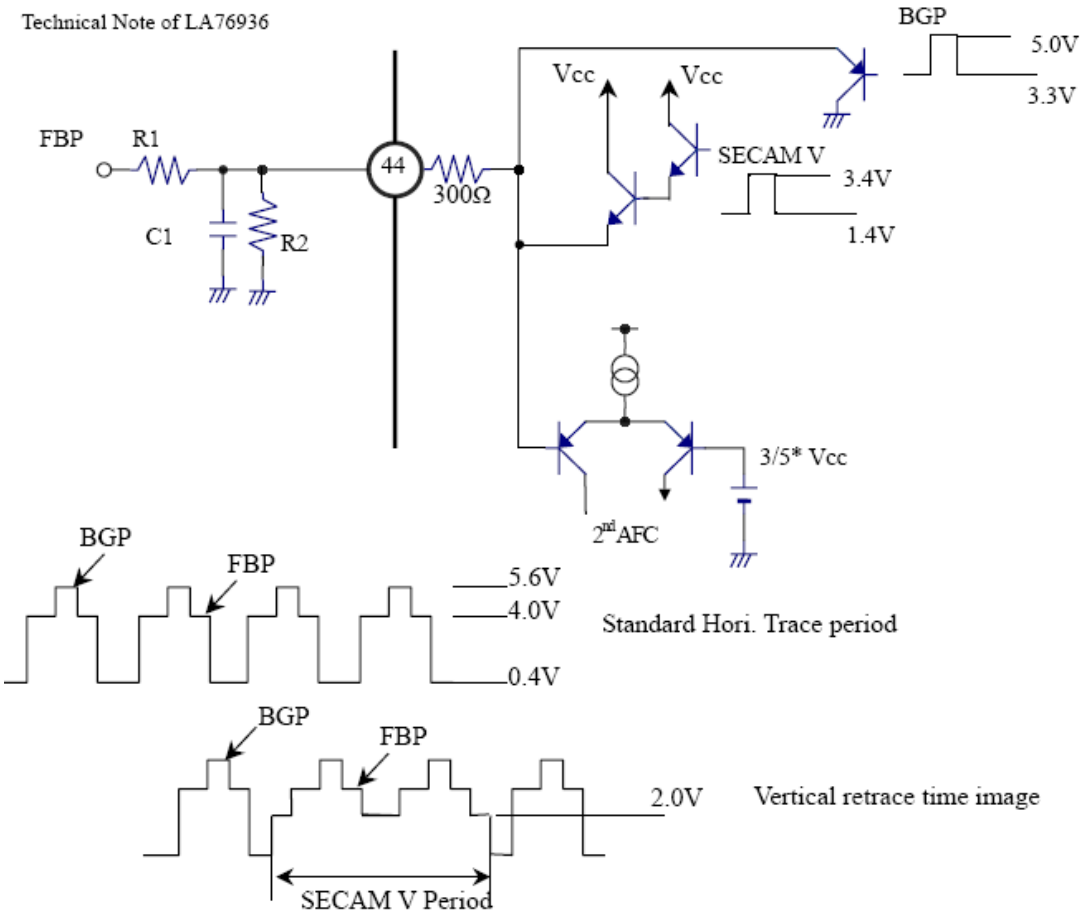
This is the input pin of flyback pulse, which is used for AFC.

The threshold voltage at which the flyback pulses are acquired internally by the IC is 3/5*Vcc. (For example, if the Vcc is 5V, it is 3V). The fly-back pulse is input via R1 and R2.

Besides, although the input flyback pulses are input to the AFC2 loop to take up the horizontal output storage time the flyback pulses must be matched to the screen center by adjusting the integration provided by R1 and C1.

This IC has a function which is used for horizontal position fine adjustment:

Horizontal Phase: the horizontal center of the screen can be adjusted by bus-controlled. (5bit)



Note 1)

The best storage time of this IC, between the rise up of Horizontal output (pin 21) and the rise up of input FBP, is about 9µs. Therefore, the storage time of television chassis is better set at 9 µs ± 2µs.

Note 2)

In LA76930 series, FBP is not used in the blanking of RGB output. RGB blanking pulse is produced in the internal count-down circuit, and the phase is depending on horizontal synchronization signal.

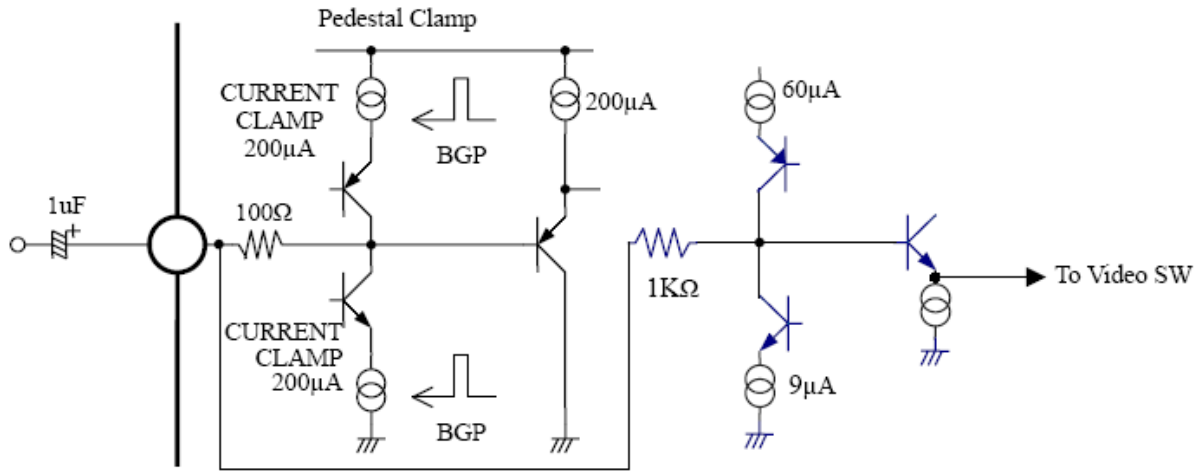
Regarding the phase and the width of blanking pulse, previously the waveform is made up and designed in FBP input circuit. But, in LA76930 series, the phase and the width of blanking pulses (H BLK R&L) can be set by BUS control. Therefore, the design of FBP input circuit (adjustment of horizontal phase, jitter characteristic etc) become easier. Also, in case of development of many chassis, this can contribute to speed up the development period.

PIN 47, 46, 45 (EXT R, G, B INPUT or S-VHS IN)

These pins can be selected as EXT RGB input pins or S-VHS input pins.
They can be used in either digital input mode or analog input mode.
A coupling capacity is necessary.
47 PIN : R INPUT or NC,
46 PIN : G INPUT or YC-Y,
45 PIN : B INPUT or YC-C

Input Signal selection:
VIN/EXT RGB SW = 1 S-VHS IN
" = 0 EXT RGB IN

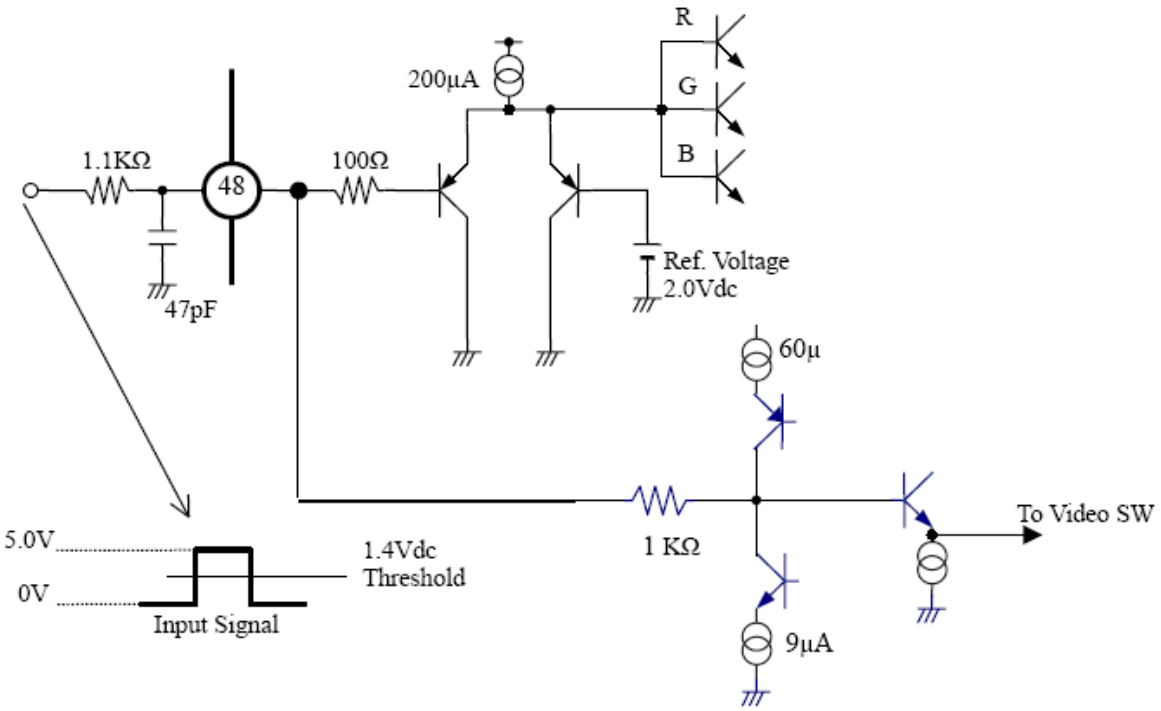
- Analog Signal 0.7V (Black Level - White Level)
- Digital Signal High Level : 5V(Max)



Note: OSD signal is controlled by brightness and OSD contrast.
(OSD signal is impressed on external video signal before brightness and contrast control)

PIN 48 (FAST BLANKING INPUT or VIDEO IN)

This pin can be selected as an EXT FAST BLANKING INPUT or VIDEO INPUT.



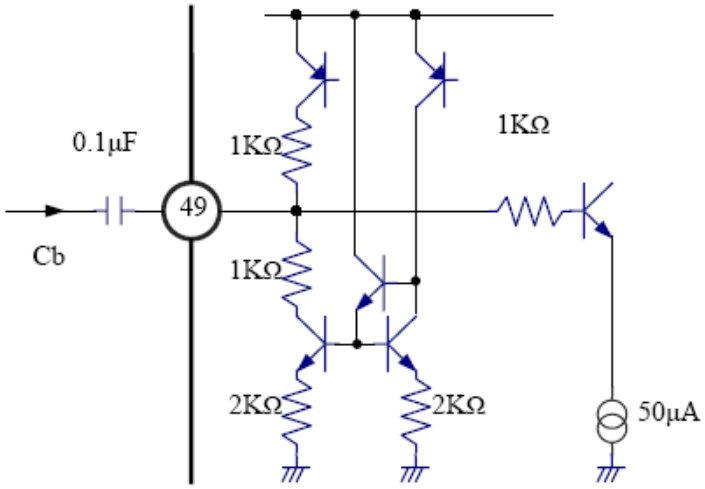
Input Selection:

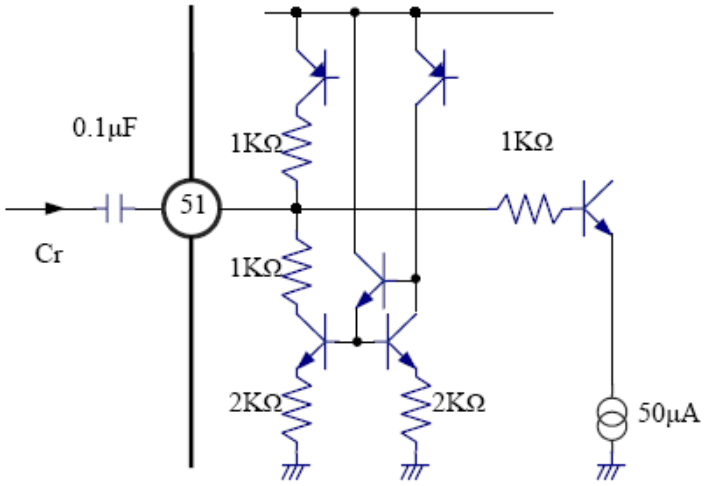
VIN/EXT RGB SW : 1 = VIDEO IN

0 = FAST BLANKING IN

PIN 49,51 (CbCr Input)

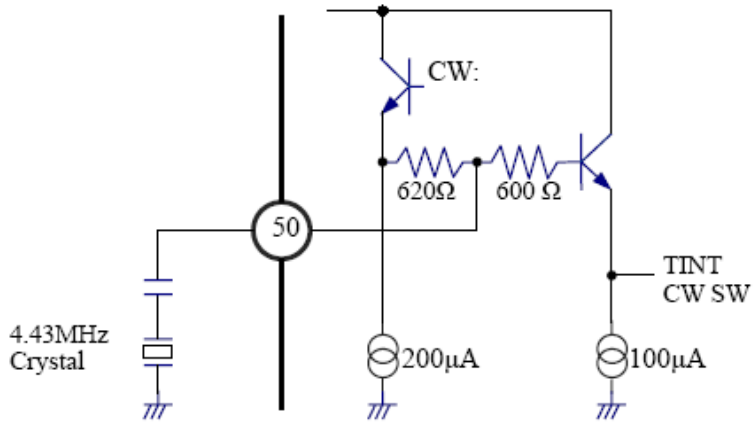
These are the Cb and Cr input pins.





PIN 50 (4.43MHz CRYSTAL)

This is a 4.43MHz x'tal connecting pin.



PIN 52 (Selected Video Output or fsc Output)

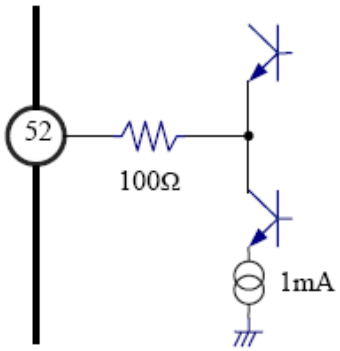
This pin can be selected as Selected Video Output or fsc signal.

In Selected Video Out Mode, this signal which is selected by a video switch among pin 56, pin 54, pin 46 or pin 48 input signals, is amplified 6dB and then output here. The output amplitude is 2Vp-p.

In fsc Output Mode, fsc signal is outputted

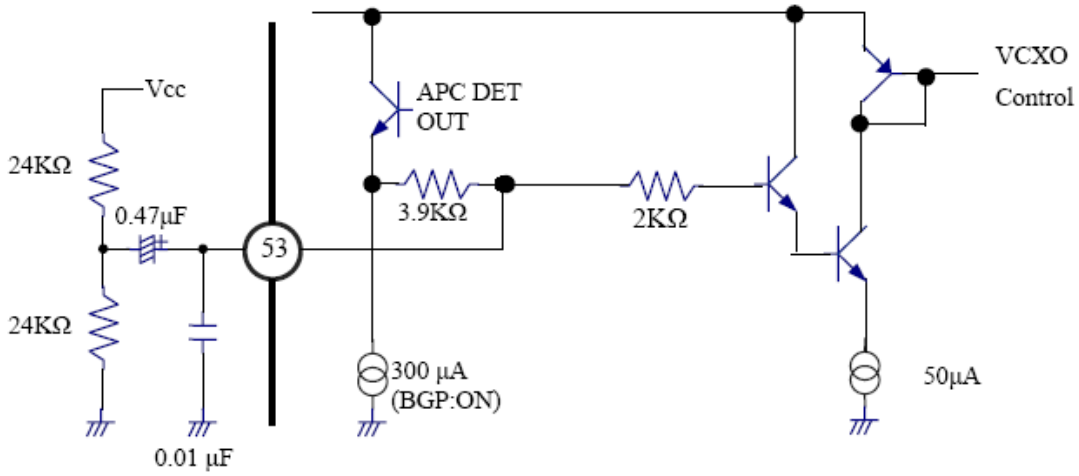
Output Selection:

SVO or fsc Output : 0 = Selected Video Out
1 = fsc signal



PIN 53 CHROMA APC FILTER)

This is a filter pin for APC filter of chroma VCXO.

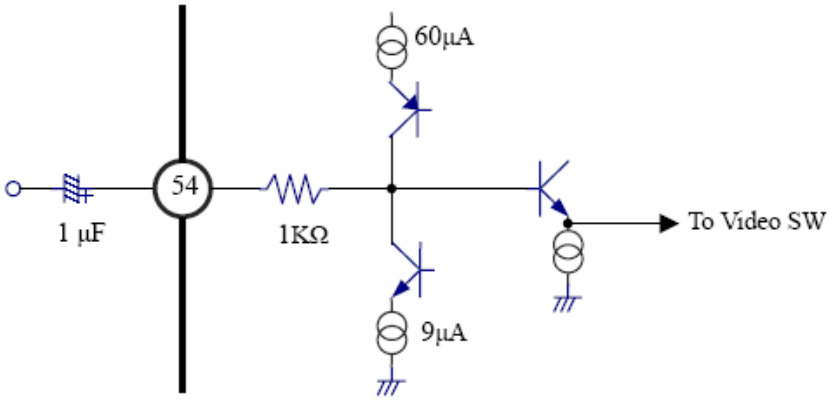


PIN 54 EXT VIDEO INPUT & Y INPUT in S-VHS MODE)

This is an external video input pin. (Y INPUT in S-VHS MODE at VIN/EXT RGB SW=0)

The pedestrian level of input signal is clamped at 1/2 Vcc by charging & discharging external capacitor.

This pin also become the input pin of Y signal in S-VHS mode at VIN/EXT RGB SW=0



PIN 55 (VIDEO CHROMA DEFLECTION VCC)

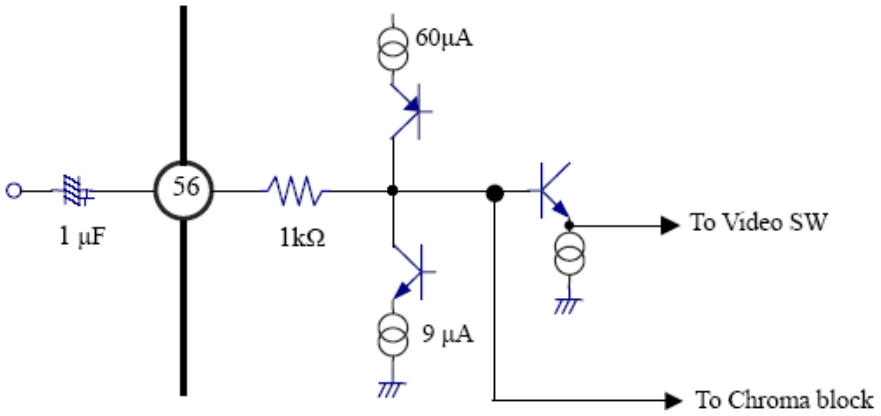
This is a Vcc pin of video/ chrome/ deflection block.

Connect a 5V to this pin.

PIN 56 (INT. VIDEO INPUT & CHROMA SIGNAL INPUT IN S-VHS MODE)

This is an internal video input pin. . (C INPUT in S-VHS MODE at VIN/EXT RGB SW=0)

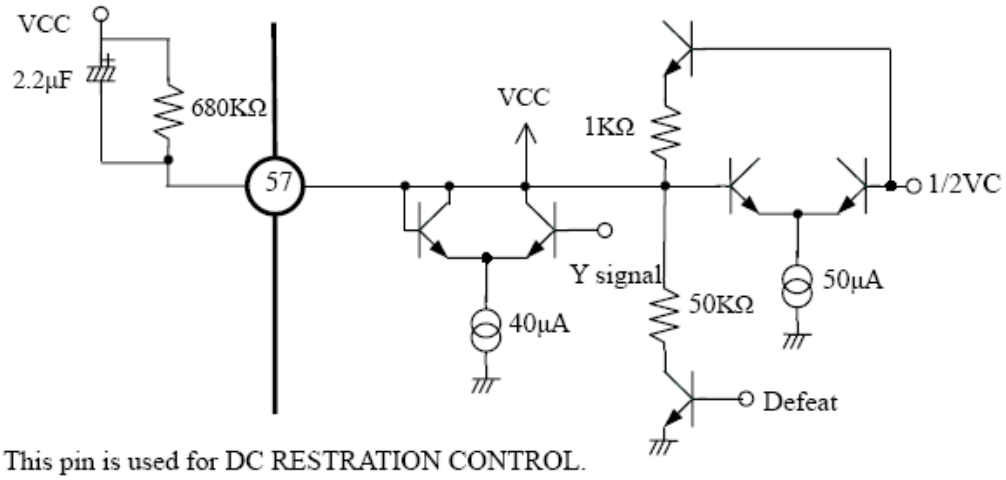
The pedestal level of input signal is clamped at 1/2 Vcc by charging & discharging external capacity. This pin also become the input pin of C signal in S-VHS mode at VIN/EXT RGB SW=0



PIN 57(BLACK STRETCH FILTER)

This is a filter pin for black peak level detection in black stretch circuit.

The capacitor is charging during black peak period, and discharging via external CR exclude black peak period. The DC level of the output and the gain of black stretch will be reduced if the value of time constant is large.



This pin is used for DC RESTRATION CONTROL.

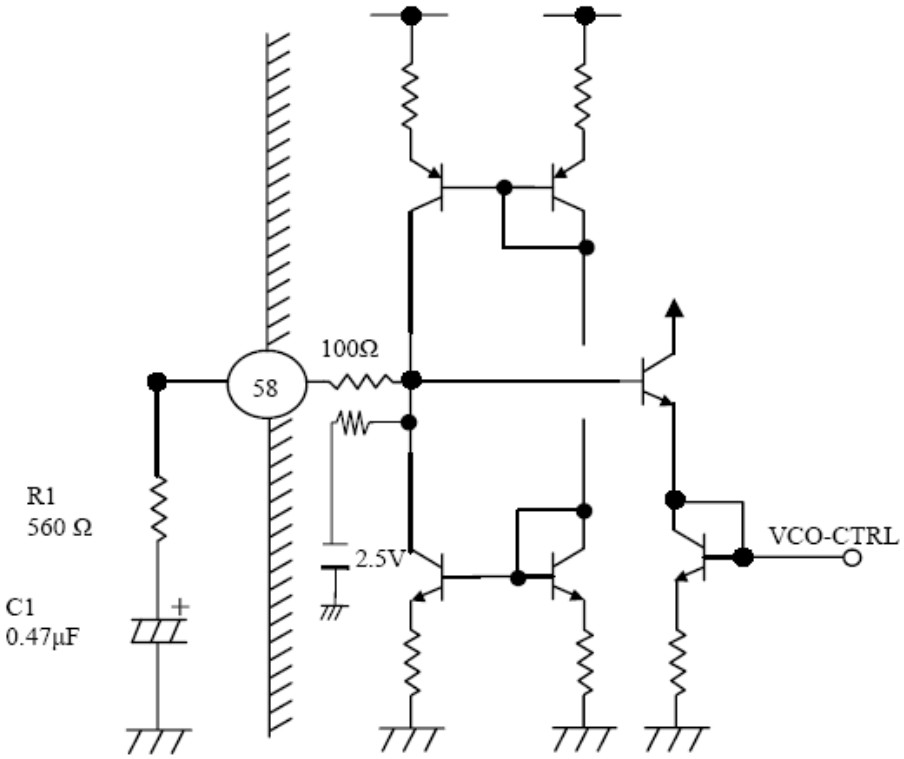
PIN 58 (PIF APC FILTER)

This is an APC filter pin for PLL circuit.

The output is achieved from the collector of the current mirror circuit. First, the APC loop gain is determined by the time constant (R1 & C1).

If R1 is increased, the loop gain will increase and the pull-in range will increase as well. But, the characteristic of the noise sensitivity will degrade at the same time, therefore our recommended value for R1 is 560Ω.

On the other hand, the time constant of APC loop is determined by the capacitor C1 and the internal resistor inside the IC. Therefore, if the capacitor C1 is variable, the time constant of loop will change largely by every step. We recommended the value of C1 is 0.47uF.

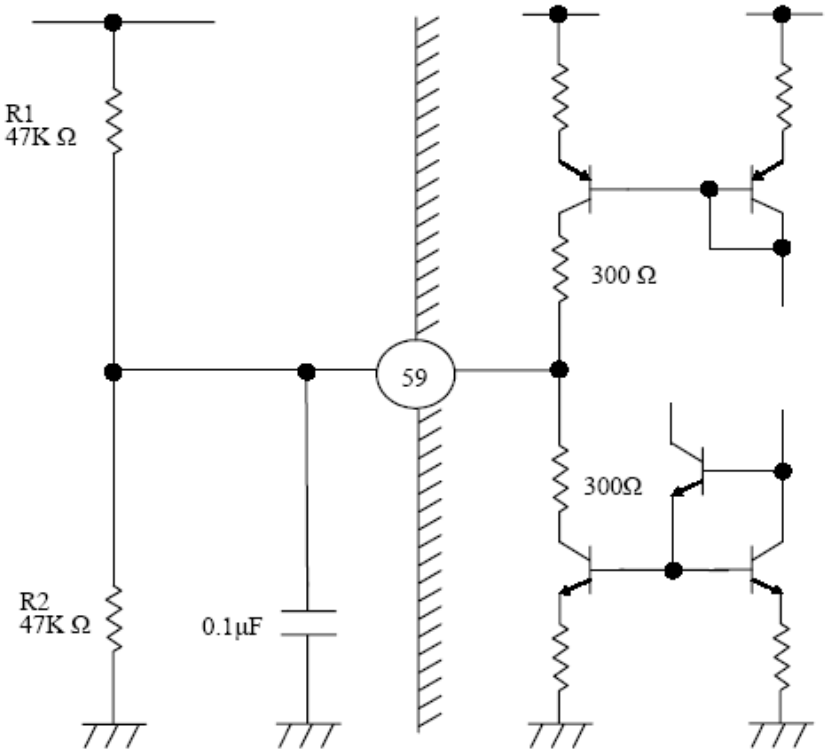


PIN 59 (AFT OUTPUT)

This is an AFT output pin.

The output is achieved from the collector of the current mirror circuit. The control sensitivity of AFT can be adjusted by the external resister (R1, R2). The voltage of pin 59 is determined by the external resister (R1, R2). The control sensitivity of AFT is about 25mV/KHz when R1 = R2 = 47KΩ.

The BUS control is fixed at "L" when IF PLL is unlocked.



The circumference circuit of pin 59

PIN 60 (VIDEO OUTPUT)

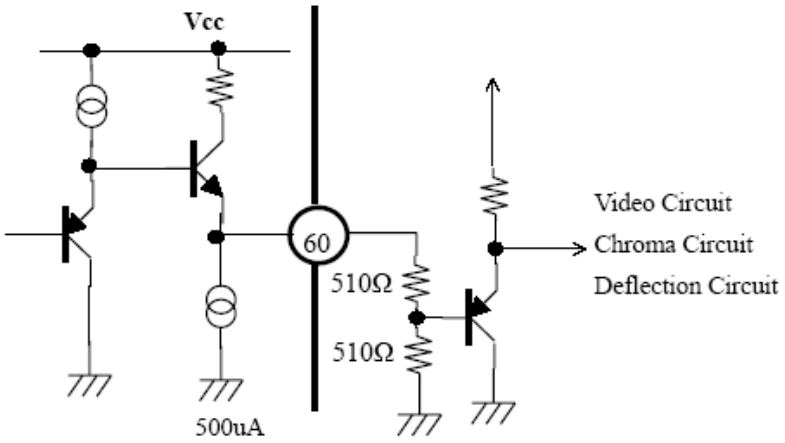
This is a video output pin.

The output is a low impedance circuit.

- The video DC output is 3.7V when there is no signal.
- Sync Tip Voltage is 1.4V
- The video amplitude is 2.0Vpp
  In addition, there is a Black Noise Inverter Circuit built-in in this IC.
- The threshold voltage of Black Noise Inverter is 0.8 V
- The replacement voltage of Black Noise Inverter is 1.8 V

The built-in sound trap is linked with the BUS (SIF SYSTEM) so that the trap frequency is set automatically depending on the SIF frequency selected.

In order to prevent the unsatisfied drive capacity of amplitude matching (1Vpp) and load (video circuit, chroma circuit, deflection circuit), we recommend application circuit below:



The circumference circuit of pin 60

PIN 61 (RF AGC OUTPUT)

This is a RF AGC output pin.

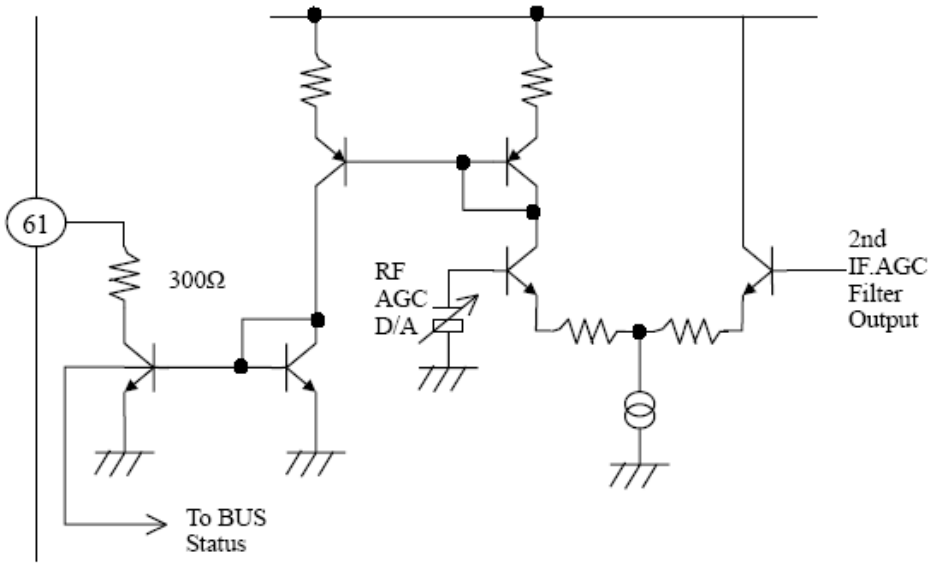
The reference voltage, which is controlled by RF AGC D/A, and the IF AGC voltage is input into differential amplifier and the output is obtained at the open collector.

The time constant is determined by the value of the external R & C.

The maximum drive current of Q1 is 1mA.

The maximum DC voltage of pin61 is 9V.

Please change the value of R for the correct DC voltage depending on the specification of tuner.

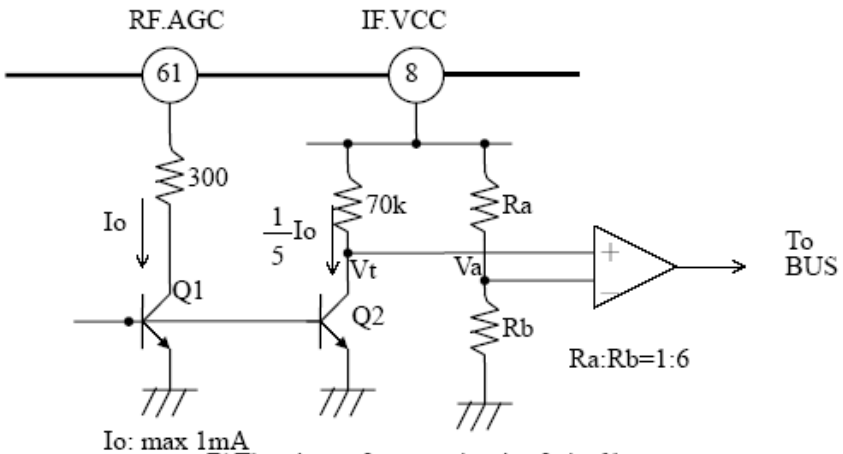


A) The circumference circuit of pin 61

A comparator, which is used for BUS status is built-in this IC. The reference voltage Va is set as Vcc*(6/7) and compare with voltage Vt below:

$$Vt = Vcc - \{Io*(1/5)*70K\Omega\}$$

* Io is the output current of pin 61.



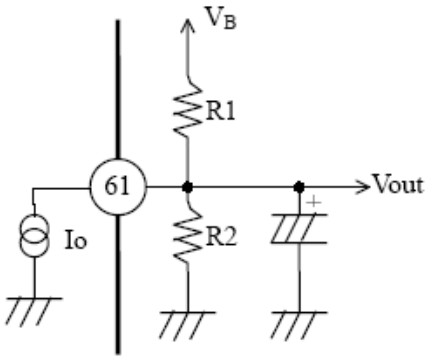
B)The circumference circuit of pin 61

〔 The example application circuit 〕

Ra:Rb=1:6 ,Vcc=5V so Va=4.3V

RFAGC Bus status change at Va=Vt

Io at this condition is 50uA



$$Vout \quad \frac{R2}{R1+R2} \quad (V_B\text{-}Io \cdot R1)$$

If the BUS status change '0⇔1' , Vout voltage is 6V.

(Condition : V_B = 9V, R1 = 30KΩ, R2 = 120KΩ , Io=50uA)

PIN 62 (IF GROUND)

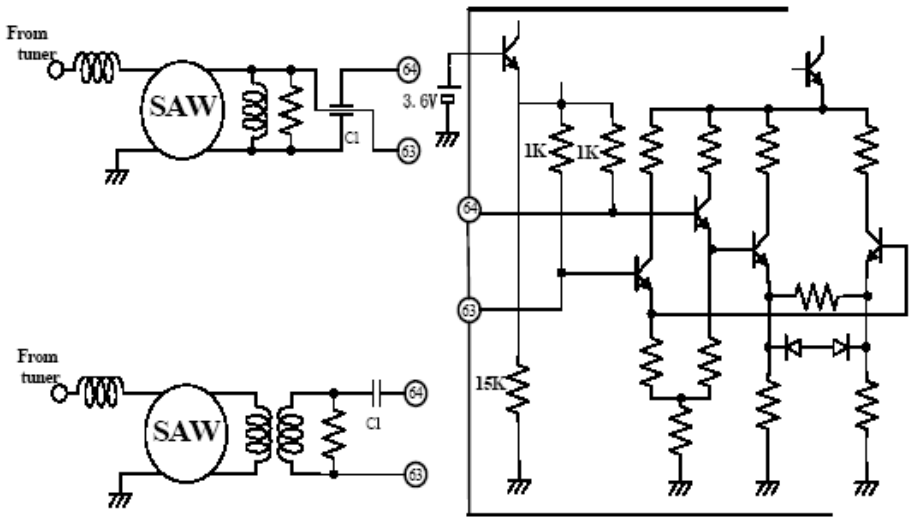
This is the ground of IF circuit.

PIN 63,64 (VIF AMP INPUT)

This is a VIF input pin.

The input impedance Ri is about 1.5KΩ and the input capacity is about 5pF.

This is a balanced input and it needs a C1(0.01uF) capacitor for coupling. The balanced error generated in the SAW filter and the printed plate can be canceled and the weak field characteristic may be improved by using C1 to cross the IC input pin layout on the printed plate.



The circumference circuit of pin 63 & 64

1.5 <<μ-COM Block>>

1.5.1 Internal communication

1. Bus control of LA76936 is controlled by the internal communication (I^2C) of μCOM. The internal communications ports of μ COM are assigned special functions such as DATA for P31, CLOCK for P32.

2. The internal communications ports (P31, P32) of μ COM are internally connected to general-purpose ports (P12 : DATA, P13 : CLOCK) through register control, so that the Bus Control can be controlled by an external device.

3. The terminal AN3 of μ COM is internally connected to the terminal AFT (PInt18) of BIP.

4. The terminal P33 of μ COM is internally connected to the terminal C_SYNC (PInt01) of BIP.

1.5.2 Recommended Oscillation Circuit and Sample Characteristics. (XT1,XT2)

The sample oscillation circuit characteristics in the table below are based on the following conditions:

- Recommended circuit parameters are verified by an oscillator manufacturer using a Sanyo provided oscillation evaluation board.
- Sample characteristics are the result of the evaluation with the recommended circuit parameters connected externally.

Recommended oscillation circuit and sample characteristics (Ta = -10 to +65°C)

Frequency	Manu-facturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	Oscillation stabilizing time		Notes
			C1	C2	Rf	Rd		typ.	max	
32.768kHz	Seiko Epson	C-002RX	T.B.D	T.B.D	T.B.D	T.B.D	4.5 – 5.5V	T.B.D	T.B.D	

Notes The oscillation stabilizing time period is the time until the VCO oscillation for the internal system becomes stable after the following conditions. (Refer to Figure 2.)

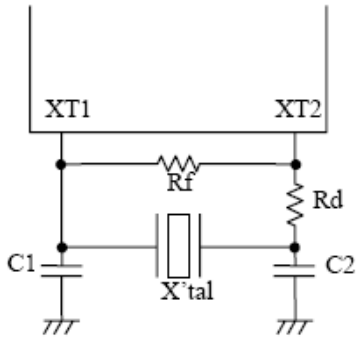
1. The VDD becomes higher than the minimum operating voltage after the power is supplied.
2. The HOLD mode is released.

The sample oscillation circuit characteristics may differ applications. For further assistance, please contact with oscillator manufacturer with the following notes in your mind.

- Since the oscillation frequency precision is affected by wiring capacity of the application board, etc., adjust the oscillation frequency on the production board.
- The above oscillation frequency and the operating supply voltage range are based on the operating temperature of -10°C to +65°C. For the use with the temperature outside of the range herein, or in the applications requiring high reliability such as car products, please consult with oscillator manufacturer.
- When using the oscillator which is not shown in the sample oscillation circuit characteristics, please consult with Sanyo sales personnel.

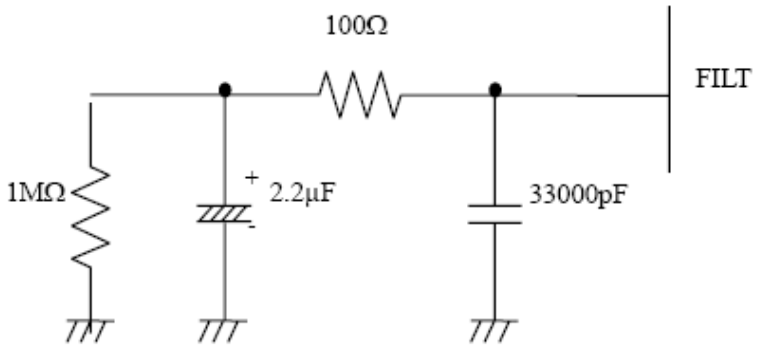
Since the oscillation circuit characteristics are affected by the noise or wiring capacity because the circuit is designed with low gain in order to reduce the power dissipation, refer to the following notices.

- The distance between the clock I/O terminal (XT1 terminal XT2 terminal) and external parts should be as short as possible.
- The capacitors' VSS should be allocated close to the microcontroller's GND terminal and be away from other GND.
- The signal lines with rapid state changes or with large current should be allocated away from the oscillation circuit.



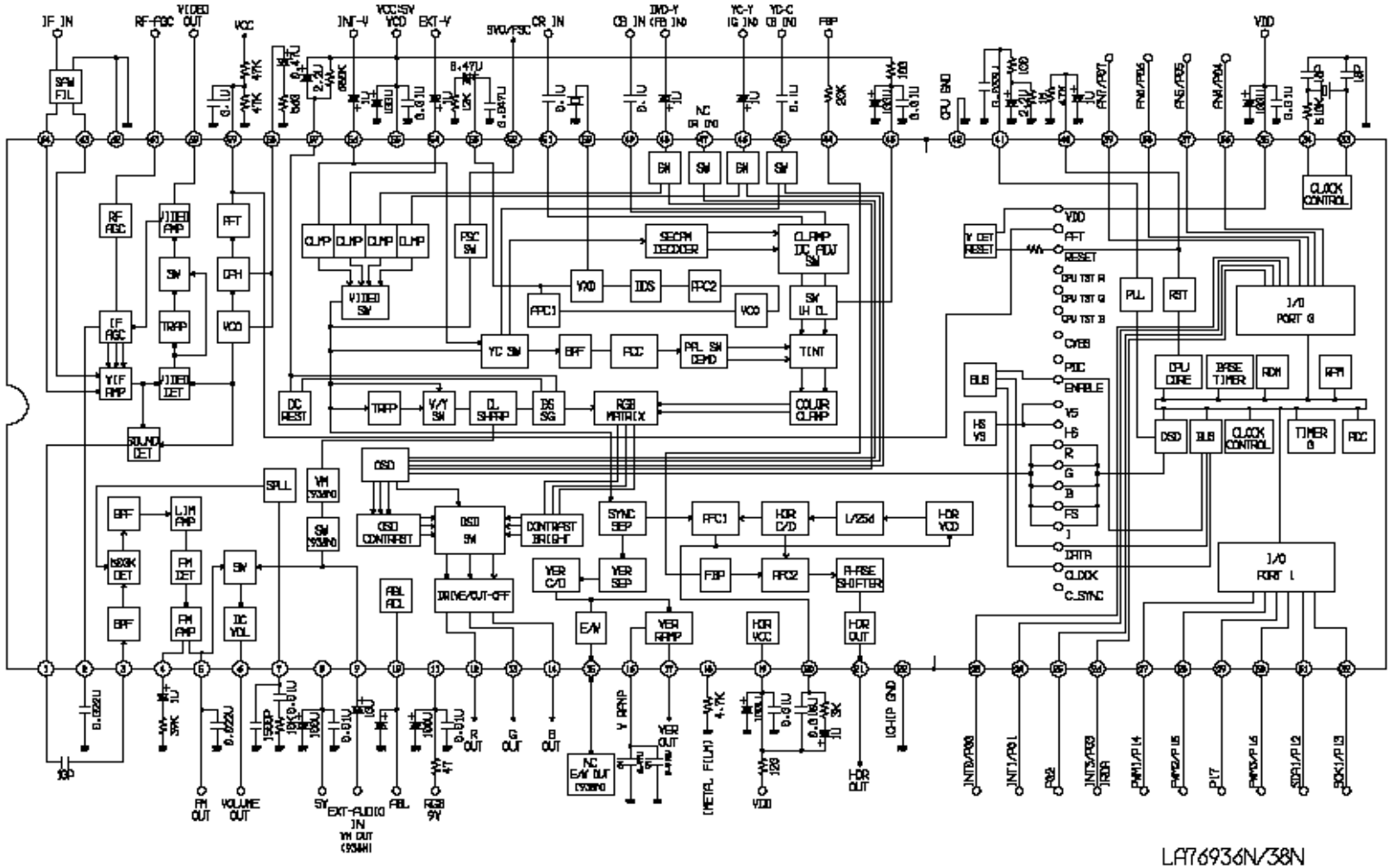
Recommended oscillation circuit.

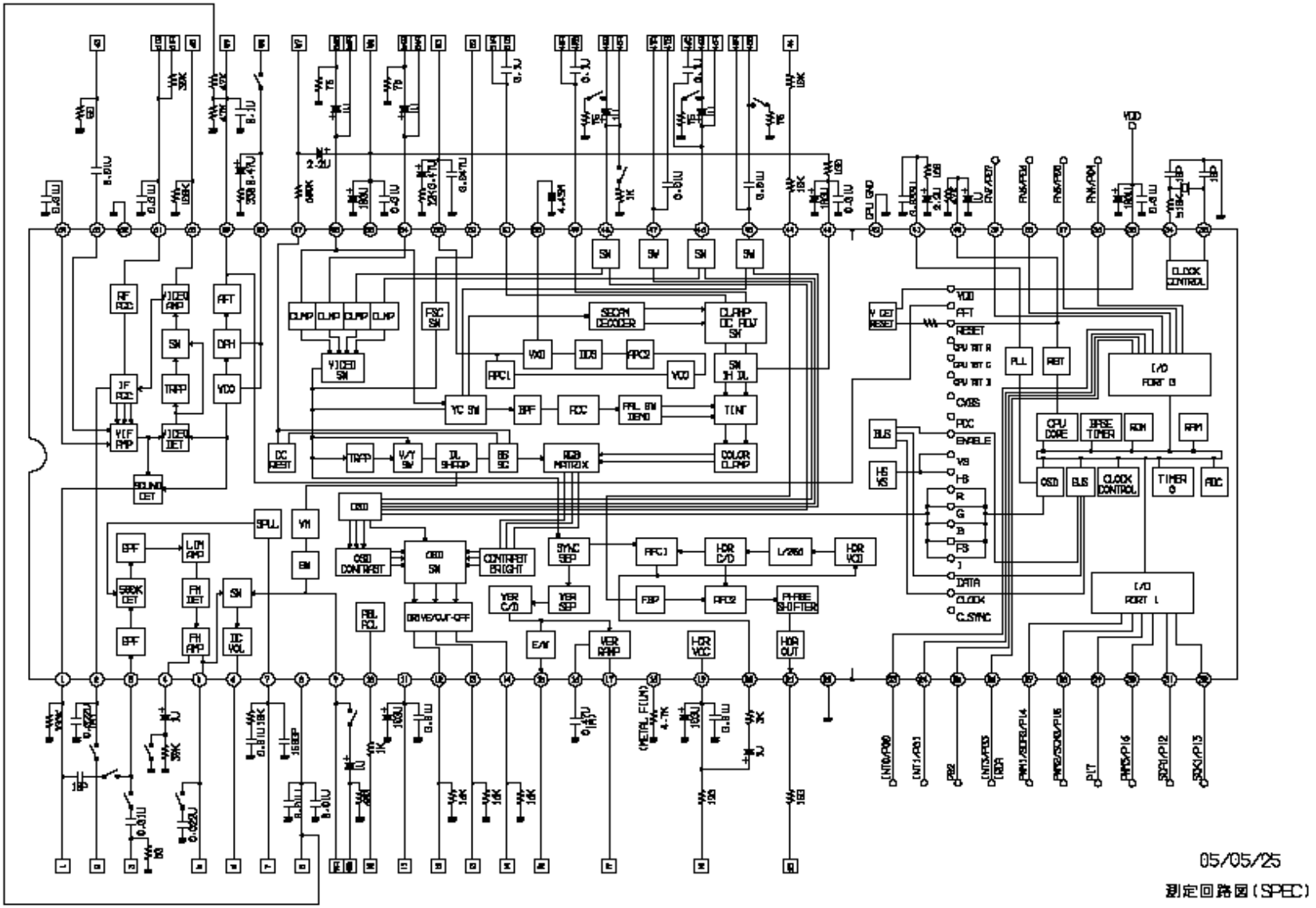
1.5.3 FILT recommended circuit



FILT recommended circuit

(Note) Place FILT parts on board as close to the microcontroller as possible.


IF IN
RF-AGC
VIDEO OUT
VCC
INT-V
VCC/5V
EXT-Y
SVO/FSC
CR IN
CB IN
DVD-Y (FB IN)
YC-Y (G IN)
YC-C (B IN)
FBP
VDD
CPU GND
SIF FIL
RF AGC
VIDEO AMP
AFT
IF AGC
TRAP
DPH
VCO
YIF AMP
VIDEO DET
SOUND DET
CLAMP
PSC SW
VIDEO SW
SECAM DECODER
CLAMP DC FDU SW
VCO
APC1
IDS
APC2
SW (H CL)
YC SW
BPF
ACC
PAL SW DEMO
TINT
DC REST
TRAP
Y/Y SW
CL SHARP
IBS SW
RGB MATRIX
COLOR CLAMP
OSD
OSD CONTRAST
OSD SW
CONTRAST BRIGHT
SYNC SEP
APC1
H-DR C/D
1/256
H-DR VCO
VER C/D
VER SEP
APC2
H-PHASE SHIFTER
DRIVE/CUT-OFF
E/W
VER RAMP
H-DR VCC
H-DR OUT
SPLL
VM SOUND
SW SOUND
LIM AMP
FM DET
FM AMP
SW
IIC VOL
ABL ACL
Y RAMP
VER OUT
H-DR OUT
CHIP GND
CLOCK CONTROL
V DET RESET
RESET
CPU TST A
CPU TST B
CPU TST C
CVBS
PDC
ENABLE
VS
HS
R
G
B
FS
DATA
CLOCK
C.SYNC
BUS
HS VS
PLL
RST
I/O PORT B
CPU CORE
BASE TIMER
ROM
RAM
DSD
IBUS
CLOCK CONTROL
TIMER B
ADC
I/O PORT A
FM OUT
VOLUME OUT
SW
EXT-AUDIO IN
YM OUT
ABL
RGB 5V
R OUT
G OUT
B OUT
E/W OUT
V RAMP
VER OUT
METAL FILM
VDD
H-DR OUT
INT0/P00
INT1/P01
P02
INT3/P03
TRDA
PWM1/P14
PWM2/P15
P17
PWM5/P16
SDA1/P12
SCK1/P13
LA76936N/38N
CPU+1CHIP PAL/NTSC/SECAM 06/01/11


05/05/25
測定回路図(SPEC)

2. EEPROM 24C08 (N602)

2.1 Features

• Write Protect Pin for Hardware Data Protection

– Utilizes Different Array Protection Compared to the AT24C08A

• Low-voltage and Standard-voltage Operation

– 2.7 (VCC = 2.7V to 5.5V)

• Internally Organized 1024 x 8 (8K)

• Schmitt Trigger, Filtered Inputs for Noise Suppression

• Bi-directional Data Transfer Protocol

• 400 kHz (2.7V) Clock Rate for AT24C08A

• 16-byte Page Write Modes

• Partial Page Writes are Allowed

• Self-timed Write Cycle (10 ms Max)

• High Reliability

– Endurance: One Million Write Cycles

– Data Retention: 100 Years

• Automotive Grade, Extended Temperature and Lead-Free Devices Available

• 8-lead PDIP Packages

2.2 Description

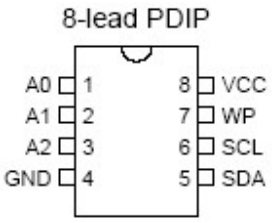
The AT24C08A provides 8192 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 1024 words of 8 bits each. In the AT24C08A, the 8K is internally organized with 64 pages of 16 bytes each. Random word addressing requires an 10-bit data word address.

The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C08A is available in space saving 8-lead PDIP package and is accessed via a 2-wire serial interface. In addition, the AT24C08A is available in 2.7V (2.7V to 5.5V) supply.

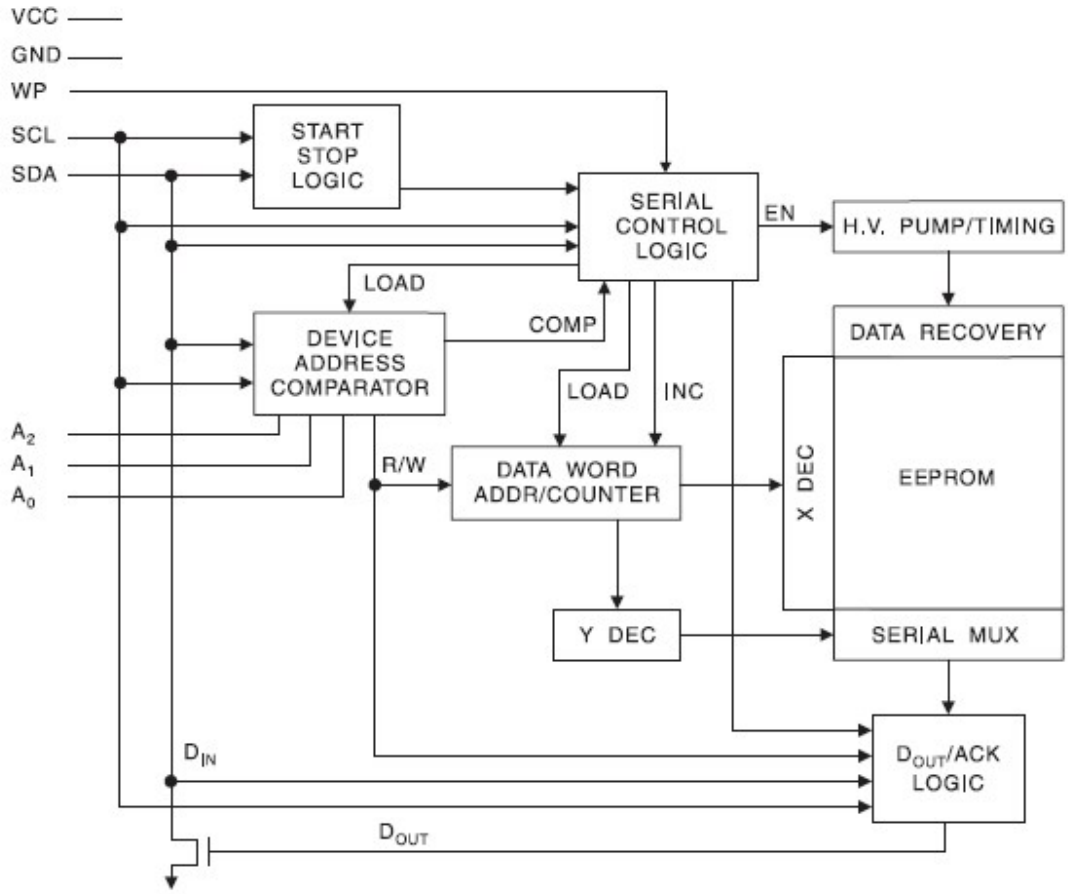
2.3 Pin Configurations

Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No-connect



2.4 Block Diagram



2.5 Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

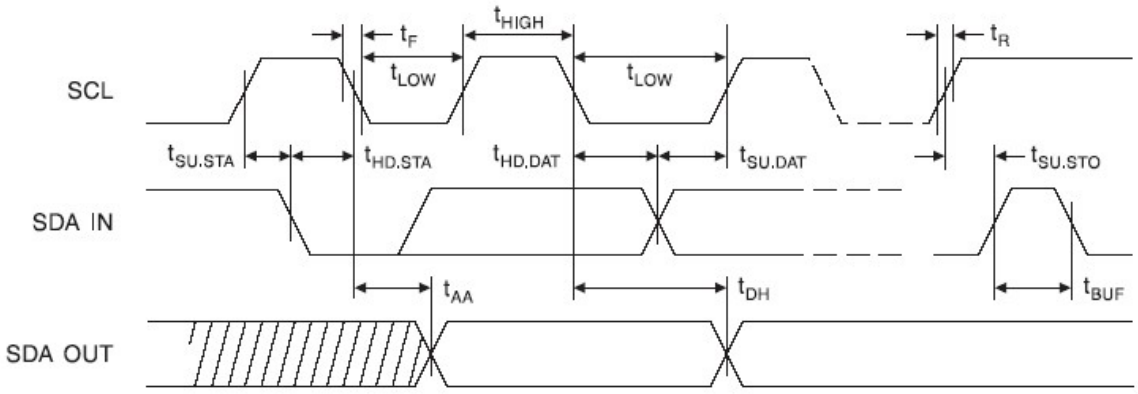
DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs. The AT24C08A does not use the device address pins, which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no-connects.

WRITE PROTECT (WP): The AT24C08A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to VCC, the write protection feature is enabled and operates as shown in the following table.

2.6 Device Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below.

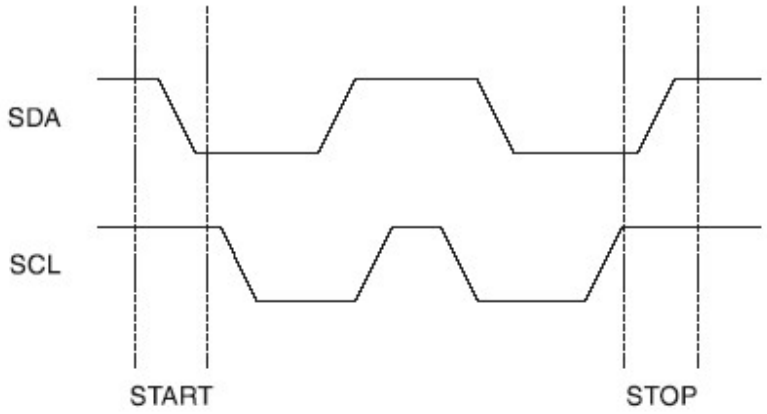
Bus Timing (SCL: Serial Clock, SDA: Serial Data I/O)



Start Condition: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command.

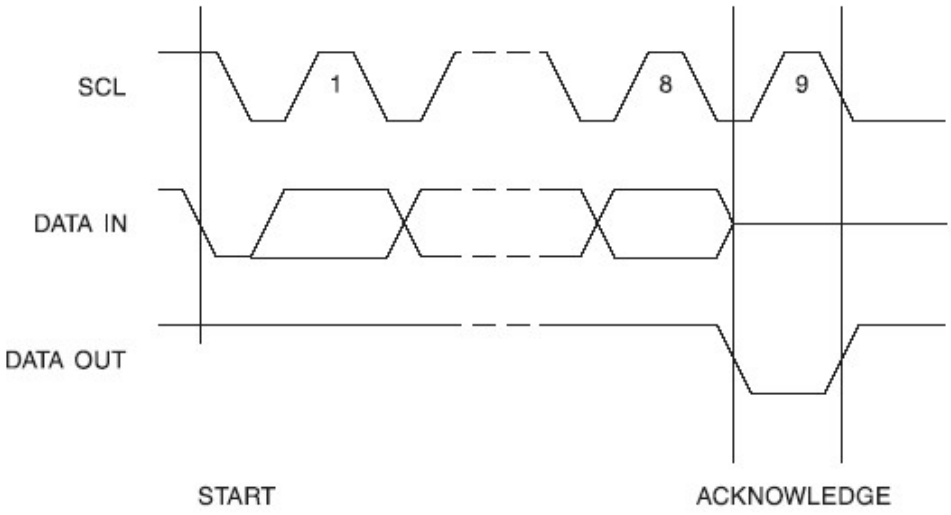
Stop Condition: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode.

Start and Stop Definition



Acknowledge: All addresses and data words are serially transmitted to and from the EEPROM in 8 bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Output Acknowledge

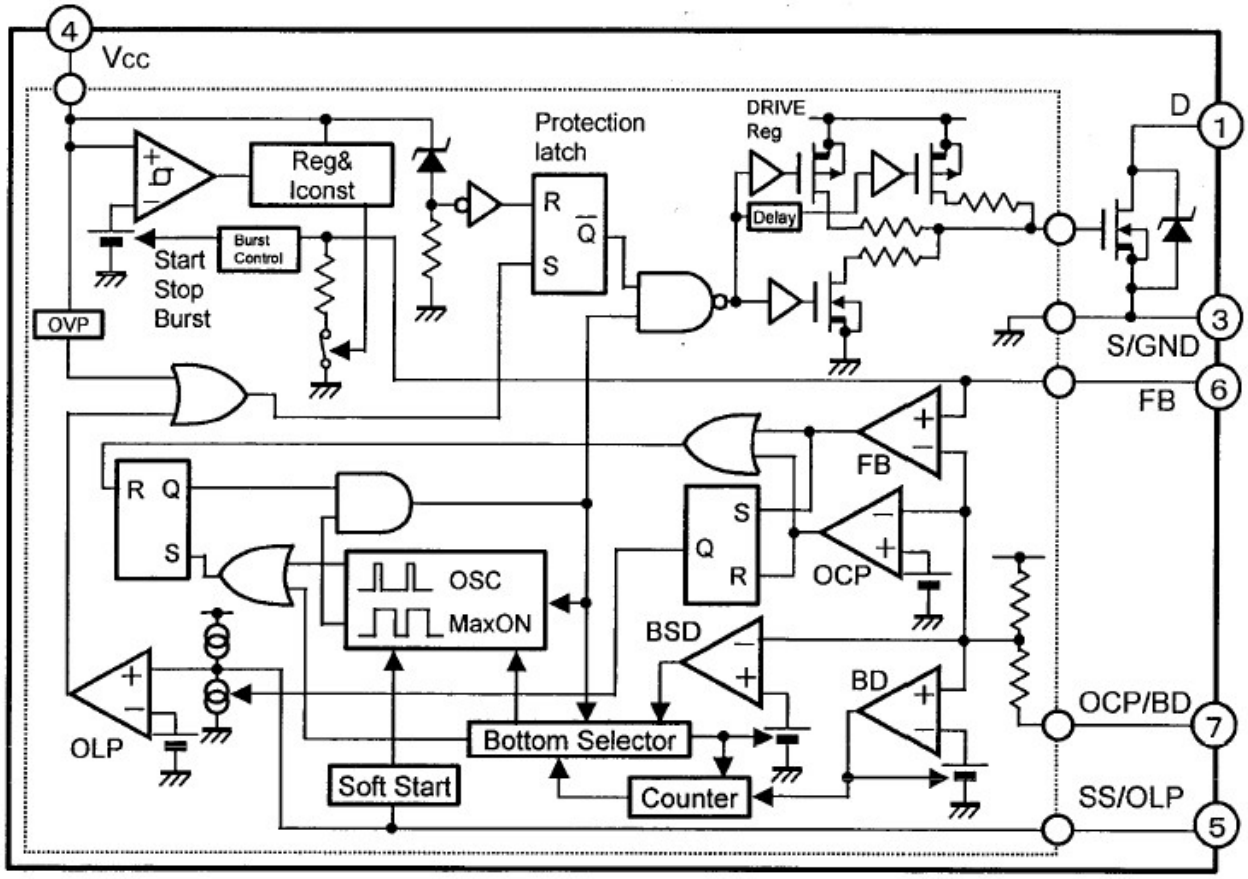


Standby Mode: The AT24C08A features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

Memory Reset: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps: (a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

3. SWITCH POWER IC －STR-W6753(N901)

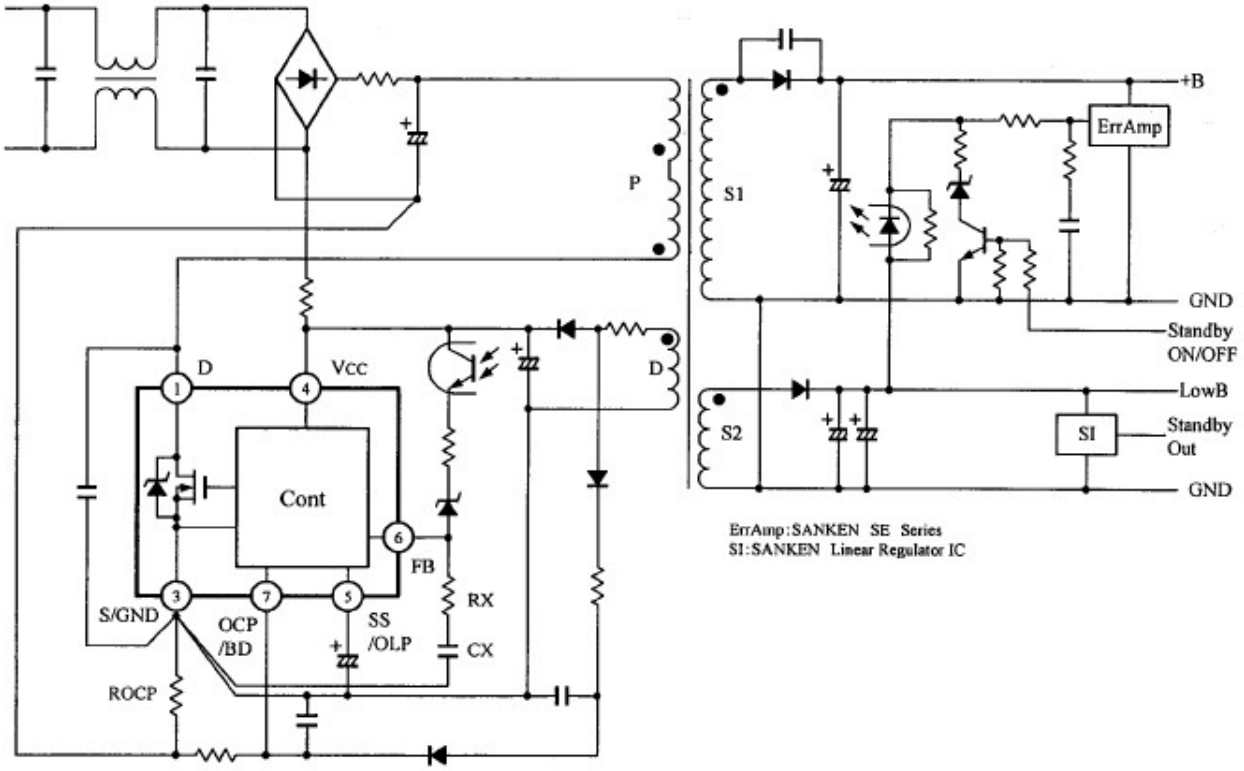
3.1 Block Diagram



3.2 Functions of each terminal

端子番号 Terminal No.	端子記号 Symbols	名称 Descriptions	機　　能 Functions
1	D	ドレイン端子 Drain terminal	MOSFET ドレイン MOSFET drain
3	S/GND	ソース/グランド端子 Source /Ground terminal	MOSFET ソース及びグランド MOSFET Source / Ground
4	Vcc	電源端子 Power supply terminal	制御回路電源入力 Input of power supply for control circuit
5	SS/OLP	ソフトスタート／過負荷時遅延設定端子 Delay at Overload/Soft Start set up Terminal	過負荷検出及びソフトスタート動作の時間設定 Overload Protection and Soft Start Operation Time set up
6	FB	フィードバック端子 Feedback terminal	定電圧制御信号入力/間欠発振制御 Constant Voltage Control Signal Input, Burst(intermittent) mode Oscillation Control
7	OCP/BD	過電流保護入力／ボトム検出端子 Overcurrent Protection Input /Bottom Detection Terminal	過電流検出信号入力/ボトム検出信号入力 Overcurrent Detection Signal Input /Bottom Detection Signal Input

3. 3 Example Application Circuit



4. VERTICAL DEFLECTION BOOSTER—STV9302B/LA78040 (N440)

4.1 Main Features

■ Power Amplifier

■ Flyback Generator

■ Output Current up to 2 App

■ Thermal Protection

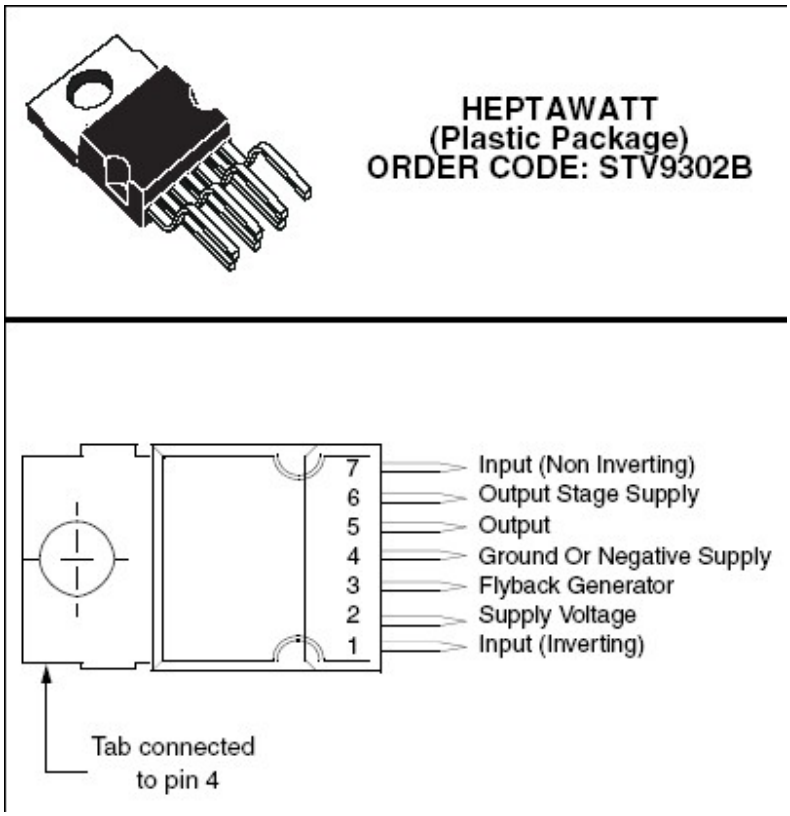
4. 2 Description

The STV9302B is a vertical deflection booster designed for TV (50-60 Hz) applications.

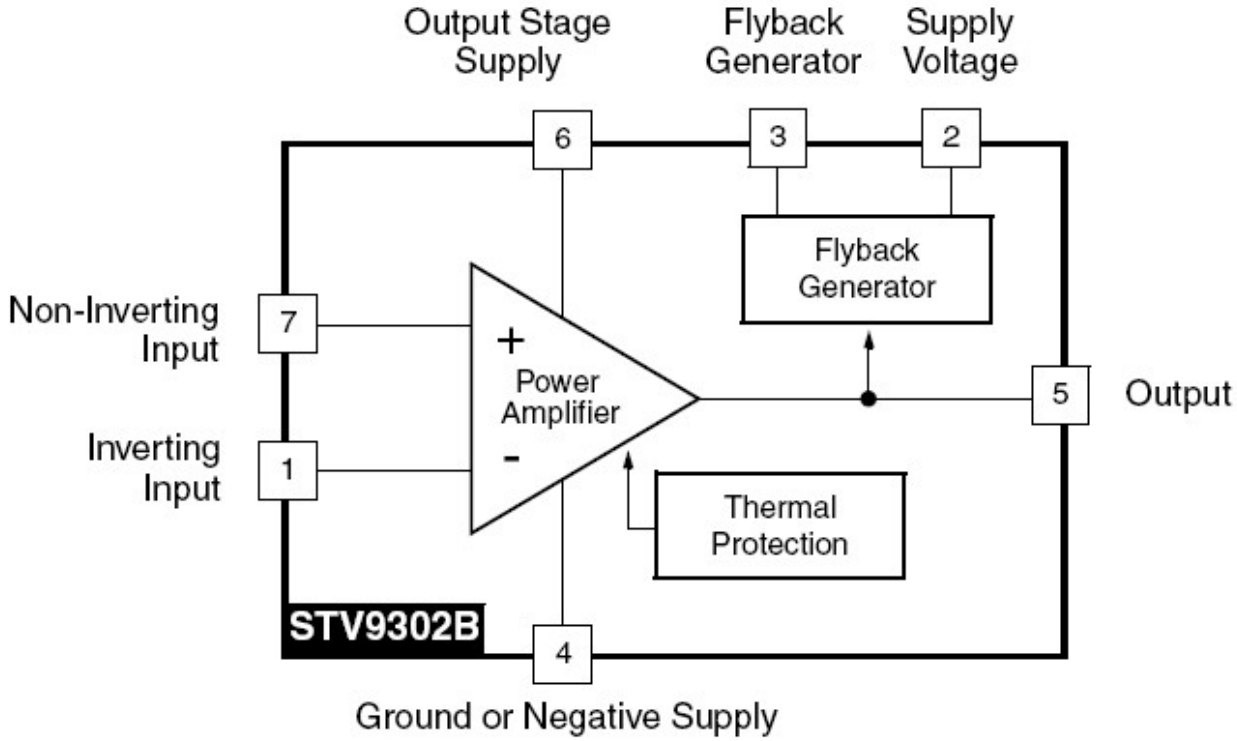
This device, supplied with up to 35 V, provides up to 2 App output current to drive the vertical deflection yoke.

The internal flyback generator delivers flyback voltages up to 70 V.

4. 3 Pin Configuration



4.4 Internal Block Diagram



4. 5 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Voltage			
V_S	Supply Voltage (pin 2) - Note 1 and Note 2	40	V
V_5, V_6	Flyback Peak Voltage - Note 2	70	V
V_3	Voltage at Pin 3 - Note 2, Note 3 and Note 6	-0.4 to (V_S + 3)	V
V_1, V_7	Amplifier Input Voltage - Note 2, Note 6 and Note 7	- 0.4 to (V_S + 2) or +40	V
Current			
I_O (1)	Output Peak Current at f = 50 to 65 Hz, t ≤10 µs - Note 4	±5	A
I_O (2)	Output Peak Current non-repetitive - Note 5	±2	A
$I_{3\ Sink}$	Sink Current, t < 1 ms - Note 3	1.5	A
$I_{3\ Source}$	Source Current, t < 1 ms	1.5	A
I_3	Flyback pulse current at f = 50 to 65 Hz, t ≤10 µs - Note 4	±5	A
ESD Susceptibility			
ESD1	Human body model (100 pF discharged through 1.5 kΩ)	2	kV
ESD2	EIAJ Standard (200 pF discharged through 0 Ω)	300	V
Temperature			
T_s	Storage Temperature	-40 to 150	°C
T_j	Junction Temperature	+150	°C

Note: 1. Usually the flyback voltage is slightly more than 2 x V_S. This must be taken into consideration when setting V_S.

2. Versus pin 4

3. V3 is higher than V_S during the first half of the flyback pulse.

4. Such repetitive output peak currents are usually observed just before and after the flyback pulse.

5. This non-repetitive output peak current can be observed, for example, during the Switch-On/Switch-Off phases. This peak current is acceptable providing the SOA is respected (Figure 8 and Figure 9).

6. All pins have a reverse diode towards pin 4, these diodes should never be forward-biased.

7. Input voltages must not exceed the lower value of either V_S + 2 or 40 volts.

4. 6 Electrical Characteristics

(V_S = 32 V, T_{AMB} = 25°C, unless otherwise specified)

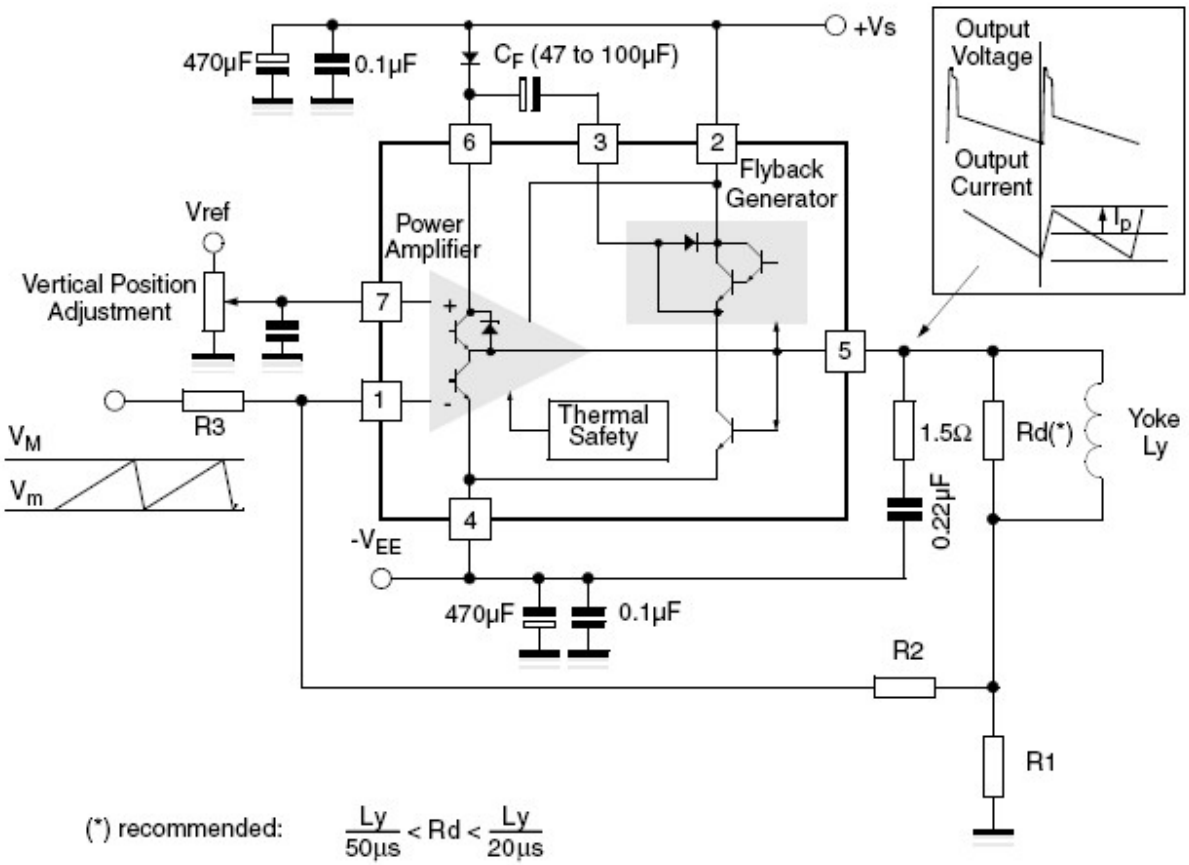
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
Supply							
V_S	Operating Supply Voltage Range (V_2-V_4)	Note 8	10		35	V	
I_2	Pin 2 Quiescent Current	I_3 = 0, I_5 = 0		5	20	mA	1
I_S	Pin 6 Quiescent Current	I_3 = 0, I_5 = 0, V_6 =35v	8	19	50	mA	1
Input							
I_1	Input Bias Current	V_1 = 1 V, V_7 = 2.2 V		- 0.6	-1.5	µA	1
I_7	Input Bias Current	V_1 = 2.2 V, V_7 = 1 V		- 0.6	-1.5	µA	
V_{IR}	Operating Input Voltage Range		0		V_S - 2	V	
V_{IO}	Offset Voltage			2		mV	
$\Delta V_{IO}/dt$	Offset Drift versus Temperature			10		µV/°C	
Output							
I_O	Operating Peak Output Current	f = 50 to 60 Hz			±1	A	
V_{5L}	Output Saturation Voltage to pin 4	I_5 = 1 A		1	1.7	V	3
V_{5H}	Output Saturation Voltage to pin 6	I_5 = -1 A		1.8	2.3	V	2
Miscellaneous							
G	Voltage Gain		80			dB	
V_{D5-6}	Diode Forward Voltage Between pins 5-6	I_5 = 1 A		1.4	2	V	
V_{D3-2}	Diode Forward Voltage between pins 3-2	I_3 = 1 A		1.3	2	V	
V_{3SL}	Saturation Voltage on pin 3	I_3 = 20 mA		0.4	1	V	3
V_{3SH}	Saturation Voltage to pin 2 (2nd part of flyback)	I_3 = -1 A		2.1		V	

8. In normal applications, the peak flyback voltage is slightly greater than 2 x (V_S - V_4). Therefore, (V_S - V_4) = 35 V is not allowed without special circuitry.

4. 7 DC-coupled Application

The yoke can be coupled either in AC or DC. IN our TV, it is DC-coupled application.

When DC coupled , the display vertical position can be adjusted with input bias. On the other hand, 2 supply sources (VS and -VEE) are required.



For calculations, treat the IC as an op-amp, where the feedback loop maintains V1 = V7.

4.7.1 Centering

Display will be centered (null mean current in yoke) when voltage on pin 7 is (R_1 is negligible):

$$V_7 = \frac{V_M + V_m}{2} \times \left(\frac{R_2}{R_2 + R_3} \right)$$

4.7.2 Peak Current

$$I_P = \frac{(V_M - V_m)}{2} \times \frac{R_2}{R_1 x R_3}$$

Example: for $V_m = 2$ V, $V_M = 5$ V and $I_P = 1$ A

Choose R_1 in the1 Ω range, for instance R_1=1 Ω

From equation of peak current: $\frac{R_2}{R_3} = \frac{2 \times I_P \times R_1}{V_M - V_m} = \frac{2}{3}$

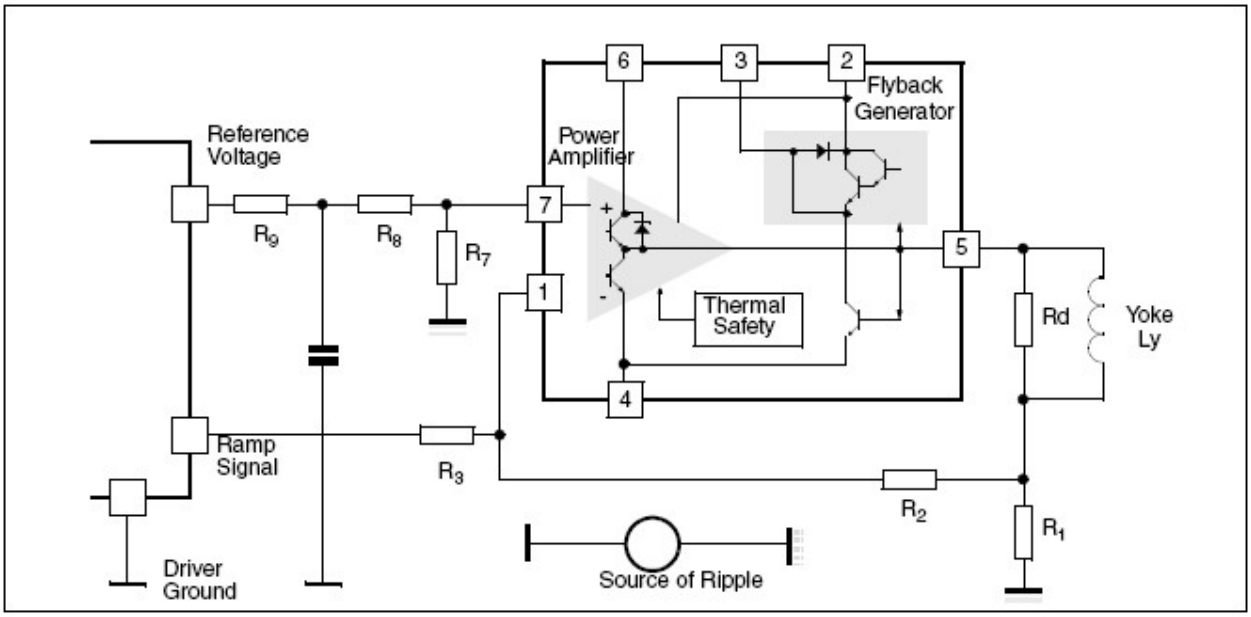
Then choose R_2 or R_3. For instance, if R_2 = 10 kΩ then R_3 = 15 kΩ

Finally, the bias voltage on pin 7 should be:

$$V_7 = \frac{V_M + V_m}{2} \times \frac{1}{1 + \frac{R_3}{R_2}} = \frac{7}{2} \times \frac{1}{2.5} = 1.4V$$

4.7.3 Ripple Rejection

When both ramp signal and bias are provided by the same driver IC, you can gain natural rejection of any ripple caused by a voltage drop in the ground, if you manage to apply the same fraction of ripple voltage to both booster inputs. For that purpose, arrange an intermediate point in the bias resistor bridge, such that (R8 / R7) = (R3 / R2), and connect the bias filtering capacitor between the intermediate point and the local driver ground. Of course, R7 should be connected to the booster reference point, which is the ground side of R1.



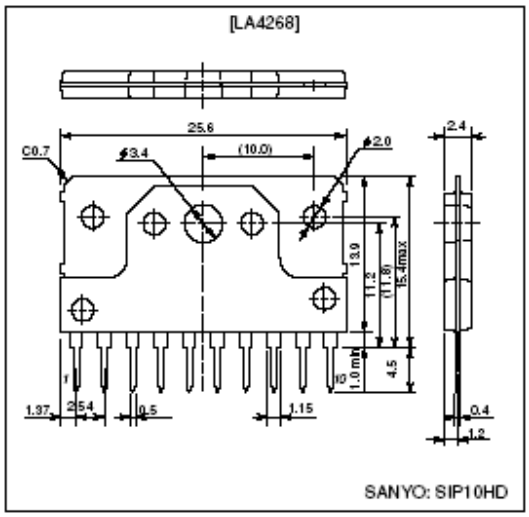
5. AUDIO POWER AMPLIFIER－LA4268/LA4278(N201)

5.1 LA4268

5.1.1 Overview

The LA4268 is a 10 W power amplifier intended for televisions.
This IC has a series of pin compatible monaural and 2-channel power amplifiers, thus allows the end product to use a common circuit boad.

5.1.2 Package Dimensions



5.1.3 Specifications

Maximum Ratings at Ta = 25°C

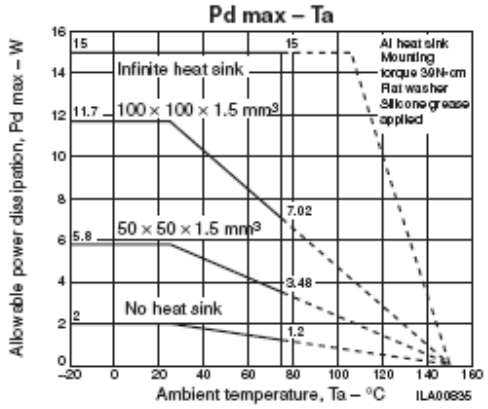
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}	Rg = 0	35	V
Maximum output current	I_O peak		2.5	A
Allowable power dissipation	Pd max	Infinite heat sink	15.0	W
Thermal resistance	θj-c		3.0	°C/W
Operating temperature	Topr		−20 to +75	°C
Storage temperature	Tstg		−40 to +150	°C

Operating Conditions at Ta = 25°C

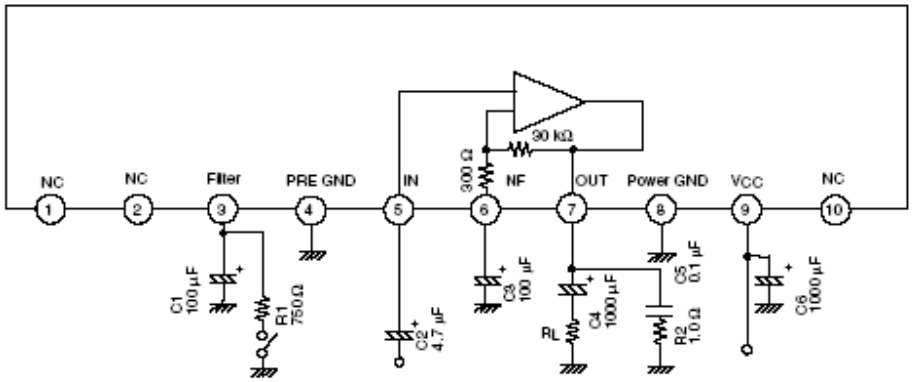
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		28	V
Load resistance	R_L		8	Ω
Operating supply voltage range	V_{CC} op	Range does not exceed Pd	10 to 34	V

Operating Characteristics at Ta = 25°C, V_{CC} = 28 V, R_L = 8 Ω, f = 1 kHz, Rg = 600 Ω, with specified board, in specified circuit

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}	Rg = 0		35	70	mA
Voltage gain	VG	V_O = 0 dBm	38	40	42	dB
Total harmonic distortion	THD	P_O = 0.5 W		0.1	0.8	%
Output noise voltage	V_{NO}	Rg = 10 kΩ, BPF = 20 Hz to 20 kHz		0.25	1.0	mV
Output power	P_O	THD = 10 %	8.0	10		W
Ripple rejection	SVRR	Rg = 0, fr = 100 Hz, Vr = 0.5 Vrms	45	55		dB



5.1.4 Pin Assignment Equivalent Diagram



* For Muting, add a resistor between pin 3 and GND. 750 Ω for the LA4266/67/68, 200 Ω for the LA4276/77.

C1: Ripple filter capacitor
Decreasing the capacitance value reduces ripple rejection. This capacitor also affects the starting time; decreasing the capacitance value makes the starting time earlier.

C2: Input capacitor
Because the DC potential of the input pin is not zero, this capacitor can not be omitted. Decreasing the capacitance value to an extremely low level lowers the low frequency response.

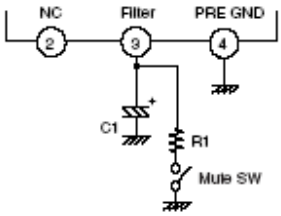
C3: Feedback capacitor
Decreasing the capacitance value lowers the low frequency response. Increasing the capacitance value makes the starting time later.

C4: Output capacitor
Decreasing the capacitance value causes insufficient power at low frequencies.

C5: Oscillation blocking capacitor
Decreasing the capacitance value causes oscillation to occur easily. Use a polyester film capacitor that has good high frequency response and temperature characteristics.
The use of an electrolytic capacitor or a ceramic capacitor may cause oscillation to occur at low temperatures.
C6: Power capacitor
Decreasing the capacitance value causes ripple to occur easily. Locating at a distance from the IC or removing this capacitor may cause oscillation to occur.
R1: Mute resistor
Refer to supplementary discussion "External Muting."
R2: Resistor connected in series with oscillation blocking capacitor
Prevents phase shift in conjunction with the oscillation blocking capacitor so that oscillation does not easily occur. There is an optimal value for the resistor; increasing or decreasing the resistance causes oscillation to occur easily.

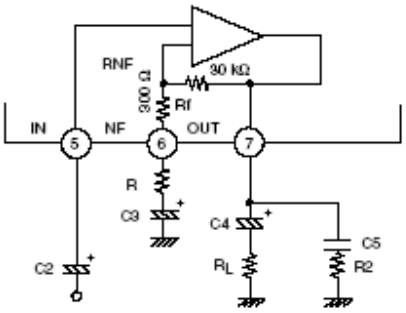
External Muting

- Pull down the electric potential of the ripple filter pin (pin 3).
  Muting becomes possible by inserting the discharge resistor R1 between pin 3 and GND. If the resistance value of R1 is too low, a popping noise is generated; if the resistance value is too high, the muting effect is reduced. (A value of 750 Ω is recommended for R1.)



Voltage Gain

The voltage gain is fixed at 40dB by the ratio of the 30 kΩ and 300 Ω internal resistors. Therefore, it is not possible to use this IC with a voltage gain greater than 40 dB. Although it is possible to use this IC with a voltage gain of less than 40 dB by adding a feedback resistor (RNF) and external resistors (R) as shown in the diagram, doing so causes oscillation to occur easily. Therefore, do not use this IC with a voltage gain of 30dB or less.



5.1.5 Notes on Using the IC

- Maximum ratings
  When this IC is used near its maximum ratings, it is possible that a slight fluctuation in the operating conditions could cause the maximum ratings to be exceeded, damaging the IC. Therefore, allow for an adequate safety margin in regards to supply voltage, etc., so that the IC is never used under conditions that exceed its maximum ratings.
- Short circuit between pins
  Applying power to the IC while a short circuit exists between two pins can cause damage or deterioration in the IC. Therefore, after mounting the IC on a board, make sure that there are no solder bridges, etc., causing a short circuit between any of the pins before applying power to the IC.
- Using the IC in a radio
  When using this IC in a radio, make sure that there is enough distance between the IC and the bar antenna.
- Printed circuit pattern
  When designing the printed circuit pattern, keep power, output, and ground lines thick and short, and determine the placement of the pattern and the components in such a way as to prevent the generation of an I/O feedback loop.
  In addition, power supply capacitor C6 and oscillation blocking capacitor C5 should be placed as close as possible to the IC pins in order to prevent oscillation.

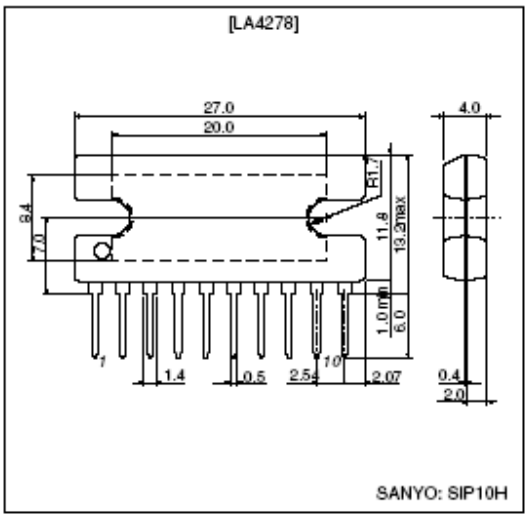
5.2 LA4278

5.2.1 Overview

The LA4278 is a 10 W 2-channel power amplifier intended for televisions.
This IC has a series of pin compatible monaural and 2-channel power amplifiers, thus allows the end product to use a common circuit boad.

5.2.2 Package Dimensions

3024A-SIP10H



5.2.3 Specifications

Maximum Ratings at Ta = 25°C

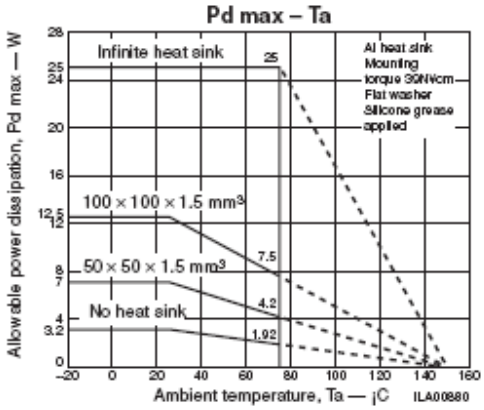
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}	Rg = 0	35	V
Maximum output current	I_O peak	Per channel	2.5	A
Allowable power dissipation	Pd max	Infinite heat sink	25.0	W
Thermal resistance	θj-c		3.0	°C/W
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +150	°C

Operating Conditions at Ta = 25°C

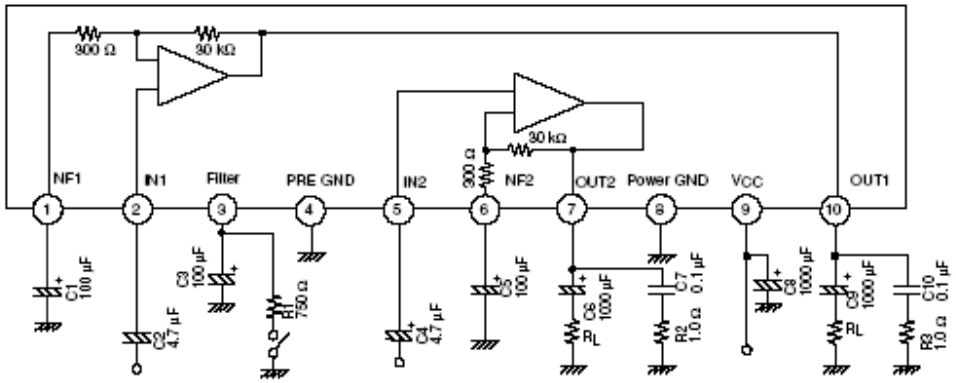
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		28	V
Load resistance	R_L		8	Ω
Operating supply voltage range	V_{CC} op	Range does not exceed Pd	10 to 34	V

Operating Characteristics at Ta = 25°C, V_{CC} = 28 V, R_L = 8 Ω, f = 1 kHz, Rg = 600 Ω, with specified board, in specified circuit

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}	Rg = 0		55	80	mA
Voltage gain	VG	V_O = 0 dBm	38	40	42	dB
Total harmonic distortion	THD	P_O = 0.5 W		0.1	0.8	%
Output noise voltage	V_{NO}	Rg = 10 kΩ, BPF = 20 Hz to 20 kHz		0.25	1.0	mV
Output power	P_O	THD = 10 %	8.0	10		W
Ripple rejection	SVRR	Rg = 0, fr = 100 Hz, Vr = 0.5 Vrms	45	55		dB
Crosstalk	CT	Rg = 10 kΩ, V_O = 0 dBm	40	55		dB



5.2.4 Pin Assignment Equivalent Diagram



* For Muting, add a resistor between pin 3 and GND. 750 Ω for the LA4266/67/68, 200 Ω for the LA4276/77.

Description of External Parts

C1, C5: Feedback capacitors

Decreasing the capacitance value lowers the low frequency response. Increasing the capacitance value makes the starting time later.

C2, C4: Input capacitors

Because the DC potential of the input pin is not zero, this capacitor can not be omitted. Decreasing the capacitance value to an extremely low level lowers the low frequency response.

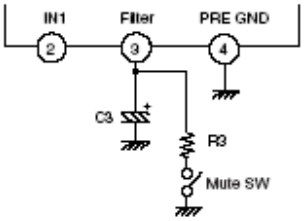
C3: Ripple filter capacitor

Decreasing the capacitance value reduces ripple rejection. This capacitor also affects the starting time; decreasing the capacitance value makes the starting time earlier.

C6, C9: Output capacitors
Decreasing the capacitance value causes insufficient power at low frequencies.
C7, C10: Oscillation blocking capacitors
Decreasing the capacitance value causes oscillation to occur easily. Use a mylar film capacitor that has good high frequency response and temperature characteristics. The use of an electrolytic capacitor or a ceramic capacitor may cause oscillation to occur at low temperatures.
C8: Power capacitor
Decreasing the capacitance value causes ripple to occur easily. Locating this capacitor at a distance from the IC or removing this capacitor may cause oscillation to occur.
R1: Muting resistor
Refer to supplementary discussion "External Muting."
R2, R3: Resistors connected in series with oscillation blocking capacitor
These prevent phase shift in conjunction with the oscillation blocking capacitor so that oscillation does not easily occur. There is an optimal value for the resistor; increasing or decreasing the resistance causes oscillation to occur easily.

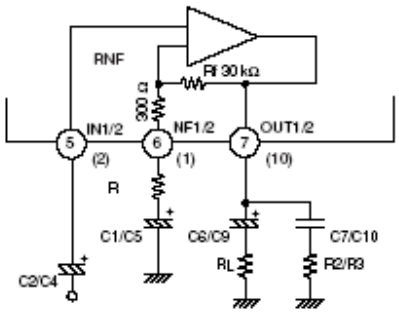
External Muting

- Pull down the electric potential of the ripple filter pin (pin 3).
  Muting becomes possible by inserting the discharge resistor R3 between pin 3 and GND. If the resistance value of R3 is too low, a popping noise is generated; if the resistance value is too high, the muting effect is reduced. (A value of 750 Ω is recommended for R3.)



Voltage Gain

The voltage gain is fixed at 40dB by the ratio of the 30 kΩ and 300 Ω internal resistors. Therefore, it is not possible to use this IC with a voltage gain greater than 40 dB. Although it is possible to use this IC with a voltage gain of less than 40 dB by adding a feedback resistor (RNF) and external resistors (R) as shown in the diagram, doing so causes oscillation to occur easily. Therefore, do not use this IC with a voltage gain of 30dB or less.



5.2.5 Notes on Using the IC

- Maximum ratings
  When this IC is used near its maximum ratings, it is possible that a slight fluctuation in the operating conditions could cause the maximum ratings to be exceeded, damaging the IC. Therefore, allow for an adequate safety margin in regards to supply voltage, etc., so that the IC is never used under conditions that exceed its maximum ratings.
- Short circuit between pins
  Applying power to the IC while a short circuit exists between two pins can cause damage or deterioration in the IC. Therefore, after mounting the IC on a board, make sure that there are no solder bridges, etc., causing a short circuit between any of the pins before applying power to the IC.
- Using the IC in a radio
  When using this IC in a radio, make sure that there is enough distance between the IC and the bar antenna.
- Printed circuit pattern
  When designing the printed circuit pattern, keep power, output, and ground lines thick and short, and determine the placement of the pattern and the components in such a way as to prevent the generation of an I/O feedback loop. In addition, power supply capacitor C8 and oscillation blocking capacitor C7 and C10 should be placed as close as possible to the IC pins in order to prevent oscillation.

6 Surround Processor IC—LV1116N（N801）

6.1 Overview

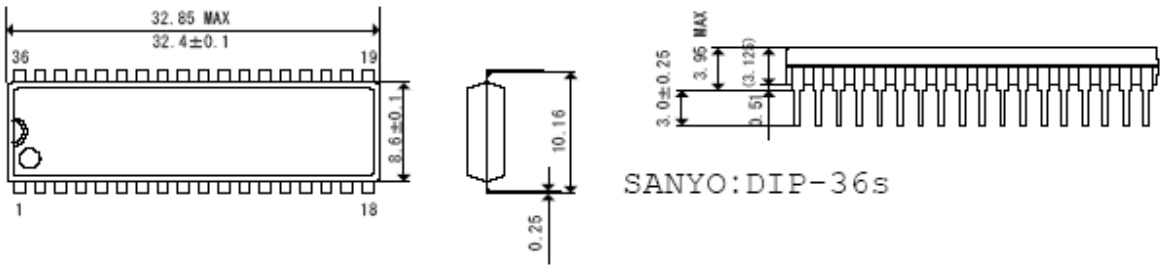
The LV1116 is a sound processor IC for use in TV set.It contains surround processing function(AViSS™), Pseudo Stereo Function, L+R output, and the major functional blocks of an electronic volume control IC.

6.2 Functions

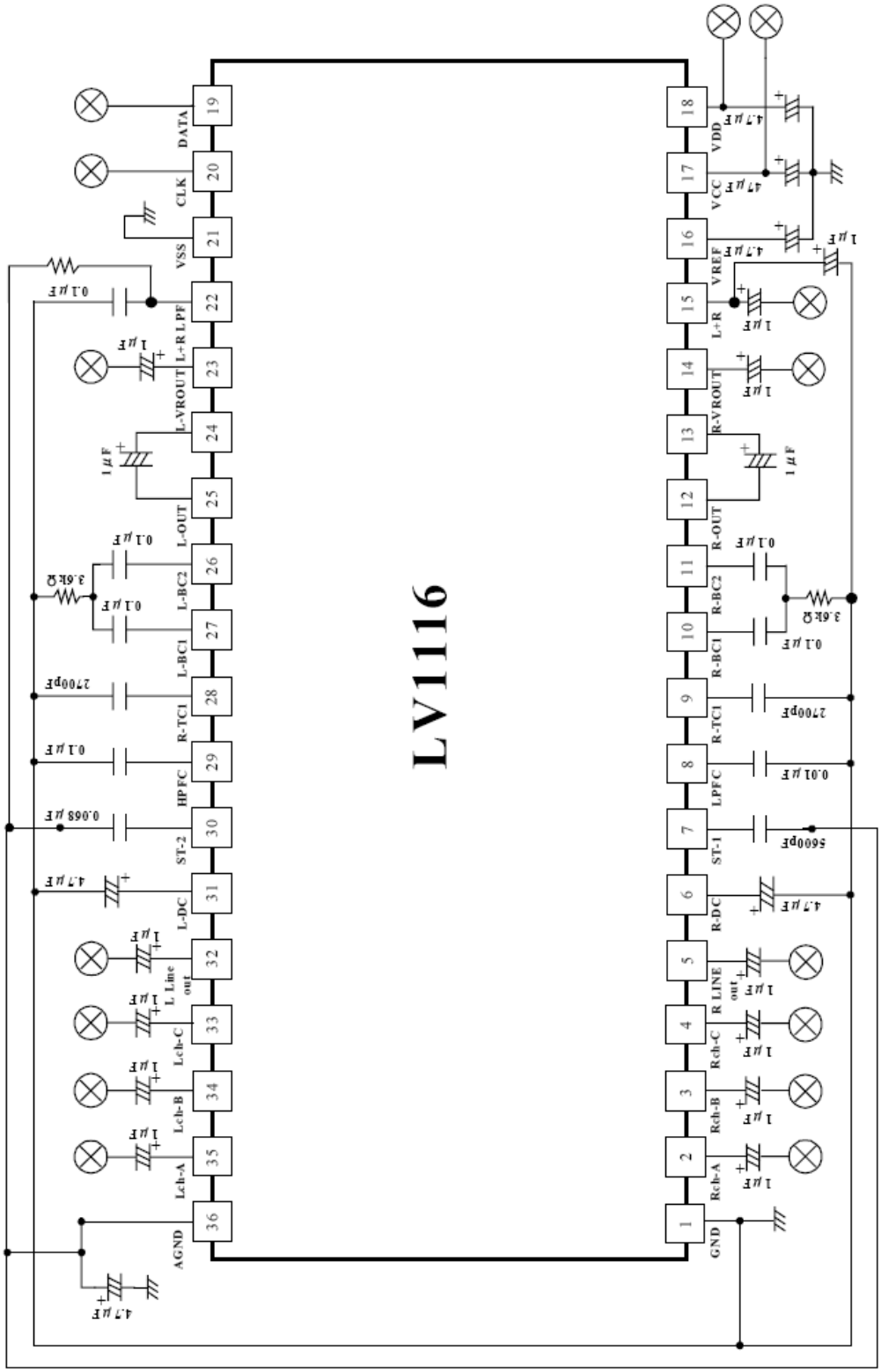
- Input Function SW(3ch stereo Inputs[L, R])
- Line out(Through output)
- Input Gain (-6dB,-4dB,0dB,4dB,6dB:5positions)
- AViSS™(ON/OFF/4 stage level control)
- Tone Control (BASS:±20dB, TREBLE:±18dB[2dBStep])
- Volume control (0dB~-14dB:1dBStep/-14dB~-80dB:2dBStep /-∞=-82dB)
- Balance Control
- Through Mode/Mute Mode
- Pseudo Stereo Function (ON/OFF/MONO control)
- L+R Output with LPF (Mute + 7stage level control:8positions)
- I^2C Bus Control

*Initial gain of L+R AMP can be controlled by resistance value of external register .

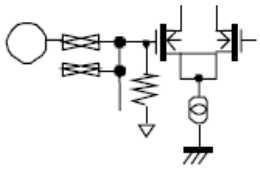
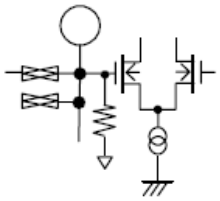
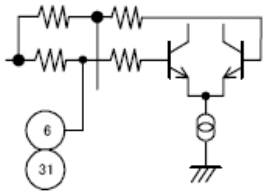
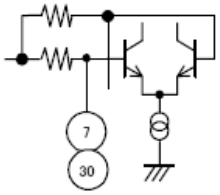
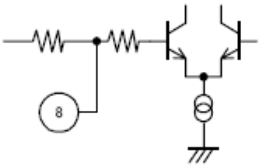
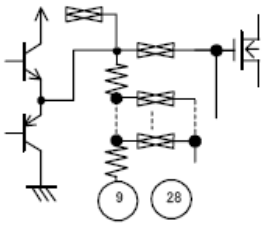
6.3 Package Dimensions

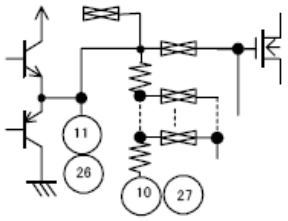
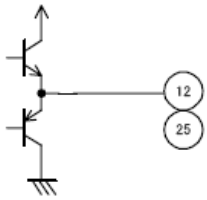
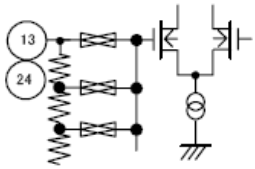
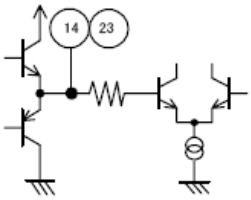
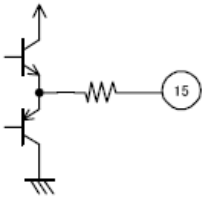
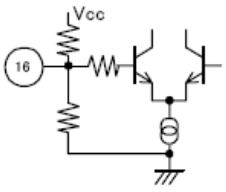


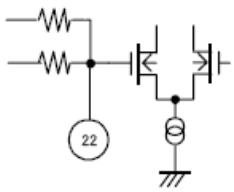
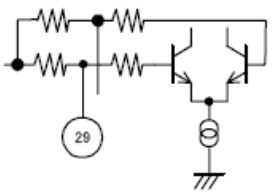
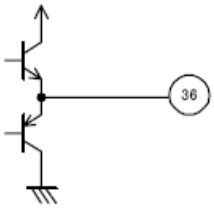
6.4 Block Diagram



6.5 Pin Function

No	Function	Voltage	Internal equivalent circuit	Remarks
1	GND	0		
2	INPUT-A(R)	VREF		Input Impedance ri=50kΩ
35	INPUT-A(L)			
3	INPUT-B(R)			
34	INPUT-B(L)			
4	INPUT-C(R)			
33	INPUT-C(L)			
5	LINE-OUT(R)	VREF		Function SW Output ro=50kΩ
32	LINE-OUT(L)			
6	DC Cut(R)	VREF		DC offset cancellation capacitor connection pin
31	DC Cut(L)			
7	ST-1	VREF		Pseudo stereo phase shift capacitor connection pin
30	ST-2			
8	AviSS LPF	VREF		Capacitor connection pin for surround low pass filter
9	TREBLE(R)	VREF		Capacitor connection pin for configuring treble filter
28	TREBLE(L)			

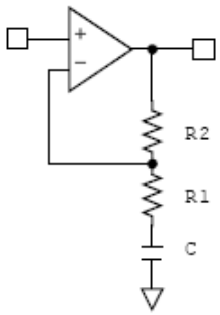
No	Function	Voltage	Internal equivalent circuit	Remarks
10	BASS-1(R)	VREF		Bass band filter configuration capacitor and resistor connection pins
27	BASS-1(L)			
11	BASS-2(R)			
26	BASS-2(L)			
12	OUT(R)	VREF		Output Impedance ro=50kΩ
25	OUT(L)			
13	EVR-IN(R)	VREF		Input Impedance ri=50kΩ
24	EVR-IN(L)			
14	EVR-OUT(R)	VREF		Output Impedance ro=50kΩ
23	EVR-OUT(L)			
15	L+R OUT	VREF		Output Impedance ro=10kΩ
16	VREF	0.5Vcc		Reference voltage
17	Vcc	Vcc		

No	Function	Voltage	Internal equivalent circuit	Remarks
18	VDD	VDD		
19	I2C-DATA			I2C control data input
20	I2C-CLK			
21	VSS	0		
22	L+R LPF	VREF		Internal resistor
29	AviSS HPF	VREF		
36	ANALOG GND	VREF		

6.6 Tone Circuit Constant Calculation Examples

Treble Band Circuit

The shelving characteristics can be obtained for the treble band.
The equivalent circuit and calculation formula during boost are indicated below.



・Calculation example 1

Specification Set frequency : f = 10000 Hz
Gain during maximum boost : G_{+18dB} = 17.5dB
Let us use R1 = 6.51kΩ and R2 = 45.19kΩ
The above constants are inserted in the following formula

$$G = 20 \times \mathrm{Log}_{10} \left(1 + \frac{R2}{\sqrt{R1^2 + (1/\omega C)^2}} \right)$$

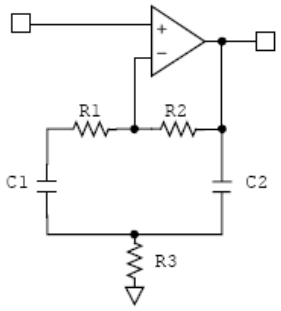
$$C = \frac{1}{2\pi f \sqrt{\left[\frac{R2}{10^{G/20}-1}\right]^2 - R1^2}}$$

$$= \frac{1}{2\pi 10000 \sqrt{\left[\frac{45190}{7.50 - 1}\right]^2 - 6510^2}} \fallingdotseq 6500 \text{ (pF)}$$

Bass Band Circuit

The equivalent circuit and the formula for calculating the external RC with a mean frequency of 100 Hz are shown below.

・Bass band equivalent circuit diagram



・Calculation example 1

specification Mean frequency : f0 = 100Hz

Gain during maximum boost : G_{+20dB} = 20dB

Let us use R1 = 0kΩ and R2 = 66.7kΩ,and C1 = C2 = C.

We obtain R3 from G = 20 dB

$$G = 20 \times \mathrm{Log}_{10}\left(1 + \frac{R2}{2R3}\right)$$

$$R3 = \frac{R2}{2(10^{G+20dB/20} - 1)} = \frac{66700}{2(10 - 1)} \fallingdotseq 3.6k\Omega$$

We obtain C from mean frequency f0 = 100 Hz

$$f0 = \frac{1}{2\pi\sqrt{(R3R2C1C2)}}$$

$$C = \frac{1}{2\pi f0\sqrt{R3R2}} = \frac{1}{2\pi \times 100\sqrt{66700 \times 3600}} \fallingdotseq 0.1uF$$

We obtain Q

$$Q = \frac{R3R2}{2R3} \times \frac{1}{\sqrt{R3R2}} \fallingdotseq 2.15$$

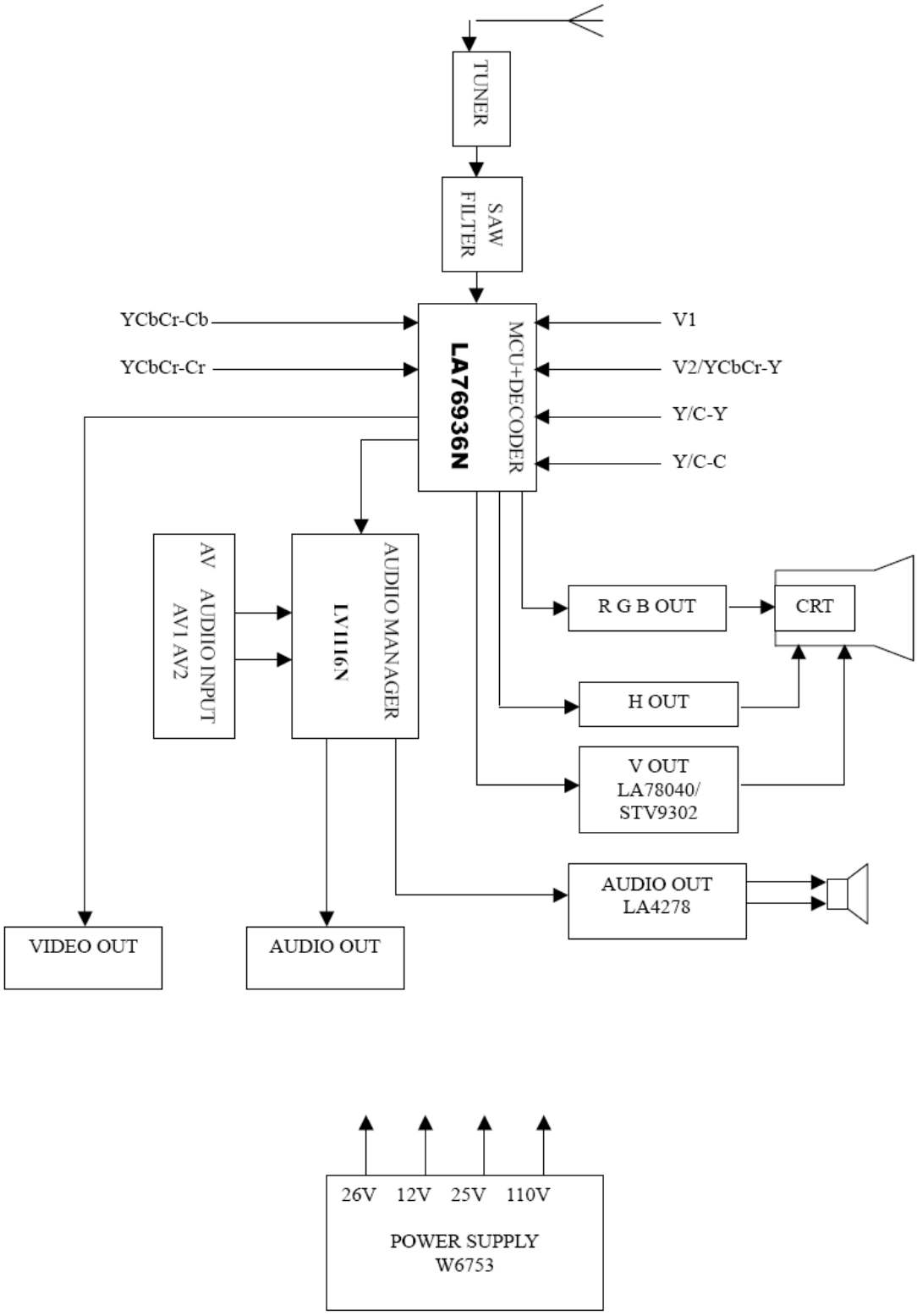
Note item when using

(1) When turning on the power, the setting inside is unsettled.
Before setting control data, it does a mute.

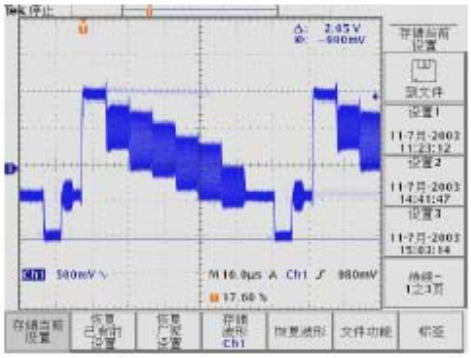
(2) To prevent the digital noise of the high frequency influence a terminal. (SCL,SDA)
It can be protected by a signal line in the ground pattern or by the shielding cable.

(3) To prevent the noise in changing a mode, please set the mute ON.

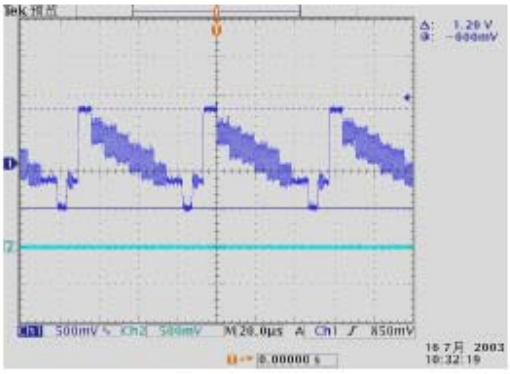
TV BLOCK DIAGRAM



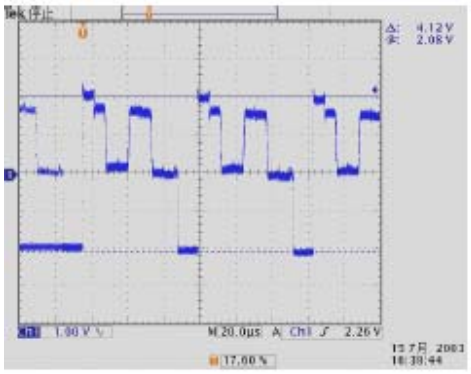
THE WAVEFORM of STICKING POINT



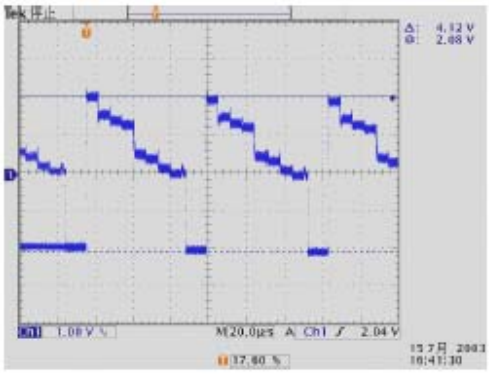
N103 PIN60 (VIDEO OUTPUT)



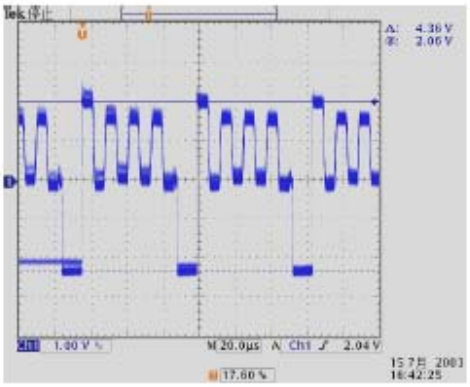
N103 PIN56(VIDEO INPUT)



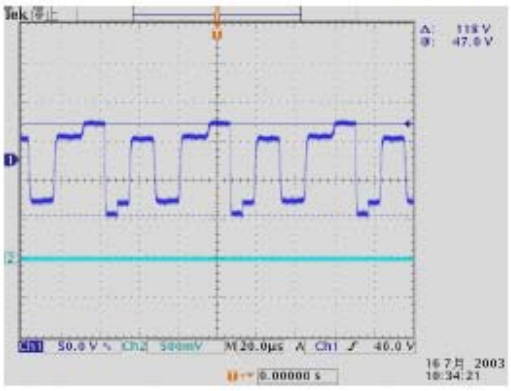
N103 PIN12（R OUTPUT）



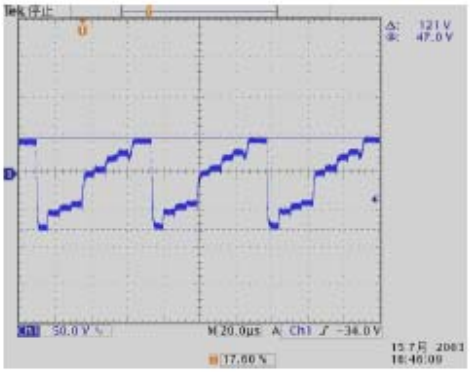
N103 PIN13（G OUTPUT）



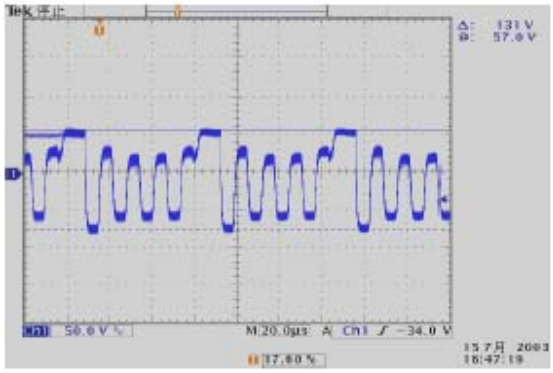
N103 PIN14（B OUTPUT）



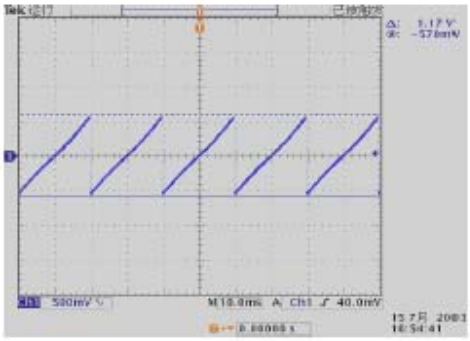
CRT ----R



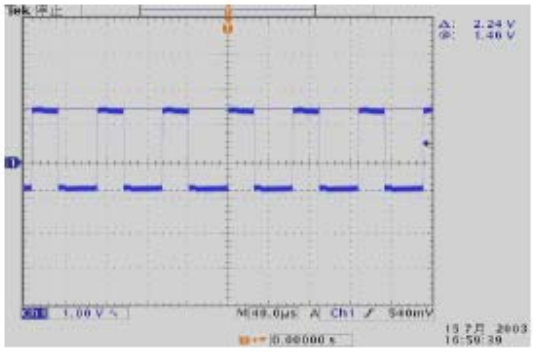
CRT------G



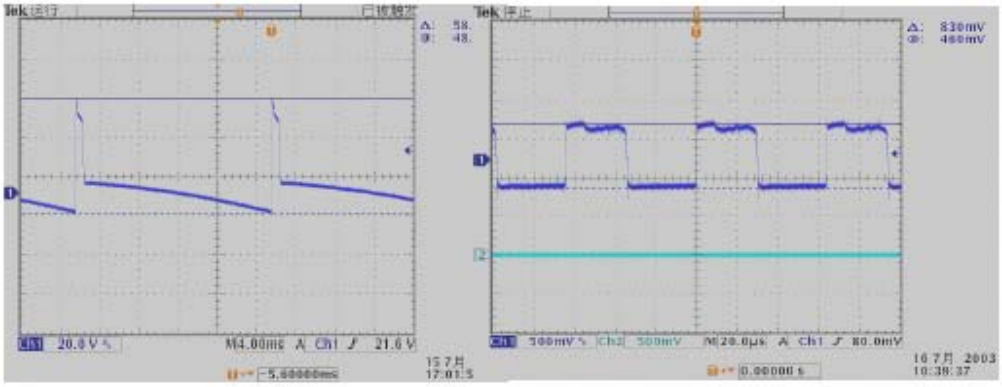
CRT ------B



N103 PIN17（VER OUTPUT）

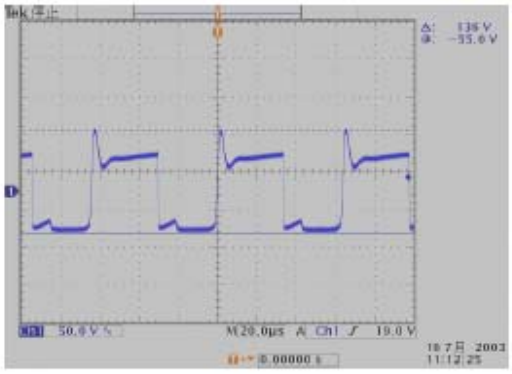


N103 PIN21（H OUTPUT）

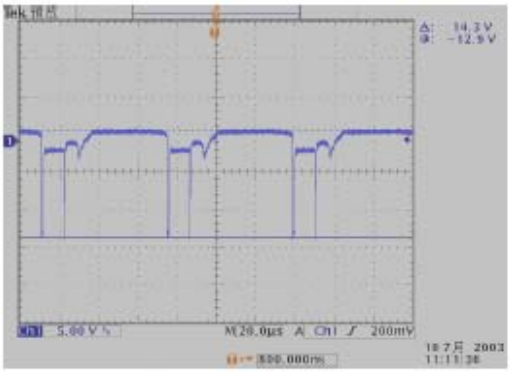


N440 PIN5（VER OUTPUT）

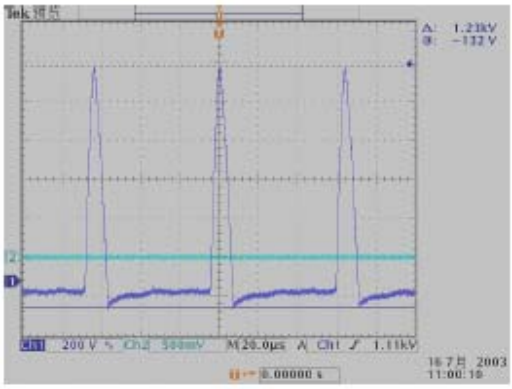
V401--B（H INPUT）



V401---C



V402---B



V402---C

Appendix 1: Schematic Circuit Diagram (KP15SA308A)

Appendix 2: PCB Layout Diagram(Main PCB、CRT PCB、Sound processor PCB)

Appendix 3: Exploded Views(KP15SA308A、K14SA208A)