

DESCRIPTION

TM1618 is an LED Controller driven ASIC. 1 segment/grid output lines, MCU digital interface, data latch, High-voltage LED driver, key scan circuit dare all incorporated into a single chip to build a highly reliable peripheral device for a single chip microcomputer. Housed in a 18-pin DIP Package, TM1618 pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

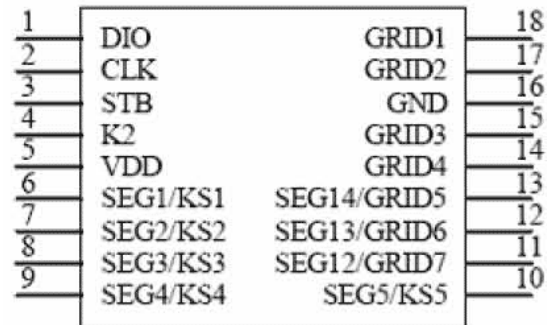
FEATURES

- CMOS Technology
- Display Modes (5segment, 7 grid to 8segment, 4grid)
- Key Scanning (5 x 1Bit)
- 8-Step Dimming Circuitry
- Serial Interface (CLK, STB, DIN, DOUT)
- Oscillatory Manners; RC Oscillation (450KHz ±5%)
- Built-in on-reset circuit
- Available in 18-pin, DIP Package

APPLICATION

- Micro-computer Peripheral Device
- VCR/VCD/DVD set
- Combi set

PIN CONFIGURATION:



TM1618

PIN DESCRIPTION

| Pin Name | Description | Explanation |
|-------------------------|-------------------------|--|
| DIO | Data Input/Output | This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit) |
| STB | Serial Interface Strobe | This pin reads initialization serial data at the rising/falling edge of the shift clock then wait for the command. The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored |
| CLK | Clock Input Pin | This pin reads serial data at the rising edge and outputs data at the falling edge. |
| NC | NC | No Connect |
| K2 | Key Data Input Pins | The data sent to these pins are latched at the end of the display cycle. (Internal Pull-Low Resistor) |
| Seg1/KS1~Seg5/KS5 | Output Segment | Segment Output Pins (p-channel, open drain) Also acts as the key source |
| Grid1 ~ Grid2 | Grid Output Pins | Grid Output Pins (N-Channel, open drain) |
| Grid3~Grid4 | Grid Output Pins | Grid Output Pins (N-Channel, open drain) |
| Seg12/Grid7~Seg14/Grid5 | Output (Seg/Grid) | Seg/Grid Multiplexing output |
| V _{DD} | Logic Power | 5V±10% |
| V _{SS} | Logic Ground | Connects the system ground |

ABSOLUTE MAXIMUM RATINGS (Ta=25 , Vss=0V)

| Parameter | Symbol | Ratings | Unit |
|-------------------------------|--------|---------------|------|
| Logic supply voltage | VDD | -0.5 ~+7.0 | V |
| Logic input voltage | VI1 | -0.5 ~VDD+0.5 | V |
| Segment driver output current | IO1 | -50 | mA |
| Grid driver output current | IO2 | +200 | mA |
| Power Loss | PD | 400 | mW |
| Supply Temperature | Topt | -40 ~+80 | |
| Storage Temperature | Tstg | -65 ~+150 | |

RECOMMENDED OPERATING RANGE

(Ta=-20 ~ +70 , Vss=0V)

| Parameter | Symbol | Min. | Typ | Max | Unit | Test Condition |
|--------------------------|-----------------|--------|-----|--------|------|----------------|
| Logic supply voltage | V _{DD} | | 5 | | V | - |
| High-level input voltage | V _{IH} | 0.7VDD | - | VDD | V | - |
| Low-level input voltage | V _{IL} | 0 | - | 0.3VDD | V | - |

ELECTRICAL CHARACTERISTICS

(Ta=-20 ~+70 , VDD=4.5 ~5.5V, Vss=0V)

| Parameter | Symbol | Min. | Typ | Max. | Unit | Test Condition |
|-------------------------------------|--------|---------|------|--------|------|----------------------------|
| High-level output current | Ioh1 | -20 | -25 | -40 | mA | Seg1 ~ Seg11, Vo=VDD-2V |
| | Ioh2 | -20 | -30 | -50 | mA | Seg1 ~ Seg11, Vo=VDD-3V |
| Low-level output current | IOL1 | 80 | 140 | - | mA | Grid1 ~ Grid6 Vo=0.3V |
| Low-level output current | Idout | 4 | - | - | mA | VO=0.4, dout |
| High-level output current tolerance | ItoIsg | - | - | 5 | % | VO=VDD-3V, Seg1 ~ Seg11 |
| Output Pull-down | RL | | 10 | | k Ω | K1~K3 |
| Input Current | II | - | - | ±1 | μA | VI=VDD/VSS |
| High-level input voltage | VIH | 0.7 VDD | - | | V | CLK, DIN, STB |
| Low-level input voltage | VIL | - | - | 0.3VDD | V | CLK, DIN, STB |
| Lag voltage | VH | - | 0.35 | - | V | CLK,DIN,STB |
| Dynamic Current | IDDdyn | - | - | 5 | mA | Display off, No-load |

SWITHCING CHARACTERISTICS

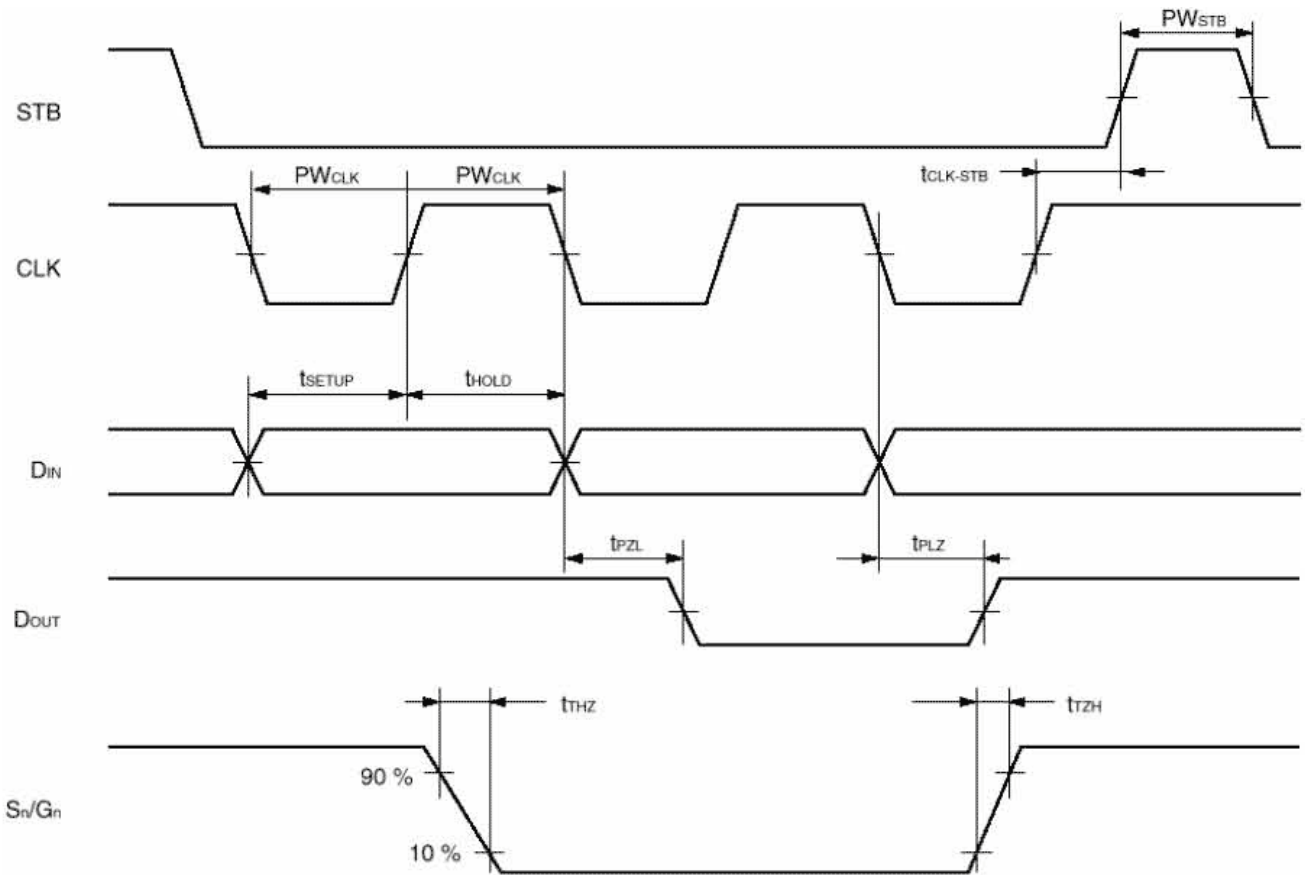
(Ta=-20 ~+70 , VDD=4.5 ~5.5V)

| Parameter | Symbol | Min. | Typ | Max. | Unit | Test Condition |
|-------------------------|--------|------|-----|------|------|--|
| Oscillation Frequency | fosc | - | 500 | - | KHz | R=16.5kΩ |
| Propagation delay time | tPLZ | - | - | 300 | ns | CLK→D _{OUT} |
| | tPZL | - | - | 100 | ns | CL=15pF, RL=10kΩ |
| Rise time | TTZH1 | - | - | 2 | μs | CL=300pF Seg1~Seg11 |
| | TTZH2 | - | - | 0.5 | μs | Grid1~Grid4 Seg12/Grid7~Seg14/Grid5 |
| Fall time | TTHz | - | - | 120 | μs | CL=300pF, Segn, Gridn, |
| Maximal clock frequency | Fmax | 1 | - | - | MHz | On 50% duty factor |
| Input capacitance | CI | - | - | 15 | pF | - |

***TIMING DIAGRAM** (Ta=-20 ~+70 , VDD=4.5 ~5.5V)

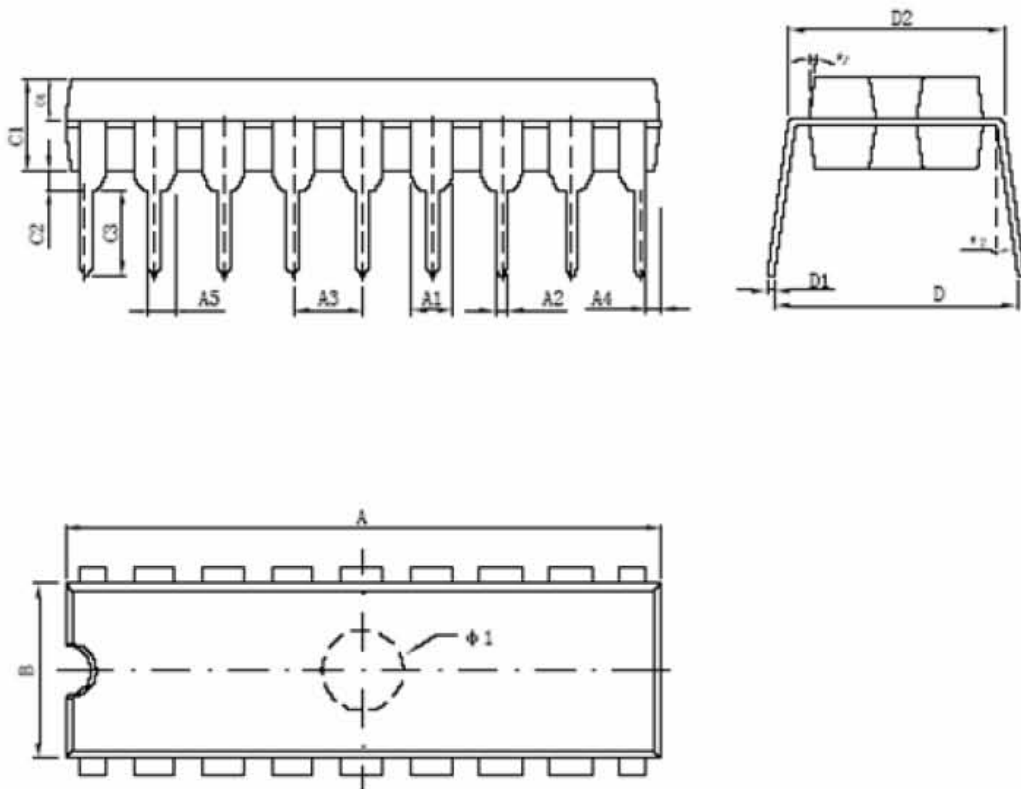
| Parameter | Symbol | Min. | Typ | Max. | Unit | Test Condition |
|--------------------|----------|------|-----|------|------|----------------|
| Clock Pulse width | PWCLK | 400 | - | - | ns | - |
| Strobe pulse width | PWSTB | 1 | - | - | μs | - |
| Data setup time | tSETUP | 100 | - | - | ns | - |
| Data hold time | tHOLD | 100 | - | - | ns | - |
| CLK→STB time | tCLK STB | 1 | - | - | μs | CLK↑→STB↑ |
| Wait time | tWAIT | 1 | - | - | μs | CLK↑→CLK↓ |

TIMING FAVEFORM



PACKAGE:

| Size | Min.(mm) | Max.(mm) | Size | Min. (mm) | Max.(mm) |
|------|----------|----------|------|-----------|----------|
| A1 | 21.9 | 22.10 | C3 | 3.4 | 3.6 |
| A1 | 1.40TYP | | C4 | 1.58TYP | |
| A2 | 0.43 | 0.57 | D | 8.10 | 8.60 |
| A3 | 2.54TYP | | D1 | 0.20 | 0.35 |
| A4 | 0.59TYP | | D2 | 7.62 | 7.87 |
| A5 | 0.95TYP | | Φ1 | 3.0TYP | |
| B | 6.3 | 6.5 | Θ1 | 8° TYP | |
| C1 | 3.4 | 3.6 | Θ2 | 5° TYP | |
| C2 | 0.6 | 0.8 | | | |



.All specs and applications shown above subject to change without prior notice.