Fuji Switching Power Supply Control IC

Green mode PWM IC

FA8A60/61/70/71

Application Note

February 2013
Fuji Electric Co., Ltd.

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Contents

Caution)

- The contents of this note will subject to change without notice due to improvement.
- The application examples or the components constants in this note are shown to help your design, and variation of components and service conditions are not taken into account. In using these components, a design with due consideration for these conditions shall be conducted.

1. Overview

FA8A27N is a current mode type switching power supply control IC possible to drive a power MOSFET directly. Despite of a small package with 8 pins, it has a lot of functions and it is best suited for power saving at the light load and decreasing external parts. Moreover it enables to realize a reduced space and a high cost-performance power supply.

2. Features

■ **Relization of low standby power**

- Built-in discharge function for AC input filter capacitor (XCAP). (Reduce loss of the discharge resistor)
- Integrated frequency decrease function improves efficiency in the middle-load region. (Frequency decrease start point is adjustable based on the settings of mounted parts.)
- Intermittent operation (burst operation) system adopted for light load operation achieves low standby power. (Burst operation start point is adjustable based on the settings of mounted parts.)
- Switching is allowed between normal operation mode and power-off mode. In power-off mode, lower standby power is ensured.
- Built-in 500V high voltage startup circuit.

■ **Various Protection are built in.**

- Overload protection (Auto recovery, Latch)
- Integrated function of correcting overload detection level depending on AC input voltage (Correction amount is adjustable based on the settings of externally mounted parts.)
- Integrated latch-off function based on external signals, overvoltage protection function, low-voltage prevention function, and overheat protection function
- nternal Soft-Start
- The lowest frequency is set to 25 kHz to prevent operation at audible frequency under light load.

■ Switching frequency jitter function realize low EMI.

■ Internal DSS (Dynamic Self Supply)

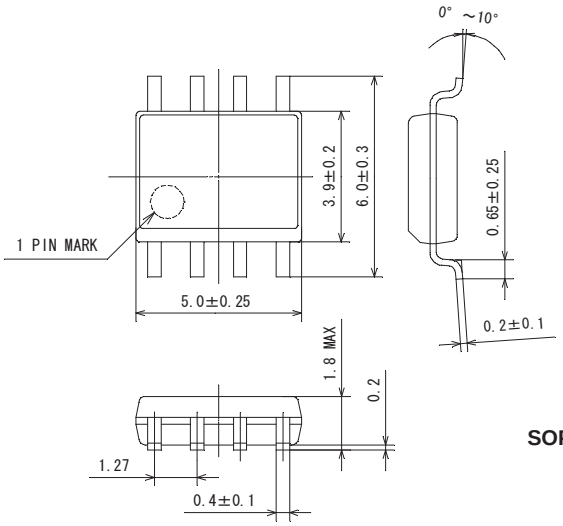
■ Drive circuit for MOSFET: -0.5A(sink)/0.5A（source）

Function list by types

Type	Discharge function for X-Capacitor	Overload protection	External latch, over-voltage protection, Over heat protection	Brown out protection
FA8A60N	No	Automatic recovery	Latch	No
FA8A61N		Latch		
FA8A70N	Yes	Automatic recovery	Latch	No
FA8A71N		Latch		

* Models scheduled to be serialized at present are not equipped with the brown out protection.

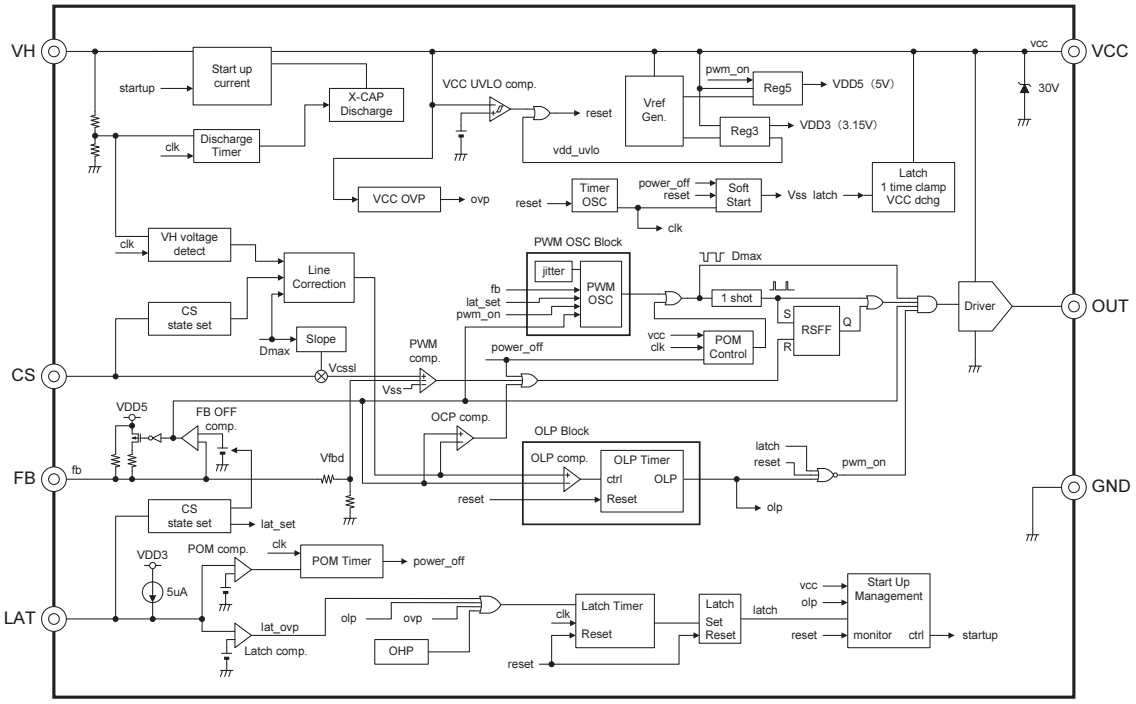
3. Outline drawing



SOP-8 outline drawing

4. Block diagram

FA8A61N(example)



5. Functional description of pins

Pin No.	Pin name	Pin Function	Note
1	LAT	External latch signal input Switching Frequency Reduction（S.F.R.）setup Switching stop FB threshold voltage setup	*1
2	FB	Feedback control signal input	*1
3	CS	Current sense input, Over Load Protection（OLP）, Over Current Protection（OCP） OLP Line Compensation（OLP L.C.）setup	*1
4	GND	Ground	—
5	OUT	Output	—
6	VCC	Power supply, Under Voltage Locking Out（UVLO）, Over Voltage Protection（OVP）detection	*1
7	（NC）	No connection	—
8	VH	High voltage input AC Input filter capacitance（XCAP）discharge	*2

*1 Connect capacitor between terminal 1pin and GND.

*2 Connect diodes and resistor between VH and the AC lines.

6. Rating & characteristics

(1) Absolute maximum ratings

Stress exceeding absolute maximum ratings may malfunction or damage the device.

"-" shows source and "+" shows sink in current descriptions.

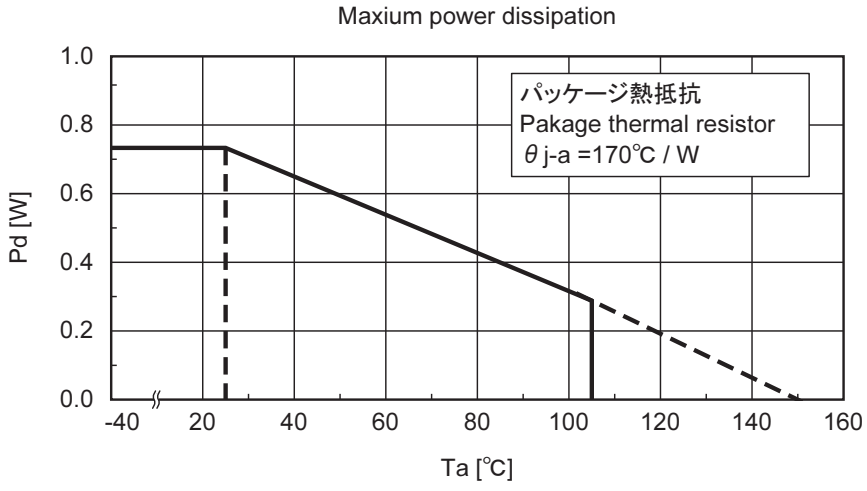
Item		Symbol	Value	Unit
LAT pin voltage		Vlat	-0.3 to 3.3	V
LAT pin current		Ilat	-100 to 100	μA
FB pin voltage		Vfb	-0.3 to 5.3	V
FB pin current		Ifb	-200 to 100	μA
CS pin voltage		Vcs	-0.3 to 3.3	V
CS pin current		Ics	-100 to 100	μA
OUT pin voltage		Vout	-0.3 to VCC+0.3	V
OUT pin current		Iout	-500 to 500	mA
OUT pin peak current *3,4		Iout_pk	-1000 to 1000	mA
VCC pin voltage		Vcc	-0.3 to 28.0	V
VCC pin current *1	At pulse voltage input	Ivcc1	-10 to 20	mA
	At minus voltage input	Ivcc2	-0.1 to 0	mA
VH pin voltage		Vvh	-0.3 to 500	V
VH pin current *3		Ivh	-0.1 to 10	mA
Power dissipation（Ta=25℃）		Pd	735	mW
Operating junction temperature		Tj	-30 to 150	℃
Storage temperature		Tstg	-40 to 150	℃

Notes）

*3 Please consider power supply voltage and load current well and use this IC within maximum temperature in o peration. The IC may cross maximum power dissipation at normal operating condition by power supply voltage or load current within peak current absolute maximum rating value.

*4 The period that exceeds 500mA must be 100ns or less.

※Maximum dissipation curve



(2) Recommended operating conditions

Item		Symbol	MIN	TYP	MAX	Unit
Supply voltage		Vcc	10	18	24	V
VH input voltage	in start-up current supplied	Vvh	50	—	400	V
	in start-up current stopped	Vvh	100	—	400	V
Resistor connected to VH pin *5		Rvh	5.6	—	50	kohm
Capacitor connected to VH pin *6		Cvh	0	—	100	pF
Capacitor connected to LAT pin *7, 9 S.F.R. : “High”		Clat	176	220	264	pF
Capacitor connected to LAT pin *7, 9 S.F.R. : “Middle”		Clat	800	1000	1200	pF
Capacitor connected to LAT pin *7, 9 S.F.R. : “Low”		Clat	2640	3300	3960	pF
Resistor connected to LAT pin *9		Rlat	150	—	300	kohm
Resistor connected to CS pin *8, 9 OLP L.C. : “Middle”		Rcs	0.3	—	0.5	kohm
Resistor connected to CS pin *8, 9 OLP L.C. : “Weak”		Rcs	1.4	—	2.1	kohm
Resistor connected to CS pin *8, 9 OLP L.C. : “Strong”		Rcs	3.9	—	5.2	kohm
Capacitor connected to VCC pin		Cvcc	22	33	56	μF
Ambiance temperature in operation		Ta	-30	—	105	℃

Notes）

*5 More than AC85V.

*6 Verify no malfunction of XCAP discharge function occurs in case of the capacitor connection.

*7 See terms concerning to switching frequency reduction characteristics in “3-4. PWM Oscillator” in “3. DC electrical characteristics”.

*8 See terms concerning to OLP line compensation characteristics in “3-6. Over load protection and current sense” in “3. DC electrical characteristics”.

*9 Connect to GND pin by the shortest distance as much as possible. In selection of these external components, make is sure that their values including temperature characteristics are satisfied with the recommended ranges.

(3) DC electrical characteristics

The characteristics in this section are those in conditions as follows unless otherwise specified. The voltages described in the conditions are DC input values (not AC input values).

Tj = 25℃, VCC = 18V, VVH = 120V, Vlat = 1.0V, VFB = 2.5V, VCS = 0V
Initial Setup: Switching Frequency Reduction: ”Low”, OLP Line Compensation: ”Middle”

Notes）
(1)The item which indicated “*1” are not 100% tested in production but guaranteed by design.
(2)No guaranteed value exists for the column of “—“.
(3)“-” shows source current and “+” shows sink current in current output characteristics.

3-1. Initial setup function（CS, LAT pins）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Initial setup time	Tiniset		84	95	106	μs
LAT source current for capactance detection	Ilatset	Vlat = 0V, In initial setup	-55	-50	-45	μA
LAT threshold voltage for capactance detection	Vlatset	In initial setup	1.5	1.6	1.7	V
LAT threshold time（1）for capactance detection	Tlatset1	In initial setup	16	19	22	μs
LAT threshold time（2）for capactance detection	Tlatset2	In initial setup	62	69	77	μs
CS source current for resistance detection	Icsset	In initial setup	85	100	115	μA
CS threshold voltage（1）for resistance detection	Vcsset1	In initial setup	70	95	120	mV
CS threshold voltage（2）for resistance detection	Vcsset2	In initial setup	260	295	330	mV
LAT sink current in UVLO	Ilatsiuv	Vvcc = 6V, Vlat = 1.5V	0.6	1.3	2	mA
LAT pin test mode set voltage	Vlattest		0.7	1.1	1.5	V
CS sink current in UVLO	Icssiuv	Vvcc = 6V, Vcs = 1.5V	0.4	1.0	1.6	mA

3-2. External latch-off function（LAT pin）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LAT output current	Ilatsrc		-5.5	-5	-4.5	μA
LAT threshold voltage for latch-off	VthlatH	Vlat increasing	1.6	1.8	2.0	V
Latch-off delay time	Tdlylat	Vlat > VthlatH	57	72	88	μs

Notes）
Switching is stopped in latch mode when LAT pin voltage Vlat is kept higher than Vthlath for Tdlylat.

3-3. Soft-start function（OUT pin）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Soft-start time *10	Tss	Vss = 470mV （internal voltage to PWM comparator）	8.5	11	13.5	ms
Steady-state operation start time *10,11	Tssend		14	17	20	ms

Notes）

*10 During start-up after UVLO and Power off mode（see “10-12. Power off mode section”）.

*11 Switching frequency jitter starts. Minmum ON pulse width：Tmin2 →Tmin1（see “3-5. Pulse width modulation section”）

3-4. PWM oscilator（FB, OUT pin）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Switching frequency	Fsw		62	65	68	kHz
Supply voltage stability	FswdV	Vvcc = 10V to 24V	-2	—	2	%
Temperature stability *1	FswdT	Tj = -30℃ to 105℃	-5	—	5	%
Frequency modulation ratio *1	Rfm	Vfb > Vfbh_h ⊿Fsw / Fsw	±5	±7	±9	%
Frequency modulation period *1	Tfm	Vfb > Vfbh_h	1	2	3	ms
Frequency reduction start FB voltage	Vfbh_h	S. F. R. : “High” *12 Freq. = Fsw×0.9	1.67	1.97	2.27	V
Frequency reduction end FB voltage	Vfbl_h	S. F. R. : “High” *12 Freq. = Fswmin×1.1	1.55	1.85	2.15	V
Frequency reduction range width	Vfbd_h	Vfbh_h – Vfbl_h	0.06	0.14	0.22	V
Frequency reduction start FB voltage	Vfbh_m	S. F. R. : “Middle” *12 Freq. = Fsw×0.9	1.46	1.76	2.06	V
Frequency reduction end FB voltage	Vfbl_m	S. F. R. : “Middle” *12 Freq. = Fswmin×1.1	1.35	1.65	1.95	V
Frequency reduction range width	Vfbd_m	Vfbh_m – Vfbl_m	0.05	0.12	0.19	V
Frequency reduction start FB voltage	Vfbh_l	S. F. R. : “Low” *12 Freq. = Fsw×0.9	1.05	1.35	1.65	V
Frequency reduction end FB voltage	Vfbl_l	S. F. R. : “Low” *12 Freq. = Fswmin×1.1	0.98	1.28	1.58	V
Frequency reduction range width	Vfbd_l	Vfbh_l – Vfbl_l	0.04	0.10	0.16	V
Minimum switching frequency	Fswmin	Vfb = 0.7V	22.5	25	27.5	kHz

Notes）

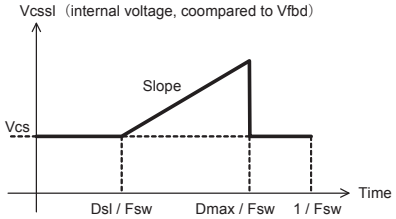
*12 Conncerning to setup condition, see “3-1. Initial setup function” and “9. Recommended operation conditions”.

3-5. Pulse width modulation（FB pin）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum duty cycle	Dmax		73	83	93	%
Minimum duty cycle	Dmin	Vfb = 0V	—	—	0	%
FB threshold voltage for stop switching	Vthfb	Vlat = 0.75V *13	0.42	0.47	0.52	V
		Vlat = 1.5V *13	0.84	0.94	1.04	V
FB output current	Ifbsrc	Vfb = 0V	-95	-75	-55	μA
Slope compensation	Slope		14	21	28	mV/μs
Duty ratio at starting slope compensation	Dsl		20	30	40	%
Minimum ON pulse width	Tmin1	In steady state	400	560	720	ns
	Tmin2	In soft start	180	280	380	ns

*13 Adjustable with Rlat（Vlat = Rlat × -Ilatsrc）.

Slope compensation voltage is added to CS voltage from the time over 30% duty ratio.



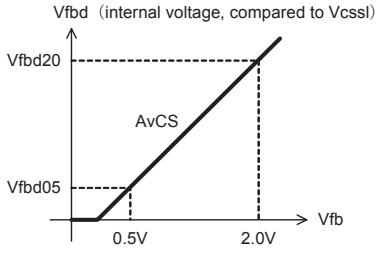
Slope compensation waveform

3-6. Over load protection and current sense（FB, CS pin）

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
FB divided voltage		Vfbd05	Vlat = 0.7V Vfb = 0.5V	10	50	90	mV
		Vfbd20	Vlat = 0.7V Vfb = 2.0V	300	360	420	mV
Voltage gain		AvCS	1.5/（Vfbd20－Vfbd05）	4.3	4.8	5.3	V/V
CS threshold voltage for over load protection	OLP.L.C. “Middle” *14	Vthcs1a	Vvhp ≦ Vvhd3	0.46	0.50	0.54	V
		Vthcs1b	Vvhd3<Vvhp≦Vvhd4	0.44	0.48	0.52	V
		Vthcs1c	Vvhd4<Vvhp≦Vvhd5	0.42	0.46	0.50	V
		Vthcs1d	Vvhd5<Vvhp≦Vvhd6	0.40	0.44	0.48	V
		Vthcs1e	Vvhd6 < Vvhp	0.38	0.42	0.46	V
		Vthcs1ab	Vthcs1a－Vthcs1b	0.01	0.02	0.03	V
		Vthcs1bc	Vthcs1b－Vthcs1c	0.01	0.02	0.03	V
		Vthcs1cd	Vthcs1c－Vthcs1d	0.01	0.02	0.03	V
		Vthcs1de	Vthcs1d－Vthcs1e	0.01	0.02	0.03	V
	OLP.L.C. “Weak” *14	Vthcs2a	Vvhp ≦ Vvhd3	0.46	0.50	0.54	V
		Vthcs2b	Vvhd3<Vvhp≦Vvhd4	0.46	0.50	0.54	V
		Vthcs2c	Vvhd4<Vvhp≦Vvhd5	0.44	0.48	0.52	V
		Vthcs2d	Vvhd5<Vvhp≦Vvhd6	0.42	0.46	0.50	V
		Vthcs2e	Vvhd6<Vvhp	0.40	0.44	0.48	V
		Vthcs2bc	Vthcs2b－Vthcs2c	0.01	0.02	0.03	V
		Vthcs2cd	Vthcs2c－Vthcs2d	0.01	0.02	0.03	V
		Vthcs2de	Vthcs2d－Vthcs2e	0.01	0.02	0.03	V
	OLP.L.C. “Strong” *14	Vthcs3a	Vvhp≦Vvhd3	0.46	0.50	0.54	V
		Vthcs3b	Vvhd3<Vvhp≦Vvhd4	0.44	0.48	0.52	V
		Vthcs3c	Vvhd4<Vvhp≦Vvhd5	0.40	0.44	0.48	V
		Vthcs3d	Vvhd5<Vvhp≦Vvhd6	0.38	0.42	0.46	V
		Vthcs3e	Vvhd6 < Vvhp	0.36	0.40	0.44	V
		Vthcs3ab	Vthcs3a－Vthcs3b	0.01	0.02	0.03	V
		Vthcs3bc	Vthcs3b－Vthcs3c	0.02	0.04	0.06	V
		Vthcs3cd	Vthcs3c－Vthcs3d	0.01	0.02	0.03	V
		Vthcs3de	Vthcs3d－Vthcs3e	0.01	0.02	0.03	V
VH peak voltage detection time		Tvhpdet		56	64	72	ms
Over current protection delay time		Tdlyocp	Vcs = 0V to 1.5V （pulse signal）	20	50	150	ns
Over load protection delay time		Tdlyolp	Vcs > Vthcsxx	160	200	240	ms

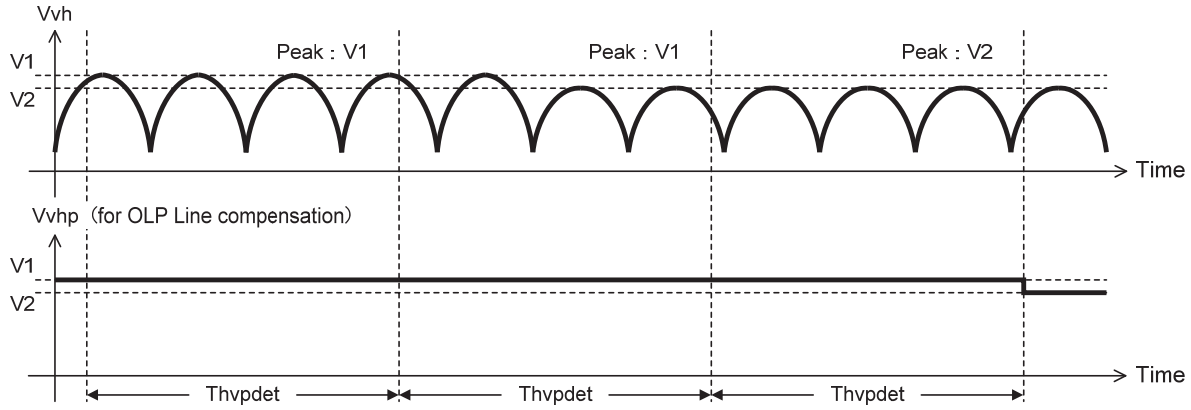
*14 Conncerning to setup condition, see “3-1. Initial setup function” and “2. Recommended operation conditions”.Conncerning to VH pin voltage condition, see OLP line compensation boundary voltage in “3-1. Initial setup function”.

Relation of FB voltage to FB divided voltage is shown in the following figure.



Relation of FB voltage Vfb to FB divided voltage Vfbd

VH peak voltage Vhp for OLP line compensation is detected and reloaded in every Tvhpdet.



VH peak voltage detection method

When CS voltage Vcs exceeds to OLP threshold voltage Vthcs, OUT is turned off after Tdlyocp, and over load flag is set to High. This flag is sampled with 0.5ms interval, and value of UP/DOWN counter for OLP increases or decrease based on whether it is High or Low respectively. If the value of UP/DOWN counter reaches 384, IC switches latch-off mode.

3-7. Drive output（OUT pin）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output low voltage	Voutl	Vfb = 0V, Iout = 100mA	0.5	1.5	2.5	V
Output high voltage *1	Vouth	Iout = -50mA	14.5	16.0	17.5	V
Output voltage at UVLO	Voutuvlo	Vvcc = 6V, Iout = 5mA	50	100	300	mV
Rise time *1	Trise	Vvcc = 24V, Cout = 1nF	40	80	120	ns
Fall time *1	Tfall	Vvcc = 24V, Cout = 1nF	20	40	70	ns

3-8. VCC section（VCC pin）

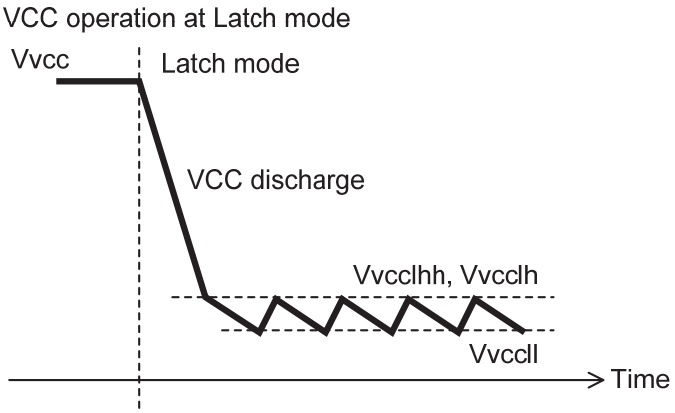
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
UVLO release voltage	Vvccon	Vvcc increasing	11.5	12.5	13.5	V
UVLO voltage	Vvccoff	Vvcc decreasing	6.0	6.5	7.0	V
UVLO hysteresis	Vvcchys	Vvccon－Vvccoff	5.0	6.0	7.0	V
UVLO release delay time *1	Tdlyvccon	Time to initial setup	50	70	90	μs
Over voltage protection threshold voltage	Vthovp	Vvcc increasing	24.5	25.5	26.5	V
Over voltage proteciton delay time *1	Tdlyovp	Vvcc > Vthovp	57	72	88	μs
VCC voltage for DSS	Vvccdssh	Vvcc increasing	8.0	8.5	9.0	V
	Vvccdssl	Vvcc decreasing	7.5	8.0	8.5	V
VCC voltage at latch-off	Vvcclhh	Vvcc discharge end	8.0	8.5	9.0	V
	Vvcclh	Vvcc upper level	8.0	8.5	9.0	V
	Vvccll	Vvcc lower level	7.5	8.0	8.5	V

Note)

DSS function : Even in case that VCC pin voltage decreases in normal operation, the start-up circuit operates for Vvcc to keep between Vvccdssh and Vvccdssl.

Switching is stopped in latch mode when VCC pin voltage Vvcc is kept higher than Vthovp for Tdlyovp.

On entering latch mode, capacitance connected to VCC pin is discharged by supply current in latch-off（Ivcclatcl: see “3-9. Power supply current”）. After that, the start-up circuit operates for Vvcc to keep between Vvccll and Vvcclh, which prevents from operating UVLO and maintains latch mode.



An operating waveform in latch-off mode

3-9. Power supply current（VCC pin）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current in operating	Ivccop1	OUT no load	0.3	0.6	1.0	mA
	Ivccop2	Vfb = 0V	0.2	0.3	0.6	mA
Supply current in latch-off	Ivcclatcl	Vvh=0V, Vvcc=15V	3.5	6	10	mA
	Ivcclat	VVh=0V, Vvcc=8V	0.2	0.3	0.45	mA
Supply current in power off mode	Ivccpom	Vlat = 0V, Vvcc = 9V, Vvh = 0V	0.05	0.15	0.3	mA
Supply current just before UVLO released	Ivccuv	Vvh = 0V, Vvcc= Vcc－0.1V	0.05	0.15	0.3	mA

3-10. High-voltage input section（VCC, VH pin）

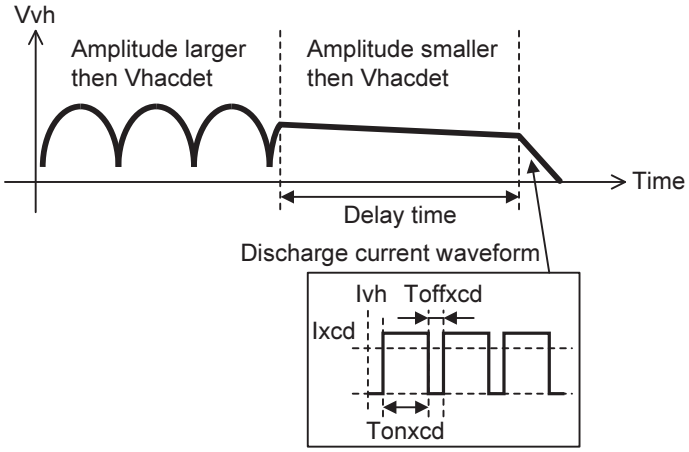
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VH input current	Ivhrun	Vvh = 450Vdc	3	5	20	μA
	Ivhstb	Vvh = 50Vdc, Vvcc = 0V	0.4	0.8	1.6	mA
		Vvh = 50Vdc, Vvcc = 6V to 11V	2.0	3.0	4.0	mA
		Vvh = 50Vdc, Vvcc = Vvccon－0.1V	1.3	3.0	4.0	mA
Charge current for VCC	Ipre	Vvh = 50Vdc, Vvcc = 0V	-1.6	-0.8	-0.4	mA
		Vvh = 50Vdc, Vvcc = 6V to 11V	-3.7	-2.7	-1.7	mA
		Vvh = 50Vdc, Vvcc=Vvccon－0.1V	-3.7	-2.7	-1.0	mA
Start-up circuit consumption current	Ivhint	Ivhstb－Ipre－Ivcc, Vvcc = Vvccon－0.1V	0.01	0.05	0.10	mA
OLP L.C. boundary voltage（3）	Vvhd3h	Vvh increasing	126	138	150	Vdc
	Vvhd3l	Vvh decreasing	114	125	136	Vdc
	Vvhd3d	Vvhd3h－Vvhd3l	7.5	12.5	17.5	Vdc
OLP L.C. boundary voltage（4）	Vvhd4h	Vvh increasing	161	175	189	Vdc
	Vvhd4l	Vvh decreasing	150	163	176	Vdc
	Vvhd4d	Vvhd4h－Vvhd4l	7.5	12.5	17.5	Vdc
OLP L.C. boundary voltage（5）	Vvhd5h	Vvh increasing	209	225	241	Vdc
	Vvhd5l	Vvh decreasing	197	213	229	Vdc
	Vvhd5d	Vvhd5h－Vvhd5l	7.5	12.5	17.5	Vdc
OLP L.C. boundary voltage（6）	Vvhd6h	Vvh increasing	257	275	393	Vdc
	Vvhd6l	Vvh decreasing	245	263	281	Vdc
	Vvhd6d	Vvhd6h－Vvhd6l	7.5	12.5	17.5	Vdc

3-11. XCAP discharge circuit（VH pin）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Average discharge current for XCAP *1	Ixcd	In XCAP discharge	1	2	4	mA
ON-time for XCAP discharge current	Tonxcd	In XCAP discharge	1.2	1.5	1.8	ms
OFF-time for XCAP discharge current	Toffxcd	In XCAP discharge	0.4	0.5	0.6	ms
VH ampulitud ensured AC detection	Vhacdet	Vvh = 67 to 124V	50	—	—	V
		Vvh = 236 to 358V	75	—	—	V
VH ampulitud garenteed AC non detection	Vhnacdet	Vvh = 67 to 97V, Vvh = 281 to 358V	—	—	5	V
Delay time for AC detection	Tacdet		40	56	72	ms

Note)

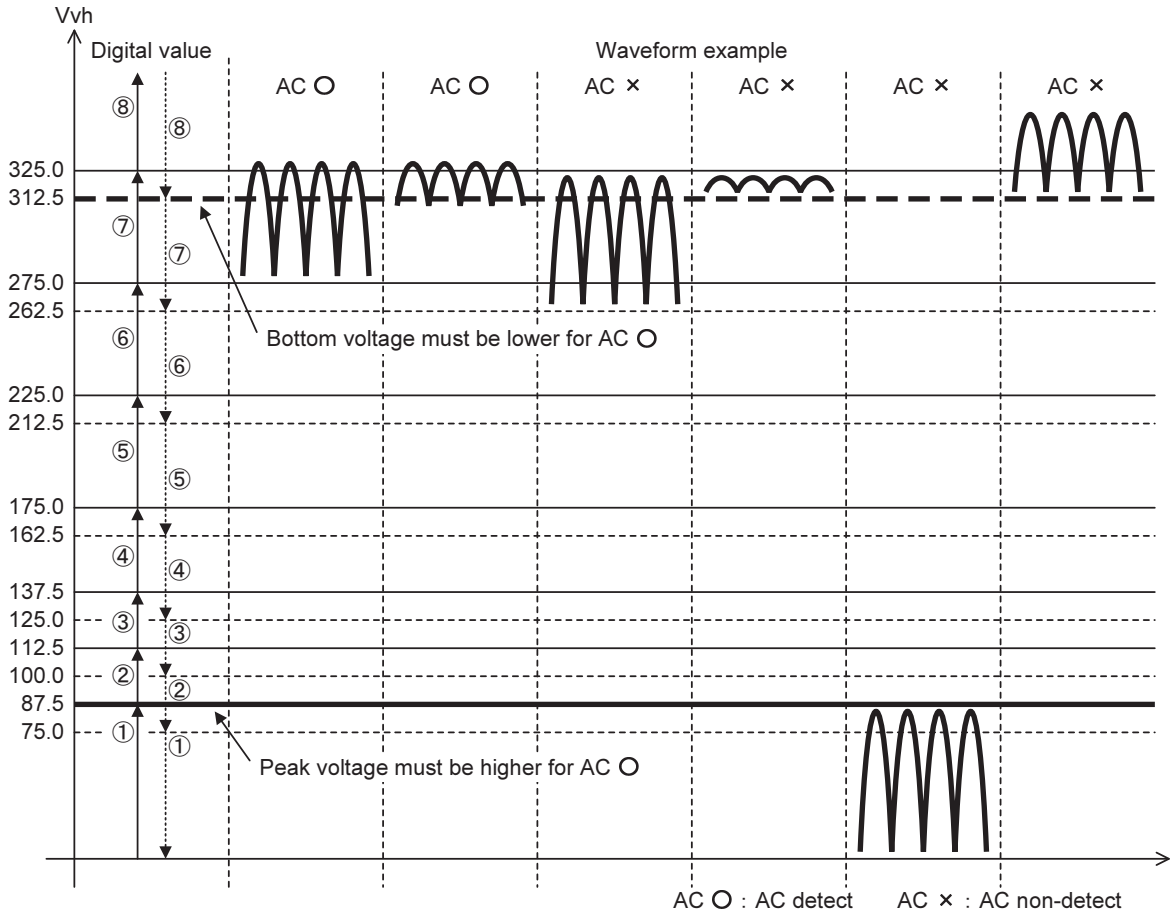
XCAP discharge starts after AC input is cut off and then VH voltage variation is not detected for AC detection delay time.



An operating waveform in XCAP discharge function.

It is VH pin voltage condition for proper AC detection that its peak is more than 87.5V （design value）and its bottom is less than 312.5V（design value）.

VH pin voltage is converted to one of 8 digital values with hysteresis characteristics. At least one increment of the digital value in each AC detection delay time Taccdet is required for judging AC supplies.



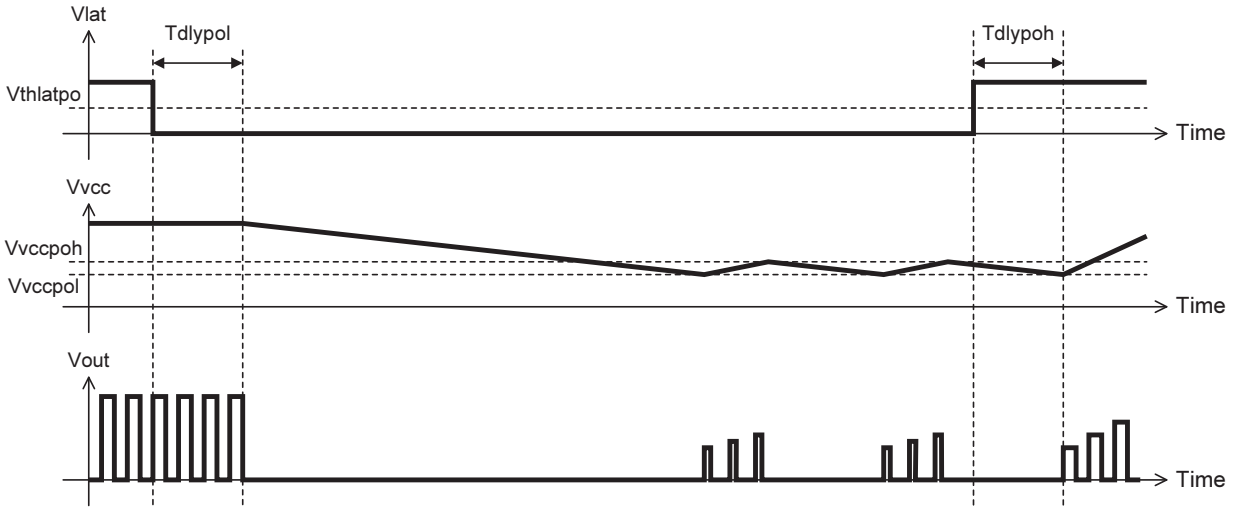
Explanation of AC detection method

3-12. Power off mode（LAT, VCC pins）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
LAT threshold voltage for power off mode	Vthlatpol	Vlat decreasing	0.50	0.55	0.60	V
	Vthlatpoh	Vlat increasing	0.55	0.60	0.65	V
	Vthlatpod	Vthlatpoh－Vthlatpol	0.02	0.05	0.08	V
Power off mode disable time in start-up	Tdlynopo	After UVLO released	115	128	141	ms
Delay time for mode switch	Tdlypoh	Power off mode to normal mode	41	56	71	μs
	Tdlypol	Normal mode to power off mode	41	56	71	μs
VCC voltage to start switching in power off mode	Vvccpol	Vlat < Vthlatpol Vvcc decreasing	7.5	8.0	8.5	V
VCC voltage to stop switching in power off mode	Vvccpoh	Vlat < Vthlatpol Vvcc increasing	8.0	8.5	9.0	V
VCC hysteresis in power off mode	Vvccpod	Vvccpoh－Vvccpol	0.2	0.5	0.8	V
ON pulse width in power off mode	Tpom	Vlat < Vthlatpol Vvcc < Vvcccpol	1.0	1.4	1.8	μs
Switching frequency in power off mode	Fpom	Vlat < Vthlatpol Vvcc < Vvcccpol	55	62.5	70	kHz

Note)

The controller swithes to power off mode after Vlat keeps lower than Vthlatpol for Tdlypol and returns to normal operation after Vlat keeps higher than Vthlatpoh for Tdlypoh. Inspite of this, normal operation is forced before Tdlynopo passes form release of UVLO. In power off mode, OUT pin switches with fixed frequency Fpom and pulse width Tpom for Vvcc to keep between Vvccpol and Vvccpoh by a current supply from a winding of a transformer of a power supply system. After Vlat keeps higher than Vthlatpoh for Tdlypoh, return power off mode starts.



An operating waveform in power off mode

3-13 Over heat protection

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Over heat protection operating temarature *1	Tohp		125	137	150	℃

When temperature exceeds Tohp and overheat protection works, OUT is turned off and IC switches latch-off mode.

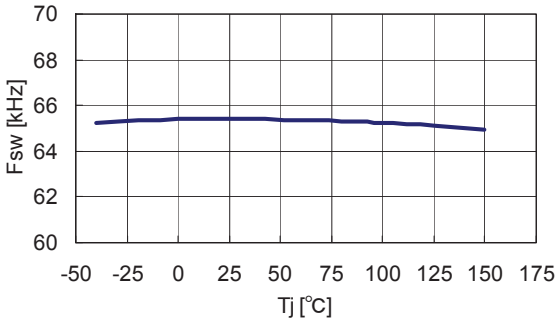
7. Characteristic curve

The characteristics in this section are under described conditions as follows unless otherwise specified.

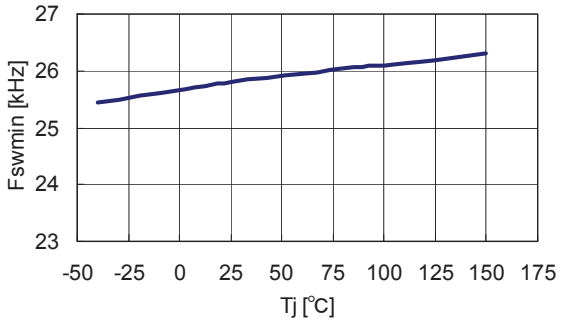
Tj = 25℃, Vvcc = 18V, Vvh = 120V, Vlat = 1.0V, Vfb = 2.5V, Vcs = 0V
Initial setup: S.F.R. : “Low”, OLP L.C. : “Middle”

Notes）
（1）“-” shows source current and “+” shows sink in current regulations of the current.
（2）The data listed here show the typical characteristics of an IC, and does not guarantee the characteristic.

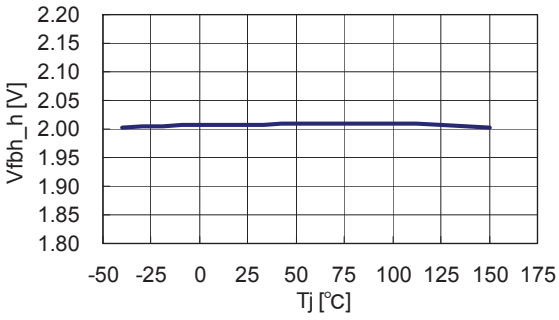
Switching frequency（Fsw）vs Junction tempreture（Tj）



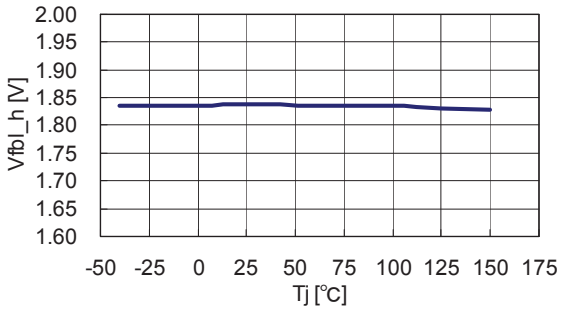
Minmum switching frequency
（Fswmin）vs Junction tempreture（Tj）



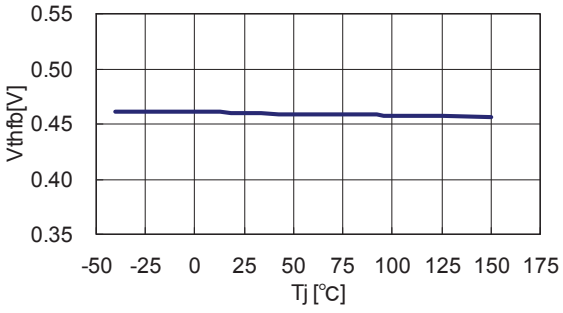
Frequency reduction start FB voltage（Vfbh_h）
vs Junction tempreture（Tj）@S.F.R.=“High”



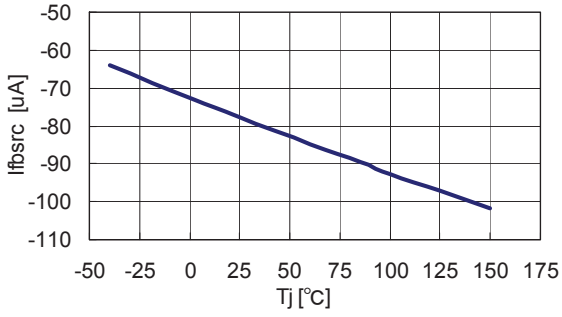
Frequency reduction end FB voltage（Vfbl_h）
vs Junction tempreture（Tj）@S.F.R.=“High”



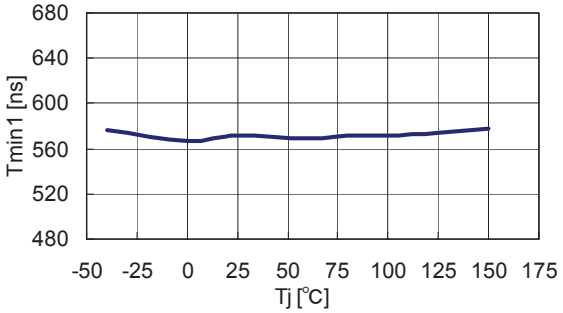
FB threshold voltage for stop switching（Vthfb）
vs Junction tempreture（Tj）@Vlat=0.75V



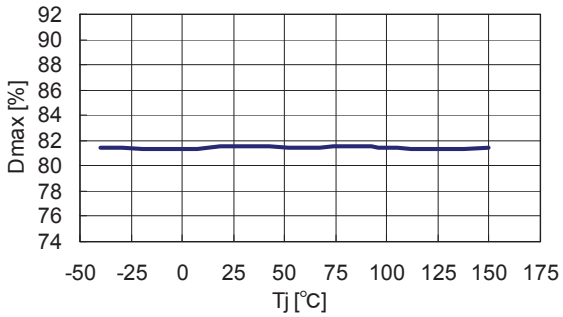
FB output current（Ifbsrc）
vs Junction tempreture（Tj）



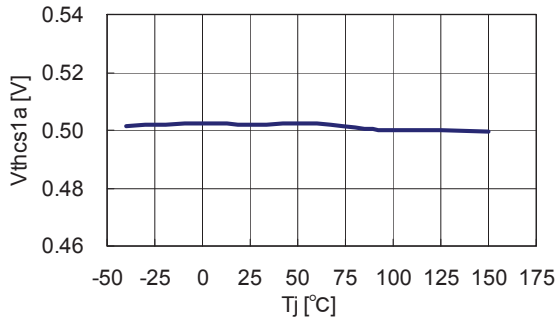
Minmum ON pulse width(Tmin1)
vs Junction tempreture(Tj)



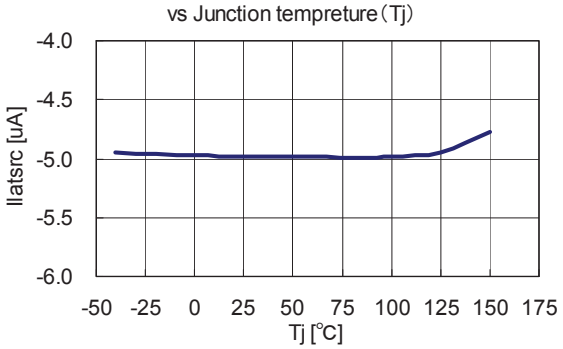
Maximum duty cycle(Dmax)
vs Junction tempreture(Tj)



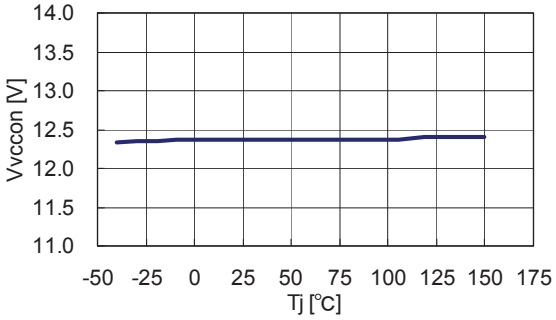
CS threshold voltage(Vthcs1a)
vs Junction tempreture(Tj)



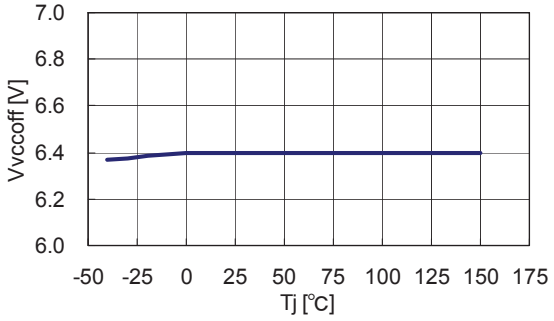
LAT output current(Ilatsrc)
vs Junction tempreture(Tj)



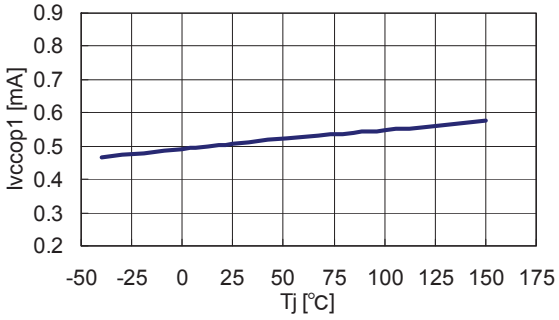
Start-up threshold voltage(Vvccon)
vs Junction tempreture(Tj)



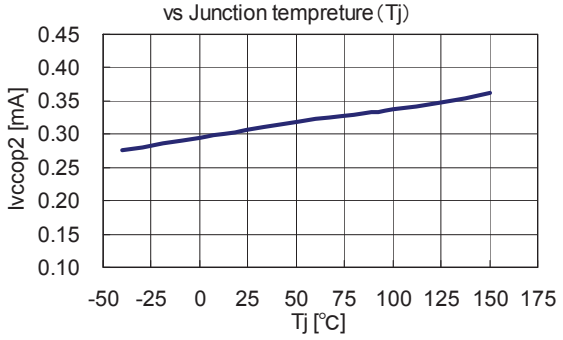
Shut-down threshold voltage(Vvccoff)
vs Junction tempreture(Tj)



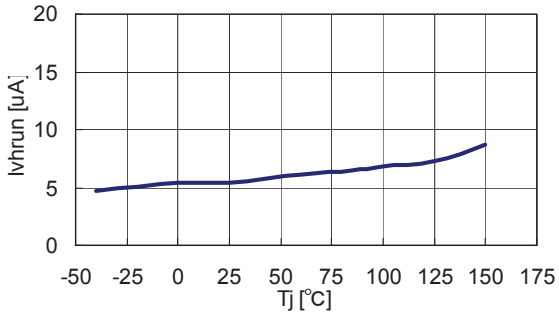
Supply current in operating(Ivccop1)
vs Junction tempreture(Tj)



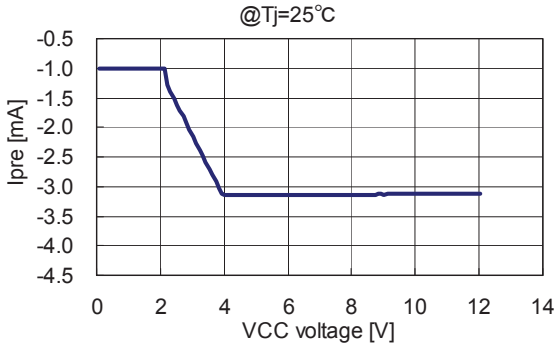
Supply current in operating(Ivccop2)
vs Junction tempreture(Tj)



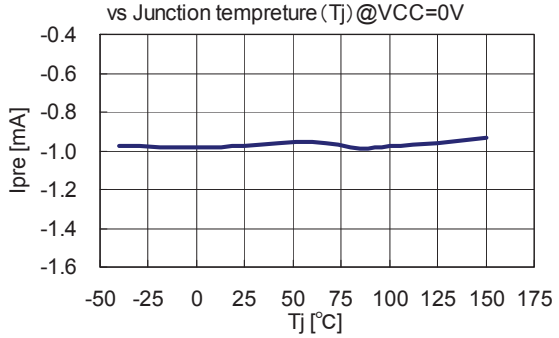
VH input current (Ivhrun)
vs Junction tempreture (Tj) @VH=450V



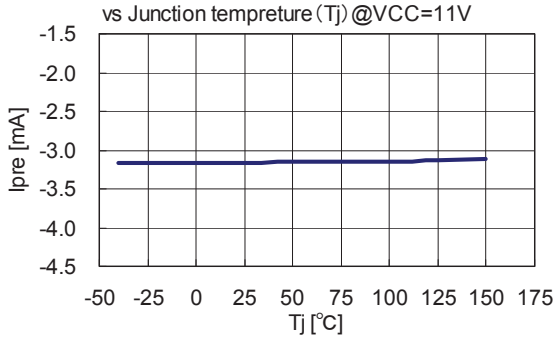
Charge current for VCC (Ipre) vs VCC voltage
@Tj=25℃



Charge current for VCC (Ipre)
vs Junction tempreture (Tj) @VCC=0V



Charge current for VCC (Ipre)
vs Junction tempreture (Tj) @VCC=11V



8. Description of the function （The values in the following description are typical values unless otherwise specified.）

(1) PWM control

FA8A27N performs current mode control. Fig.1 shows a circuit block for basic operations, and Fig.2 shows a timing chart.

A trigger signal having the switching frequency that is output from the oscillator is input to the PWM (F.F.) through the one-shot circuit as a set signal. Then the output of the PWM as well as the OUT pin voltage reaches the High state.

On the other hand, the current comparator (PWM comp.) monitors the MOSFET current, and if the threshold voltage is reached, a reset signal is output. When a reset signal is input, the output of PWM (F.F.) as well as the OUT pin voltage reaches the Low state.

Therefore, The ON pulse width of the OUT pin is thus controlled with the threshold voltage of the PWM comparator (PWM comp.).The output is controlled by changing the threshold voltage of this PWM comp. with feedback signals.

As shown in Fig.1,FB pin voltage and soft-start level input PWM comparator. These signal enabled the lower voltage, as PWM threshold voltage.

The maximum MOSFET current is limited by the voltage of line correction and current detection resistor Rs.

The oscillator outputs pulses for determining the maximum duty cycle. Using these pulses, the maximum duty cycle has been set to 83% (typ).

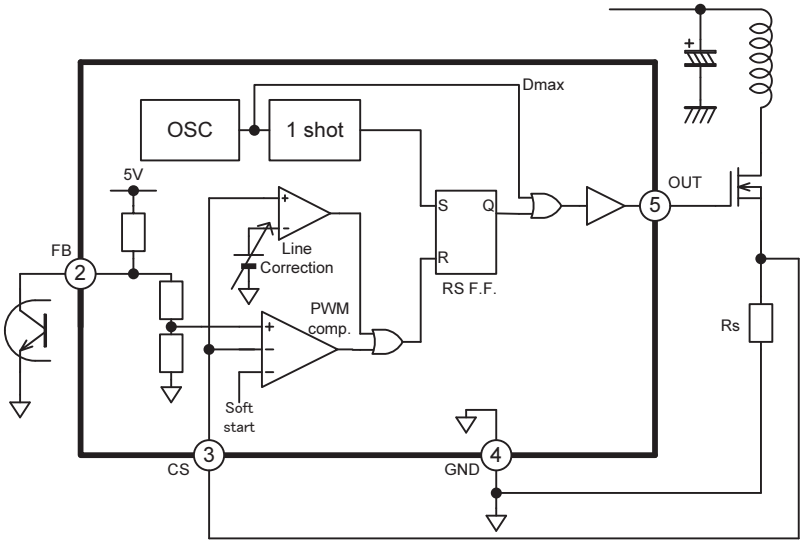


Fig1. Current mode basic operation circuit block

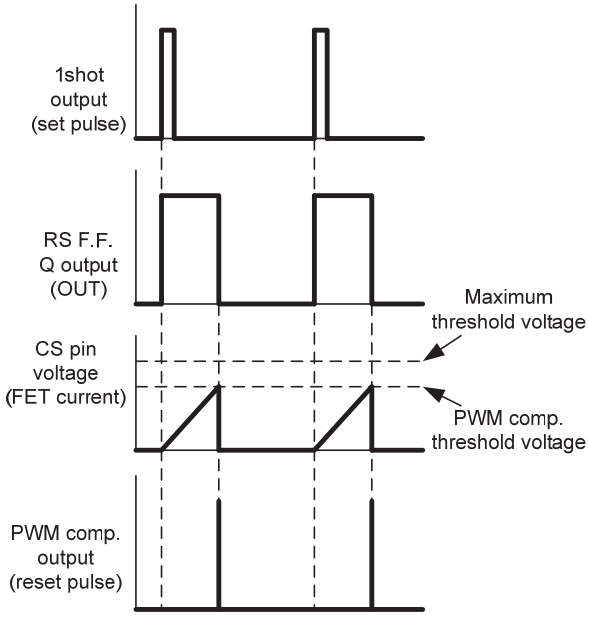


Fig2. Current mode basic operation timing chart

(2) Initial setup function

Switching frequency reduction characteristic（S.F.R.）and OLP line compensation characteristics（OLP L.C.）are decided by initial setup. Initial setup starts when UVLO release delay time（Tdlyvccon : see “3-8. VCC section”）passes after UVLO is released.

S.F.R. can be chosen from three kinds of characteristics, it depends on charging time of the capacitance which connect to LAT pin. LAT pin capacitance（Clat）is charged with the current for LAT capacitance detection （Ilatset）, the selection is decided by the time（LAT threshold time for capacitance detection : Tlatset1,Tlatset2） when LAT voltage （Vlat）exceeds LAT capacitance detecting voltage （Vlatset）. With time for Vlat > Vlatset, “High" is chosen when shorter than Tlatset1, “Middle" is chosen at the time between Tlatset1 and Tlatse2, and "Low" is chosen when longer than Tlatset2. In addition, Clat is discharged until Tdlyvccon passes, and after Tlatset2 passes. And when Tiniset passes, initial setup is end, Ilatsrc（see “3-2. External latch-off function”）is provided from LAT pin, and normal operation starts.

OLP L.C. can be chosen from three kinds of characteristics, it depends on the value of resistance（Rcs）which connect to CS pin. The selection is decided by comparison of CS pin voltage（Vcs）which is decided by flowing the current for CS resistance detection（Icsset）to Rcs and CS resistance detecting voltage（Vcsset1, Vcsset2）. “Middle” is chosen when Vcs < Vcsset1, “Weak” is chosen when Vcsset1 ≦ Vcs ≦ Vcsset2, “Strong” is chosen when Vcs > Vcsset2. In addition, Rcs is discharged until Tdlyvccon passes. And when Tiniset passes, initial setup is end, it becomes normal operation and performs a current sense.

XCAP discharge and switching frequency jittering function become effective from the first time Vlat < Vthlatpol（see “3-12. Power off mode”）after initial setup is end. In addition, when only recommendation resistance and capacitance are connected to LAT pin, Vlat < Vthlatpol at the time of initial setup is end.

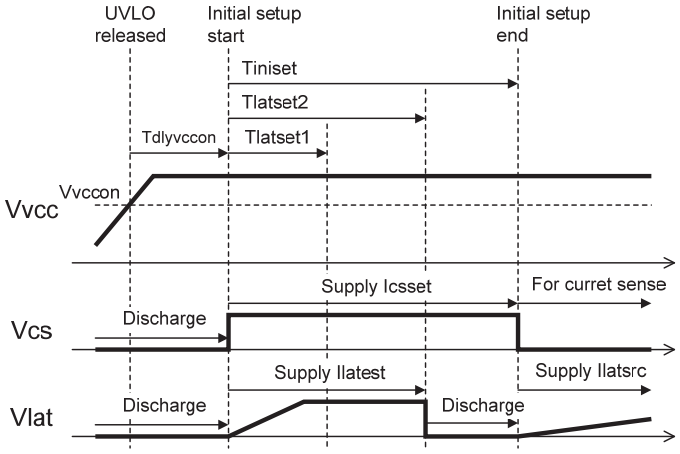


Fig.3 Initial setup operation

S.F.R.

Setting	Time for Vlat > Vlatset	Reccomended Clat [pF]
High	< Tlatset1	220±20%
Middle	Tlateset1 ～ Tlatset2	1000±20%
Low	> Tlatset2	3300±20%

OLP L.C.

Setting	Vcs @ Tiniset	Reccomended Rcs [kΩ]
Middle	< Vcsset1	0.3～0.5
Weak	Vcsset1 ～ Vcsset2	1.4～2.1
Strong	> Vcsset2	3.9～5.2

When test mode set voltage input to LAT pin before UVLO is released, IC runs in test mode and a frequency modulation function and a XCAP discharge function do not operate after initial setup is end. To cancel a test mode, stop inputting voltage to LAT pin and restart IC.

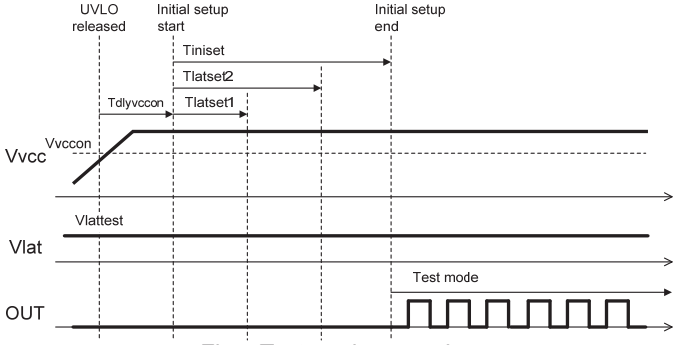


Fig.4 Test mode operation

(3) Minimum ON pulse width function

When the MOSFET is turned on, a surge current is generated due to discharge corresponding to the capacitance of the main circuit and gate drive current. If this surge current reaches the CS pin threshold voltage, normal pulses may not be generated from the OUT pin.
To avoid this phenomenon, a minimum ON width of OUT pin output is set within the one-shot circuit block of the IC.
If a trigger signal having the switching frequency is input from the oscillator, a pulse having a specific width is output as a PWM latch (F.F.) set signal.
Since the set signal has priority over the input signal of the PWM latch, the output of the PWM latch (F.F.) is not reversed while the set signal from the one-shot circuit is being input, even if a reset signal is input from the current comparator (CS comp.) (See Fig.1)
As a result, the input to the CS pin is kept invalid for the specified period of time immediately after the output pulse is generated from the OUT pin (minimum ON width), and made not to respond to the surge current at turn-on. (See Fig.5)

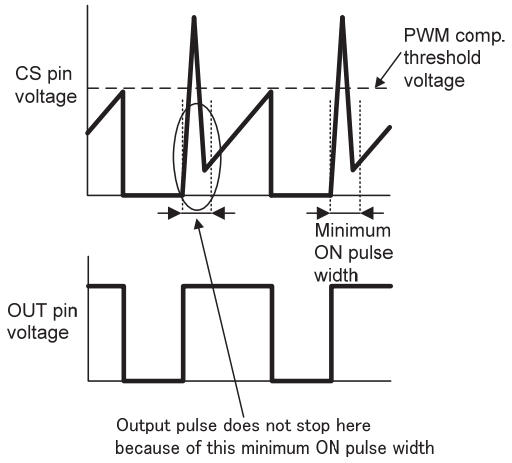


Fig5. Minimum ON pulse

(4) Frequency decrease function

The switching frequency for normal operation mode is set to 65 kHz inside the IC. To decrease loss under light load, however, the function of decreasing switching frequency under light load is provided. Frequency under light load decreases to the lowest frequency almost linearly in proportion to the FB pin voltage. The minimum frequency is set to 25 kHz.

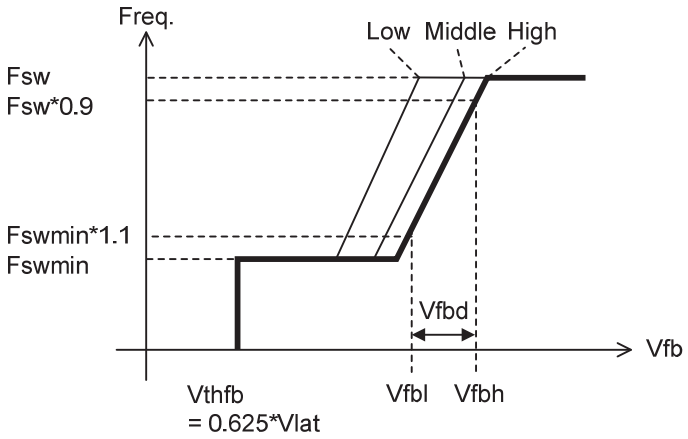


Fig.6 FB-pin voltage vs. switching frequency

(5) Burst operation function

To achieve low standby power, burst operation is automatically started under light load. If the FB pin voltage decreases to lower than the pulse stop FB voltage, switching is stopped. On the contrary, if the FB voltage increases to higher than the pulse stop FB voltage, switching is restarted. The FB pin voltage repeats overshoot and undershoot across the pulse stop FB voltage. Continuous pulses are output in this overshoot period, and a long stopping period is obtained in the undershoot period.

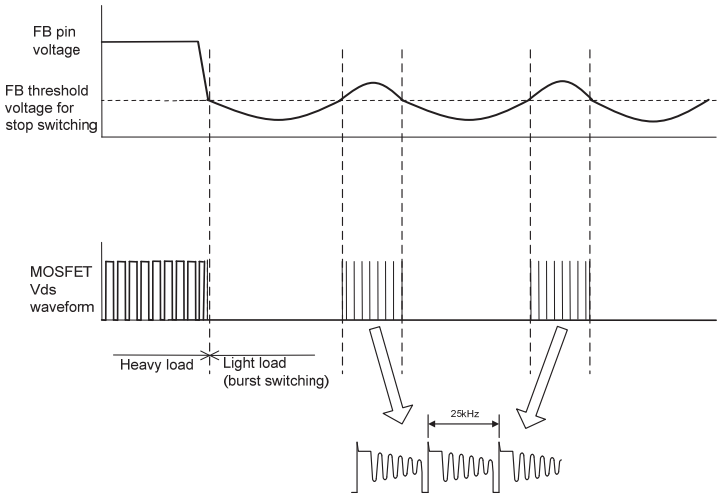


Fig.7 Burst operation at light load

(6) Frequency decrease start and burst operation start point adjusting function

To decrease switching loss under light load, frequency decrease function is integrated. However, if the frequency is decreased under heavy-load conditions, a problem of output ripple may arise. In addition, to achieve low standby power, burst operation function is integrated. However, if burst operation is performed under heavy-load conditions, audible noise may be generated from the transformer. With this IC, the frequency decrease start point and the burst operation start point are respectively adjusted based on the settings of the resistor and the capacitor connected between the LAT pin and the GND.

(7) Power off mode function

If the LAT pin voltage is decreased to 0.55 V or lower, the power-off mode is entered. In this mode, the control by FB pin voltage is invalidated. If the VCC pin voltage decreases to 8.0 V or lower, switching is started, whereas if the voltage increases to 8.5 V or higher, switching is stopped. These operations are repeated to forma a lower-frequency burst waveform, thus achieving lower standby power. Since the output voltage becomes dependent on the turn ratio of the secondary winding of transformer to the VCC auxiliary winding, a DC-DC converter, etc. may become necessary.

(8) Frequency diffusion (Spread spectrum)

FA8AxxN perform frequency modulation of ± 7.0 kHz for switching frequency 65 kHz. This function enables more noise energy of the switching to disperse compared to the case with fixed frequency and obtains a conduction EMI reduction effect. While the reduction effect depends on the filter parts mounted on the power supply board, effective use of this function allows the reduction of the number of the filter parts and the constants.

In addition, Since the frequency diffusion function is always subjected to frequency variation, it is effective to reduce conduction EMI at light load.

(9) DSS(Dynamic Self Supply) function

When power is turned on, the capacitor connected to the VCC pin is charged by the current supplied to the VCC pin from the startup circuit via the HV pin, and voltage increases. When this voltage exceeds the ON threshold voltage of 12.5 V, the power supply for internal circuit is turned on, and switching is started. At this time, if the voltage supplied from the VCC auxiliary winding is higher than 8 V, the startup circuit is operated only at the time of startup, and after the startup, operation is performed with the voltage of the auxiliary winding used as the power supply. However, if the voltage supplied from the auxiliary winding decreases to lower than 8 V due to switching to low-output voltage in standby mode due to the time of latch stop by overvoltage and overload, operation is continued with the VCC voltage maintained between 8 V and 8.5 V by ON/OFF of the startup circuit.

With FA8A68N, only in the case of latch stop, this function interrupts operation, thus the VCC pin voltage decrease to the OFF threshold voltage, and automatic recovery is achieved by restarting the IC.

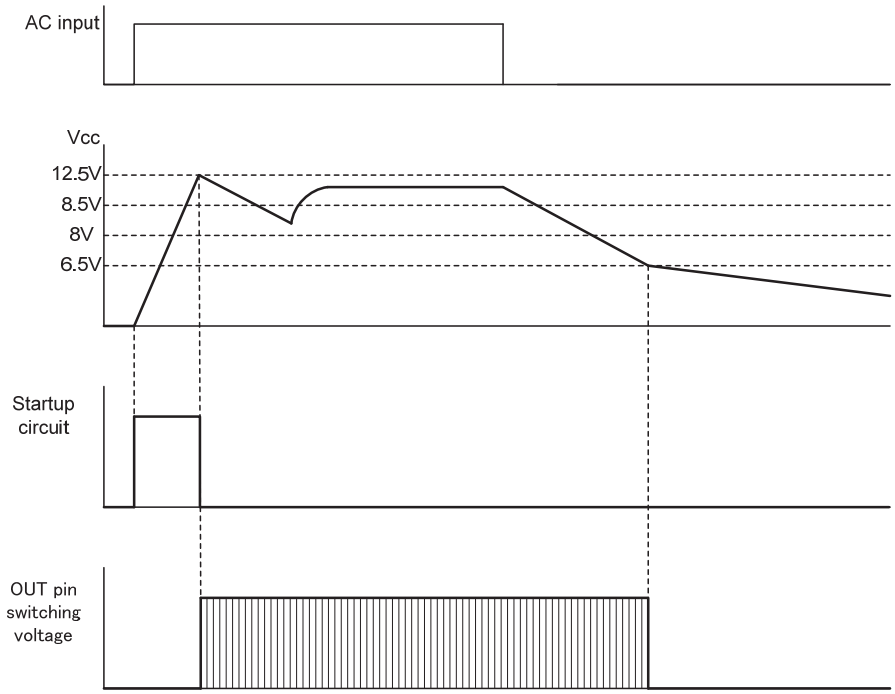


Fig.8 Startup and shutdown (When auxiliary winding voltage is higher than 8V)

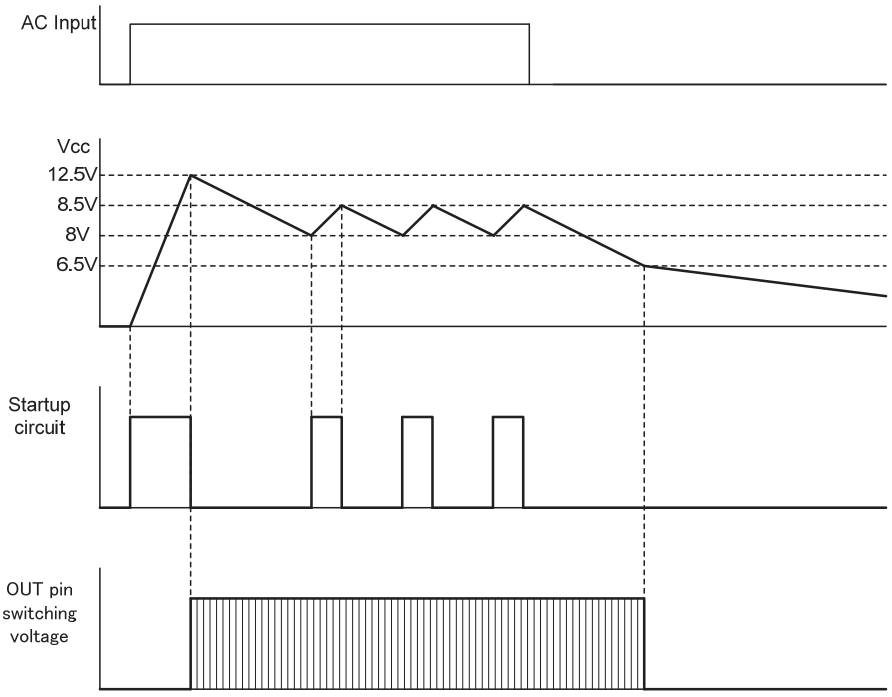


Fig.9 Startup and shutdown (When auxiliary winding voltage is lower than 8V)

(10) Operation under overload (Automatic recovery type and timer latch type series are available.)

■Automatic recovery type

If the CS pin voltage exceeds the overload protection CS threshold voltage, and that state continues for 200 ms, namely the overload protection stop delay time, under overload, switching is forcibly stopped.

When switching is stopped, supply of current from the auxiliary winding is stopped, and the VCC pin voltage decreases to 11.5 V or lower, the startup circuit is operated, and the VCC voltage is maintained within a range from 11.5 V to 12 V. When 1400 ms elapses after the switching is stopped, switching is resumed. If overload state is continuing at that time, start and stop operations are repeated. If normal load is resumed, operation goes back to normal.

Note, however, that since an up-down counter is used to count the overload protection stop delay time, to clear the up-count, down-count of the same period is required. Consequently, if a state where the overload period (1) is longer than the normal operation period (2) continues, count-up time is accumulated, and overload protection is actuated in time shorter than the overload protection stop delay time. Be careful if the operation undergoes overload and normal load conditions repeatedly.

At the time of startup, the output voltage must be increased to the setting within 200 ms.

The Automatic recovery function operates normally even when external power is input directly to the VCC pin because the automatic recovery operation is controlled by an integrated timer.

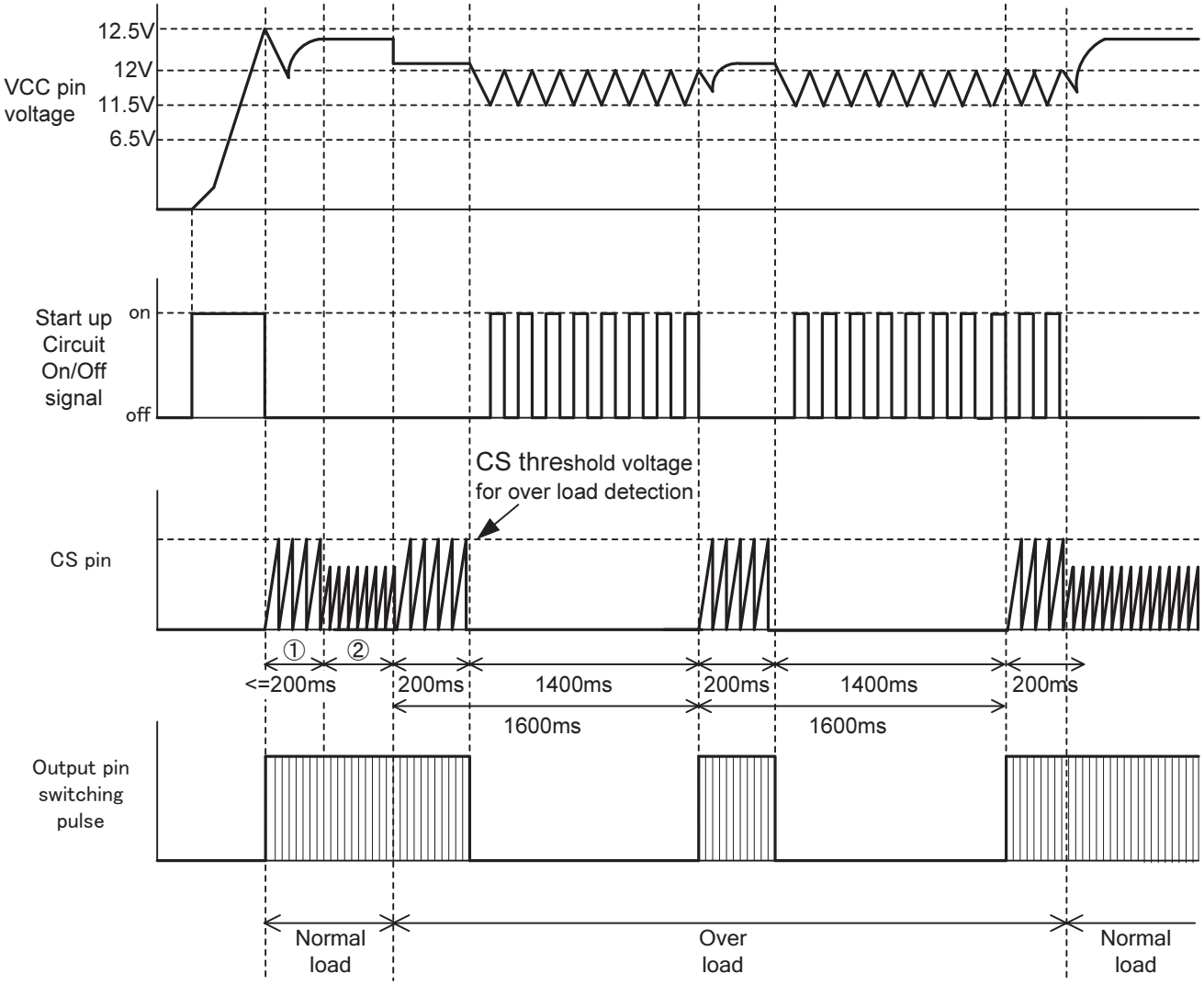


Fig.10 Operation under overload (Auto recovery type)

■Timer latch type

If the CS pin voltage continues exceeding the overload protection CS threshold voltage for 200 ms, namely the overload protection stop delay time, or longer under overload, switching is stopped and the latch stop maintain this stopping state. In a state where switching is stopped by overload latch, VCC voltage is supplied by the startup circuit and operation suspension state is maintained.

Note, however, that since an up-down counter is used to count the overload protection stop delay time, to clear the up-count, down-count for the same period is required. Consequently, if a state where the overload period (1) is longer than the normal operation period (2) continues, count-up time is accumulated, and overload protection is actuated in time shorter than the overload protection stop delay time. Be careful if the operation undergoes overload and normal load conditions repeatedly.

To reset the overload latch, it is necessary to stop the supply of VCC voltage from the startup circuit by interrupting the input voltage, thereby decreasing the VCC voltage to 6.5 V, namely OFF threshold voltage, or lower.

Note that at the time of startup, the output voltage must be increased to the setting within 200 ms.

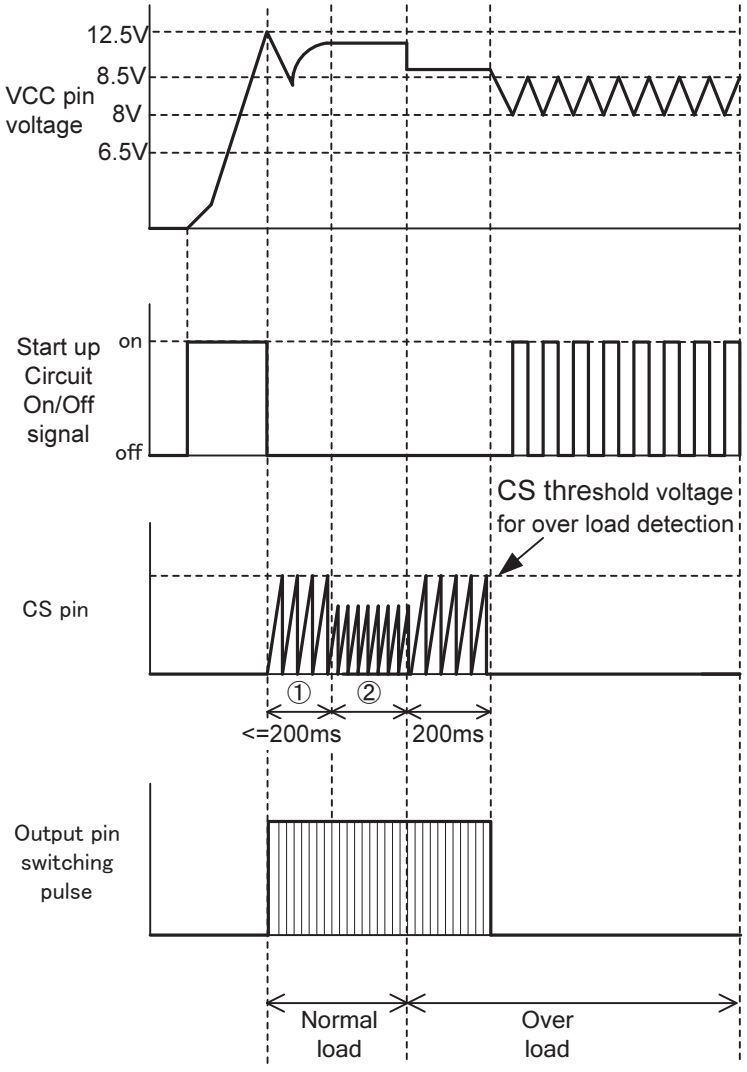


Fig.11 Operation under overload (Timer latch type)

(11) Over voltage protection

If the secondary output voltage reaches a state of overvoltage, the voltage of the auxiliary winding also increases. The VCC pin has a function of detecting the voltage of this auxiliary winding, and if the VCC pin voltage continues exceeding 25.5 V for 72 μs, latch stop is implemented. If latch stop is implemented, the VCC pin voltage is maintained by the startup circuit, and the latch stop state is continued. This state is maintained until the VCC pin voltage decreases to the OFF threshold voltage at UVLO or lower by interrupting the input voltage.

With FA8A68N, the VCC pin voltage is not maintained by the startup circuit after the switching is stopped. Automatic recovery is implemented by restarting IC when the VCC pin voltage is decreased to the OFF threshold voltage.

(12) Latch stop function by external signals

Latch stop is implemented by pulling up the LAT pin to 1.8 V or higher externally for 72 μs or longer. After the latch stop, the VCC pin voltage is maintained by the startup circuit, and latch stop state is continued. This state is maintained until the VCC pin voltage decreases to the OFF threshold voltage at UVLO or lower by interrupting the input voltage.

With FA8A68N, the VCC pin voltage is not maintained by the startup circuit after the switching is stopped. Auto restoration is implemented by restarting the IC when the voltage is decreased to the OFF threshold voltage.

(13) Under voltage lockout function (UVLO)

To prevent circuit malfunction under under-voltage conditions, a low-voltage malfunction prevention circuit is integrated. If the VCC voltage increases from 0V, the IC starts operating when VCC = 12.5 V, and when the VCC voltage decreases, the operation is stopped when VCC = 6.5 V.

(14) Soft start function

When switching is started at the time of startup or automatic recovery after the interruption for overload protection, the overcurrent limit threshold voltage of the CS pin gradually increases, and furthermore the lowest ON width is fixed to Tmin2 (0.28 μs) to prevent surge voltage Vds of the MOSFET at the time of startup. The overcurrent limit threshold voltage reaches approximately 470 mV when soft start time Tss of 11 ms has elapsed after the start of switching. Furthermore, when Tssend (17 ms) is reached, the lowest ON width switches to Tmin1 (0.56 μs), and at the same time the frequency diffusion function is actuated.

(Vss voltage:See block diagram)

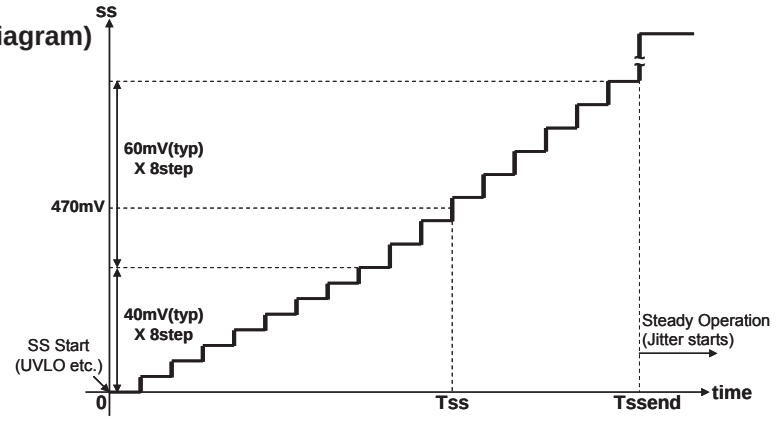


Fig.12 Soft start function

(15) Function of correcting the dependence of overload detection level on input voltage + correction amount adjusting function

The overload detection level varies depending on the input voltage. This IC detects the input voltage, and depending on that voltage, changes the overload protection CS threshold voltage, thereby correcting the dependency on the input voltage.

Since the dependency on the input voltage varies depending on the specifications of power supply, the correction amount can be adjusted using an external resistor mounted between the CS pin and the MOSFET.

(16) Internal overheat protection function

If the IC temperature increases to 137°C or higher, switching is stopped by latch stop. Once latch stop is implemented, the VCC pin voltage is maintained by the startup circuit, and the latch stop state is continued. This state is maintained until the VCC voltage decreases to the OFF threshold voltage or lower by interrupting the input voltage.

With FA8A68N, the VCC pin voltage is not maintained by the startup circuit after the switching is stopped. Automatic recovery is implemented by restarting the IC when the voltage is decreased to the OFF threshold voltage.

(17) Discharge function of the input filter X-capacitor at AC power interruption (Provided or not provided depending on series.)

By connecting the VH pin to the capacitor of the input filter by full-wave rectification connection, the X-capacitor of the input filter can be discharged when AC input power is interrupted. This function eliminates discharge resistance, thereby decreasing standby power.

The recommended capacitance of connectable X-capacitor is 2 μF or lower.

(Requirement in UL60950 regarding electric shock: The voltage value of the power supply input part shall be attenuated to 37% or lower of the peak value within 1 s after the AC input voltage is interrupted.)

9. How to use each pin and advice for designing

(The values that appear in the following description are typical values, unless otherwise specified.)

(1) Pin No. 1 (LAT pin)

Function

(i) Implements latch stop by external signals.

(ii) Adjusts operation mode switching point under light load.

(iii) Switches to power off mode

How to use

(i) Latch stop by external signals

- Connection method

Pull up the LAT pin by external signals.

Figures 13 and 14 provide typical connections of the overvoltage protection circuit.

- Operation

If the LAT pin voltage exceeds 1.8 V and this state continues for 72 μs or longer, the output switching is stopped and thus latch stop is implemented.

If latch stop is implemented, the VCC pin voltage is maintained within a range from 8.0 V to 8.5 V by the startup circuit, and thus the latch stop state is continued.

To reset that state, decrease the VCC voltage to 6.5 V, namely the OFF threshold voltage at UVLO, or lower.

With FA8A68N, the VCC pin voltage is not maintained by the startup circuit after the switching is stopped.

Automatic recovery is implemented by restarting the IC when the VCC voltage is decreased to the OFF threshold voltage.

(ii) Operation mode switching point adjustment under light load

(Adjustment of frequency decrease start points and burst operation start points)

- Connection method

Connect a resistor and a capacitor between the LAT pin and the GND. (See Fig. 15.)

- Operation

The frequency decrease start point can be adjusted in three stages depending on the capacitance of the capacitor.

At the time of startup, depending on the time until the 50 μA source current output from the LAT pin charges the capacitor connected between the LAT pin and the GND to the specified threshold voltage, frequency decrease start FB voltage can be adjusted in three stages. See specifications for three frequency decrease start FB voltage conditions.

Depending on the resistance value, the burst operation start point can be adjusted linearly under light load.

During normal operation, 5 μA source current is output from the LAT pin, and depending on the voltage generated at the resistor connected to the LAT pin and the GND, the pulse stop FB voltage of the FB pin can be adjusted linearly. The pulse stop FB voltage of the FB pin becomes approximately 0.63 times the voltage generated at the resistor connected between the LAT pin and the GND by the LAT pin source current of 5 μA in normal operation.

(iii) Power off mode switching function

- Connection method

The LAT pin is pulled down by external signals.

Figure 16 is a typical connection diagram.

- Operation

By decreasing the LAT pin voltage to 0.55 V, namely the power off mode threshold voltage, or lower, power off mode is entered.

Once the power off mode is entered, feedback control at normal FB pin voltage is stopped as shown in Fig. 17, switching start and stop are repeated based on the VCC pin voltage value, and by decreasing the burst frequency, lower standby power is achieved. If the VCC pin voltage increases to 8.5 V or higher, switching is stopped, whereas switching is started when the value decreases to 8.0 V or lower. Consequently, since the output voltage becomes dependent on the turn ratio of secondary winding of the transformer to the VCC auxiliary winding, a DC-DC converter, etc. may become necessary.

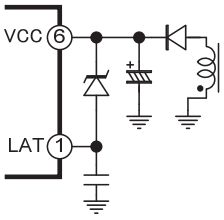


Fig.13 Overvoltage protection on the secondary side1

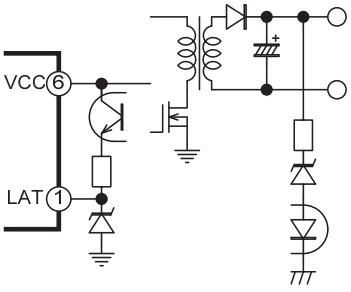


Fig.14 Overvoltage protection on the secondary side2

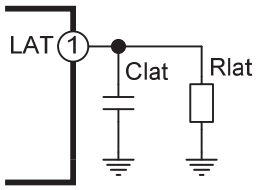


Fig.15 LAT pin: Adjustment under light load

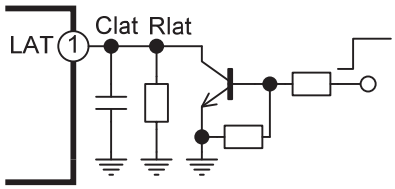


Fig.16 Power off mode switching circuit

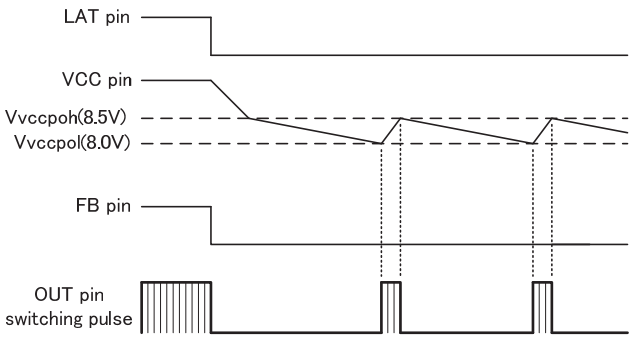


Fig.17 Power off mode operation waveform

Advice for designing

(1) Caution in pulling up LAT pin by external signals

By increasing the LAT pin voltage to 2.0 V (max.) or higher for the period of 72 μs, latch stop is implemented, but since the LAT pin voltage (absolute maximum ratings) is 3.3 V, the LAT pin must be clamped in order that the voltage falls within the range from 2.0 V to 3.3 V.

Therefore connect a Zener diode between the LAT pin and the GND as shown in Fig. 14.

Although the LAT pin integrates a Zener diode, the LAT pin current is 300 μA or lower (absolute maximum ratings). The Zener diode connected between the LAT pin and the GND can also be omitted by suppressing the input current to 300 μA or lower using a limiting resistor. Note, however, that delay time is generated due to external parts until the LAT pin voltage is increased because a resistor and a capacitor are connected between the LAT pin and the GND. Furthermore, attention should be paid because the IC integrates latch delay time of 72 μs.

(2) Adjusting the frequency decrease start point

With this IC, the frequency decrease start point can be adjusted in three stages by the capacitor connected between the LAT pin and the GND.

See the specifications for the three frequency decrease start FB voltage conditions.

To select each condition, connect the following capacitors between the LAT pin and the GND.

frequency decrease start point	Clat
To select high point	176pF＝＜Clat＝＜264pF
To select medium point	800pF＝＜Clat＝＜1200pF
To select low point	2640pF＝＜Clat＝＜3960pF

Note that since the capacitor also has a role of stabilizing the threshold voltage at the burst operation switching point as described below, mount the capacitor at a point as close to the LAT pin as possible. Caution should be paid, in particular, when the capacitance of the capacitor is small.

(3) Adjusting the burst operation start point

With this IC, the burst operation start point can be adjusted linearly by the resistor connected between the LAT pin and the GND. The pulse stop FB voltage of the FB pin becomes approximately 0.63 times the voltage generated at the resistor connected between the LAT pin and the GND by the LAT pin source current of 5 μA in normal operation.

Meanwhile, since external latch stop threshold voltage of 1.6 V (min.) and power off mode threshold voltage (including hysteresis) of 0.65 V (max.) are set to the LAT pin voltage, the adjustable range of LAT pin voltage usable for burst switching point adjustment is from 0.65 V to 1.6 V.

Rlat>=LAT voltage(0.65V) / LAT pin source current（MIN)
Rlat>=0.65V / 4.5uA
Rlat>=145kΩ(Recommended operation condition)

Rlat=<LAT voltage (1.6V) / LAT pin source current（MAX)
Rlat=<1.6V / 5.5uA
Rlat=<290kΩ(Recommended operation condition)

Consequently, recommended resistance value must fall within the following range with fluctuation and temperature characteristics taken into consideration:

145 kΩ = <Rlat = <290 kΩ.

The pulse stop FB voltages are as follows when the following resistors are connected:

270 kΩ (typ) (±1%): 270 kΩ (typ)*5 μA (typ)*0.63=0.85 V
150 kΩ (typ) (±1%): 150 kΩ (typ)*5 μA (typ)*0.63=0.47 V.

(The pulse stop FB voltage is approximately 0.63 times the LAT pin voltage.)

Since the pulse stop FB voltage of the FB pin is approximately 0.63 times the LAT pin voltage in normal

operation, the pulse stop FB voltage fluctuates if noise enters the LAT pin. Therefore, connect the capacitor to be placed between the LAT pin and the GND at a position as close to the LAT pin as possible. Caution should be paid when the capacitance of the capacitor is small.

(4) Fluctuation of continuous switching frequency at the time of burst operation

The continuous switching frequency in burst operation is basically 25 kHz as shown in Fig. 17. However, if the overshoot voltage of the FB pin at continuous switching exceeds the FB threshold voltage at the minimum frequency, the frequency decrease range is entered, and as shown in Fig. 15, the frequency may fluctuate and audible noise may be generated from the transformer. In such a case, make an adjustment so as to decrease the burst operation start point and increase the frequency decrease start point, which may improve the situation.

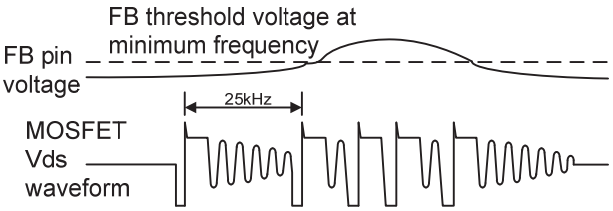


Fig.18 Burst operation waveform

(2) Pin No. 2 (FB pin)

Function

(i)Input feedback signals from the error amplifier on the secondary side.

(ii)Reduce switching frequency.

(iii)Stops switching for burst operation.

How to use

(i) Feedback signal input

• Connection method

Connect the optocoupler corrector to this pin will allow reguration. At the same time, to prevent generation of noise, connect a capacitor in parallel to the optocoupler (Fig. 21).

• Operation

Pin No. 2 is biased from the IC internal power supply via the resistance. The FB pin voltage is level-shifted and input into the current comparator to provide the threshold voltage of the MOSFET current signals to be detected with the CS pin.

(ii) Frequency decrease function

• Connection method

The same as feedback signal input in (i)

• Operation

The switching frequency in normal operation mode is set to 65 kHz inside the IC. If the FB pin voltage decreases under light load, the frequency decreases almost linearly in proportion to this voltage. The lowest frequency is 25 kHz.

The frequency decrease start point can be adjusted in three stages depending on the capacitance of the capacitor connected between the LAT pin and the GND as shown in Fig. 22.

(iii) Burst operation

• Connection method

The same as feedback signal input in (i)

• Operation

FB pin voltage decreases under light load. If the FB pin voltage decreases to lower than the pulse stop FB voltage, switching is stopped. On the contrary, if the FB voltage increases to higher than the pulse stop FB voltage, switching is restarted. By repeating this operation, burst operation is achieved. To undershoot the FB pin voltage significantly at the time of burst operation, the internal FB pin resistance is switched (Fig. 21).

With this IC, the pulse stop FB voltage, which serves as a burst operation switching point, can be adjusted linearly in accordance with the resistance value of the resistor connected between the LAT pin and the GND as shown in Fig.20 .

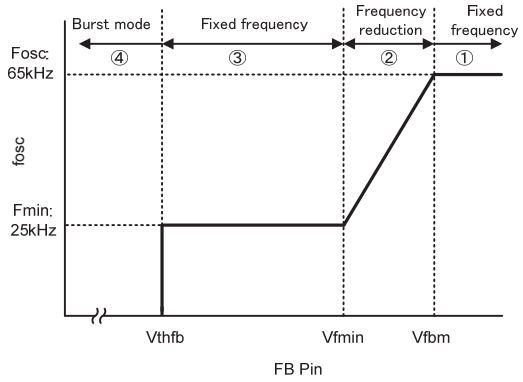


Fig.19 FB pin voltage and oscillating frequency

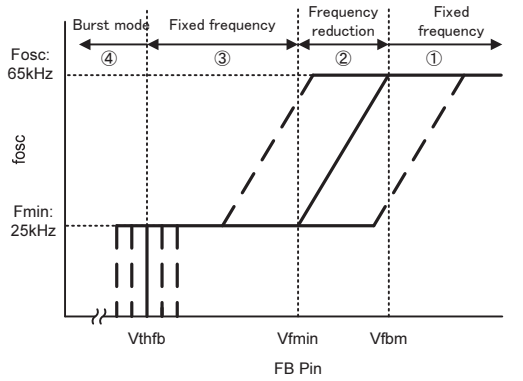


Fig.20 Operation adjusting function under light load

Advice for designing

The FB pin provides threshold voltage of the current comparator. If noise is added to the pin, output pulse fluctuation may result. To prevent generation of noise, a capacitor having the capacitance of approximately 100 pF to 0.01 μF is connected for use as shown in Fig. 21.

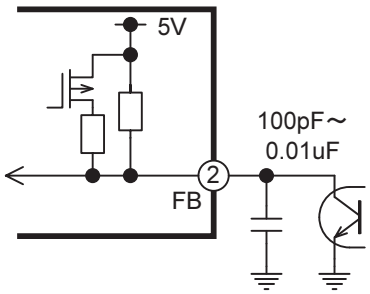


Fig.21 FB pin circuit

(3) Pin No. 3 (CS pin)

Function

(i) Detects the current value of MOSFET and limits the current.

(ii) Detects overload state.

(iii) Adjusts the correction amount of dependency of the overload detection level on the input voltage.

How to use_

(i) Current detection and current limiting

• Connection method

Connect a current detecting resistor Rs between the MOSFET source pin and the GND. The current signals of the MOSFET generated in the resistor are input (Fig. 22).

• Operation

The current signals of the MOSFET input to the CS pin is then input to the current comparator, and if it reaches the threshold voltage determined by the FB pin, the MOSFET is turned off. This FB pin voltage fluctuates due to the feedback circuit from the output voltage to control the MOSFET current.

The CS pin voltage also is input in the OLP_CS comparator, and the MOSFET current under overload, etc. is limited to the current determined by the overload CS threshold voltage and the current detection resistor Rs.

(ii) Overload detection

• Connection method

The same as the current detection and current limiting in (i)

• Operation

If the state where current is limited because the CS pin voltage has reached the overload CS threshold voltage continues for 200 ms or longer, that state is judged to be overload state. In the case of timer latch type, switching is stopped, detecting overload state, and the latch stop mode maintain this stopping state. In the case of automatic recovery type, intermittent operation is performed under overload, and normal operation is resumed when overload state is reset. See 8.(9) Overload operation for details.

(iii) Adjusting the correction amount of dependency of overload detection level on the input voltage

• Connection method

As shown in Fig. 23, add a resistor Rcs between the current detecting resistor of the MOSFET and the CS pin. If the CS pin includes a CR filter, adjustment can be made using that resistance value. (Fig. 24)

• Operation

The overload detection level becomes high as the input voltage becomes high. This IC detects the input voltage, and corrects the dependency of the overload detection level on the input voltage by switching the overload protection CS threshold voltage (Vcsth) of the CS pin at each point of the input voltage. However, since the dependency of overload detection level on the input voltage varies depending on the specifications of the power supply (such as L value of the transformer and output capacity etc.), the correction amount can be adjusted.

As the adjusting method, at the time of startup only, constant source current (100 μA) is output from the CS pin for a specified period of time, and the correction amount is adjusted depending on the voltage generated at the resistor connected between the CS pin and the GND (such as a resistor inserted between the current detecting resistor of the MOSFET and the CS pin). The correction amount can be adjusted under three conditions. See Figs. 22, 23, and 24 for the notion of three correction conditions. Weak has the smallest amount of input voltage correction, followed by Middle, and then by Strong.

In addition, since hysteresis applies to the overload protection threshold voltage switching point and overload detection level varies in accordance with the increase/decrease of the input voltage, adjustment requires special attention.

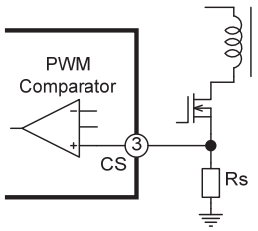


Fig.22 CS pin current detection

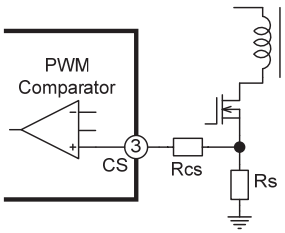


Fig.23 Adjustment of the correction amount of overload on input voltage (1)

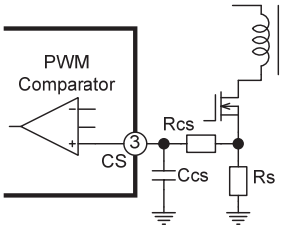


Fig.24 CS pin filter

Advice for designing

(1) Inserting a filter

This IC integrates a blanking function to suppress the effect of surge current that is generated at turn-on part of the MOSFET. However, if the surge generated at this turn-on part is large, or due to external noise, malfunction may result. In such cases, add a CR filter to the CS pin as shown in Fig. 24.

Select a filter depending on the magnitude of the noise, but the selection requires special attention because delay factor increases, thereby increasing fluctuation in overload detection level if the time constant of Rcs × Ccs increases. Install the capacitor Ccs at a place as close to the IC as possible to ensure effective operation, and pay special attention in installing wiring. Depending on the time constant of the filter, the overload detection level and load point for switching into burst operation (burst point) vary, thus causing generation of audible noise and affecting standby power. Be sure to check thoroughly.

(2) Adjusting the correction amount of dependency of overload detection level on the input voltage

By adding a resistor between the current detection resistor of the MOSFET and the CS pin, the correction amount of dependency of overload detection level on the input voltage can be adjusted. However, if a CR filter is included, unless the CR time constant is adjusted by changing the value of the capacitor along with the resistance value, the overload detection level itself may fluctuates, thereby inhibiting appropriate adjustment of the correction amount. If such adjustment is considered to be cumbersome, add a separate resistor R1 between the CR filter and the CS pin as shown in Fig. 28, and the correction amount can be adjusted with the CR filter constant fixed. Note, however, that the resistance value with correction amount adjusted is a resultant value of R1 + Rcs. If the time constant of the CR filter increases, the dependency of the overload detection level on the input voltage increases, whereas decreased time constant decreases the dependency. For fine-adjusting the correction amount, adjust the time constant of the CR filter at the same time. Note, however, that if the time constant of the filter is changed, the overload detection level itself changes, and as a result, level readjustment may be required.

correction amount	Rcs or R1 + Rcs
To select Middle	0.3 kΩ = <Rcs or R1 + Rcs = <0.5 kΩ
To select Weak	1.4 kΩ = <Rcs or R1 + Rcs = <2.1 kΩ
To select Strong	3.9 kΩ = <Rcs or R1 + Rcs = <5.2 kΩ

(Rs is ignored because its resistance value is small.)

(3) Fine-adjusting the overload detection level

Although the overload detection level is basically determined by resistor Rs, to fine-adjust the overload detection level, add resistor R2 as shown in Fig. 29, and input the voltage obtained by dividing by resistors Rcs and R2 to the CS pin. Note that the correction amount of dependency of overload detection level on the input voltage is adjusted using a resultant value of Rcs and R2.

correction amount	Rcs × R2/(Rcs + R2)
To select Middle	0.3 kΩ = <Rcs × R2/(Rcs + R2) = <0.5 kΩ
To select Weak	1.4 kΩ = <Rcs × R2/(Rcs + R2) = <2.1 kΩ
To select Strong	3.9 kΩ = <Rcs × R2/(Rcs + R2) = <5.2 kΩ

(Rs is ignored because its resistance value is small.)

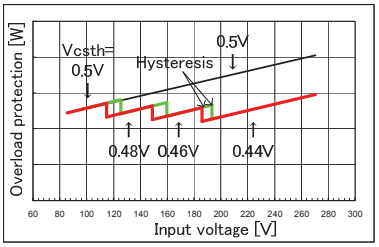


Fig.25 Overload correction: Weak

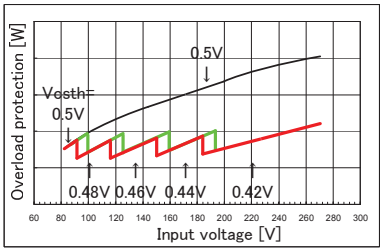


Fig.26 Overload correction: Middle

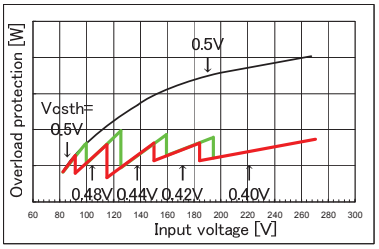


Fig.27Overload correction: Strong

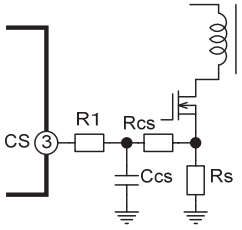


Fig.28 Adjustment of the correction amount of overload on input voltage (2)

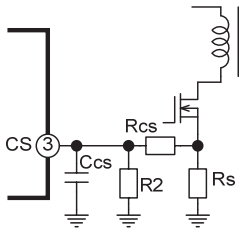


Fig.29 Fine adjustment of overload detection level

(4) Fine-adjusting the burst operation start point under light load

If burst operation is started under heavy load, audible noise may be generated from the transformer. This IC is equipped with a function of adjusting the burst operation start point by changing the pulse stop FB voltage by the resistor connected between the LAT pin and the GND, but it is necessary to design the pulse stop FB voltage at approximately 0.4 V or higher because of the saturation voltage of a optocoupler to be connected to the FB pin. Consequently, to decrease the burst point, add resistor R3 between the CS pin and the OUT pin (Fig. 30). If R3 is connected, positive bias voltage is applied to the CS pin voltage while the MOSFET is ON, and thus FB pin voltage remains relatively high. If the FB pin voltage decreases to the same as or lower than the pulse stop FB voltage, burst operation begins. Consequently, if the FB pin voltage remains relatively high, burst operation hardly occurs under light load, and the burst point can thus be decreased further. When adding a resistor between the CS pin and the OUT pin, sufficient effect may not be achieved if Rcs is small. To prevent this, increase Rcs and decrease Ccs while fixing the time constant of the filter. (When R3 is to be added: Rcs = 470Ω or higher is recommended.)

Note, however, that the standby power may increase and the overload detection level may change if R3 is added. With this IC, since the dependency of the overload detection level on the input voltage is corrected, this correction amount deviates. Be sure to check thoroughly.

(4) Pin No.4 (GND pin)

Function

Pin No. 4 serves as the basis of the voltage of each part of the IC.

(5) Pin No. 5 (OUT pin)

Function

Drives the MOSFET

How to use

• Connection method

Connect pin No. 5 to the MOSFET gate (Figs. 31, 32, and 33).

• Operation

While the MOSFET remains ON, it is in high state, and VCC voltage is output.

While the MOSFET remains OFF, it is in low state, and 0 voltage is output.

Advice for designing

Connect the gate resistor to limit the current fed to the OUT pin or prevent vibration of gate pin voltage.

Adjust the gate resistor not to exceed the IC output current rating of 0.5 A (source) and 0.5 A (sink).

Note, however, that the peak current of up to ±1A can be fed during a period of 100 ns or shorter.

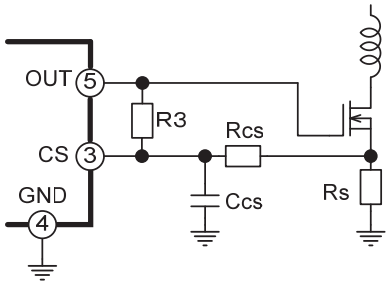


Fig.30 Burst operation point adjustment

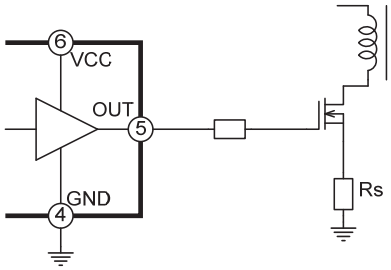


Fig.31 OUT pin circuit (1)

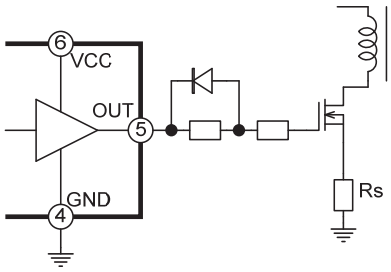


Fig.32 OUT pin circuit (2)

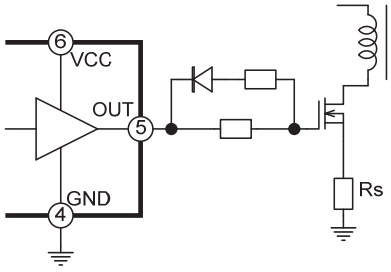


Fig.33 OUT pin circuit (3)

(6) Pin No.6 (VCC pin)

Function

(i) Supplying the power of IC

(ii) Preventing malfunction by detecting low voltage

(iii) Latch stopping at secondary-side over voltage

How to use

(i) Supplying power of IC

- Connection method

Generally, the auxiliary winding voltage provided in the transformer is rectified/smoothed and connected. (Fig. 34). Or DC power from outside is connected (Limited to the products of series without brown-out function).

- Operation

Set the voltage supplied from the auxiliary winding during normal operation to fall within a range from 10 to 24 V (recommended operation condition). Since the startup circuit is actuated if the VCC pin voltage decreases to 8 V or lower, 10 V or higher is recommended not to actuate the startup circuit.

This IC integrates the DSS function. If there is no supply of voltage from the auxiliary winding, the startup circuit is controlled to be turned ON/OFF to maintain the VCC pin voltage within the range from 8 V and 8.5 V.

Consequently, it is also possible to operate the IC by the current supplied from the startup circuit without using the auxiliary winding, which is not recommended basically because the standby power increases. If the IC is to be operated only by the startup circuit, it is necessary to decrease the power consumed by the IC so that it falls within the maximum rating by adjusting the startup resistance of the VH pin. However, if the resistance becomes too large, the current to be supplied to the VCC becomes insufficient, thereby inhibiting operation. Pay special attention to the adjustment. Note that IC operation using the current supplied from the startup circuit only may become infeasible depending on the circuit configuration or circuit component values, etc.

(ii) Preventing malfunction by detecting low voltage

- Connection method

Same as (1)

- Operation

To prevent circuit malfunction when supply voltage decreases, a circuit to prevent malfunction at low voltage is incorporated. When the VCC supply voltage decreases, the IC stops its operation at VCC=6.5V.

When the IC stops operating to prevent malfunction by the low voltage protection function, the OUT pin is forcefully put in Low state.

The latch mode of the protection circuit will also be reset.

(iii) Overvoltage protection on the secondary side

- Connection method

The same as the connection method in (i)

- Operation

If the VCC pin voltage exceeds 25.5 V and that state continues for 72 μs or longer, output switching is stopped, and latch stop is implemented.

Once latch stop is implemented, the VCC pin voltage is maintained within the range from 8.0 V to 8.5 V, and the state of latch stop is continued.

Resetting is implemented by decreasing the VCC voltage to the OFF threshold voltage of 6.5 V at UVLO or lower.

With FA8A68N, the VCC pin voltage is not maintained by the startup circuit after the switching is stopped. Automatic recovery is implemented by restarting the IC when the voltage is decreased to the OFF threshold voltage.

Advice for designing

(1) Connection of the bypass capacitor

Since large current is fed to the VCC pin when the MOSFET is driven, relatively large noise tends to be generated. In addition, noise is also generated from the current supplied by the auxiliary winding. If this noise is large, malfunction of the IC may result. To minimize the noise that is generated at the VCC pin, add a bypass capacitor C2 (0.1 μF or higher) adjacent to the VCC pin of the IC, between VCC and the GND, as shown in Fig. 31, in addition to the electrolytic capacitor.

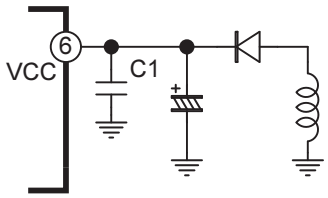


Fig.34 VCC circuit

(2) Adjustment of power supply voltage input range

The recommended supplied voltage range is 10 V to 24 V. When the load is light, the VCC pin voltage decreases, whereas when the load is heavy, the voltage increases, thus deviating from the power supply voltage range. In such cases, change the resistor between the VCC pin and the diode to adjust the voltage. Also, by adding beads core at the foot of the resistor, voltage fluctuation may be suppressed.

If the above methods do not work, it is recommended to change the secondary winding and the auxiliary winding of the transformer to bifilar winding.

(3) When directly supplying power to the VCC pin
(Limited to the products of series without input filter X-capacitor discharge function and brown-in/out function)
When supplying power directly to the VCC pin without using the VH pin, open the VH pin or short-circuit the VH pin and the VCC pin.
If the equipment is used with the VH pin connected to the GND, leak current may be generated.

(7) Pin No.7 (N.C.)

Since this pin is placed adjacent to the high-voltage pin, it is not connected to inside the IC.

(8) Pin No. 8 (VH pin)

Function

(ⅰ) Supplies startup current.
(ⅱ) Discharges the charge of input filter X-capacitor when AC input is interrupted.
(ⅲ) Provides brown-in/brown-out function.

How to use

(ⅰ) Supplying startup current

- Connection method
  Connect to a high-voltage line via a startup resistor and a diode (Figs. 35, 36, and 37).
- Operation
  This IC integrates a startup circuit having a withstand voltage of 500 V, achieving low power consumption.
  In Fig. 35, the half-wave rectification waveform of the AC input voltage is input to the VH pin.
  The startup time of this method is the longest of the three connection methods. If the AC input voltage is interrupted after the IC implements latch stop for overload protection or overvoltage protection, supply of current from the VH pin is stopped, and thus the state of latch stop can be reset in a period as short as several seconds.
  Note that although this IC integrates the input filter X-capacitor discharge function applicable when the AC power is interrupted, discharge is guaranteed only when the full-wave rectification waveform is connected. If connection is made to a half-wave rectification waveform, discharge may not be conducted depending on the voltage polarity of the input filter X-capacitor at the time of AC power interruption, and therefore separate discharge measures must be taken.

  In Fig. 36, the full-wave rectification waveform of the AC input voltage is input to the VH pin. The startup time of this method is approximately half of that of the half-wave rectification shown in Fig. 32. The input filter X-capacitor discharge function is actuated while the AC input voltage is interrupted, and latch stop state can also be reset in a short time.

  In Fig. 37, the VH pin is connected to a position after the AC input voltage has been rectified and smoothed. The startup time of this method is the shortest of the three connection methods. With this method, however, even if AC input voltage is interrupted after latch stop of the IC is implemented, it takes time to reset the state of latch stop because the voltage charged in the input capacitor is added to the VH pin. Note that resetting generally requires several minutes after AC power input is interrupted although the duration depends on the operation conditions.
  If the VH pin is connected to a position after the AC input voltage has been rectified and smoothed (DC waveform input), the discharge function of the input filter X-capacitor may malfunction, thus resulting in heating or break. Do not adopt this connection method for products of series equipped with the X-capacitor discharge function.

If power is turned on, the capacitor connected to the VCC pin is charged due to the current supplied from the startup circuit to the VCC pin via the VH pin, and the VCC voltage increases. When the ON threshold voltage of 12.5 V of the low-voltage malfunction prevention circuit (UVLO) is exceeded, the internal supply is started to operate the IC. If VCC is supplied from the auxiliary winding, the startup circuit is stopped.
Meanwhile, if power is not supplied from the auxiliary winding, the current supplied from the startup circuit is used for the normal operation of the IC.
Consequently, it is also possible to operate the IC by the current supplied from the startup circuit without using the auxiliary winding, which is not recommended basically because the standby power increases. If the IC is to be operated only by the startup circuit, it is necessary to decrease the power consumed by the IC so that it falls within the maximum rating by adjusting the startup resistance of the VH pin. However, if the resistance becomes too large, the current to be supplied to the VCC becomes insufficient, thereby inhibiting operation. Pay special attention to the adjustment. Note that IC operation using the current supplied from the startup circuit only may become infeasible depending on the circuit configuration or circuit component values, etc.

(ii) Input filter X-capacitor discharge function

(Provided or not provided depending on series.)

- Connection method

  Operates by the connection method shown in Fig. 33 only.

- Operation

  The AC input voltage is monitored by the VH pin, and when the AC input is cut off, the discharging function of the X capacitor will operate after 56ms of delay time.

  The function discharges the X-capacitor repeating ON and OFF state; ON state is for 1.5ms with average current of 2mA and OFF state is for 0.5ms.

(iii) Brown-in, brown-out function

(Provided or not provided depending on series.)

- Connection method

  Same as the connection method of (i)

- Operation

  AC line voltage is monitored by VH pin directly. When VH pin voltage rises over 105Vdc of brown in threshold, IC will start operating. When VH pin voltage drops below 98Vdc of the brown out threshold for over 72ms of the delay time, IC will stop switching. During the switching stop period due to the brown-out function, the starting circuit is ON/OFF controller and the VCC voltage is held in the range of 12V/11.5V.

Advice for designing

(1) Starting resistor

To prevent damage to the IC due to surge voltage of the AC line, it is recommended to connect a starting resistor of 5.6 kΩ to 50 kΩ to the VH pin in series. Startup is allowed up to 50 kΩ, but give sufficient consideration because the startup time varies depending on the capacitor of the VCC pin.

This starting resistor cannot be adjusted to control the startup time and startup voltage. If a resistor of 50 kΩ or higher is connected, startup may be inhibited.

(2) Capacitance of X-capacitor when the input filter X-capacitor discharge function is used

To satisfy the requirements of UL60950 regarding electric shock, this IC integrates a discharge function for attenuating the voltage value at the power input part to 37% or lower of the peak value within 1 s after the AC input voltage is interrupted. The recommended capacitance of connectable X-capacitor is 2 μF or lower.

(3) When supplying power directly to the VCC pin

(Limited to the products of series without input filter X-capacitor discharge function and brown-in/out function)

When supplying power directly to the VCC pin without using the VH pin, open the VH pin or short-circuit the VH pin and the VCC pin.

If the equipment is used with the VH pin connected to the GND, leak current may be generated.

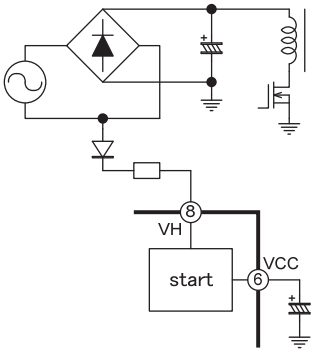


Fig.35 VH pin circuit (1)

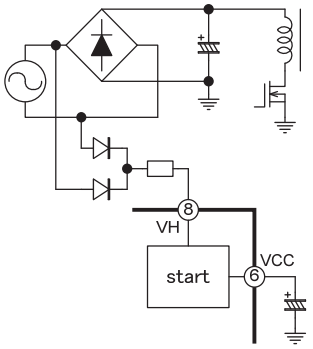


Fig.36 VH pin circuit (2)

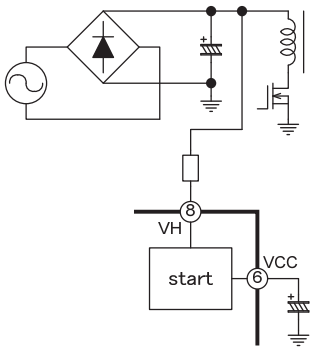


Fig.37 VH pin circuit (3)

(It restricts to the series article containing X-capacitor discharge function.)

(9) Other advice on designing

(1) Capacitance of X-capacitor when the Input filter X-capacitor discharge function is used

To satisfy the requirements of UL60950 regarding electric shock, this IC integrates a discharge function of attenuating the voltage value at the power input part to 37% or lower of the peak value within 1 s after the ACV input voltage is interrupted. The recommended capacitance of connectable X-capacitor is 2 μF or lower.

(2) Preventing malfunction due to negative voltage of the pin

If large negative voltage is applied to each pin of the IC, the parasitic devices inside the IC may be operated, thus causing malfunction. Confirm that the voltage of -0.3 V or less is not applied to each pin.

The vibration of the voltage generated after the MOSFET is turned-off may be applied to the OUT pin through the parasitic capacitance, resulting in a case in which negative voltage is applied to the OUT pin.

In addition, negative voltage may be applied to the IS pin due to the vibration of surge current generated at the turn-on of the MOSFET.

In such cases, connect a Schottky diode between each pin and the GND. The forward voltage of the Schottky diode can suppress the negative voltage at each pin. In this case, use a Schottky diode whose forward voltage is low. Fig. 35 and Fig.36 are typical connection diagram where a Schottky diode is connected to the OUT pin.

(3) Loss calculation

To use the IC within its rating, it is necessary to confirm the loss of the IC. However, since it is difficult to measure the loss directly, the method of confirming the loss by calculation is shown below. If the voltage applied to the VH pin is defined as VVH, the current fed to the VH pin during operation as IVHrun, power supply voltage as VCC, supply current as Iccop1, gate input charge of the MOSFET to be used as Qg, and switching frequency as fsw, the total loss Pd of the IC can be calculated using the following formula.

$$P_d \approx V_{CC} \times (ICC_{op1} + Q_g \times f_{sw}) + V_{vh} \times IVH_{run}$$

A rough value can be found using the above formula, but note that Pd is slightly larger than the actual loss value. Also note that each specific characteristic value has temperature characteristics or variation.

Example:

If the VH pin is connected to a half-wave rectification waveform with AC240V input, the average voltage to be applied to the VH pin is approximately 215 V. In this state, assume that VCC = 20 V, Qg = 80 nC, and fsw = 65 kHz (when Tj = 25°C). Since IVHrun = 5 μA and Iccop1 = 0.6mA from the specifications, the standard IC loss can be calculated as follows:

Pd ≈ 20V x (0.6mA + 80nC x 65kHz) + 215V x 5μA
≈ 117mW

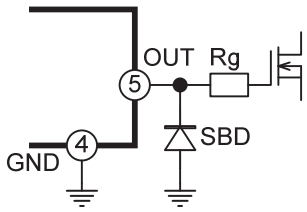


Fig.38 Negative voltage prevention circuit for OUT pin

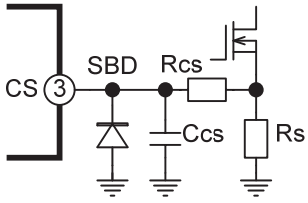


Fig.39 Negative voltage prevention circuit for CS pin

10. Precautions for pattern design

In the switching power supply, large pulse current flows in the GND wiring and surge voltage (noise) is generated. The noise may causes malfunction of the IC. (unstable voltage, unstable waveform, abnormal latch stop, etc.) Malfunction may also be caused by injected surge voltage/current such as lighting surge test, AC line surge test and electrostatic discharge test. Please design the PCB layout and trace with consideration of the followings to prevent the malfunction.

Current path in switching power

(1) Main circuit current which flows from input smoothing capacitor to transformer primary winding, MOSFET and current sense resistor.
(2) Current which flows from auxiliary winding to VCC capacitor.
(3) Driving current which flows from IC to the MOSFET
(4) Control circuit current around the IC such as feedback signal
(5) Filter current which flows between primary and secondary via the Y-Capacitor.

Points in pattern designing

・GND wiring of the above 1)-5) should be separated so as not to affect each other.
・To minimize the surge voltage of MOSFET, loop length of the main circuit should be designed as short as possible.
・The electrolytic capacitor between VCC pin and GND should be connected close to the IC.
・The bypass capacitor of the VCC pin should be connected as close as possible to the IC.
・Capacitors for filter such as FB pin and CS pin should be connected close to each pin using the shortest wiring.
・The loop area of CS pin and GND wiring should be as small as possible.
・The current sense resistor and electrolytic capacitor should be connected as short as possible.
・The IC and control circuit should not be arranged inside the main circuit loop.
・Control circuit and signal wiring should not be placed under the transformer so as not to affect the leakage flux.

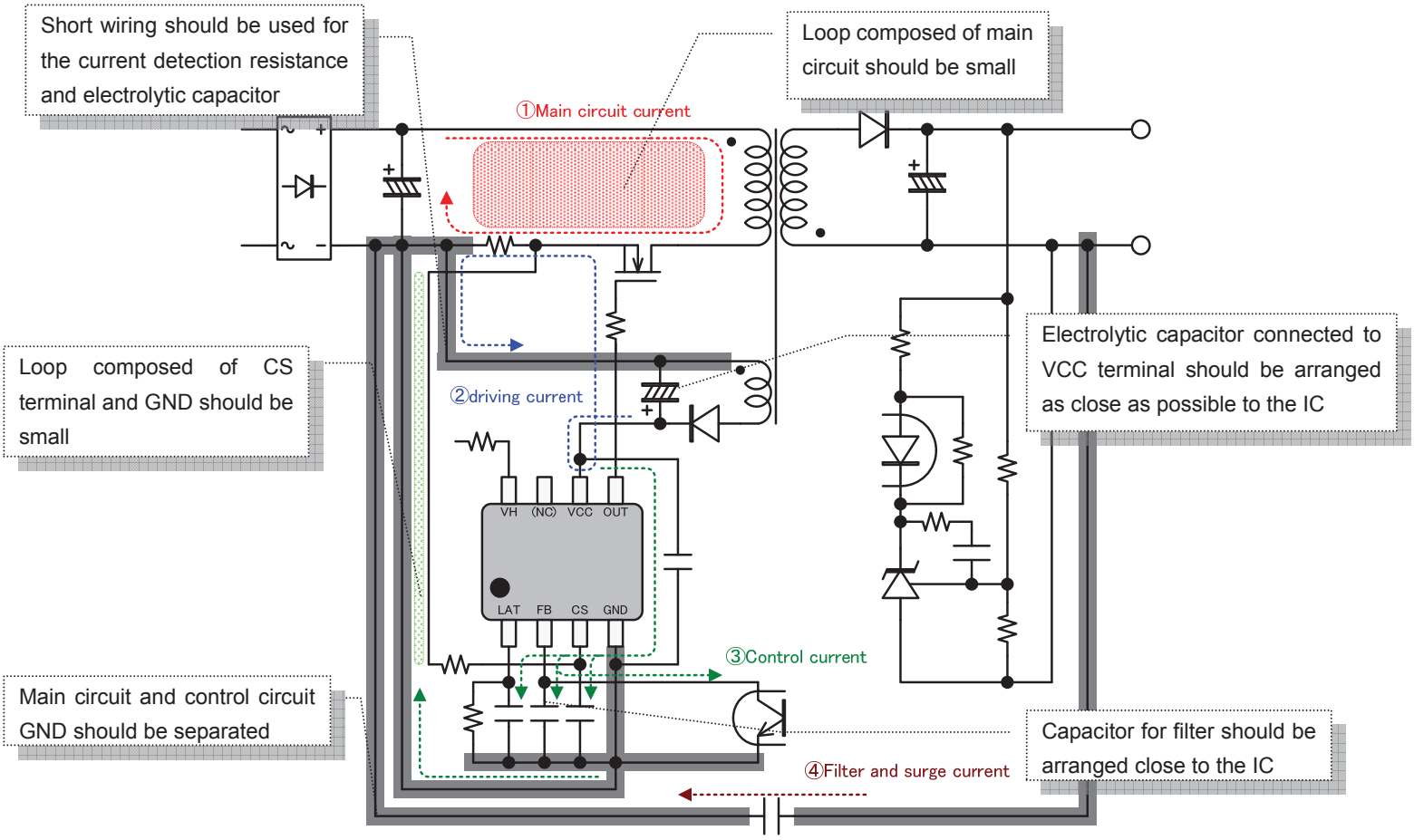
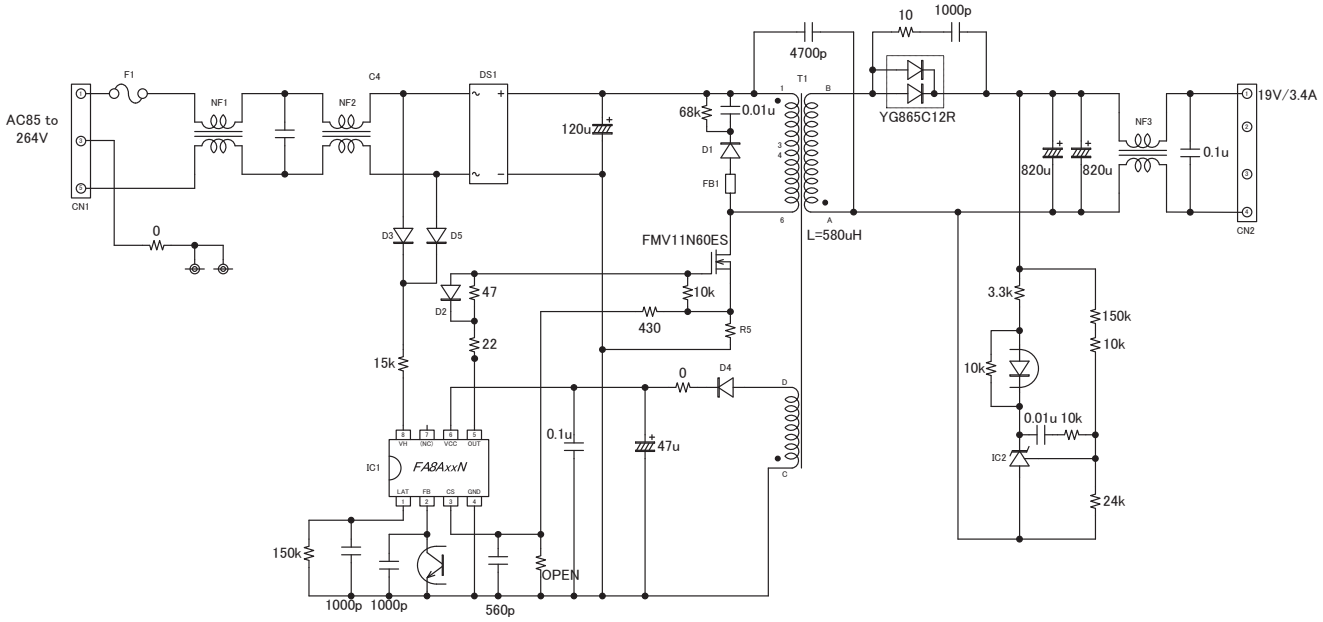


Fig.40 Pattern design image

11. Application circuit example

The typical application circuit shown here provides specifications common to each IC series.



Note: This application circuit is a reference material for describing typical usage of this IC, and does not guarantee the operation or characteristics of the IC.