ESS Technology, Inc.

ES8381
Phoenix DVD Processor
Data Sheet

DESCRIPTION

The ES8381 Phoenix processor is a single-chip DVD processor supporting DVD video, MPEG-4 ASP and DivX® Home Theater playback.

The Phoenix DVD processor is ideal for stand-alone DVD players, DVD receivers, DVD/VCR combos and DVD A/V mini-component systems. It incorporates a high-quality deinterlacer and a TV encoder that supports HD (720p/1080i) and Macrovision™ protected progressive (480p/576p) and interlaced video output. The HD output is ideal for the display of JPEG pictures, and when used with the built-in video scaler, allows up-conversion of unprotected video to HD resolution.

The Phoenix processor is built on the ESS proprietary dual CPU Programmable Multimedia Processor (PMP) core consisting of 32-bit RISC and 64-bit DSP processors that deliver the best DVD feature set. It integrates a servo controller, RF amplifier, read channel, ECC, servo DSP, and MCU. The Phoenix processor employs a unified memory architecture to ensure the lowest possible system memory cost. A USB full-speed host controller is built-in for connection to Flash memory cards.

The Phoenix processor servo controller supports all popular optical pick-up units (OPU). Its high performance error handling allows for playback of scratched and fingerprinted media.

The Phoenix processor has unmatched audio features including an integrated high quality 8-channel audio digital to analog converter (DAC) and a stereo analog to digital converter (ADC). Additionally, it supports the DVD-Audio, CD-DA, HDCD, MP3, WMA, AAC, and Dolby ProLogic™ II digital audio formats and Karaoke.

The ES8381 Phoenix DVD processor provides a 12-bit/24-bit YCbCr interface for connection to an HDMI transmitter. When HDMI in 24-bit mode is not required, a 16-bit host interface is available for connection to CF and SM memory cards and xD picture cards, as well as to an IDE hard drive. Similarly, a serial interface is built-in to connect the Phoenix processor to SD, MMC, MS and MS Pro devices.

The ES8381 Phoenix DVD processor is available in a 256-pin Plastic Quad Flat Pack (PQFP) device package.

UNDER NDA FOR EASTECH

FEATURES

- Built-in RF amplifier and servo controller.
- High-performance focusing, sledding, tracking and CLV/CAV spindle servo control.
- DVD-Video, DVD-R/RW, DVD+R/RW, SVCD, VCD, CD-ROM, CD-R/RW, CD-DA support.
- DivX Home Theater quality video at full screen (D1).
- MPEG-4 Advanced Simple Profile video including GMC and QPEL support.
- Pixel-adaptive de-interlacer.
- Scaler for video up-conversion to 1080i/720p.
- NTSC/PAL encoder with six video DACs for concurrent composite, S-Video and YUV video outputs.
- Macrovision protected, NTSC/PAL interlaced, and progressive scan (480p/576p) video output.
- HD component output for JPEG picture and video.
- CCIR656/601 YUV 4:2:2 input/output.
- 12-bit/24-bit YCbCr output for HDMI transmitter.
- Stereo audio ADC.
- SPDIF digital audio input and output.
- 8-channel audio DAC (ES8381CC/CE only).
- 8-channel PWM controller for Class D power bridges (ES8381CD/CF only).
- USB full-speed host controller.
- OSD controller supports 256 colors in 8 degrees of transparency.
- Sub-picture Unit (SPU) decoder supports karaoke lyric, subtitles and EIA-608 compliant Line 21 captioning.
- JPEG digital photo support (Kodak Picture CD™ and Fujifilm FujiColor CD™).
- DVD-Audio multi-channel playback including MLP and 24-bit LPCM decode, CPPM decryption and watermark detection (ES8381CE/CF only).
- Dolby Digital, Dolby ProLogic, and Dolby ProLogic II.
- DTS Surround.
- SRS TruSurround®.
- MPEG Multichannel, AAC, MP3 and WMA.
- Professional karaoke with full scoring scheme.
- Serial UART port.
- 16-bit DRAM interface for up to 128-Mb capacity.
- 8-bit EPROM/Flash interface for up to 4 banks x 4 MB.
- Lead-free leads using 98%-Sn/2%-Cu or 98%-Sn/2%-Bi (see soldering requirement on page 164).

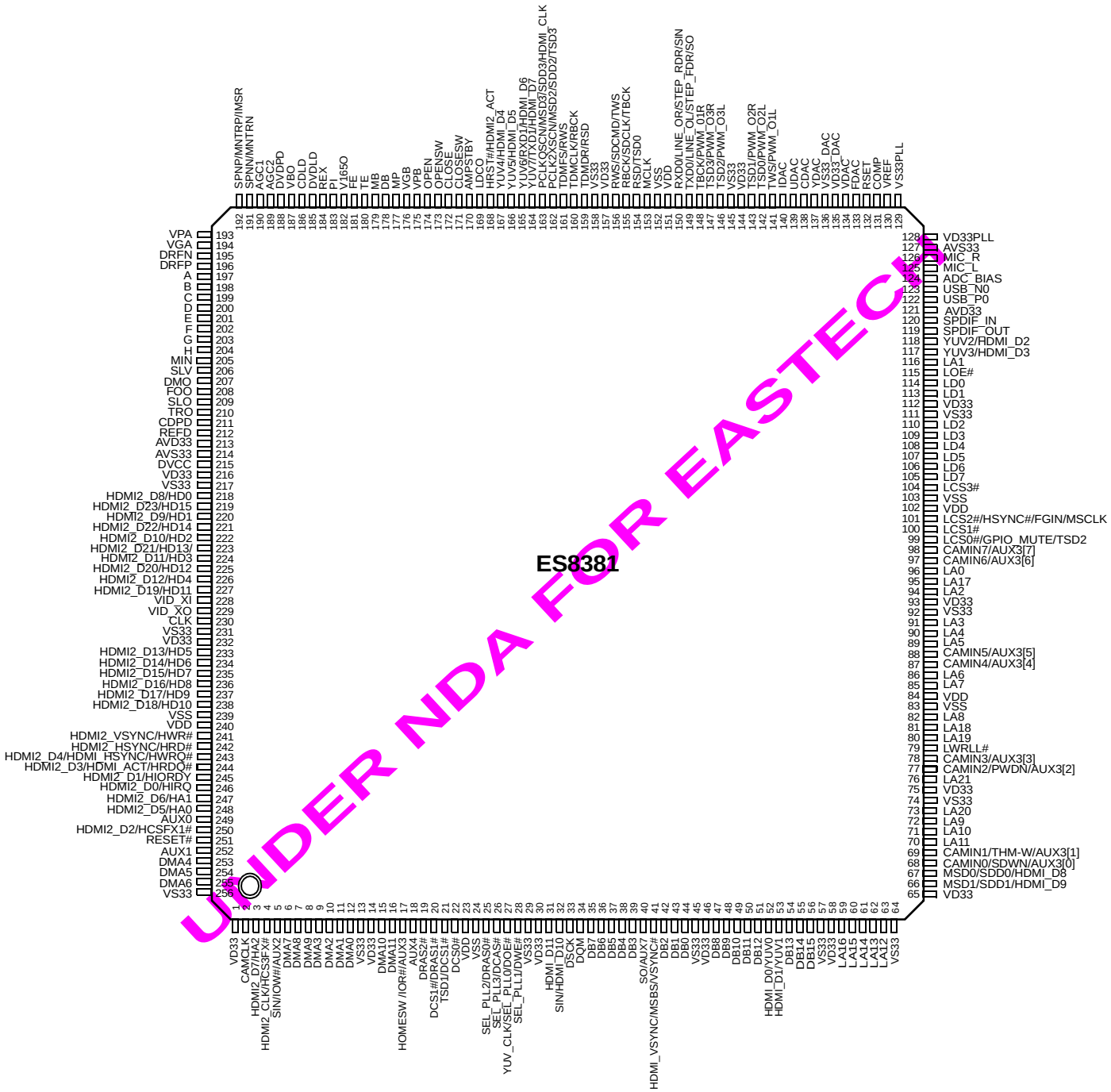
TABLES

Table 1 ES8381 Pin Description 8
Table 2 ES8381 Device Interfaces 18
Table 3 ES8380 MCU Memory Space Range . . . 27
Table 4 MCU Write Side Registers 28
Table 5 MCU Read Side Registers 29
Table 6 ES8381 Spindle Motor Modes 29
Table 7 Focus Control System Parameter Descriptions 30
Table 8 Focus Servo Equalizer Changed Coefficients 31
Table 9 Alternate Gain Types 31
Table 10 Backup Gain Locations and Events 31
Table 11 Focus Search Parameters and Addresses 32
Table 12 Tracking Servo Equalizer Changed Coefficients 33
Table 13 Long Seek Parameters 36
Table 14 Channel Addressing For Averaging 37
Table 15 Channel Addressing For Offset 37
Table 16 Reflection Detection Judgment Methods 39
Table 17 Focus And Tracking Health Monitor Bits 41
Table 18 ESS RISC Interrupts 44
Table 19 Line 21 Standard Character Set 47
Table 20 Line 21 Special Character Set 48
Table 21 Video Error Concealment Modes 49
Table 22 Packet Commands for ATAPI Devices . . . 50
Table 23 CF-ATA Command Set 51
Table 24 Typical DRAM Configurations 52
Table 25 DRAM Configurations and Signal Pins 53
Table 26 Safe Caption Area Dimensions 54
Table 27 ESS RISC Clock Relationship to Pixel Clocks 55
Table 28 ES8381 Servo Controller Command Set 56
Table 29 ES8381 Register Address Map 57
Table 30 RAM Core 0 Registers 79
Table 31 RAM Core 1 Registers 91
Table 32 Hex Values for Wait States 123
Table 33 Compact Flash True IDE Mode I/O Read Timing 141
Table 34 Compact Flash True IDE Mode I/O Write Timing 142
Table 37 SDRAM Interface Timing 150
Table 38 SDRAM Read and Write Timing 150
Table 42 USB Full-Speed Mode Timing 154
Table 43 USB Low-Speed Mode Timing 154
Table 44 DC Electrical Characteristics 160
Table 45 Video DAC DC Electrical Characteristics 161
Table 46 Video DAC AC Electrical Characteristics 161
Table 47 VFD Interface Characteristics 161
Table 48 Audio Performance 162

UNDER NDA FOR EASTECH

ES8381 PINOUT DIAGRAM

The device pinout for the ES8381 is shown in Figure 1.



UNDER NDA FOR EASTECH

Figure 1 ES8381 Device Pinout

ES8381 PIN DESCRIPTION

Table 1 lists the pin descriptions for the ES8381.

NOTE: HDMI_D11:0, HDMI_CLK, HDMI_ACT, HDMI_VSYNC and HDMI_HSYNC are for 12-bit HDMI mode.

NOTE: HDMI2_D23:0, HDMI2_CLK, HDMI2_ACT, HDMI2_VSYNC, and HDMI2_HSYNC are for 24-bit HDMI mode, and ***cannot*** co-exist with the IDE host port.

Table 1 ES8381 Pin Description

Names	Pin Number(s)	I/O	Definitions
VD33	1, 14, 30, 46, 58, 65, 75, 93, 112, 144, 157, 216, 232	P	I/O power supply.
CAMCLK	2	I	Camera clock.
HDMI2_D7	3	O	HDMI data 7 (24-bit HDMI mode).
HA2		I/O	Host address 2.
HCS3FX#	4	I/O	Host chip select 3 (secondary).
HDMI2_CLK		O	HDMI pixel clock (24-bit HDMI mode).
AUX2	5	I/O	Auxiliary port 2.
IOW#		O	I/O write strobe (active-low).
SIN		I	UART serial data in.
DMA11-0	16, 15, 8, 7, 6, 255, 254, 253, 9, 10,11, 12	O	DRAM address bus.
VS33	13, 29, 45, 57, 64, 74, 92, 111, 145, 158, 217, 231, 256	G	Ground.
HOMESW	17	I/O	Sled home switch position detector.
AUX3		I/O	Auxiliary port 3.
IOR#		O	I/O read strobe (active-low).
AUX4	18	I/O	Auxiliary port 4.
DRAS2#	19	O	DRAM row address strobe 2 (active-low).
DCS1#	20	O	DRAM chip select 1 (active-low).
DRAS1#		O	DRAM row address strobe 1 (active-low).
DCS1#	21	O	DRAM chip select 1 (active-low).
TSD1		O	Audio transmit serial data port 1.
DCS0#	22	O	DRAM chip select 0 (active-low).
VDD	23, 84, 102, 151, 240	P	Core power supply.
VSS	24, 83, 103, 152, 239	G	Ground.

UNDER NDA FOR EASTECH

Table 1 ES8381 Pin Description (Continued)

<table>
<tr><th>Names</th><th>Pin Number(s)</th><th>I/O</th><th>Definitions</th></tr>
<tr><td>DRAS0#</td><td rowspan="2">25</td><td>I/O</td><td>DRAM row address strobes (active-low).</td></tr>
<tr><td>SEL_PLL2</td><td>I/O</td><td>Strap pin. System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available PLL bit settings. Strapped to VD33PLL or VS33PLL via 4.7-kΩ resistor; read-only during reset.
<table>
<tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Type (MHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Bypass</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>121.5MHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>128.25MHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>135MHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>141.75MHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>155.25MHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>162MHz</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>148.5MHz</td></tr>
</table></td></tr>
<tr><td>DCAS#</td><td rowspan="2">26</td><td>O</td><td>DRAM column address strobe (active-low).</td></tr>
<tr><td>SEL_PLL3</td><td>I</td><td>Clock source select. Strapped to VD33PLL or VS33PLL via 4.7-kΩ resistor; read only during reset.
<table>
<tr><th>SEL_PLL3</th><th>Clock Source</th></tr>
<tr><td>1</td><td>Crystal oscillator</td></tr>
<tr><td>0</td><td>CLK input</td></tr>
</table></td></tr>
<tr><td>DOE#</td><td rowspan="3">27</td><td>O</td><td>DRAM output enable (active-low).</td></tr>
<tr><td>SEL_PLL0</td><td>I</td><td>Strap pin. Refer to the description and matrix for SEL_PLL2, pin 25.</td></tr>
<tr><td>YUV_CLK</td><td>I/O</td><td>YUV clock.</td></tr>
<tr><td>DWE#</td><td rowspan="2">28</td><td>O</td><td>DRAM write enable (active-low).</td></tr>
<tr><td>SEL_PLL1</td><td></td><td>Strap pin. Refer to the description and matrix for SEL_PLL2, pin 25.</td></tr>
<tr><td>HDMI_D11</td><td>31</td><td>O</td><td>HDMI data 11 (12-bit HDMI mode).</td></tr>
<tr><td>HDMI_D10</td><td rowspan="2">32</td><td>O</td><td>HDMI data 10 (12-bit HDMI mode).</td></tr>
<tr><td>SIN</td><td>I</td><td>UART serial data in.</td></tr>
<tr><td>DSCK</td><td>33</td><td>O</td><td>Output clock to DRAM.</td></tr>
<tr><td>DQM</td><td>34</td><td>O</td><td>Data input/output mask.</td></tr>
<tr><td>DB15-0</td><td>56, 55, 54, 51, 50, 49, 48, 47, 35, 36, 37, 38, 39, 42, 43, 44</td><td>I/O</td><td>DRAM data bus.</td></tr>
<tr><td>AUX7</td><td rowspan="2">40</td><td>I/O</td><td>Auxiliary port 7.</td></tr>
<tr><td>SO</td><td>O</td><td>UART serial data out.</td></tr>
<tr><td>VSYNC#</td><td rowspan="3">41</td><td>I/O</td><td>Vertical sync (active-low).</td></tr>
<tr><td>MSBS</td><td>I/O</td><td>Memory Stick bus strobe.</td></tr>
<tr><td>HDMI_VSYNC</td><td>O</td><td>HDMI vertical sync (12-bit HDMI mode).</td></tr>
</table>

UNDER NDA FOR EASTECH

Table 1 ES8381 Pin Description (Continued)

Names	Pin Number(s)	I/O	Definitions
YUV0	52	O	YUV pixel 0 output data.
HDMI_D0		O	HDMI data 0 (12-bit HDMI mode).
YUV1	53	O	YUV pixel 1 output data.
HDMI_D1		O	HDMI data 1 (12-bit HDMI mode).
LA21-0	76, 73, 80, 81, 95, 59, 60, 61, 62, 63, 70, 71, 72, 82, 85, 86, 89, 90, 91, 94, 116, 96	O	SRAM address bus.
MSD1	66	I/O	Memory Stick data I/O 1.
SDD1		I/O	SD data I/O 1.
HDMI_D9		O	HDMI data 9 (12-bit HDMI mode).
MSD0	67	I/O	Memory Stick data I/O 0.
SDD0		I/O	SD data I/O 0.
HDMI_D8		O	HDMI data 8 (12-bit HDMI mode).
AUX3[0]	68	I/O	Aux3 data I/O 0.
SDWN		I	Shutdown status from Class D driver.
CAMIN0		I	Camera input 0.
AUX3[1]	69	I/O	Aux3 data I/O 1.
THM-W		I	Thermal warning status from Class D driver.
CAMIN1		I	Camera input 1.
AUX3[2]	77	I/O	Aux3 data I/O 2.
PDWN		O	Power down Class D driver.
CAMIN2		I	Camera input 2.
AUX3[3]	78	I/O	Aux3 data I/O 3.
CAMIN3		I	Camera input 3.
LWRLL#	79	O	SRAM bus write enable (active-low).
AUX3[4]	87	I/O	Aux3 data I/O 4.
CAMIN4		I	Camera input 4.
AUX3[5]	88	I/O	Aux3 data I/O 5.
CAMIN5		I	Camera input 5.
AUX3[6]	97	I/O	Aux3 data I/O 6.
CAMIN6		I	Camera input 6.
AUX3[7]	98	I/O	Aux3 data I/O 7.
CAMIN7		I	Camera input 7.

UNDER NDA FOR EASTECH

Table 1 ES8381 Pin Description (Continued)

Names	Pin Number(s)	I/O	Definitions
LCS0#	99	O	SRAM bus chip select (active-low).
GPIO_MUTE		O	Mute.
TSD2		O	Audio transmit serial data port 2.
LCS1#	100	O	SRAM bus chip select (active-low).
LCS2#	101	O	SRAM bus chip select (active-low).
HSYNC#		I/O	Horizontal sync (active-low).
FGIN		I	Spindle hall sensor input.
MSCLK		I/O	Memory Stick clock.
LCS3#	104	O	SRAM bus chip select (active-low).
LD7-0	105:110, 113, 114	I/O	SRAM data bus.
LOE#	115	O	SRAM bus data output enable (active-low).
YUV3	117	O	YUV pixel 3 output data.
HDMI_D3		O	HDMI data 3 (12-bit HDMI mode).
YUV2	118	O	YUV pixel 2 output data.
HDMI_D2		O	HDMI data 2 (12-bit HDMI mode).
SPDIF_OUT	119	O	S/PDIF output.
SPDIF_IN	120	I	S/PDIF input.
AVD33	121, 213	P	Analog power for audio ADC, USB, and flash.
USB_P0	122	I/O	Positive analog USB signal.
USB_N0	123	I/O	Negative analog USB signal.
ADC_BIAS	124	O	Audio ADC bias voltage out.
MIC_L	125	I	Audio ADC MIC L.
MIC_R	126	I	Audio ADC MIC R.
AVS33	127, 214	G	Analog ground for audio ADC, USB and flash.
VD33PLL	128	P	Power for PLL blocks.
VS33PLL	129	G	Ground for PLL blocks.
VREF	130	I	Internal voltage reference to video DAC.
COMP	131	I	Compensation input.
RSET	132	I	DAC current adjustment resistor input.

UNDER NDA FOR EASTECH

Table 1 ES8381 Pin Description (Continued)

<table>
<tr><th>Names</th><th>Pin Number(s)</th><th>I/O</th><th>Definitions</th></tr>
<tr><td>FDAC</td><td>133</td><td>O</td><td>Video DAC Output:
<table>
<tr><th>Value</th><th>F DAC (pin 133)</th><th>V DAC (pin 134)</th><th>Y DAC (pin 137)</th><th>C DAC (pin 138)</th><th>U DAC (pin 139)</th><th>I DAC (pin 140)</th></tr>
<tr><td>0</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>C</td><td>N/A</td><td>N/A</td></tr>
<tr><td>1</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>C</td><td>CVBS2</td><td>N/A</td></tr>
<tr><td>2</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>C</td><td>N/A</td><td>N/A</td></tr>
<tr><td>3</td><td>CVBS/Chroma</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>CVBS2</td><td>N/A</td></tr>
<tr><td>4</td><td>CVBS/Chroma</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>5</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>Pb</td><td>Pr</td><td>Yi</td></tr>
<tr><td>6</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>Pb</td><td>Pr</td><td>N/A</td></tr>
<tr><td>7</td><td>N/A</td><td>SYNC</td><td>G</td><td>B</td><td>R</td><td>N/A</td></tr>
<tr><td>8</td><td>CVBS/Chroma</td><td>Chroma</td><td>Y</td><td>Pb</td><td>Pr</td><td>Yi</td></tr>
<tr><td>9</td><td>CVBS</td><td>CVBS1</td><td>G</td><td>B</td><td>R</td><td>Yi</td></tr>
<tr><td>10</td><td>CVBS</td><td>CVBS1</td><td>G</td><td>R</td><td>B</td><td>Yi</td></tr>
<tr><td>11</td><td>N/A</td><td>SYNC</td><td>G</td><td>R</td><td>B</td><td>N/A</td></tr>
<tr><td>12</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>Pr</td><td>Pb</td><td>N/A</td></tr>
<tr><td>13</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>Pr</td><td>Pb</td><td>Yi</td></tr>
<tr><td>14</td><td>Chroma</td><td>Y</td><td>G</td><td>R</td><td>B</td><td>N/A</td></tr>
</table>
F: CVBS/chroma signal for simultaneous mode.
Y: Luma component for YUV and Y/C processing.
C: Chrominance signal for Y/C processing.
U: Chrominance component signal for YUV mode.
V: Chrominance component signal for YUV mode.
i: Interlaced luma only for simultaneous processing.</td></tr>
<tr><td>VDAC</td><td>134</td><td>O</td><td>Video DAC output. Refer to description and matrix for FDAC pin 133.</td></tr>
<tr><td>VD33_DAC</td><td>135</td><td>P</td><td>Power supply for VDAC.</td></tr>
<tr><td>VS33_DAC</td><td>136</td><td>G</td><td>Ground for VDAC.</td></tr>
<tr><td>YDAC</td><td>137</td><td>O</td><td>Video DAC output. Refer to description and matrix for FDAC pin 133.</td></tr>
<tr><td>CDAC</td><td>138</td><td>O</td><td>Video DAC output. Refer to description and matrix for FDAC pin 133.</td></tr>
<tr><td>UDAC</td><td>139</td><td>O</td><td>Video DAC output. Refer to description and matrix for FDAC pin 133.</td></tr>
<tr><td>IDAC</td><td>140</td><td>O</td><td>Video DAC output. Refer to description and matrix for FDAC pin 133.</td></tr>
<tr><td>TWS</td><td rowspan="2">141</td><td>O</td><td>Audio transmit frame sync output.</td></tr>
<tr><td>PWM_O1L</td><td>I/O</td><td>Audio hyperstream out.</td></tr>
<tr><td>TSD0</td><td rowspan="2">142</td><td>O</td><td>Audio transmit serial data port 0.</td></tr>
<tr><td>PWM_O2L</td><td>I/O</td><td>Audio hyperstream out.</td></tr>
<tr><td>TSD1</td><td rowspan="2">143</td><td>O</td><td>Audio transmit serial data port 1.</td></tr>
<tr><td>PWM_O2R</td><td>I/O</td><td>Audio hyperstream out.</td></tr>
</table>

UNDER NDA FOR EASTECH

Table 1 ES8381 Pin Description (Continued)

Names	Pin Number(s)	I/O	Definitions
TSD2	146	O	Audio transmit serial data port 2.
PWM_O3L		I/O	Audio hyperstream out.
TSD3	147	O	Audio transmit serial data port 3.
PWM_O3R		I/O	Audio hyperstream out.
TBCK	148	I/O	Audio transmit bit clock.
PWM_O1R		I/O	Audio hyperstream out.
TXD0	149	O	Serial port 0 transmit.
LINE_OL		O	Audio line out.
STEP_FDR		O	Step motor control forward drive.
SO		O	UART serial data out.
RXD0	150	I	Serial port 0 receive.
LINE_OR		I/O	Audio base out.
STEP_RDR		I	Step motor control reverse drive.
SIN		I	UART serial data in.
MCLK	153	I/O	Audio master clock for audio DAC.
RSD	154	I	Audio receive serial data.
TSD0		O	Audio transmit serial data port 0.
RBCK	155	I/O	Audio receive bit clock.
TBCK		I/O	Audio transmit bit clock.
SDCLK		I/O	SD clock.
RWS	156	I	Audio receive frame sync.
TWS		O	Audio transmit frame sync output.
SDCMD		I	SD command strobe.
TDMDR	159	I	TDM serial data.
RSD		I	Audio receive serial data.
TDMCLK	160	I	TDM bit clock.
RBCK		I/O	Audio receive bit clock.
TDMFS	161	I	TDM frame sync.
RWS		I	Audio receive frame sync.
PCLK2XSCN	162	I/O	27-MHz screen clock.
MSD2		I/O	Memory Stick data I/O 2.
SDD2		I/O	SD data I/O 2.
TSD3		O	Audio transmit serial data port 3.

UNDER NDA FOR EASTECH

Table 1 ES8381 Pin Description (Continued)

Names	Pin Number(s)	I/O	Definitions
PCLKQSCN	163	O	13.5-MHz screen clock.
HDMI_CLK		I/O	HDMI pixel clock (12-bit HDMI mode).
MSD3		I/O	Memory Stick data I/O 3.
SDD3		I/O	SD data I/O 3.
YUV7	164	O	YUV pixel 7 output data.
TXD1		O	Serial port 1 transmit.
HDMI_D7		O	HDMI data 7 (12-bit HDMI mode).
YUV6	165	O	YUV pixel 6 output data.
RXD1		I	Serial port 1 receive.
HDMI_D6		O	HDMI data 6 (12-bit HDMI mode).
YUV5	166	O	YUV pixel 5 output data.
HDMI_D5		O	HDMI data 5 (12-bit HDMI mode).
YUV4	167	O	YUV pixel 4 output data.
HDMI_D4		O	HDMI data 4 (12-bit HDMI mode).
HRST#	168	I/O	Host reset.
HDMI2_ACT		O	Active HDMI source (24-bit HDMI mode).
LDCO	169	O	CD/DVD laser diode select.
AMPSTBY	170	O	Power amplifier standby.
CLOSESW	171	I	Tray closed detector.
CLOSE	172	O	Drive to close tray.
OPENSW	173	I	Tray open detector.
OPEN	174	O	Drive to open tray.
VPB, VPA	175, 193	P	RF AFE analog power.
VGB, VGA	176, 194	G	RF AFE ground.
MP	177	I/O	Peak hold capacitor for Mirror.
DB	178	I/O	Bottom hold capacitor for Defect.
MB	179	I/O	Bottom hold capacitor for Mirror.
TE	180	O	Tracking error output.
FE	181	O	Focus error output.
V165O	182	O	Reference voltage for servo analog output signals.
PI	183	O	Photodiode subbeam addition input signal.
REX	184	I/O	Biasing resistor.
DVDLD	185	O	DVD laser diode control.
CDLD	186	O	CD laser diode control.
VBO	187	O	2.1V CPU reference voltage.
DVDPD	188	I	Power down for DVD.

UNDER NDA FOR EASTECH

Table 1 ES8381 Pin Description (Continued)

Names	Pin Number(s)	I/O	Definitions
AGC2	189	I/O	AGC2 capacitor.
AGC1	190	I/O	AGC1 capacitor.
SPNN	191	I/O	Negative spindle rotation detect in.
MNTRN		I/O	Negative differential output for monitor.
SPNP	192	I/O	Positive spindle rotation detect in.
MNTRP		I/O	Positive differential output for monitor.
IMSR		I/O	Optical pickup unit categorization analog in.
DRFN	195	I	Negative differential RF input from OPU.
DRFP	196	I	Positive differential RF input from OPU.
A-H	197:204	I	OPU outputs, DC coupled.
MIN	205	I	Envelope input from Mirror.
SLV	206	O	Data slicer level output. Connected to external capacitor.
DMO	207	O	Spindle drive.
FOO	208	O	Focus drive.
SLO	209	O	Sled drive.
TRO	210	O	Track drive.
CDPD	211	I	Power down for CD.
REFD	212	I	Flash reference decouple.
DVCC	215	P	1.2V power for flash.
HD0	218	I/O	Host data 0.
HDMI2_D8		O	HDMI data 8 (24-bit HDMI mode).
HD15	219	I/O	Host data 15.
HDMI2_D23		O	HDMI data 23 (24-bit HDMI mode).
HD1	220	I/O	Host data 1.
HDMI2_D9		O	HDMI data 9 (24-bit HDMI mode).
HD14	221	I/O	Host data 14
HDMI2_D22		O	HDMI data 22 (24-bit HDMI mode).
HD2	222	I/O	Host data 2
HDMI2_D10		O	HDMI data 10 (24-bit HDMI mode).
HD13	223	I/O	Host data 13.
HDMI2_D21		O	HDMI data 21 (24-bit HDMI mode).
HD3	224	I/O	Host data 3
HDMI2_D11		O	HDMI data 11 (24-bit HDMI mode).
HD12	225	I/O	Host data 12.
HDMI2_D20		O	HDMI data 20 (24-bit HDMI mode).

UNDER NDA FOR EASTECH

Table 1 ES8381 Pin Description (Continued)

Names	Pin Number(s)	I/O	Definitions
HD4	226	I/O	Host data 4
HDMI2_D12		O	HDMI data 12 (24-bit HDMI mode).
HD11	227	I/O	Host data 11.
HDMI2_D19		O	HDMI data 19 (24-bit HDMI mode).
VID_XI	228	I	Crystal clock in.
VID_XO	229	O	Crystal clock out.
CLK	230	I	System clock.
HD5	233	I/O	Host data 5.
HDMI2_D13		O	HDMI data 13 (24-bit HDMI mode).
HD6	234	I/O	Host data 6.
HDMI2_D14		O	HDMI data 14 (24-bit HDMI mode).
HD7	235	I/O	Host data 7.
HDMI2_D15		O	HDMI data 15 (24-bit HDMI mode).
HD8	236	I/O	Host data 8.
HDMI2_D16		O	HDMI data 16 (24-bit HDMI mode).
HD9	237	I/O	Host data 9.
HDMI2_D17		O	HDMI data 17 (24-bit HDMI mode).
HD10	238	I/O	Host data 10.
HDMI2_D18		O	HDMI data 18 (24-bit HDMI mode).
HDMI2_VSYNC	241	O	HDMI vertical sync (24-bit HDMI mode).
HWR#		I/O	Host write (active-low).
HDMI2_HSYNC	242	O	HDMI horizontal sync (24-bit HDMI mode).
HRD#		I/O	Host read (active-low).
HDMI_HSYNC	243	O	HDMI horizontal sync (12-bit HDMI mode).
HDMI2_D4		O	HDMI data 4 (24-bit HDMI mode).
HWRQ#		I/O	Host write request (active-low).
HDMI2_D3	244	O	HDMI data 3 (24-bit HDMI mode).
HDMI_ACT		I/O	Active HDMI source (12-bit HDMI mode).
HRDQ#		I/O	Host read request (active-low).
HDMI2_D1	245	O	HDMI data 1 (24-bit HDMI mode).
HIORDY		I/O	Host I/O ready.
HDMI2_D0	246	O	HDMI data 0 (24-bit HDMI mode).
HIRQ		I/O	Host interrupt.
HDMI2_D6	247	O	HDMI data 6 (24-bit HDMI mode).
HA1		I/O	Host address 1.

UNDER NDA FOR EASTECH

Table 1 ES8381 Pin Description (Continued)

Names	Pin Number(s)	I/O	Definitions
HDMI2_D5	248	O	HDMI data 5 (24-bit HDMI mode).
HA0		I/O	Host address 0.
AUX0	249	I/O	Auxiliary port 0.
HDMI2_D2	250	O	HDMI data 2 (24-bit HDMI mode).
HCS1FX#		O	Host chip select 1 (primary).
RESET#	251	I	Reset (active-low).
AUX1	252	I/O	Auxiliary port 1.

UNDER NDA FOR EASTECH

ES8381 DEVICE INTERFACES

Table 2 lists the device interfaces for the ES8381.

Table 2 ES8381 Device Interfaces

Name	Pin Names	Pin Numbers	I/O	Definition
Audio Port Interface	TSD1	21	O	Audio transmit serial data port 1.
	TSD2	99	O	Audio transmit serial data port 2.
	SPDIF_OUT	119	O	Sony/Philips Digital Interface audio output.
	SPDIF_IN	120	I	Sony/Philips Digital Interface audio input.
	ADC_BIAS	124	O	Audio ADC bias voltage out.
	MIC_L	125	I	Audio ADC_MIC L.
	MIC_R	126	I	Audio ADC_MIC R.
	TWS	141	O	Audio transmit frame sync out.
	PWM_O1L		O	Audio hyperstream out.
	TSD0	142	O	Audio transmit serial data port 0.
	PWM_O2L		O	Audio hyperstream out.
	TSD1	143	O	Audio transmit serial data port 1.
	PWM_O2R		O	Audio hyperstream out.
	TSD2	146	O	Audio transmit serial data port 2.
	PWM_O3L		O	Audio hyperstream out.
	TSD3	147	O	Audio transmit serial data port 3.
	PWM_03R		O	Audio hyperstream out.
	TBCK	148	I/O	Audio transmit bit clock.
	PWM_01R		O	Audio hyperstream out.
	LINE_OL	149	O	Audio left channel out.
	LINE_OR	150	O	Audio right channel out.
	MCLK	153	I/O	Audio master clock for audio DAC.
	RSD	154	I	Audio receive serial data.
	TSD0		O	Audio transmit serial data port 0.
	RBCK	155	I/O	Audio receive bit clock.
	TBCK		I/O	Audio transmit bit clock.
	RWS	156	I	Audio receive frame sync.
	TWS		O	Audio transmit frame sync out.
	TSD3	162	O	Audio transmit serial data port 3.
	TDMDR	159	I	TDM serial data.
	RSD		I	Audio receive serial data.
	TDMCLK	160	I	TDM bit clock.
	RBCK		I/O	Audio receive bit clock.

UNDER NDA FOR EASTECH

Table 2 ES8381 Device Interfaces (Continued)

Name	Pin Names	Pin Numbers	I/O	Definition
Audio Port Interface (continued)	TDMFS	161	I	TDM frame sync.
	RWS		I	Audio receive frame sync.
Auxiliary Port Interface	AUX7-0	40, 32, 31, 18, 17, 5, 252, 249	I/O	Primary auxiliary port I/Os.
	AUX3[7:0]	98, 97, 88, 87, 78, 77, 69, 68	I/O	Aux3 data I/Os.
Clock Interface and Reset	DSCK	33	O	Output clock to video memory.
	VID_XI	228	I	27-MHz crystal clock input.
	VID_XO	229	O	27-MHz crystal clock output.
	CLK	230	I	System clock.
	RESET#	251	I	Reset input (active-low).
Filter and Reference Voltage Interface	VREF	130	I	Internal voltage reference to video DAC.
	COMP	131	I	Compensation input.
	V165O	182	O	Reference voltage for servo analog output signals.
High Definition Media Interface	HDMI2_CLK	4	I/O	HDMI pixel clock (24-bit HDMI mode).
	HDMI_D11-0	31, 32, 66, 67, 164-167, 117, 118, 53, 52	O	HDMI data bus (12-bit HDMI mode).
	HDMI_CLK	163	I/O	HDMI pixel clock. (12-bit HDMI mode)
	HDMI2_ACT	168	I/O	Active HDMI source (24-bit HDMI mode).
	HDMI_ACT	244	I/O	Active HDMI source (12-bit HDMI mode).
	HDMI2_D23-0	219, 221, 223, 225, 227, 238, 237, 236, 235, 234, 233, 226, 224, 222, 220, 218, 3, 247, 248, 243, 244, 250, 245, 246	O	HDMI data bus (24-bit HDMI mode).
	HDMI_VSYNC	41	I/O	HDMI vertical sync (12-bit HDMI mode).
	HDMI2_VSYNC	241	I/O	HDMI vertical sync (24-bit HDMI mode).
	HDMI2_HSYNC	242	I/O	HDMI horizontal sync (24-bit HDMI mode).
	HDMI_HSYNC	243	I/O	HDMI horizontal sync (12-bit HDMI mode).

UNDER NDA FOR EASTECH

Table 2 ES8381 Device Interfaces (Continued)

Name	Pin Names	Pin Numbers	I/O	Definition
Host Port Interface	HA[2:0]	3, 247, 248	I/O	Host address bus.
	HCS3FX#	4	O	Host chip select 3.
	IOW#	5	O	I/O write strobe.
	IOR#	17	O	I/O read strobe.
	HRST#	168	O	Host reset.
	HD[15:0]	219, 221, 223, 225, 227, 238, 237, 236, 235, 234, 233, 226, 224, 222, 220, 218	I/O	Host data bus.
	HWR#	241	I/O	Host write.
	HRD#	242	O	Host read.
	HWRQ#	243	O	Host write request.
	HRDQ#	244	O	Host read request.
	HIORDY	245	I	Host I/O ready input.
	HIRQ	246	I/O	Host interrupt.
	HCS1FX#	250	O	Host chip select 1.
Power and Ground	VD33	1, 14, 30, 46, 58, 65, 75, 93, 112, 144, 157, 216, 232	P	I/O power supply.
	VS33	13, 29, 45, 57, 64, 74, 92, 111, 145, 158, 231, 256	G	Ground.
	VDD	23, 84, 102, 151, 240	P	1.2V core power supply.
	VSS	24, 83, 103, 152, 239	G	Ground.
	AVD33	121	P	Analog power for audio ADC and USB.
	AVS33	127	G	Analog ground for audio ADC and USB.
	VD33PLL	128	P	Power supply for PLL blocks.
	VS33PLL	129	G	Ground for PLL blocks.
	VD33_DAC	135	P	Power supply for video DAC.
	VS33_DAC	136	G	Ground for video DAC.
	AVDD3	213	P	3.3V analog power for flash.
	AVSS	214	G	Analog ground for flash.
	DVCC	215	P	1.2V power for flash.

UNDER NDA FOR EASTECH

Table 2 ES8381 Device Interfaces (Continued)

Name	Pin Names	Pin Numbers	I/O	Definition
OPU/Loader Interface	HOMESW	17	O	Sled home switch position detector.
	FGIN	101	I	Spindle hall sensor input.
	TXD0	149	O	Transmit serial port 0.
	RXD0	150	I	Receive serial data port 0.
	TXD1	164	O	Transmit serial port 1.
	RXD1	165	I	Receive serial data port 1.
	LDCO	169	O	CD/DVD laser diode select.
	AMPSTBY	170	O	Power amplifier standby.
	CLOSESW	171	I	Tray closed detector.
	CLOSE	172	O	Drive to close tray.
	OPENSW	173	I	Tray open detector.
	OPEN	174	O	Drive to open tray.
	VPB, VPA	175, 193	P	RF preamp analog power.
	VGB, VGA	176, 194	G	RF preamp analog ground.
	MP	177	I	Peak hold capacitor for Mirror detect input.
	DB	178	I	Bottom hold capacitor for Defect flag.
	MB	179	I/O	Bottom hold capacitor for Mirror detect input.
	TE	180	I	Tracking error.
	FE	181	I	Focus error.
	V165O	182	O	1.65V reference voltage for servo analog output signals.
	PI	183	I	Photodiode subbeam addition input.
	REX	184	I/O	Biasing resistor.
	DVDLD	185	O	DVD laser diode control.
	CDLD	186	O	CD laser diode control.
	VBO	187	O	2.1V CPU reference voltage.
	DVDPD	188	I	Power down for DVD.
	AGC2-1	189, 190	I/O	AGC2-1 capacitors.
	SPNN	191	I/O	Negative spindle rotation detect in.
	MNTRN		I/O	Negative differential output for monitor.
	SPNP	192	I/O	Positive spindle rotation detect in.
	MNTRP		I/O	Positive differential output for monitor.
	IMSR		I/O	Optical pickup unit categorization analog in.
	DRFN	195	I	Negative differential RF input from OPU.
	DRFP	196	I	Positive differential RF input from OPU.
	A-H	197-204	I	OPU outputs, DC coupled.

UNDER NDA FOR EASTECH

Table 2 ES8381 Device Interfaces (Continued)

Name	Pin Names	Pin Numbers	I/O	Definition
OPU/Loader Interface (continued)	MIN	205	I	Envelope input from Mirror.
	SLV	206	O	Data slicer level output.
	DMO	207	O	Spindle drive.
	FOO	208	O	Focus drive.
	SLO	209	O	Sled drive.
	TRO	210	O	Tracking drive.
	CDPD	211	I	Power down for CD.
	REFD	212	I	Flash reference decouple.
Removable Storage Card Interface	MSBS	41	I/O	Memory Stick bus strobe.
	MSD3-0	163, 162, 66, 67	I/O	Memory Stick data I/Os 3-0.
	SSD3-0		I/O	SD data I/Os 3-0.
	MSCLK	101	I/O	Memory Stick clock.
	SDCLK	155	I/O	SD clock.
	SDCMD	156	I	SD Command strobe.
Static RAM (SRAM) Interface	LA[21:0]	76, 73, 80, 81, 95, 59, 60, 61, 62, 63, 70, 71, 72, 82, 85, 86, 89, 90, 91, 94, 116, 96	O	SRAM address bus.
	LWRLL#	79	O	SRAM write enable.
	LCS[3:0]#	99:101, 104	O	SRAM chip select.
	LOE#	115	O	SRAM bus data output enable.
	LD[7:0]	105:110, 113, 114	I/O	SRAM data bus.
Synchronous DRAM (SDRAM) Interface	DMA[11:0]	16, 15, 8, 7, 6, 255, 254, 253, 9, 10,11, 12	O	DRAM address bus.
	DRAS[2:0]#	19, 20, 25	O	DRAM row address strobe outputs.
	DCS1#	20	O	DRAM chip select output.
	DCS[1:0]#	21, 22	O	DRAM chip select outputs.
	DCAS#	26	O	DRAM column address strobe output.
	DOE#	27	O	DRAM output enable.
	DWE#	28	O	DRAM write enable output.
	DSCK	33	O	Output clock to DRAM.
	DQM	34	O	DRAM data I/O mask output.
	DB[15:0]	56, 55, 54, 51, 50, 49, 48, 47, 35, 36, 37, 38, 39, 42, 43, 44	I/O	DRAM data bus.

UNDER NDA FOR EASTECH

Table 2 ES8381 Device Interfaces (Continued)

Name	Pin Names	Pin Numbers	I/O	Definition
TDM Interface	TDMDR	159	I	TDM serial data.
	TDMCLK	160	I	TDM bit clock.
	TDMFS	161	I	TDM frame sync.
UART Port	SIN	5, 32, 150	I	UART serial data in.
	SO	40, 149	O	UART serial data out.
USB Port	USB_P0	122	I/O	Positive analog USB signal.
	USB_N0	123	I/O	Negative analog USB signal.
Video DAC Interface	FDAC	133	O	CVBS/chroma signal for simultaneous mode.
	VDAC	134	O	Composite component signal for YUV mode.
	YDAC	137	O	Luma component signal for YUV mode and Y/C processing.
	CDAC	138	O	Chrominance component signal for Y/C processing.
	UDAC	139	O	Chrominance component signal for YUV mode.
	IDAC	140	O	Interlaced luma component signal for simultaneous mode.
Video Interface	CAMCLK	2	I	Camera clock.
	YUV_CLK	27	I/O	YUV clock.
	VSYNC#	41	I/O	Vertical sync.
	HSYNC#	101	I/O	Horizontal sync.
	CAMIN7-0	98, 97, 87, 86, 78, 77, 69, 68	I	Camera inputs 7-0.
	YUV[7:0]	164, 165, 166, 167, 117, 118, 53, 52	O	Video out.
	PCLK2XSCN	162	I/O	27.0-MHz screen clock.
	PCLKQSCN	163	O	13.5-MHz screen clock.

SYSTEM BLOCK DIAGRAM

A sample system block diagram for the ES8381 Phoenix DVD player board design is shown in Figure 2.

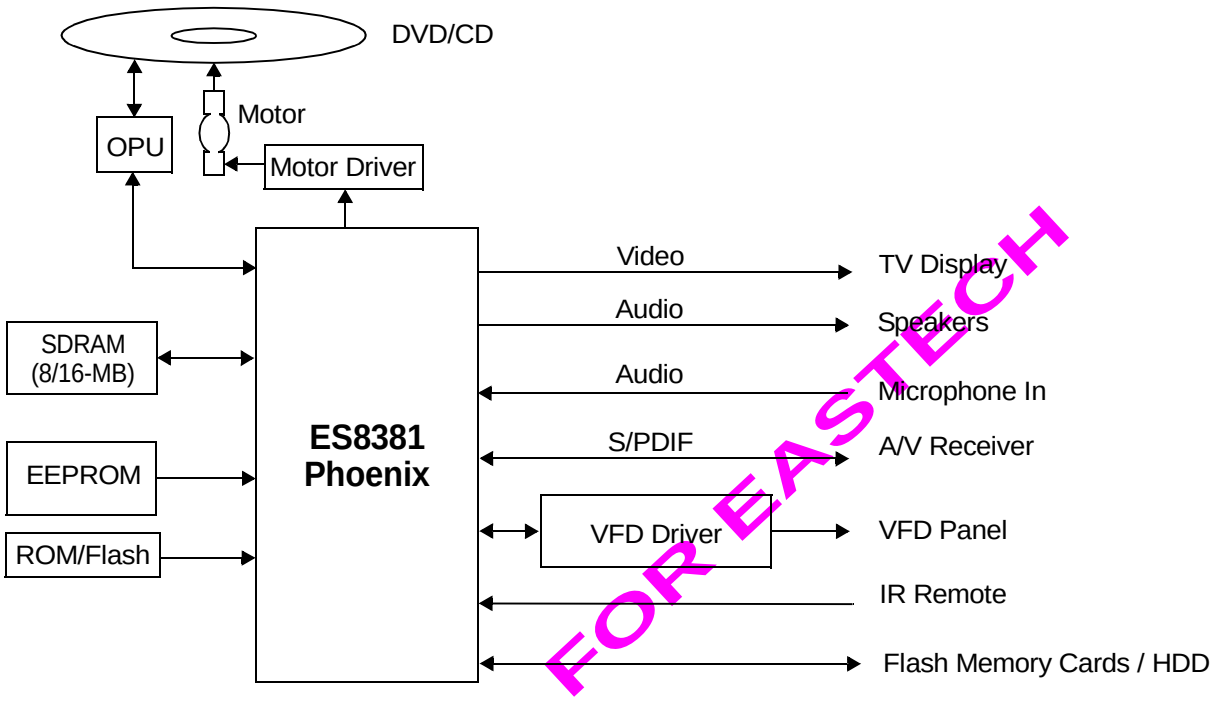


Figure 2. ES8381 Phoenix System Block Diagram

UNDER NDA FOR EASTECH

FUNCTIONAL DESCRIPTION

Figure 3 shows the internal block diagram for the ES8381 processor.

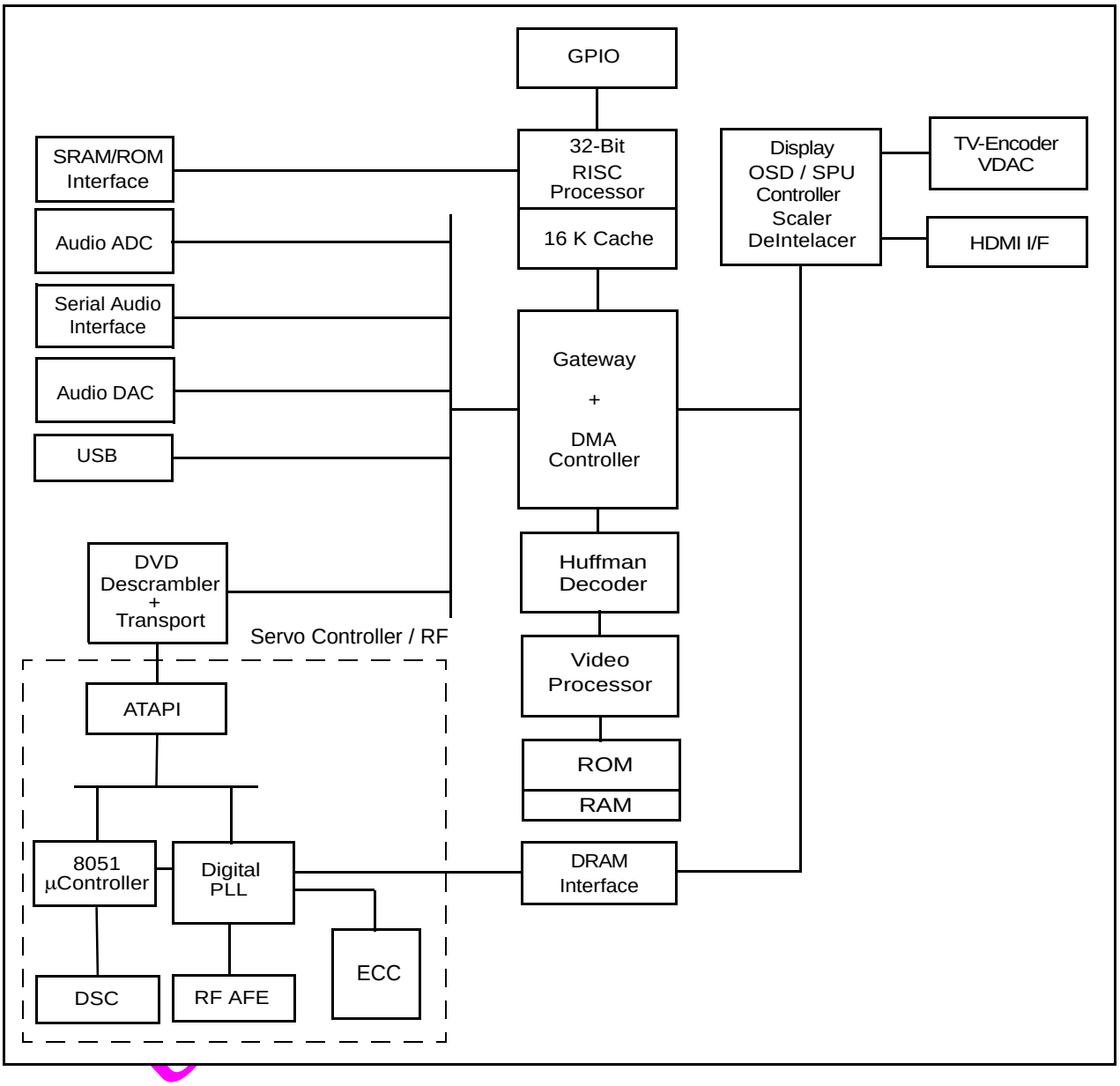


Figure 3 ES8381 Phoenix Block Diagram

ES8381 Device Architecture

The ES8381 device architecture is comprised of an embedded digital servo controller with ECC decoder, a video encoder, 2-channel audio DAC, stereo ADC, and a full-featured DVD processor.

Servo Controller

As shown in Figure 4, a highly simplified view of the servo controller portion features:

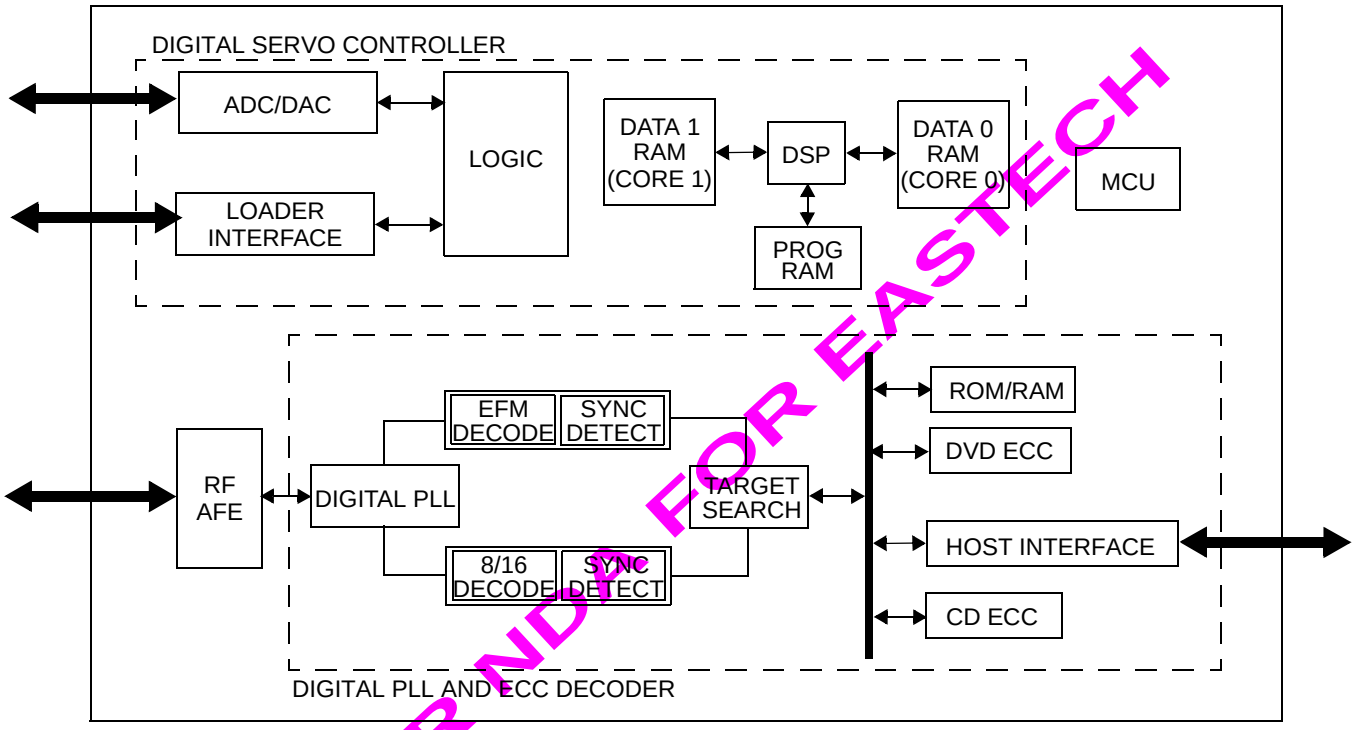
- Microcontroller Unit (MCU)
- Digital PLL + ECC Decoder
- Digital Servo Controller (DSC)
- RF Preamp

The servo controller section accepts the analog signals from the RF preamp, digitizes them, and uses digital signal processing to control focus, tracking, spindle speed, and sled position (the four closed-loop servo functions).

The servo controller also interacts with the system controller (MCU), which commands the servo controller to seek a particular track, play a track, switch from one layer to another, and similar actions.

Finally, the servo controller performs calibration and adjustment functions to compensate for local conditions such as temperature, disc reflectivity changes, supply voltages, various manufacturing variations, and the aging of components within the DVD servo mechanism.

The digital servo ECC decoder and RF AFE block diagram appears in Figure 4



UNDER NDA FOR EASTECH

Figure 4 Servo Controller/RF AFE Block Diagram

RF Preamp W/R

Data Read Cycle

During a data read cycle, the software loads the address information into RF Preamp Control write side register 08h, and the RF Preamp Data is read at register 09h. When the software polls the read side register 08h, a read back of the SR_TRANS_ON_RF bit (bit 4) that returns a 0 indicates that the serial port is busy reading the data.The serial port is free when this bit returns a 1.

Data Write Cycle

During a data write cycle, the software loads the address information into RF Preamp Control write side register 08h, and the data to be written into RF Preamp Data write side register 09h (read side). When the software polls the interface status, a read back of the SR_TRANS_ON_RF bit (bit 4) that returns a 0 indicates that the serial line is busy writing the data. The serial port is free when this bit returns a 1.

Digital Servo Controller

The digital servo includes an internal DSP, on-chip RAM and ROM, control logic, a loader interface, a serial interface, and an on-chip ADC-DAC, and interfaces with the MCU.

The MCU handles the high-level functions of optical disk and front-end system control. The interface between the servo controller and the MCU is illustrated in Figure 5.

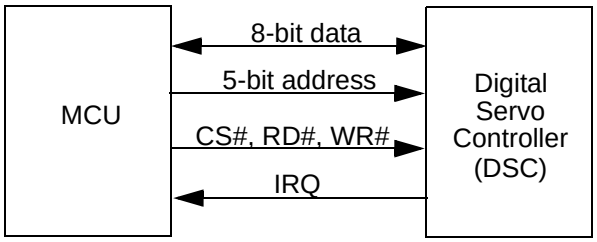


Figure 5 Servo Controller / MCU Interface

Accessing Servo Internal Registers

The register space of the servo internal registers constitute 256 bytes of the MCU memory space, ranging from 0x0000h to 0x00FFh.

The breakdown of the MCU memory space is listed in Table 3.

Table 3 ES8380 MCU Memory Space Range

MCU Memory Space	Device Block
0x0000 — 0x001F	Servo DSP registers
0x0020 — 0x005F	System control registers
0x0060 — 0x00FF	Digital PLL / ECC Decoder registers

Access to ECC DRAM

MCU needs two consecutive address writes to specify locations in the ECC DRAM. MCU can read and write to DRAM by following the procedures below:

Writing to ECC DRAM

1. MCU should poll bit 0 of register 0x0040 to make sure DMA channel is not busy before starting.
2. In the first address write cycle, MCU specifies {HAH, HAL} where HAH = 0xFF and HAL should specify the upper address bits of the DRAM location. During this cycle MCU asserts data with:
   - § Bits [7:5] = 010 indicating a write request.
   - § Bits [4:0] should indicate the number of bytes to write into DRAM (maximum = 31).
3. In the second address write cycle, MCU specifies the lower 16 address bits of the DRAM. During this same cycle, MCU's data bus will contain the first byte that will get written into DRAM.
4. MCU writes data destined to DRAM one byte at a time to address 0x0041.
5. Once all the data have been written, MCU polls bit 0 of register 0x0040 for the status of data transfer to DRAM (1=busy, 0 = finished).

If data bits [7:5] are set to 110 in step 2, this puts the hardware into data descrambling mode. In this mode, 2064 bytes (1 sector) of DVD data will be read out starting from the address specified in steps 2 and 3.

The data will be read out, descrambled and written into the DRAM destination address specified by registers 0x003D (middle byte), 0x003E (lowest byte) and 0x004B (highest byte) automatically by the hardware. To check the completion of the process, MCU can poll bit 0 of register 0x0040 to make sure it is cleared to zero.

UNDER NDA FOR ESS TECH

Reading from ECC DRAM

1. MCU should poll bit 0 of register 0x0040 to make sure DMA channel is not busy before starting.
2. In the first address write cycle, MCU specifies {HAH, HAL} where HAH = 0xFF and HAL should specify the upper address bits of the DRAM location. During this cycle MCU asserts data with:

§ Bits [7:5] = 001 indicating a read request.

§ Bits [4:0] should indicate the number of bytes to read from DRAM (maximum 31).

3. In the second address write cycle, MCU specifies the lower 16 address bits of the DRAM. Internal hardware will discard the data on the MCU data bus at this time.
4. MCU polls bit 0 of register 0x0040 for the status of data transfer from DRAM (1=busy, 0 = finished).
5. When bit 0 is cleared to zero, MCU can read data from address 0x0041.
6. Repeat steps 4 and 5 as necessary until all data has been transferred.

MCU Interrupts

The front-end hardware provides four interrupt signals (INT0, INT1, INT2, INT3) to notify the MCU that a hardware event has occurred. The INT1 signal is used for the debug port between the back-end and the front-end. When asserted, INT1 informs the MCU that the back-end has written data to the debug port register and is available for reading.

The INT2 and INT3 interrupts are used for DVD-RAM playback. INT2 is a PIDOK interrupt, which is asserted by ECC hardware after PID value is written into PID registers. INT3 is a PIDRDY interrupt that is asserted after the ECC hardware accepts the unrecorded sector information.

The INT0 is constructed from a set of eight interrupt sources; becoming active as soon as any one of them becomes active. The source of INT0 is indicated at the interrupt reason register, INTRQ_REASON (addr = 0x0033), and can be cleared or masked by setting the corresponding bit at the interrupt clear register, INTRQ_CLEAR (addr=0x0034), and interrupt mask register, INTRQ_MSK (addr=0x0035).

MCU — DSC Write Operation

The MCU sends data and/or command to the DSC through its set of interface write registers located between addresses 0000h and 001Fh. The most important registers are listed in Table 4. Refer to the Registers section of this document for all other registers.

Table 4 MCU Write Side Registers

Register Name	Address	Description
COMMAND	0001h	Stores the current command code.
MODE_CONTROL_L (low byte)	0002h	15-4: Reserved. 3: Servo error clear. Writing 1 to this location clears the servo error flags. 2-1: Reserved. 0: CPU_FCLR: Clears IRQ when a 1 is written to this bit.
MODE_CONTROL_H (high byte)	0003h	
PARAMETER_INPUT_L (low byte)	0004h	Low byte of MCU data to servo controller.
PARAMETER_INPUT_H (high byte)	0005h	High byte of MCU data to servo controller
RF_AMP_ADDRESS	0008h	RF preamp address. Starts data transmission to RF preamp.
RF_AMP_DATA	0009h	Stores data to be written to RF preamp.

When MCU wants to send a command to the servo controller, it first writes a parameter low to address 0004h, and a parameter high to address 0005h (these two in any order), followed by command to address 0. With the exception of reset command, the servo controller will return an IRQ (active-low) once the controller completes the command.

The MCU waits for the IRQ before it issues the next command. The servo controller on its own may also send an IRQ to MCU in case the controller detects an error. The IRQ status can be read as the highest bit of status high register (address 0001h).

MCU — DSC Read Operation

The MCU receives data and/or status information from the DSC through its set of interface read registers located between addresses 0000h and 001Fh.

UNDER NDA FOR EASTECH

The most important registers are listed in Table 5.

Table 5 MCU Read Side Registers

Register Name	Address	Description
STATUS_L (low byte)	0000h	7: FGNG; Abnormal spindle speed while in FG Mode. 6-5: Reserved.

Spindle Servo Control System

The spindle servo control system of the ES8381 is turned on and off by the DMON command (0x06). There are three different modes of spindle motor control. These modes vary according to the sources of the feedback data used in deriving the next value for motor drive voltage. The spindle servo control system of the ES8381 is depicted in Figure 6.

Figure 6 Spindle Servo Control System Block Diagram

The modes supported are listed in Table 6.

UNDER NDA FOR EASTECH

CAV Mode

The constant angular velocity (CAV) mode is based on the FG signal if a spindle hall sensor is present or on an estimate of the rotational frequency by the servo DSP. CAV mode is used specifically during the disk acceleration and brake periods, during track seeking, or in conjunction with the other modes.

Quasi-CLV mode

The Quasi-CLV mode is the default mode of control used by the ES8381 as its intermediate stage during spindle motor startup, track seeking and abnormal motor condition resolution procedures. The MCU can select between the 18T mode and 6T modes by the parameter associated with the DMMODE command (opcode= 0x08).

CLV Mode

The constant linear velocity (CLV) mode is the most refined mode of control used by the ES8381.

In CLV mode, the ES8381 measures the period of the PG in frequency mode and the phase difference between the PGREF and PG signals in phase mode. The measured values are used to make corrections to the drive signal in order to rotate the spindle at the desired CLV speed.

Focus Servo Control System

Focus Equalizer

The focus servo mainly controls the pickup lens vertical position to keep the beam focused on the surface of the media. This is achieved through the focus equalizer, which adjusts the focus output control signal (FOO) according to the focus error (FE). The overall focus control system shown in Figure 7 is described in Table 7. Focus servo equalizer changed coefficients are listed in Table 8.

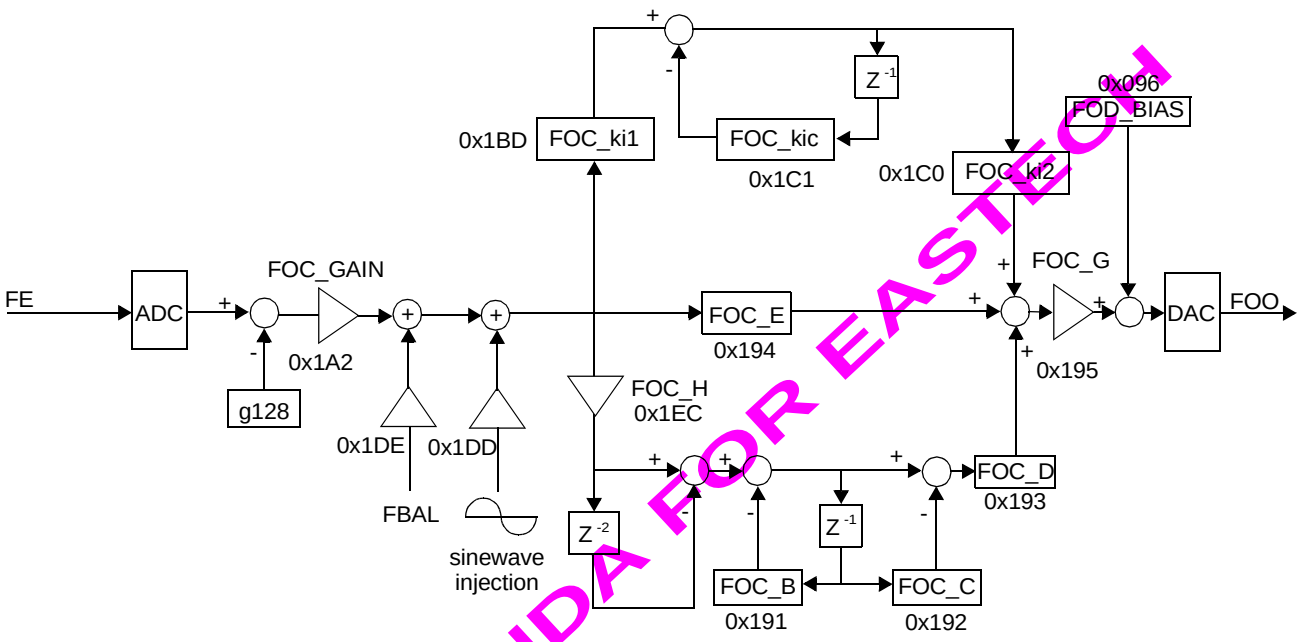


Figure 7 Focus Equalizer Diagram

UNDER NDA FOR EASTECH

Table 7 Focus Control System Parameter Descriptions (Continued)

Parameter	Description
g128	Null value of FE. This is the dc offset value.
FOC_GAIN	Focus equalizer input side gain.
FBAL	Value after focus balance calibration.
FOC_Ki1, FOC_Kic, and FOC_Ki2	Integrator (phase lag) path gains.
FOC_E	Proportional path gain.
FOC_B, FOC_C, FOC_D, and FOC_H	Derivative (phase lead) path gains.
FOC_G	Focus equalizer output side gain.
FOD_BIAS	Offset adjustment for FOO.

Table 8 Focus Servo Equalizer Changed Coefficients

Parameter	Working Address	_SH Gain	_SK Gain	_BD Gain	_BA Gain	_PB Gain	Backup
FOC_Ki1	0x1BD	0x0AD	0x0C9	0x0E3	0x0EF	0x0B8	0x0C8
FOC_B	0x191	0x0AE	0x09A	0x0DE	0x0EA	0x092	—
FOC_C	0x192	0x0AF	0x09B	0x0DF	0x0EB	0x093	—
FOC_H	0x1EC	0x0AC	0x076	0x077	0x078	0x0B7	0x075
FOC_E	0x194	0x0B0	0x09D	0x0E1	0x0ED	0x0B9	0x095
FOC_D	0x193	—	—	—	—	—	0x094

Some gains of the focus servo equalizer have alternate locations in RAM core 0 in order to compensate the closed loop focus servo under various conditions. These alternate gains are loaded at appropriate times, and are described in Table 9.

Table 9 Alternate Gain Types

Gain Type	Description
_SH gain	These gains are loaded into the working locations when the shock filter detects a shock and the shock response flag is turned on. These gains continue to be in effect, as long as shock detection is indicating a shock. Firmware can bring these gains into effect by using command F_WRAD (opcode = 0x98) with parameter_h, bit 7 set to 1 and parameter_l set to 4.
_SK gain	These gains are loaded into the working locations at the beginning of a long seek operation. These gains continue to be in effect, until a track lock is detected to have been regained at the end of the seek operation, i.e. these gains are also used during track pull in operation at the end of a seek. Firmware can bring these gains into effect by using command F_WRAD (opcode=0x98) with parameter_h, bit 7 set to 1 and parameter_l set to 1.
_BD gain	These gains are loaded into the working locations at the beginning of black drop out (BDO) defect signal processing. These gains continue to be in effect, until the BDO is gone. Firmware can bring these gains into effect by using command F_WRAD with parameter_h, bit 7 set to 1 and parameter_l set to 2.

Table 9 Alternate Gain Types (Continued)

Gain Type	Description
_BA gain	These gains are loaded into the working locations at the termination of BDO. These gains continue to be in effect, for a pre-determined time period after the BDO is gone. Firmware can bring these gains into effect by using command F_WRAD with parameter_h, bit 7 set to 1 and parameter_l set to 3.
_PB gain	These gains are loaded into the working locations to bring back the gains to play back gains, at the end of a seek, or BDO, or shock. Firmware can bring these gains into effect by using command F_WRAD (opcode = 0x98) with parameter_h, bit 7 set to 1 and parameter_l set to 5.

For example, the working value of FOC_Ki1 is stored at working address RAM core 1, address 0xBD. During a seek operation the working address is loaded with the parameter value stored at address Ram0:0xC9. The ES8381 hardware automatically implements the parameter swap.

Backup gain locations (0x0c8, 0x075, 0x095, 0x094): The four gains FOC_Ki1, FOC_H, FOC_E and FOC_D have backup locations in mirror format. These backup gains are reloaded into working locations during the events listed in Table 10.

Table 10 Backup Gain Locations and Events

Event	Location
End of focus pull in	0x0C8 (2's complement) = 0x1BD.
End of focus layer jump	0x0C8 (2's complement) = 0x1BD 0x075 (2's complement) = 0x1EC 0x095 (2's complement) = 0x194 0x094 (2's complement) = 0x193

UNDER NDA FOR ESS TECH

Focus Search

A focus search is executed by the ES8381 in response to a C_FCON command (0x81).

For DVD, the following steps are executed:

1. The objective lens is first moved to its top position (focus search scan start point, see address 0x1C9).
2. Starting from this point a slow descent is started. During this descent to the focus search scan end point (see address 0x1C8), the values of FE and AS1 (AS1 is the same as BSUM signal) are monitored. A focal point approach point is recognized when a high value of FE (decided by FE>FE_PULL_IN) as well as low value of AS1 (decided by AS1<AS1_VICINITY_H) is detected.
3. Near the focus point, the scan speed of the objective lens is slowed to the value specified in RAM address 0x1CA. Subsequently when FE crosses its null point (g128), the focus closed loop servo is turned on.

For CD:

1. The objective lens is first taken to its bottom most position and a slow ascent is started.
2. During the ascent, the focus vicinity is flagged by (FE<FE_PULL_IN) and (AS1<AS1_VICINITY_H).
3. The filter start condition is controlled by parameter bit 2 of C_FCON command. If this bit is cleared, the focus equalizer is started when FE crosses its null point (g128). When bit 2 is set, the filter is started when FE crosses FP_BRK_FE.

If the parameter bit 0 of C_FCON is set, a braking pulse will be applied to the focus actuator just before starting the filters. After the focus vicinity is detected, the brake pulse begins when FE crosses FP_BRK_FE. The brake pulse has the width of FP_BRK_CNT_LMT*SI. The strength of the lock pulse is FOC_LOC_PLS. Table 11 lists the focus search parameters and their addresses.

Table 11 Focus Search Parameters and Addresses

Parameter	Address
FE_PULL_IN	0x333, high byte.
AS1_VICINITY_H	0x33C, high byte.
FP_BRK_FE	0x33E, high byte.
FP_BRK_CNT_LMT	0x336, high byte.
FOC_LOC_PLS	0x363, low byte.

Focus Pull In (Parameter Bit 0 Cleared)

The focus pull-in characteristics for DVD and CD modes with parameter bit 0 cleared are depicted in Figure 8.

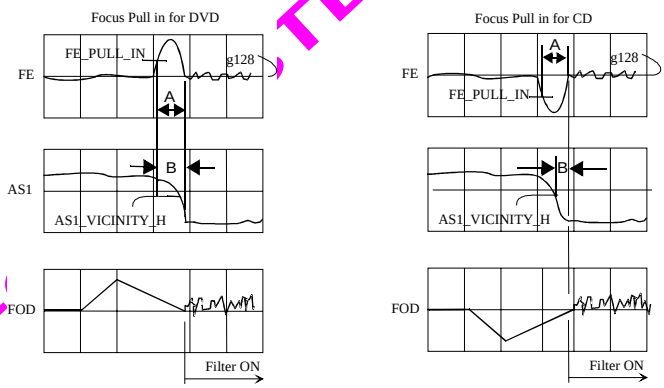


Figure 8 Focus Pull-In (With Parameter Bit 0 Cleared)

Focus Pull In (Bit 0 Set, Bit 2 Cleared)

The focus pull-in characteristics for DVD and CD modes with parameter bit 0 set and parameter bit 2 cleared are depicted in Figure 9.

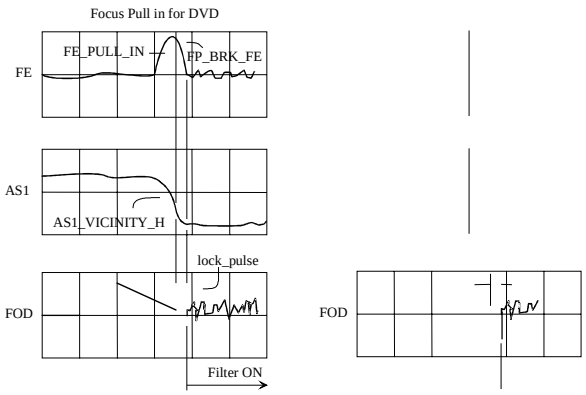


Figure 9 Focus Pull In (With Parameter Bit 0 Set and Bit 2 Cleared)

UNDER NDA F , TECH

Tracking and Sled Servo Control System

Tracking Equalizer

Tracking equalization is achieved through the tracking equalizer, which adjusts the tracking output control signal (TRO) according to the tracking error (TE).

A block diagram of the tracking equalizer is depicted in Figure 10.

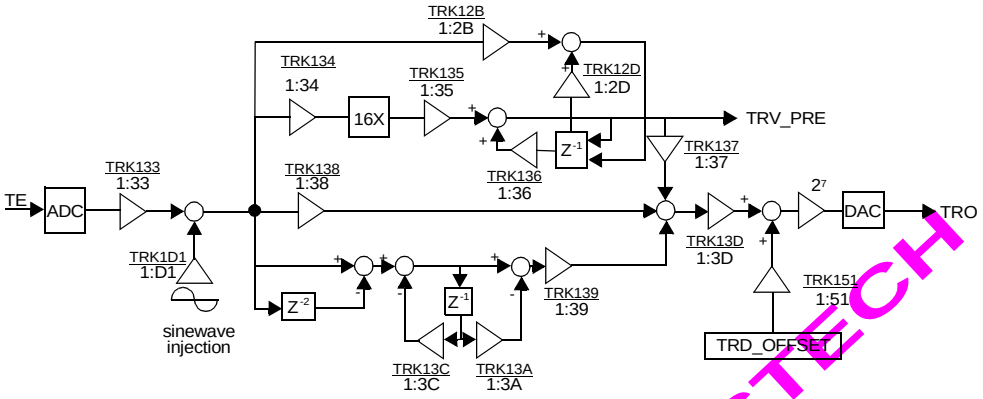


Figure 10 Tracking Equalizer During Playback

The working copies of the tracking filter gain are typically located in RAM core 1.

To compensate the closed-loop tracking servo under various conditions some coefficients of the tracking equalizer are changed, according to Table 12.

Table 12 Tracking Servo Equalizer Changed Coefficients

Parameter	Working Address	_SH Gain	_SK Gain	_BD Gain	_BA Gain	_PB Gain
TRK12B	0x12B	0x0A6	0x0B1	0x0CB	0x0CC	0x0CD
TRK134	0x134	0x0A7	0x0B2	0x0CE	0x0CF	0x0D0
TRK138	0x138	0x0A8	0x0B3	0x0D1	0x0D2	0x0D3
TRK139	0x139	0x0A9	0x0B4	0x0D4	0x0D5	0x0D6
TRK13A	0x13A	0x0AA	0x0B5	0x0D7	0x0D8	0x0D9
TRK13C	0x13C	0x0AB	0x0B6	0x0DA	0x0DB	0x0DC

For example, the working value of TRK12B is stored at working address Ram1:0x2B. During a seek operation, the working address is loaded with the parameter value stored at address Ram0:0xB1. The ES8381 hardware automatically implements the parameter swap.

Tracking Pull-In

Tracking pull-in is executed in response to a C_TRON command (opcode 0x86). Upon receiving this command, the servo controller will initialize the internal states of tracking equalizer and start the track pull-in procedure.

After the track is pulled-in and track following mode has been attained, the command will terminate. This command should be issued only during focus-on condition. During track pull-in, the pickup lens is moved in a radial direction using the C_RSEEKI and C_RSEEKO commands (opcodes 0x1D and 0x1E for short seek, or 0x9D and 0x9E for long seek). By moving in a radial direction, the pickup lens follows the velocity of the moving tracks. This is the velocity mode of track operation.

After allowing some transient settling time specified in RAM1:0x8b, when a sufficiently slow relative speed between the pickup lens and the tracks is attained, the tracking equalizer is started at the on-track position. This check is available when address 0x0E, bit4 is set and the value of the slow speed threshold is TRK_SLOW_SPEED_THR, low byte of address 0x33d.

Sled Equalizer

While the tracking servo controls the fine movement of the lens, the sled servo handles the coarse motion to span the entire length of the disk in track following mode. The sled equalizer receives the TRV_PRE signal (see Figure 10) and generates output signal (SLO) to drive the sled motor, as shown in Figure 11.

UNDER NDA FOR EASTECH

.

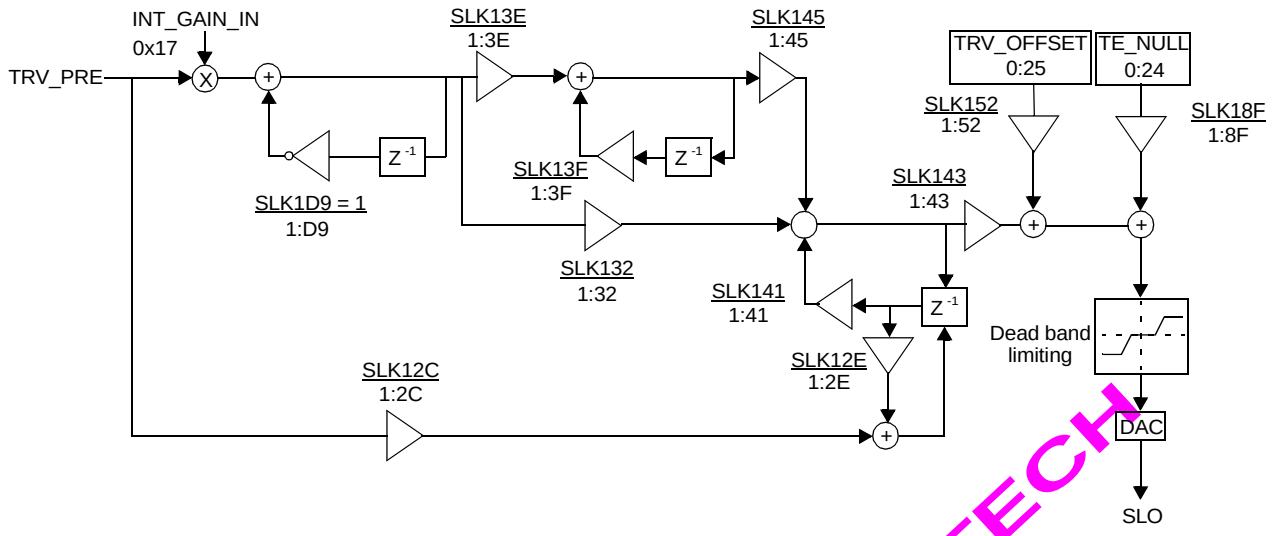


Figure 11 Sled Track Following Equalizer

The dead band circuit at the output of the equalizer is designed to prevent sled chatter. The parameters that control the dead band are defined in Figure 12.

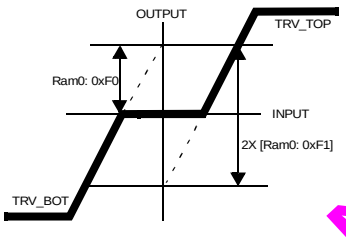


Figure 12 Sled Dead Band Parameters

Servo Seek Tracking

ES8381 implements two different modes of track seeking.

- Short seek based on RSEEKI (0x1D) and RSEEKO (0x1E) commands.
- Long seek based on C_RSEEKI (0x9D) and C_RSEEKO (0x9E) commands.

Track cross (TKCRS) and off-track (OFTR) signals are used to detect both the direction of seeking inwards or outwards, and the relative speed of the lens with respect to the rotating disk.

Short Seek

The short seek mode permits consecutive one-track jump motions to be made in both the inward (RSEEKI) and outward (RSEEKO) directions. This mode permits precise motion to be attained, and is used when approaching the destination track or when seeking a close-by track.

The parameters for the individual jumps as well as the delay between successive jumps are programmable. Starting and stopping pulses of appropriate strength, duration are applied to TRD at appropriate times to realize the jump. The parameters that configure these short seek jumps are defined in Figure 13, Figure 14, and Figure 15.

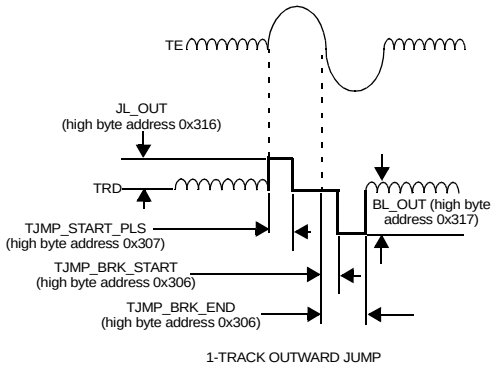


Figure 13 Single-Track Outward Jumping

UNDER NDA FOR EASTECH

Figure 17 shows the four possible set points for the filter, which are labeled as VR0, VR1, VR2, and VR3. The velocity measurement and the associated set points are sine-adjusted internally for the proper direction of the seek operation being performed.

Feed-forward Correction

Across the transitions of the velocity set points, a feed-forward term can be applied selectively in the sled circuit. The shape of this term is described in Figure 18, and is controlled by parameters: FF_GAIN (RAM1:0x71), FF_THR_1 (Bits [14:0]), FF_THR_2 (Bits [14:0]).

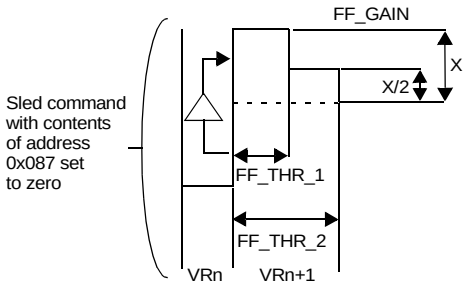


Figure 18 Applying Feed-Forward Correction

Whether to apply the feed-forward correction or not is decided by FF_CFG3, FF_CFG2, FF_CFG1, FF_CFG0 - (bits 11-8 of address 0x383 respectively). When a corresponding bit is 1, the feed-forward correction is applied when entering the corresponding velocity set point. The parameters used during long seek operation are listed in Table 13.

Table 13 Long Seek Parameters

Parameter	Address	Bits
TW	—	Measured half track velocity
VREF0	0x300	Low byte
VREF1	0x300	High byte
VREF2	0x301	Low byte
VREF3	0x301	High byte
FF_THR_1	0x31C	[14:0]
FF_THR_2	0x31D	[14:0]
VSQ0	0x320	
VSQ1	0x321	
VSQ2	0x322	
VSQ3	0x323	
SLED_OFFSET0	0X324	High byte: outward seek. Low byte: inward seek
SLED_OFFSET1	0x325	High byte: outward seek
SLED_OFFSET2	0x326	Low byte: inwards seek.
SLED_OFFSET3	0x327	High byte: outwards seek
VTRD_GN0	0x32A	
VTRD_GN1	0x32B	
VTRD_GN2	0x32C	
VTRD_GN3	0x32D	
TRK_SLOW_SPEED_THR	0x33D	Low byte
VR_TRANSITION_PT_1	0x349	
VR_TRANSITION_PT_2	0x34A	

Auto Adjustment Functions

The ES8381 supports a variety of automatic adjustment functions to support reading the various optical media formats for playback.

The ES8381 performs the following types of auto adjustments and calibrations:

1. Analog offset and calibration.
2. Focus and tracking balance adjustment.
3. Gain adjustment.
4. Loop gain adjustment of focus servo and tracking servo.

Calibrations

Offset Calibration

The servo initialization and offset calibration is typically performed when the drive is first powered-on or following the insertion of each new disc in order to cancel out the dc offsets which come from the RF preamp (FE, TE, CE, AS1, VREFIN, VREFOUT), and which connect to the actuators (FOD, TRD, TRV, and DMO).

The offset calibration procedure is executed in response to a C_ADDA (0x92) command. This command can be used in two different modes, Mode 0 and Mode 1, as follows.

In Mode 0 operation, two channels are specified by the address in parameter bits 10:8. The two channels are referred as high order and low order. The bits 7:0 specify the averaging parameters. The specified two channels are averaged and the results are returned to MCU.

If the parameter bit 11 is set, the low order channel offset is automatically adjusted such that the current value of the channel is read as 0x80 after ADC conversion. Similar adjustment for high order channel is done if parameter bit 12 is set.

Prior to averaging procedure, this command will set the tracking actuator output (or the focus actuator output if the parameter bit 14 is set) to the value specified by memory location Ram1:0xC6. For this mode, parameter bit 13 should be cleared to zero.

In Mode 1 operation, the MCU sets the offset for a specified channel to be the value of parameter bits 7:0. Only one channel can be set at a time. The channel is primarily specified by the parameter bits 10:8.

The low or high order channel is further selected by parameter bit 11, such that high order channel is selected when parameter bit 11 is set, and the low order channel when this bit is cleared. For this mode, parameter bit 13 should be set.

UNDER NDA FOR EASTECH

Channel Addressing (Averaging)

Channel addressing for averaging is performed when Mode 0 operation is selected. The averaging values for parameter bits 10:8 in Mode 0 operation are listed in Table 14.

Table 14 Channel Addressing For Averaging

Parameter Bits [10:8}	High Order Values	Low Order Values
000	Reference voltage out for focus and tracking coil power amplifier (VREFOUT).	DAC.
001	Analog signal proportional to data ripple in BSUM signal; 8-bit ADC input (RFENV).	Tracking Error (TE).
010	Photo diode sum signal (same as BSUM; 8-bit ADC input) (AS1).	Center Error (CE).
011	—	Reference voltage in for analog signals generated by RF preamp (VREFIN).
100	Focus Error (FE).	Focus Out Drive signal (same as FOO); 8-bit DAC output (FOD).
101	Minimum tracking error (TE-MIN).	Maximum tracking error (TE-MAX).
110	—	Undefined (XX).
111	—	Spindle CLV phase error.

Channel Addressing (Offset)

Channel addressing for offset is performed when Mode 1 operation is selected. The offset values for parameter bits 10:8 in Mode 1 operation are listed in Table 15.

Table 15 Channel Addressing For Offset

Parameter Bits [10:8}	High Order Values	Low Order Values
000	Reference voltage out for focus and tracking coil power amplifier (VREFOUT).	DAC.

Table 15 Channel Addressing For Offset (Continued)

Parameter Bits [10:8}	High Order Values	Low Order Values
001	Analog signal proportional to data ripple in BSUM signal; 8-bit ADC input (RFENV).	Tracking Error (TE).
010	Photo diode sum signal (same as BSUM; 8-bit ADC input) (AS1).	Center Error (CE).
011	—	Reference voltage in for analog signals generated by RF preamp (VREFIN).
100	Focus Error (FE).	Traverse (Sled) drive signal offset (same as SLO); 8-bit DAC output (TRV_OFSET).
101	—	Focus Out Drive null offset (FOD_NULL).
110	—.	Tracking drive signal null offset (same as TRO); 8-bit DAC output (TRD_NULL).
111	—	Spindle drive signal offset (SP_OFSET).

Focus Balance Adjustment

Focus balance adjustment is executed in response to a C_ADSFCIN (0x83) command. Focus balance adjustment finds the operating point of the focus servo that maximizes RFENV signal by adjusting focus balance signal FBAL. This command can be operated in Automatic mode or MCU mode.

In Automatic mode, the value of FBAL is searched such that the DC value of RFENV is maximized. The total number of iterations allowed is set by FBAL_ITER_LIMIT and if convergence is not achieved an error is returned to CPU.

The search increment is specified by Ram0:0x97 and the initial estimate is determined by Ram0:0x91. Parameter bit 2 of C_ADSFCIN command should be cleared for this mode of operation.

UNDER NDA FOR EASTECH

In MCU mode, a single value is sent out to FBAL, which is decided by the contents of memory RAM0:0x91, and the corresponding value of RFENV is measured and returned to the CPU. Parameter bit 2 of C_ADSFCIN command should be set for this mode operation.

Auto-Adjust For Dual-Layer DVDs

The ES8381 performs two types of independent auto-tuning for both single-layer and dual-layer DVDs. The software invokes the C_FOJMP command (0x82h) to facilitate both the loading and saving of the auto-adjustment parameters of the two layers.

These auto-adjustment parameters include offset, tracking balance, tracking sensor gain, focus loop gain, and tracking loop gain adjusted result. Also, the related external RF preamp registers settings are saved and loaded by this command.

Layer Jump

A layer jump is executed in response to a C_FOJMP (0x82) command. If the disc is a dual layer DVD, this command can be used to jump from layer to layer. This command applies a set of starting and stopping pulses to the focus actuator. These pulses can be generated in different ways. The starting pulse can be generated by two methods (decided by C_FOJMP command parameter bit 2).

The stopping pulse is configured by the parameter bits 6:5 and bits 10:9. If bit 10 is set, stop pulse is extended until FE crosses the null point. If bit 10 is cleared, bits 6:5 decide the width of stopping pulse. If bit 9 is cleared, the stop pulse will be completed as directed by bits 6:5. However if bit 9 is set, then the stop pulse will be terminated as soon as the FE-null crossing is detected.

Post brake pulse behavior is decided by bits 8:7. After the stopping pulse, normally (bit 7 and bit 8 cleared) the DSP waits until FE-null crossing condition is reached before starting focus closed loop filter. A braking pulse will be inserted before starting filter if parameter bit 8 is set.

On the other hand, if bit 7 is set, then filter is started immediately after the stop pulse ends, without waiting for FE null crossing condition. This also implies no braking pulse before starting the filter even if bit 8 is set. The parameter bits 1 and 0 decide the destination layer. If the bit 1 is clear, bit 0 decides the target layer (0: target layer is layer #0; 1:target layer is layer #1). If the bit 1 is set, then bit 0 is ignored and a focus change is performed, i.e., if the current layer is 0, then target is set to be 1 and vice versa.

The basic structures of focus up and focus down jumps are depicted in Figure 19.

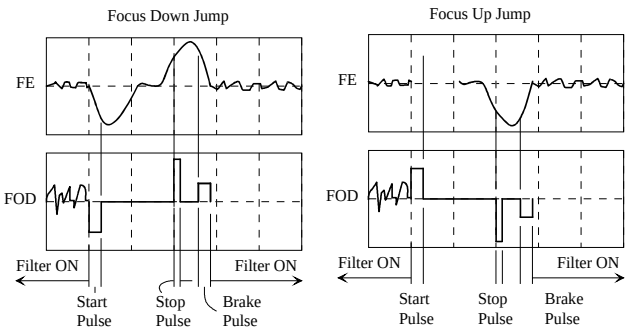


Figure 19 Focus Up and Down Jump Diagrams

Disc Detection and Discrimination

The ES8381 implements disc detection and discrimination in response to a C_DSKSRCH (0x80) command. The command has two modes of operation.

Detection and Discrimination Mode

Before issuing the command in this mode, both laser and spindle (FG mode) should be turned on. The sled is first moved to its innermost position and then moved out for a specified amount of time.

The focus actuator is then moved to its topmost position first in preparation to cycle the actuator down to its bottommost position. The speed of movement and top position are decided by the contents of RAM1:0x99. A slow descent follows until the bottommost position, specified by the contents of RAM1:0x9A, is reached.

The presence of a disc is detected if AS1 signal crosses the high byte of address 0x330 during this downward scan. If no disc is detected, the C_DSKSRCH command terminates and returns a “no disc” response to the CPU. The “no disc” response is the low byte return value of the C_DSKSRCH command set to 0x0000 being received from the servo controller, which returns the focus actuator to its nominal position.

If the disc is detected, the focus actuator is moved from its bottommost position to its topmost position. During this scan, the minimum and maximum values of FE are recorded, along with the maximum value of RFENV, minimum value of AS1 and cmin (i.e. the value of AS1 when RFENV is maximum).

If multiple peaks for AS1, RFENV and FE exist, the values for global peaks are recorded for cmin, AS1 min and RF max. Values for each local peak are recorded into an array for FE_min, FE_max, RF_max, and AS1_min. Three local peaks at most are recorded by the servo controller.

UNDER NDA FOR EASTECH

Parameters that are used for isolating individual peaks are called S-curves. An identifiable S-curve should pass through FE_S_LOW, FE_S_HIGH and FE_RETURN in that sequence, and should have at least the width of FE_S_WIDTH.

The presence of the disc is reported to the CPU by setting the low byte return value of the C_DSKSRCH command to 1. A typical focus error S-curve is depicted in Figure 20.

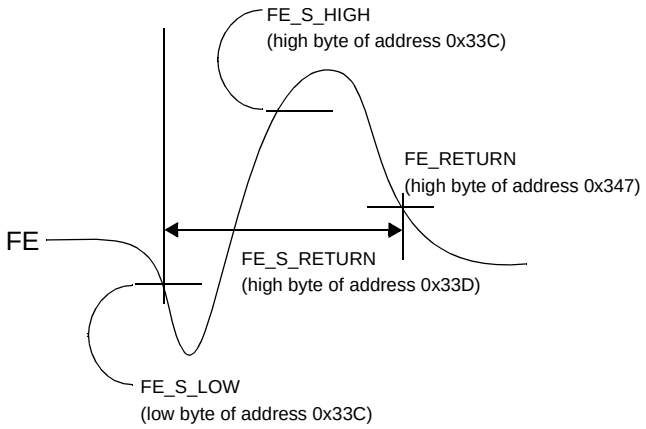


Figure 20 Focus Error S-Curve

The high byte return value of the C_DSKSRCH command returned by the servo controller will be set to the correct reflection distance. Reflection distance is a value proportional to the time elapsed between the disc surface and data surface when the optical pickup unit (OPU) is ascending.

A reflection is detected either by comparing RFENV with a threshold set by address 0x399, by the status of MIRR pin 147, or by the logical OR of these conditions. The judgment method used by bits 6:5 of address 0x0E is listed in Table 16.

Table 16 Reflection Detection Judgment Methods

Bit Value	Detection Method
00	No reflection detection.
01	Threshold on RFENV
10	MIRROR.
11	RFENV threshold or MIRROR.

The value of reflection distance is such that actual time between the reflections is equal to the following equation:

(Reflection Distance) x (Sampling_Rate) x (System_Clock_Period) x (Reflection_Resolution) x 32.

The values of Sampling_Rate and Reflection_Resolution are set at addresses 0x389 and the low byte of 0x360. The MCU is expected to read the recorded signal values using the C_DDR command to further distinguish between the different types of discs. Figure 21 shows waveforms associated with disc detection and discrimination.

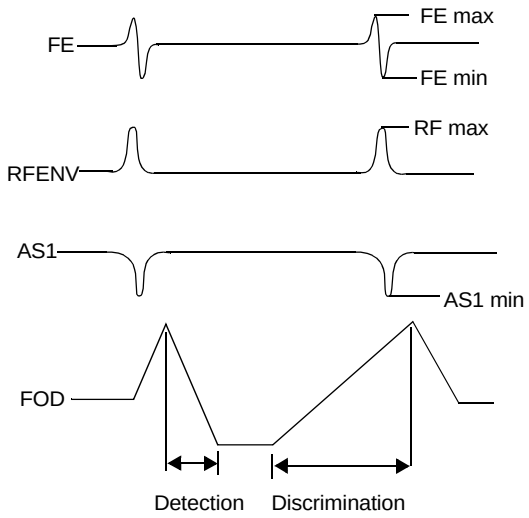


Figure 21 Detection and Discrimination Timing Diagrams

UNDER NDA FOR EASTECH

Sled Inner Movement Mode

This mode is used only for moving the sled to its innermost position and then moving it outward for a specified amount of time. This move out time is specified by contents of RAM1:0x97. The sled drive strengths for inward and outward movements during this operation are constants and are programmable by parameters SLED_GO_OUT_VAL (high byte of address 0x365) and SLED_GO_IN_VAL (low byte of address 0x365) for outward and inward sled movement respectively.

Tracking Loop Gain Calibration

The tracking loop gain calibration procedure calibrates the loop gain of the tracking servo such that the tracking system response remains invariant across different loaders, disks, and operating conditions. This calibration is performed when the servo controller receives the T_ABC (0x9C) command from the MCU. The amplitude or gain measurement is returned for both high byte and low byte after executing the command. Executing the command involves feeding a stimulus sine wave into the tracking loop, as shown in Figure 22.

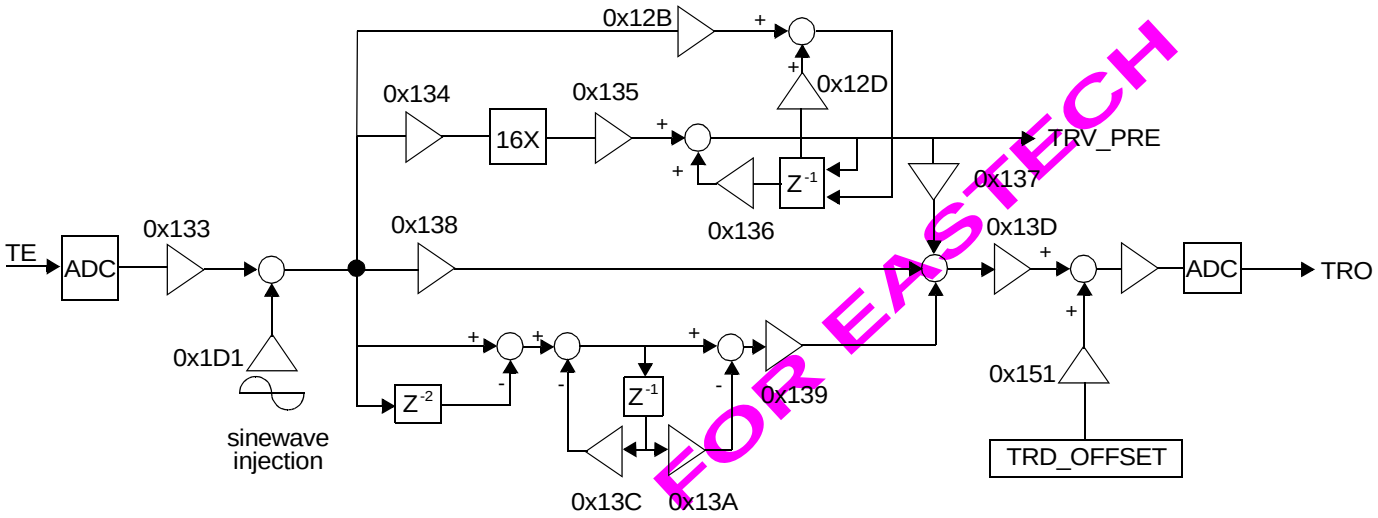


Figure 22 Sine Wave Injection Into Tracking Equalizer

Focus Loop Gain Calibration

The focus loop gain calibration procedure is performed upon reception of the F_ABC (0x9B) command. The command works exactly as the command T_ABC, except that this command should be executed when focus is on and tracking is off.

Tracking Balance Adjustment

Tracking balance adjustment is performed in response to a C_ADSTR (0x85) command. The tracking balance adjustment process implements the same two modes of operation used for focus balance adjustment, Automatic mode and MCU mode.

UNDER NDA FOR EASTECH

In Automatic mode, the value of TBAL is found such that the DC offset of the TE input is equal to TE_OFFSET (high byte of 0x332), within the accuracy of TE_HIGH (high byte of 0x334) and TE_LOW (low byte of 0x334). The values of TE_HIGH and TE_LOW should be centered around a value of 0x80.

The total number of iterations allowed for the search is decided by TBAL_ITER_LIMIT (low byte of 0x338). If the convergence is not achieved within the parameters set, an error is returned to CPU. The mode of search can be set to be incremental or envelope type decided by parameter bit 2 of C_ADSTR command.

In MCU mode, a single value is sent out to TBAL, which is decided by the contents of memory Ram0:0xBD, and the corresponding value of DC offset in TE is measured and returned to CPU. Parameter bit 2 of C_ADSTR command should be set for this mode operation.

Servo Protection Function

Defect Detection And Protection

Defect protection attempts to reduce the deleterious effects of dark defect also known as BDO (input from RF preamp at DFCT pin 146) or bright defect (Mirror or Interruption) from affecting the focus, tracking, and spindle servos.

BDO detection uses the DFCT signal generated by the external RF preamp. The ES8381 detects bright defect from either an externally generated signal through MIRR pin 147 or its own internally generated signal.

When a defect is detected, the focus, tracking and spindle servos will execute a defect hold function to prevent loss of focus, track jump or deviation from the spindle CLV speed.

Focus And Tracking Health Monitors

ES8381 implements two types of health monitors, a focus health monitor (FHM) and a tracking health monitor (THM). During playback mode, bits in register address 0x381 can turn on these health monitors. Whenever either the FHM or THM are triggered due to abnormal conditions, an interrupt is generated by the servo controller. These bits are listed in Table 17.

Table 17 Focus And Tracking Health Monitor Bits

Bit Number	Setting And Description
Bit 3	1 = Turn on FHM. 0 = Turn off FHM.
Bit 10	1 = Turn on THM. 0 = Turn off THM.

UNDER NDA FOR EASTECH

Digital PLL and ECC Decoder

The ES8381 includes a digital PLL, which performs channel bit recovery, and an ECC decoder, which performs error correction during CD and DVD playback. The ECC decoder consists of a DVD-DSP and a CD-DSP.

Digital PLL

The digital PLL converts samples of the RF signal into channel bits for EFM decoding. The following operations are implemented:

- Sampling using a Flash ADC,
- DC estimation,
- second-order PLL,
- zero crossing detection, and,
- bit adjustment.

The bit adjustment function converts the scaled run-lengths (distances between zero crossings) into channel bits. The digital PLL detects and corrects run-lengths, which violate the DVD and CD run-length coding constraints. In addition, the digital PLL generates the sliced data signal used for the spindle servo.

ECC Decoder

The ECC decoder consists of a CD-DSP and a DVD-DSP.

CD ECC Processor

In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity. For C2 correction, the code is created with 24-byte information and 4-byte parity. Both C1 and C2 are Reed Solomon codes with a minimum distance of 5.

The ES8381 uses a refined strategy to achieve double correction for C1 and quadruple correction for C2. To prevent C2 miscorrection, a C1 pointer is attached to data after C1 decoding to improve the C2 decoder's error correction capability. The error flags of C2 decoder also generated and can be used for audio interpolation.

The ES8381 also performs a 32-bit CRC that is applied on bytes 0 to 2067 of the sector, for CD-ROM Mode 1, on bytes 16 to 2075 for CD-ROM XA Mode 2 Form 1, or on bytes 16 to 2351 bytes of CD-ROM XA Mode 2 Form 2. In each case, a CRC remainder value of zero indicates that the sector being examined is error free; otherwise the sector data contains errors. The CRC condition of the latest VCD sector is indicated at CRC status register (0x00E0).

DVD-DSP

The DVD-DSP features:

- Target search hardware
- Sync frame synchronization
- 16-bit to 8-bit EFM+ demodulation
- DVD ECC processor
- ID error correction

In addition, the DVD-DSP performs other functions such as data de-interleaving, data sector descrambling, EDC generation and detection and SDRAM interface.

Target Search (DVD Mode)

When the servo has completed a seek operation and the optical pickup unit (OPU) is focused and on-track, the DVD-DSP can enter the target sector search mode under MCU command.

Prior to initiating target search, the MCU prepares the DVD-DSP hardware by specifying the DVD start page (0x00B0, bits 4-0) and DVD end page (0x00B1, bits 4-0) pointers. Target searching is invoked when the MCU loads the target address at registers 0x00A4h, 0x00A5h, 0x00A6h and sets the NEW_SEARCH_START bit (0x00A0).

The DVD-DSP automatically performs the auto-compare function between the target sector address and the sector ID data. Once target synchronization is achieved DVD-DSP starts writing decoded data frames at the location specified by DVD start page until DVD end page is reached. MCU can extend the DVD end page at any time to buffer more data.

Sync Frame Synchronization

Acquisition of the DVD SYNC pattern (32 channel bit pattern occurring every 1488 channel bits) is important for subsequent operations and for improving disk playability. The detection of a sync pattern indicates the start of a DVD sync frame. If there are errors in the incoming data, the sync detector could be triggered by a false sync pattern.

To detect and protect the SYNC mark the DVD sync detection circuit features a robust search and protection mode for the synchronization pattern. Internal hardware will move from search mode to protect mode and vice-versa, depending on the position and frequency of occurrence of the sync mark within or outside the sync protection window.

EFM+ Demodulation

After all sync patterns are stripped from the incoming data stream, the EFM+ demodulation procedure converts 16-bit data symbols into 8-bit data values. Whenever 16-bit symbols are not found in the demodulation tables, the resulting 8-bit value will be marked as an erasure and passed to the ECC processor.

After demodulation and prior to error correction, sector ID is extracted, error corrected, and stored in the DVD current sector (3-0) registers (B8h - BBh). Whenever a valid sector ID is detected hardware generates CRCOK interrupt to MCU. The DVD-DSP can tolerate errors in the sector ID data. The maximum number of allowed consecutive CRC errors is set in the DVD-RC_CTRL register (0x00A0).

DVD ECC Processor

The DVD ECC processor supports (182,172) Reed-Solomon code in the inner code (PI) and (208,192) in the outer code (PO).

The two correction codes can correct up to V errors and S erasures within the following error correction limits:

$$(2*V) + S \leq \text{checkbytes}$$

Each data row has 10 PI checkbytes; therefore the PI correction can correct up to 5 errors, 10 erasures or any combination of errors that satisfies the above equation. Whenever the number of errors and erasures exceeds 10, no data in the PI row will be modified; instead, all of the bytes in the row will be marked as an erasure, and passed to the PO error correction process. Similarly, each data column has 16 PO checkbytes; therefore, the PO correction can correct up to 8 errors, 16 erasures, or any combination of errors and erasures that meet the above equations.

ID Error Correction

This is a six byte (four ID bytes and two IED bytes) Reed-Solomon decoder, which operates on the first six bytes of each DVD data sector. This decoder can correct up to 1 byte of error and is executed after the completion of PI and PO error correction process.

CD-DSP

The CD-DSP features:

- Target search hardware
- CD EFM decoder
- CD ECC processor
- SDRAM interface

Target Search (CD Mode)

The MCU prepares CD-DSP by specifying the CD start page (D4h) and CD end page (D5h) pointers. Target search is invoked when MCU loads the desired target address at registers D0h, D1h, D2h and sets the NEW_SEARCH_START bit in the VCD RC Control Register (C0h.1).

UNDER NDA FOR EASTECH

The CD-DSP automatically performs the auto-compare function between the target sector address and the sector ID data. Once target synchronization is achieved, the DVD-DSP starts writing decoded data frames at the location specified by the CD start page until the CD end page is reached. MCU can extend the CD end page at any time to buffer more data.

CD EFM Decoder

The CD EFM decoder performs three main functions:

- Conversion of the 14-bit channel data to 8-bit (demodulation),
- Frame sync detection and protection, and
- Generation of the frame sync timing signal for spindle servo.

CD disks contain a frame sync which is recorded approximately every 136µs (every 588 channel bits). This signal is used as a reference to recognize the data within a frame; therefore, recognizing the frame sync properly is extremely important for improving playability.

The sync pattern may be lost due to many factors such as defects on the disk, jitter of the PLL and rotational disturbances. ES8381 implements a robust sync protection function in cases where sync shift causes the sync to deviate from the 588-bit interval or an extra sync is detected outside a sync protection window. Under certain situations successive sync patterns may be detected at 588-bit intervals outside the protection window. In this case, the ES8381 realizes the re-synchronization operation to the new window.

DVD Backend Processor

The DVD processor of the ES8381 consists of a RISC processor, two independent CRT controllers, transport stream parser, video encoder, dedicated SRAM and DRAM DMA controllers, On-Screen Display (OSD) controller, subpicture unit decoder, and video processor.

ESS RISC Processor

Embedded in the ES8381 is the 32-bit data pipelined ESS RISC processor, with a combined 16 kb instruction and data cache subsystem. For applications involving an external host processor the communications between a host processor and the ES8381 is handled by a host interface module. The host interface can also be used for high speed data input and output.

PMP Operation

The Programmable Multimedia Processor (PMP) core consists of the ESS RISC core and the video processor core. The ESS RISC core and the video processor operate in parallel and have separate data paths and data buses. The data paths and data buses are interconnected by the internal circuitry in the device architecture.

RISC Core

The ESS RISC core can either work alone or with an external DSP to supervise the operation of both the internal SRAM and DRAM DMA controllers. During encoding operations, the ESS RISC core can retrieve

UNDER NDA FOR EASTECH

architecture are a screen display controller, a digital video encoder with five DACs, a video input block, video system interfaces, FIFOs and DMA controllers.

The PMP core resource can be accessed only from the ESS RISC core. Together, the ESS RISC and the video processor cores form ESS Technology's field-proven PMP engine.

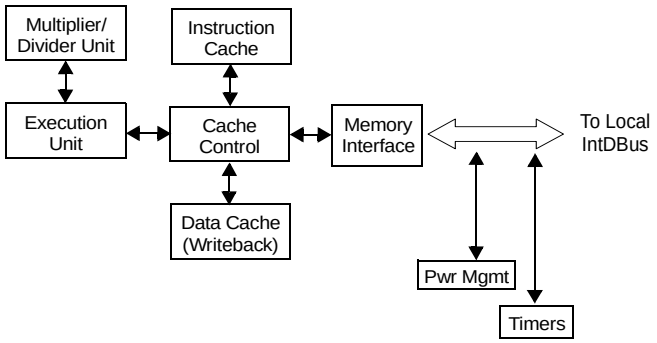


Figure 23 ESS RISC Block Diagram

RISC Interrupts

Twelve events can cause interrupts to the ESS RISC. Each event has a status bit to indicate the occurrence of the event and an enable bit to mask it from interrupting the ESS RISC. Table 18 lists all of the ESS RISC interrupts and the conditions that cause them.

Table 18 ESS RISC Interrupts

Interrupt	Group	Caused By Condition	How To Clear
Video IRQ	0	Video line number equals value in'videoirq'register	RISC EPROM and SRAM wait states
Timer	0	Timer register wraps from 3FFFFh to 00000h	Writing1 to 'clrirq' register bit 3
BCDW	0	DMA Bus Controller Data is waiting to be read after DBUSREAD command	Reading the 'rlatch' register
Cmd Empty	0	DMA Bus Controller Command Queue goes empty	Writing a command to 'cmdque'
H En Idle	1	Huffman Encoder state machine goes idle	Writing 1 to 'clrirq' register bit 2

Table 18 ESS RISC Interrupts (Continued)

Interrupt	Group	Caused By Condition	How To Clear
H De Idle	1	Huffman Decoder state machine goes idle	Writing 1 to 'clrirq' register bit 1
Data Transfer	1	Either Host-to-RISC Data TRE or RISC-to-Host DW (Host can select)	TRE cleared when RISC reads data; DW cleared when RISC writes data
Block Done	1	After DMA controller has read six blocks of RLAs from VP to DRAM	Write any data to 'clrhmade' register
Cmd Half-Empty	2	DMA Bus Controller Command Queue is less than or equal to half full	Write commands to 'cmdque' so queue becomes over half full
Debug	2	DEBUGIRQ pin goes high	DEBUGIRQ pin goes low
FIFO Level	2	Either Encoder Output FIFO or Decoder Input FIFO reach certain fullness	Writing 1 to bit 8 of 'mipctlreg' register
Host to RISC	2	Host sets Host-to-RISC interrupt bit 7 of 'HostControl0' register (Host address 2)	Writing 1 to bit 0 of 'mipctlreg' register

Command Queue and Video Processor

Command Queue

The command queue module controls the video processor module. The command queue allows the RISC to be decoupled from the video processor module by building a command list of instructions used to control its operation. The command list includes instructions for handling video processor DMA, data transfers, send and receive instructions, and waits to receive the current status of the video processor.

The depth of the command queue is approximately 64 entries. When the command queue is setting up DMAs for the video processor, the command queue automatically writes to DMA channel 0 of the bus controller. The BUSCON_CMDQUE_VPDMASETUP register accepts the video processor DMA access requests being routed to the command queue and prioritizes them in the respective order received.

UNDER NDA FOR EASTECH

The incoming commands are always executed in the order they are written to the queue by the RISC. Both requests for 7-bit vales of delta-Y longwords (DELY[6:0]) and 9-bit values of delta-X scan lines (DELX[8:0]) are processed. The BUSCON_CMDQUE_VPDMAADDR register stores the DMA addresses of the incoming commands so that the command can be decoded when execution takes place.

The BUSCON_CMDQUE_STATUS register constantly monitors the status of the command queue. The command queue of the ES8381 receives its DMA inputs from two of the three key bus controller registers.

Video Processor

The video processor consists of a programmable SIMD engine and 2 kb of internal cache memory. The video processor module performs instruction processing for four types of instructions:

- memory instructions
- conditional branch instructions
- compute instructions
- compute immediate instructions.

The video processor executes macroblock level tasks, such as predictive coding, motion estimation, and motion compensation. The video processor can also be used for a wide range of time-critical signal processing tasks, including Dolby Digital (AC-3) audio decoding and both video pre-processing and post-processing.

The video processor enables the ES8381 to perform arbitrary vertical filtering and scaling of outgoing video. The video processor is controlled by 32-bit and 16-bit wide dual issue micro-instructions. Commonly used microcode subroutines are stored in 8 kB of internal microcode ROM, while less frequently used microcode segments can be downloaded on demand to 2 kB of internal microcode RAM.

DMA Controller

The DMA bus controller is controlled by the video processor and controls multiple DMA channels for the transfer of 32-bit data between:

- video data bus and memory
- video decoder and memory
- ESS RISC and memory
- ESS RISC and video data bus.

Writes from the ESS RISC to the video processor command bus are also performed by the DMA bus controller, along with waits on status readback from the video processor status bus. A separate DMA channel is used for memory refresh. To improve memory bandwidth utilization, internal gateway FIFOs are used extensively. The DMA controller includes two registers in the device architecture that interface directly to the video processor.

The BUSCON_VP_CONTROL register performs all video processor microcode loading and reset. The BUSCON_VP_STAT register provides the status of the internal command queue of the video processor while monitoring the status of all sequencing, data transfers and I/O states.

Transport Stream Parser

The ES8381 incorporates a micro-programmable system demultiplexer capable of handling MPEG-1 system stream, MPEG-2 program stream, MPEG-2 transport stream, and other proprietary system multiplexes. The transport mechanism contains a 32-entry packet ID table and satisfies the transport requirements of the DVB standard.

The transport stream parser performs parsing of all packetized elementary streams (PESs) and selects the destinations for all of the audio and video elements in a given bit stream for processing by the ESS RISC engine. Each PES has a packet ID (PID) table, which includes a 4-bit destination field.

The transport stream parser determines the destination of the elements so that the ESS RISC engine knows where to send the final data output after processing. After processing, the transport stream parser also performs data flushing of all the buffer FIFOs in the device.

Input and Output CRT Controllers

The video output timing of the ES8381 is controlled by a pixel clock and the horizontal and vertical sync signals. Pixels are clocked out of the ES8381 by the pixel clock. The sync signals determine when the active video data is transferred.

The timing of the active video and sync signals is determined by the two independent CRT controllers inside the ES8381. The input CRT controller is slaved to the timing of CAMCLK from a camera or other video input source.

The input CRT controller uses HSYNCCAM and VSYNCCAM to determine when active video data is transferred. The clock timing of the output CRT controller is independent of the input CRT controller, and can either be internally generated or slaved to another video sync source.

Video MPEG Decoder

The Phoenix MPEG decoder module performs both MPEG-1 and MPEG-2 decoding. A high-speed Huffman engine decodes MPEG Variable Length Codes (VLCs),

UNDER NDA FOR EASTECH

using built-in MPEG-1 and MPEG-2 VLC tables. A programmable RAM-based table controls automatic switching from one VLC table to the next.

During decoding, the ESS RISC processor parses the MPEG data all the way to the macro-block level. A special start code search engine is used to locate the next MPEG start code, Macroblock address increments, macroblock modes, and motion vectors, which are encoded in VLC, are read from the Non-Run Length Amplitude (NRLA) FIFO, one of the two FIFOs of the Huffman engine. RLA data that constitutes the DCT coefficients are directly transferred to the SIMD DSP.

The RISC processor then orchestrates the transfer of prediction macro-block data to the SIMD DSP and the execution of various SIMD DSP microcode routines, including de-quantization, inverse DCT, and motion compensation. The resulting reconstructed blocks are transferred under RISC control back to the DRAM frame buffer for subsequent post-processing and display.

NTSC/PAL Video Encoder

The NTSC/PAL video encoder accepts digital linear CCIR656/601 YCbCr at the standard 13.5-MHz pixel data rate. Various color space conversion modes are provided to match the input data to the required output format. The data is then filtered to limit the bandwidth of the signals to within the supported ranges of the selected video standard.

The output of the encoder is fed directly into the output FIFO. The ESS RISC is also capable of writing variable length data into the FIFO in order to insert any non-TCOEFF parts into the bitstream. The RISC writes variable length data to the output FIFO up to 10 bits at a time. Smaller tokens can be written by right justifying fewer bits in the least significant bits of the data field. Since the output FIFO is shared between the ESS RISC and the encoder, the ESS RISC should only write to it when the encoder is idle.

The encoder generates all the necessary synchronization signals for NTSC and PAL standards, which are inserted into the composite and luma outputs. Digital syncs are also provided for the rest of the system.

The encoder also generates the corresponding sub-carrier frequency for color encoding. The encoder generates pixels at both square and nonsquare pixel data rates. This represents a pixel sampling rate of 13.5 MHz for both the NTSC and PAL video data streams.

These measurements assume internal 2x and 4x pixel data rate clock sources. Most of the processing is performed at a 2x pixel rate. The output rate is at a 4x pixel rate, which allows the output filtering to consist of a few passive components.

The encoder is a mixed digital/analog design that incorporates five 10-bit video DACs in the device architecture. This level of video DAC incorporation allows the ES8381 to generate composite, luma, and chroma outputs both in Y/C and YUV modes. The S-video luma and chroma outputs are summed internally to generate the composite video output in Y/C mode.

All filtering of the luminance and chrominance signals is performed using DSP techniques. The filters are programmable so that the encoder can provide enhanced bandwidth video for S-video output, but can also provide correctly band-limited signals for composite NTSC/PAL. The sync:white ratio is 40:100 IRE for NTSC, and 43:100 IRE or 34:100 IRE for PAL.

On-Screen Display Controller

The 8-bit On-Screen Display (OSD) controller provides display support for 256 palletized colors in eight degrees of transparency and can occupy the entire viewable area of a display or a portion of the display, depending on the system design. The OSD bitmap, which is stored in the reference memory, is multiplexed into the output video stream before color space conversion is performed.

The ES8381 performs its 3-bit blending of the on-screen display information when the LDMD bit (bit 2) of the VID_SCN_OSD_MISC register is set, enabling bits 2:0 of the VID_SCN_OSD_PALETTE registers to establish the desired blending value for the different types of pixel modes required.

The settings of the MODE field (bits 1:0) in the VID_SCN_OSD_MISC register determine the level of blending. Bits 3 of the VID_SCN_OSD_PALETTE registers enable the actual blending when set at 0. Modes 1 (2 bit/pixel), 2 (4 bits/pixel) and 3 (8-bit/pixel) are supported. For mode 3 (8-bit/pixel), the upper four bits of the pixel are the blend information, while the lower four bits of the pixel are the palette index and the blend information in the palette is ignored.

Subpicture Unit Decoder

The Subpicture Unit (SPU) decoder separates and decodes the run-length subpicture pixel data stream and the corresponding subpicture commands that change the color and contrast values of each pixel type for different regions.

The output YUV of the SPU decoder is blended with the main video screen YUV values, depending on the contrast values. The SPU decoder supports four pixel types, coded 00, 01, 10, and 11. Each type represents a color (YUV) and contrast value (blending value with main picture).

UNDER NDA FOR EASTECH

The subpicture display area can also be divided into several horizontal stripes, each potentially with a different set of color/contrast values. Each stripe can be divided vertically into a maximum of 9 vertical regions (default 0, and changes 1-8), each region containing its own color/contrast value for each pixel type. In addition, there is a highlight feature that overrides all other color/contrast information for the SPU.

Main subpicture commands, such as SPU on/off, setting the size of the subpicture display area, default color and contrast, and the pointers to the color/contrast and pixel data are done by the ESS RISC engine. The ESS RISC sets the appropriate registers in the SPU, as well as the DMA channel for the command and data FIFOs, based on these commands.

SPU Video Data Framing

The SPU decoder receives its incoming video data in the data framing scheme depicted in Figure 24. During decoding, the incoming SPU data packet is parsed for its pixel data and for its display control sequence information for decompression during video playback. If the last packet received by the SPU decoder is less than 2048 bytes, the packet will be stuffed with extra bytes.

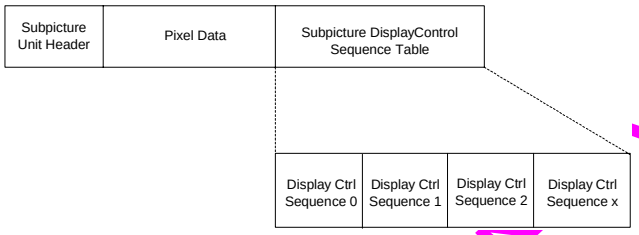


Figure 24 Typical Subpicture Data Framing Format

Coding and Media Content Protection

The ES8381 supports a variety of captioning, coding and media content protection schemes that allow it to support media playback, regardless of the video encoding system used as the broadcast television standard for a specific country or geographic region.

NTSC Closed Captioning

The ES8381 supports the NTSC-compatible Line 21 captioning character set as required by EIA-608 and by FCC Part 15.119. The ES8381 displays the caption information during the blanked active line time of Line 21. The ES8381 also detects the two-byte codes required by FCC Part 15.119 in the bitstream so that it can recognize the embedded captioning data that would otherwise go undetected during DVD playback.

Line 21 Standard Character Set

The ASCII-based Line 21 character set appearing in Table 19 is the same as the one found in EIA-608 and in FCC Part 15.119.

Table 19 Line 21 Standard Character Set

Code	Symbol	Description
20		space
21	!	exclamation mark
22	“	quotation mark
23	#	number sign or pound sign
24	$	dollar sign
25	%	percent sign
26	&	ampersand
27	‘	apostrophe
28	(	open parenthesis
29	)	close parenthesis
2A	á	lowercase a with acute accent
2B	+	plus sign
2C	,	comma
2D	-	hyphen or minus sign
2E	.	period
2F	/	slash
30	0	zero
31	1	one
32	2	two
33	3	three
34	4	four
35	5	five
36	6	six
37	7	seven
38	8	eight
39	9	nine
3A	:	colon
3B	;	semicolon
3C	<	less-than sign
3D	=	equal sign
3E	>	greater-than sign
3F	?	question mark
40	@	at sign
41	A	uppercase A
42	B	uppercase B
43	C	uppercase C
44	D	uppercase D
45	E	uppercase E
46	F	uppercase F
47	G	uppercase G

UNDER NDA - FOR EASTECH

Table 19 Line 21 Standard Character Set (Continued)

Code	Symbol	Description
48	H	uppercase H
49	I	uppercase I
4A	J	uppercase J
4B	K	uppercase K
4C	L	uppercase L
4D	M	uppercase M
4E	N	uppercase N
4F	O	uppercase O
50	P	uppercase P
51	Q	uppercase Q
52	R	uppercase R
53	S	uppercase S
54	T	uppercase T
55	U	uppercase U
56	V	uppercase V
57	W	uppercase W
58	X	uppercase X
59	Y	uppercase Y
5A	Z	uppercase Z
5B	[	open square bracket
5C	è	lowercase e with acute accent
5D	]	close square bracket
5E	ì	lowercase i with acute accent
5F	ò	lowercase o with acute accent
60	ù	lowercase u with acute accent
61	a	lowercase a
62	b	lowercase b
63	c	lowercase c
64	d	lowercase d
65	e	lowercase e
66	f	lowercase f
67	g	lowercase g
68	h	lowercase h
69	i	lowercase i
6A	j	lowercase j
6B	k	lowercase k
6C	l	lowercase l
6D	m	lowercase m
6E	n	lowercase n
6F	o	lowercase o
70	p	lowercase p
71	q	lowercase q
72	r	lowercase r
73	s	lowercase s
74	t	lowercase t

Table 19 Line 21 Standard Character Set (Continued)

Code	Symbol	Description
75	u	lowercase u
76	v	lowercase v
77	w	lowercase w
78	x	lowercase x
79	y	lowercase y
7A	z	lowercase z
7B	ç	lowercase c with cedilla
7C	÷	division sign
7D	Ñ	uppercase N-tilde
7E	ñ	lowercase n-tilde
7F	□	solid block

Line 21 Special Character Set

The Line 21 special character set appearing in Table 20 is the same as the one found in EIA-608 and in FCC Part 15.119.

Table 20 Line 21 Special Character Set

Hex	Example	Alternate	Description
30		See note[1]	Registered mark symbol
31	°		Degree sign
32	½		1/2 symbol
33	¿		Inverted (open) question mark (inverse query)
34	TM	See note[1]	Trademark symbol
35	¢		Cents symbol
36	£		Pounds sterling
37	♪		Musical note
38	à		Lowercase a, grave accent
39			Transparent space
3A	è		Lowercase e, grave accent
3B	â		Lowercase a with circumflex
3C	ê		Lowercase e with circumflex
3D	î		Lowercase i with circumflex
3E	ô		Lowercase o with circumflex
3F	û		Lowercase u with circumflex

NOTE: The registered and trademark symbols are used to satisfy certain legal requirements. There are various legal ways in which these symbols may be drawn or displayed. For example, the trademark symbol may be drawn with the “T” next to the “M” or over the “M.” It is preferred that the trademark symbol be superscripted, i.e., XYZ™. It is left to each individual manufacturer to interpret these symbols in any way that meets the legal needs of the user.

UNDER NDA FOR EASTECH

Macrovision

The ES8381 implements analog content protection of prerecorded media with the Macrovision anti-copy process.

Progressive Scan

The ES8381 supports the progressive scan reconstruction process as well as interlaced video for the NTSC and PAL formats during DVD playback. The ES8381 supports both baseline and progressive JPEG decoding.

In order to show a progressive image, the CRT controllers of the ES8381 are driven to generate and refresh the scan lines used to create the active display at a rate double that of the refresh speed used by the NTSC system in order to draw an entire frame in the same amount of time it takes to draw a single field.

The progressive scan features of the ES8381 make the faster screen refresh possible, allowing for a flicker-free picture of superior quality to be displayed during DVD playback, while also reducing the number of scan lines visible to the unaided eye.

Unlike interlaced video, every scan line of a complex video frame is refreshed when using progressive scan. Since the reconstruction process of de-interlaced video is a digital process, the reconstruction process is a lossless one during A/D and D/A conversion of the bitstream.

Video Error Concealment

The MPEG decoder handles bitstream errors while performing video error concealment during DVD and VCD/SVCD playback.The ES8381 processors all support the three modes of video error concealment presented in Table 21.

Disk Error Concealment

When a read error occurs during DVD playback, Video Object units (VOBUs) are skipped by the ES8381. If the number of VOBUs to be skipped exceeds the range of the available data, the ES8381 skips some sectors on the media until the presence of a new error correction control block is detected in the bitstream.

HDMI Interface

The ES8381 includes a High Definition Media Interface

UNDER NDA FOR EASTECH

Device Interfaces

Audio Interface

The audio interface is a bidirectional serial port that connects to an external audio ADC/DAC for the transfer of PCM (pulse coded modulation) audio data in I²S format. It supports 16-, 24-, and 32-bit audio frames. No external master clock is required.

The ES8381 offers three audio interface modes:

1. Stereo mode using the TSD0 pin.
2. Dolby Digital (AC-3) 5.1 channel mode using the TSD[3:0] pins.
3. Dolby Digital (AC-3) 5.1 channel mode using the S/PDIF pin.

The ES8381 audio mode configuration is selectable, allowing it to interface directly with low-cost audio DACs and ADCs. The audio port provides a standard I²S and S/PDIF (IEC958) interface input and output.

Stereo mode is in I²S format while 5.1 channel Dolby Digital 5.1 channel audio output can be channeled through both the I²S interface and the S/PDIF. The S/PDIF interface consists of a bi-phase mark encoder, which has low skew.

The transmit I²S interface supports the 128, 192, 256, 384, and 512 sampling frequency formats, where sampling frequency Fs is usually 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, or 192 kHz. The audio samples for the I²S transmit interface can be 16, 18, 20, 24, and 32-bit samples.

For Linear PCM audio stream format, the ES8381 supports 48 kHz and 96 kHz. Dolby Digital audio only supports 48 kHz. The ES8381 incorporates a built-in programmable analog PLL in the device architecture in order to generate a master audio clock.

The MCLK pin is for the audio DAC clock and can either be an output from or an input to the ES8381. Audio data out (TSD) and audio frame sync (TWS) are clocked out of the ES8381 based on the audio transmit bit clock (TBCK). Audio receive bit clock (RBCK) is used to clock in audio data in (RSD) and audio receive frame sync (RWS).

Host Interface

The host interface of the ES8381 allows communication between the RISC and an external host, and is comprised of three ports. Two of these ports are the 8-bit wide debug and command ports, with the third being the 16-bit wide DMA port. The command port transfers control and status information between the host and the ES8381. The external host controls the ES8381 through the command port.

The debug port provides a path to the RISC core for debugging purposes. This allows programmers access to the state of the hardware and the software without disturbing the command or DMA ports.The DMA port transfers data to be multiplexed with the audio and video data in an encoded bitstream. This mechanism allows applications such as file transfers to occur. Additionally, the DMA port can carry both the audio and the encoded bitstream.

The host interface has two registers that control the operation of the flags and interrupts, R_HOSTRQSTAT and R_HOSTMASK for the RISC side and H_HOSTRQSTAT and H_HOSTMASK for the host side. Flags indicate the readiness of the ES8381 to accept or supply data over the host interface DMA channel. Interrupts may be used for exception indication from RISC-to-host or from host-to-RISC. The interrupts are maskable.

The pulse width high times of the HRRQ# and HWRQ# signals are defined as minimum values only. The maximum values of these parameters are software dependent. The internal DMA channel bandwidth depends upon the presence of other DMA operations in the ES8381.

Storage Device Interfaces

The ES8381 supports the AT Attachment Packet Interface (ATAPI), Compact Flash (CF), Integrated Drive Electronics (IDE), Memory Stick (MS), SD and Smart Media interfaces.

ATA/IDE Interface

The host interface directly supports ATAPI devices with PIO modes. The ATA/IDE interface can directly control two devices through the use of the HCS1FX# and HCS3FX# signals. The ATA/IDE interface of the ES8381 uses a command execution protocol that allows for the operation of hard disk drives. Table 22 lists the packet commands and the respective command codes for ATAPI devices, as specified by SFF-8090i.

Table 22 Packet Commands for ATAPI Devices

Code	Command Name
00h	TEST UNIT READY
03h	REQUEST SENSE
04h	FORMAT UNIT
12h	INQUIRY
1Bh	START/STOP UNIT
1Eh	PREVENT/ALLOW MEDIUM REMOVAL
23h	READ FORMAT CAPACITIES
25h	READ CAPACITY
28h	READ (10)

UNDER NDA FOR EASTECH

Table 22 Packet Commands for ATAPI Devices (Continued)

Code	Command Name
2Ah	WRITE (10)
2Bh	SEEK
2Eh	WRITE AND VERIFY (10)
2Fh	VERIFY (10)
35h	SYNCHRONIZE CACHE
42h	READ SUBCHANNEL
43h	READ TOC/PMA/ATIP
44h	READ HEADER
45h	PLAY AUDIO (10)
46h	GET CONFIGURATION
47h	PLAY AUDIO MSF
4Ah	GET EVENT/STATUS NOTIFICATION
4Bh	PAUSE/RESUME
4Eh	STOP PLAY/SCAN
51h	READ DISC INFORMATION
52h	READ TRACK/RZONE INFORMATION
53h	RESERVE TRACK/RZONE
54h	SEND OPC INFORMATION
55h	MODE SELECT (10)
58h	REPAIR RZONE
5Ah	MODE SENSE (10)
5Bh	CLOSE TRACK/RZONE/SESSION/BORDER
5Dh	SEND CUE SHEET
A1h	BLANK
A2h	SEND EVENT
A3h	SEND KEY
A4h	REPORT KEY
A6h	LOAD/UNLOAD MEDIUM
A7h	SET READ AHEAD
A8h	READ (12)
AAh	WRITE (12)
ACh	GET PERFORMANCE
ADh	READ DMP STRUCTURE
B6h	SET STREAMING
B9h	READ CD MSF
BAh	SCAN
BBh	SET CD SPEED
BCh	PLAY CD
BDh	MECHANISM STATUS
BEh	READ CD
BFh	SEND DMP STRUCTURE

Compact Flash Interface

The ES8381 provides True IDE Mode I/O support for the Compact Flash storage card interface found on a variety of removable storage cards used by digital cameras and MP3 players. The ES8381 uses its host interface to communicate with Compact Flash devices.

By implementing Compact Flash support, the ES8381 can readily detect the insertion and removal of a Compact Flash card, which also constitutes a hot-swapping event. During a hot-swapping event, the CARD_DETECT signal is asserted by the Compact Flash, allowing it to determine the presence of the removable storage card fully inserted into its socket.

The ES8381 permits both 8- and 16-bit common memory I/O accesses with a removable storage card via the host interface. Table 23 lists the CF-ATA command set.

Table 23 CF-ATA Command Set

Class	Command	Code
1	CHECK POWER MODE	E5h or 98h
1	EXECUTE DRIVE DIAGNOSTIC	90h
1	ERASE SECTOR(S)	C0h
1	IDENTIFY DRIVE	ECh
1	IDLE	E3h or 97h
1	IDLE IMMEDIATE	E1h or 95h
1	INITIALIZE DRIVE PARAMETERS	91h
1	READ BUFFER	E4h
1	READ LONG SECTOR	22h or 23h
1	READ MULTIPLE	E4h
1	READ SECTOR(S)	20h or 21h
1	READ VERIFY SECTOR(S)	40h or 41h
1	RECALIBRATE	1Xh
1	REQUEST SENSE	03h
1	SECURITY DISABLE PASSWORD	F6h
1	SECURITY ERASE PREPARE	F3h
1	SECURITY ERASE UNIT	F4h
1	SECURITY FREEZE LOCK	F5h
1	SECURITY SET PASSWORD	F1h
1	SECURITY UNLOCK	F2h
1	SEEK	7Xh
1	SET FEATURES	EFh
1	SET MULTIPLE MODE	C6h
1	SET SLEEP MODE	E6h or 99h
1	STAND BY	E2h or 96h
1	STAND BY IMMEDIATE	E0h or 94h
1	TRANSLATE SECTOR	87h
1	WEAR LEVEL	F5h

UNDER NDA FOR EASTECH

Table 23 CF-ATA Command Set (Continued)

Class	Command	Code
2	FORMAT TRACK	50h
2	WRITE BUFFER	E8h
2	WRITE SECTOR(S)	30h or 31h
2	WRITE LONG SECTOR	32h or 33h
2	WRITE SECTOR(S) W/O ERASE	38h
3	WRITE VERIFY	3Ch
3	WRITE MULTIPLE	C5h
3	WRITE MULTIPLE W/O ERASE	CDh

Memory Stick Interface

The ES8381 supports playback of digital media in the Memory Stick. This type of media can be applied to many types of devices, including but not limited to, MP3 players and digital still cameras.

More detailed Memory Stick specifications and information can be found at the Memory Stick Technical Support website at http://www.memorystick.org.

Memory Stick Addressing

The ES8381 supports cluster-style addressing when data is being stored to a Memory Stick device, which makes the data as accessible from the device as it would be from a hard disk drive.

System SRAM Interface

The system SRAM interface controls access to optional external SRAM which can be used for RISC code, stack, and data. The SRAM bus supports four independent address spaces, each having programmable bus width and wait states. The interface can support not only SRAM but also ROM/EPROM and memory-mapped I/O ports for standalone applications.

The signals for the SRAM bus are generated from the internal RISC clock and are timed in integer multiples of clock cycles, except for the write strobe, which is delayed by one-half cycle from the address setup and advanced one-half cycle from the start of the next access cycle.

The on-chip SRAM also allows the ESS RISC core to download subroutines for the video processor core. The ESS RISC core activates the video processor core by writing to the command queue, which selects a subroutine either from the external EPROM, flash memory or by the video memory interface.

Shared SRAM/SDRAM Access

The ES8381 servo includes hardware support for shared 8-bit SDRAM and SRAM access through its direct access to the host interface port.

Subcode Preprocessing

The 14-bit subcode status information is loaded prior to 8-by-14 modulation (EFM) in CD mode, and prior to 8-by-16 modulation (EFM+) in DVD mode.The CD/DVD DSP then performs error correction and data synchronization.

DRAM Memory Interface

The ES8381 provides a glueless 16-bit interface to DRAM memory devices used as video memory for a DVD player. The maximum amount of memory supported is 16 MB of Synchronous DRAM (DRAM). The memory interface is configurable in depth to support 128-Mb addressing.

The memory bus interface generates all the control signals to interface with external memory. The ES8381 supports different configurations using the memory configuration bits SDCFG[1:0] (bits 12:11), the SD8BIT bit (bit 14), and SD64M bit (bit 15) in the BUSCON_DRAM_CONTROL register. Configurations can be implemented in many ways. Table 24 lists the typical DRAM configurations used by the ES8381.

Table 24 Typical DRAM Configurations

Mem. Size (MB)	Bit Order				Memory Configuration (Mb per pc)
	SD64M	SD8BIT	SDCFG1	SDCFG0	
2	0	0	0	1	1 pc: 512Kx16x2 (16 Mb)
4	0	0	0	0	2 pcs: 512Kx16x2 (16 Mb)
4	0	1	0	1	2 pcs: 1Mx8x2 (16 Mb)
8	0	1	0	0	4 pcs: 1Mx8x2 (16 Mb)
8	1	0	X	X	1 pc: 1Mx16x4 (64 Mb)
16	1	0	X	X	2 pc: 1Mx16x4 (64 Mb)
16	1	1	X	X	2 pc: 2Mx8x4 (64 Mb)
16	1	1	X	X	1 pc: 2Mx16x4 (128 Mb)

The memory interface controls access to both external DRAM or EDO memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers.

At high clock speeds, the memory bus interface has sufficient bandwidth to support the decoding and displaying of CCIR656/601 resolution images at full frame rate.

DRAM Considerations

The ES8381 uses DRAM with a programmed CAS# latency of three clocks (CL = 3) and sequential burst of full page length. Performance based on DRAM is double that

UNDER NDA FOR EASTECH

of EDO. DRAM must be software configured before any memory access. The programmable DRAM refresh period can be modified to meet any desired configuration.

DRAM Address Mapping

The memory address (LA) is mapped to the DMA address, which is formed by ADDR in the BUSCON_DMA_ADDR registers. The result is then converted into the DRAM control signals using the SDCFG[1:0] configuration bits (bits 12:11) and the SD8BIT bit (bit 14) in the BUSCON_DMA_CONTROL register.

DRAM Configuration Requirements

Table 25 lists the DRAM memory size configurations, each with its corresponding signal pins.

Table 25 DRAM Configurations and Signal Pins

Size (MB)	DRAM 0	DRAM 1	DRAM2	DRAM3	Memory Type
2	DCAS# DRAS0# DCS0# DB[0:15]	—	—	—	512Kx16x2 (16 Mb)
4	DCAS# DRAS0# DCS0# DB[0:15]	DCAS# DRAS0# DCS1# DB[0:15]	—	—	512Kx16x2 (16 Mb)
4	DCAS# DRAS0# DCS0# DB[0:7]	DCAS# DRAS0# DCS# DB[8:15]	—	—	1Mx8x2 (16 Mb)
8	DCAS# DRAS0# DCS0# DB[0:7]	DCAS# DRAS0# DCS0# DB[8:15]	DCAS# DRAS0# DCS1# DB[0:7]	DCAS# DRAS0# DCS1# DB[8:15]	1Mx8x2 (16 Mb)
8	DCAS# DRAS0# DCS0# DB[0:15]	—	—	—	1Mx16x4 (64 Mb)
16	DCAS# DRAS0# DCS0# DB[0:15]	DCAS# DRAS0# DCS1# DB[0:15]	—	—	1Mx16x4 (64 Mb)
16	DCAS# DRAS0# DCS0# DB[0:7]	DCAS# DRAS0# DCS0# DB[8:15]	—	—	2Mx8x4 (64 Mb)
16	DCAS# DRAS0# DCS0# DB[0:15]	—	—	—	2Mx16x4 (128 Mb)

TDM Interface

The ES8381 implements a high-speed, bidirectional serial bus known as a TDM interface that supports a number of high-speed serial protocols. The TDM interface can also act as a general-purpose 16-Mbps serial link when not constrained by TDM protocols.

The TDM interface provides an easy connection between the ES8381 and available communications chips. The TDM interface is a time-division-multiplexed bus that multiplexes byte data on up to 64 channels. Time slot 0 starts after N (which can be set in the XMT/RCVDELAY register) clocks after the frame starts.

Each slot is eight clock periods long, and either transmits or receives byte data during a write cycle or a read cycle. Immediately after slot 0 completes, slot 1 starts and so on. Each channel is allocated a different time slot on the bus, and the ES8381 can be set to send and receive data in any combination of different time slots.

Data is assumed to be ordered by time slot; e.g., if time slots 6, 8, and 17 are used, the first DMA byte sent to memory would be in time slot 6, followed by time slots 8 and 17 in order. All DMA byte reordering is done in software. The interface consists of frame sync signal TDMFS, data receive signal TDMDR, and bit clock signal TDMCLK.

The timing of the data transfer is externally controlled. The TDM interface can support a number of different timings. The TDM interface can transfer data at a maximum rate of 16 Mbps, with a more typical configuration supporting a data rate of up to 4.096 Mbps with a frame sync frequency of 8 kHz. The TDM interface programmability includes independent receive, transmit, and frame sync clock edge selection and independent receive and transmit data offsets.

USB Host Controller

The ES8381 has two pins devoted to the USB host controller that supports the host channel: USB_P0 pin 122 and USB_N0 pin 123.

Data Encoding/Decoding and Transfer

The USB is a polled bus, which means the host controller initiates all data transfers. Most bus transactions involve the transmission of up to three packets, the token packet, the data packet and the handshake packet.

Token packets are typically sent at the beginning of a USB transaction so as to define the transfer type. The Data packets typically follow Token packets during transactions that require data payloads to be transferred between USB devices. The direction of data transfer is specified in the token packet. The source of the transaction then sends a data packet or indicates it has no data to transfer.

UNDER NDA FOR EASTECH

The destination, in general, responds with a handshake packet indicating whether the transfer was successful. Handshake packets usually return from the receiver to the sender, providing feedback indicating whether or not the data transfer was successful.

The USB employs Non-Return to Zero Inverted (NRZI) data encoding during packet transmission. In NRZI encoding, a 1 is represented by no change in level, while a zero is represented by a change in level.

Video Interface

Video Display Output

The video output section controls the transfer of video frames stored in memory to the internal TV encoder of the ES8381. The output section consists of a programmable CRT controller capable of operating either in Master or Slave mode. Figure 26 shows the display timing on the screen.

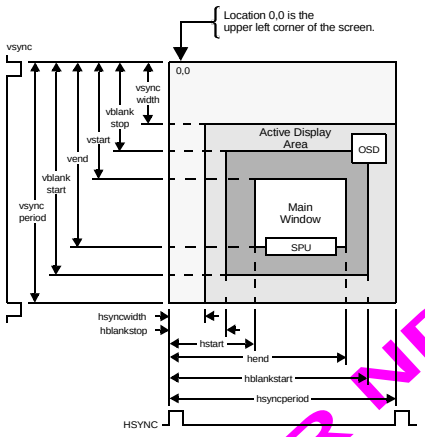


Figure 26 Video Output Timing

The video output section features internal line buffers that allow the outgoing luminance and chrominance data to match the internal clock rates with external pixel clock rates, easily facilitating YUV4:2:2 to YUV4:2:0 component and sample conversion. Arbitrary horizontal decimation and interpolation is achieved by a polyphase filter.

Together with programmable line dropping/duplication circuitry and micro-code based post-processing running on the video processor, the ES8381 is capable of arbitrating image conversion. Examples include SIF to CCIR656/601, letter-box, NTSC to PAL, and PAL to NTSC conversions.

Video Bus

The ES8381 video bus transfers digital video pixels out of the chip. In standalone applications the video bus will be connected to a monitor or an LCD panel. In workstation applications, the output bus will feed an overlay circuit so that the output video appears in a window of the Graphical User Interface (GUI).

The video bus has 8 YUV data pins that transfer luminance and chrominance (YUV) pixels in CCIR656/601 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance.

Safe Caption Area

The ES8381 draws the safe caption area required by FCC Part 15.119, as shown in Figure 27.

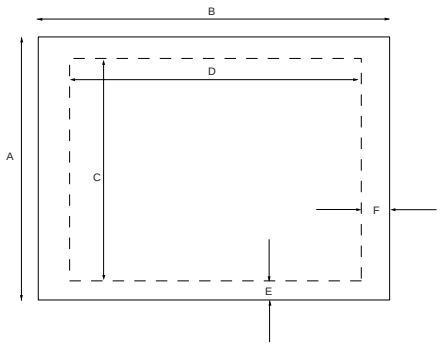


Figure 27 Safe Caption Area

The dimensions of the safe caption area are listed in Table 26.

Table 26 Safe Caption Area Dimensions

Label	Dimension	Percent of Picture Height
A	Television picture height	100.0
B	Television picture width	133.33
C	Height of safe caption area	80.0
D	Width of safe caption area	106.67
E	Vertical portion of safe caption area	10.0
F	Horizontal portion of safe caption area	13.33

UNDER NDA FOR ESS TECH

Video Post-Processing

The ES8381 video post-processing circuitry provides support for the color conversion, scaling, and filtering functions through a combination of special hardware and software. Horizontal up-sampling and filtering is done with a programmable, 7-tap polyphase filter bank for accurate non-integer interpolations. Vertical scaling is achieved by repeating and dropping lines in accordance with the applicable scaling ratio.

Figure 28 shows the video post-processing functional blocks. The first two processing steps are performed by the video processor core. Video post-processing can be applied on the decoded images to improve the picture quality.

The next stage in the processing, applicable only to low resolution MPEG-1 video, is an interlacing filter that generates even and odd fields from decoded frames for applications that use a TV screen. The filter improves both the spatial and temporal appearance of the decoded images on interlaced displays.

Figure 28 Video Post-Processing

Following the interlacing filter is an interpolation section that uses bilinear interpolation to increase the resolution of

UNDER NDA FOR EASTECH

SERVO CONTROLLER COMMAND SET

The command set for the servo controller of the ES8381 is listed in Table 28.

Table 28 ES8381 Servo Controller Command Set

Command Code	Command Name	Description
0x01	DSKTYPE	Identifies the type of optical disk media present in the loader.
0x02	WRDT	Writes data to servo controller RAM location.
0x03	WRAD	Writes address to servo controller RAM location. Used with WRDT for data writes.
0x04	RD	Read data from servo controller RAM location.
0x05	—	Reserved.
0x06	DMON	Start spindle in CAV (FG) mode.
0x07	DMOF	Stop spindle.
0x08	DMMODE	Set spindle operating mode. Used with DMON.
0x09	SETRPM	Set spindle speed for FG mode.
0x10 — 0x17	—	Reserved.
0x18	STON	Servo still on.
0x19	STOF	Servo still off.
0x1A — 0x1C	—	Reserved.
0x1D	RSEEKI	Short seek inward.
0x1E	RSEEKO	Short seek outward.
0x1F — 0x7F	—	Reserved.
0x80	C_DSKSRCH	Calibrate detect and discriminate disk.
0x81	C_FCON	Calibrate focus pull in.
0x82	C_FOJMP	Calibrate focus jump.
0x83	C_ADSFCIN	Calibrate focus balance adjust.
0x84	—	Reserved.
0x85	C_ADSTR	Calibrate tracking adjust.
0x86	C_TRON	Calibrate tracking pull in.
0x87	C_ADSFC	Calibrate tracking fine adjust.
0x88	C_FCOF	Tracking and Focus off.
0x89	C_TROF	Tracking off.
0x8A	—	Reserved.
0x8B	C_HALT	Allow RAM access.
0x8C — 0x8F	—	Reserved.
0x90	BDO	Black drop out.
0x91	—	Reserved.
0x92	C_ADDA	Calibrate channel address.
0x93	C_DLAY	Calibrate sled delay.
0x94	C_DDR	Calibrate derived and recorded values.
0x95	C_RST	Reset.
0x96	C_FOC_CHK	Calibrate focus pull in check.
0x97	F_WRDT	Write data to memory during playback.
0x98	F_WRAD	Write address to memory during playback. Used before F_WRDT.
0x99	G_WRDT	Write data to memory during focus on and tracking off.
0x9A	G_WRAD	Write address to memory during focus on and tracking off. Used before G_WRDT.
0x9B	F_ABC	Add loop gain to focus on and tracking off.
0x9C	T_ABC	Add loop gain to tracking on and focus off.
0x9D	RSEEKI	Long seek inward.
0x9E	RSEEKO	Long seek outward.

UNDER NDA FOR EASTECH

REGISTERS

The register address map for the ES8381 is presented in Table 29.

Table 29 ES8381 Register Address Map

Register Section	Address Range	Description
Servo Front End Registers	***0x0000 — 0x00FF***	
Servo DSP Registers	0x0000 — 0x001F	8051 Interface Registers
System Control Registers	0x0020 — 0x005F	ATAPI and System Interface Registers
		Spindle Configuration Registers
		Tracking Servo Registers
		Focus And Sled Servo Configuration Registers
Digital PLL And ECC Decoder Registers	0x0060 — 0x00FF	ECC DMA Controller Registers
		ECC DVD Mode Registers
		ECC VCD Mode Registers
Digital Servo Controller Registers	***0x010 — 0x3FF***	
Memory Interface Registers	0x010 — 0x0FF	RAM Core 0 Registers
	0x100 — 0x1FF	RAM Core 1 Registers
Internal Servo Registers	0x280 — 0x2FF	Spindle Registers
	0x300 — 0x37F	Tracking Servo Registers
	0x380 — 0x3FF	Focus Servo Registers
DVD Processor Back End Registers	***0x20001000 — 0x2000E0BC***	
System Control Registers	0x0 — 0x5	Host Interface Host Side Registers
Video Interface Registers	0x20001000 — 0x20001058	Video Output Registers
	0x20001100 — 0x2000117C	On-Screen Display Controller Registers
	0x20001300 — 0x200013D4	Digital Video Encoder Registers
	0x20001400 — 0x200014A4	HDMI Interface Registers
	0x20001600 — 0x20001760	Subpicture Unit Decoder Registers
	0x200017B0 — 0x200017D4	SPU Contrast Index Registers
	0x20001780 — 0x200017A4	SPU Color Index Registers
Host Interface Registers	0x20003000 — 0x20003028	Host Interface RISC Side Registers
	0x20004000 — 0x20004038	Host Interface RISC-SRAM Registers
	0x20005400 — 0x20005500	I²C Registers
	0x20005600 — 0x20005640	Secure Digital Card Registers
Bus Controller Registers	0x20008000 — 0x20008004	Bus Controller (Video Processor) Registers
	0x20008100 — 0x20008114	Bus Controller (Memory Controller) Registers
	0x20008200 — 0x2000C000	Bus Controller (Command Queue) Registers
PCI Registers	0x2000C400 — 0x2000C420	Configuration Registers
Audio Registers	0x2000D008 — 0x2000D018	Audio Interface Registers
	0x2000D01C — 0x2000D034	S/PDIF Output Interface Registers
	0x2000D080 — 0x2000D094	Audio ADC Registers
	0x2000E080 — 0x2000E0BC	S/PDIF Receiver Registers

UNDER NDA FOR ESS ECP

Servo DSP Registers

The registers for the servo controller section of the ES8381 are listed in this section.

8051 Interface Registers

System Control **(0x0000h)**
W **Default: N/A**

—	SODE SEL	—
7:2	1	0

Bit Definitions:

Bits	Name	Description
7:2	—	Reserved
1	SODE SEL	Single or Double Ended Configuration Select for PWM Outputs.
0	—	Reserved

Low Byte Status **(0x000h)**
R **Default: N/A**

IRQ	DLYR	DCKDN	CLVON	STON	TRON	FCON	DMON
15	14	13	12	11	10	9	8

FGNG	—	CLVNG	ATN	CC	ERR	RDY
7	6:5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	IRQ	Interrupt Status.
14	DLYR	Disk Layer: 1 = Layer 1 0 = Layer 0
13	DCKDN	Disk Check Done.
12	CLVON	CLV Mode Enable: 1 = Spindle motor is in CLV mode.
11	STON	Still On Condition Status: 1 = Still on
10	TRON	Tracking On Condition Status: 1 = Tracking on
9	FCON	Focus On Condition Status: 1 = Focus on.
8	DMON	Spindle Motor On Condition Status: 1 = Spindle motor on.
7	FGNG	FG Mode No Good Condition Status: When set, this bit indicates abnormal spindle speed while in FG mode. 1 = Abnormal spindle speed in FG mode.
6:5	—	Reserved
4	CLVNG	CLV Mode No Good Condition Status: When set, this bit indicates abnormal spindle speed while in CLV, 6T/18T or CD mode. 1 = Abnormal spindle speed in CLV, 6T/18T or CD mode.
3	ATN	Attention: When set, this bit indicates that the servo has detected an abnormal condition while no command is being processed. 1 = Abnormal condition present.
2	CC	Command Complete: When set, this bit indicated that the command has been completed. 1 = Command has been completed.
1	ERR	Error Detect: When set, this bit indicates that the servo has detected an abnormal condition. 1 = Abnormal condition detected.
0	RDY	Ready: When set, this bit indicates the servo is ready to execute the next command. 1 = Ready to execute next command.

Command **(0x0001h)**
W **Default: N/A**

COMCODE
7:0

The Command register stores the current command code.

Bit Definitions:

Bits	Name	Description
7:0	COM CODE	Command code value.

UNDER NDA FOR EASTECH

High Byte Status (0x0001h)
R **Default: N/A**

IRQ	DLYR	DCKDN	CLVON	STON	TRON	FCON	DMON
15	14	13	12	11	10	9	8

FGNG	—	CLVNG	ATN	CC	ERR	RDY
7	6:5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	IRQ	Interrupt Status.
14	DLYR	Disk Layer: 1 = Layer 1 0 = Layer 0
13	DCKDN	Disk Check Done.
12	CLVON	CLV Mode Enable: 1 = Spindle motor is in CLV mode.
11	STON	Still On Condition Status: 1 = Still on.
10	TRON	Tracking On Condition Status: 1 = Tracking on.
9	FCON	Focus On Condition Status: 1 = Focus on.
8	DMON	Spindle Motor On Condition Status: 1 = Spindle motor on.
7	FGNG	FG Mode No Good Condition Status: When set, this bit indicates abnormal spindle speed while in FG mode. 1 = Abnormal spindle speed in FG mode.
6:5	—	Reserved.
4	CLVNG	CLV Mode No Good Condition Status: When set, this bit indicates abnormal spindle speed while in CLV, 6T/18T or CD mode. 1 = Abnormal spindle speed in CLV, 6T/18T or CD mode.
3	ATN	Attention: When set, this bit indicates that the servo has detected an abnormal condition while no command is being processed. 1 = Abnormal condition present.
2	CC	Command Complete: When set, this bit indicated that the command has been completed. 1 = Command has been completed.
1	ERR	Error Detect: When set, this bit indicates that the servo has detected an abnormal condition. 1 = Abnormal condition detected.
0	RDY	Ready: When set, this bit indicates the servo is ready to execute the next command. 1 = Ready to execute next command.

Mode Control, Low Byte (0x0002h)
W **Default: N/A**

—	SERRCLR	—	CPU_FCLR
15:4	3	2:1	0

Bit Definitions:

Bits	Name	Description
15:4	—	Reserved
3	SERR CLR	Servo Error Clear: Writing 1 to this location clears the servo error flags.
2:1	—	Reserved
0	CPU_ FCLR	CPU Force Clear: Clears IRQ when 1 is written to this bit.

Servo Error Type (0x0002h)
R **Default: N/A**

—	SLED_ ERR	HI_RPM_ ERR	MIRROR _ERR	FHM_ FINAL	THM_ FINAL
7:5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:5	—	Reserved
4	SLED_ ERR	Sled hit its inner home switch.
3	HI_RPM_ ERR	High spindle speed detected.
2	MIRROR _ERR	Mirror detected.
1	FHM_ FINAL	Focus failure detected.
0	THM_ FINAL	Tracking failure detected.

Mode Control, High Byte (0x0003h)
W **Default: N/A**

—	SERRCLR	—	CPU_FCLR
15:4	3	2:1	0

Bit Definitions:

Bits	Name	Description
15:4	—	Reserved
3	SERR CLR	Servo Error Clear: Writing 1 to this location clears the servo error flags.
2:1	—	Reserved
0	CPU_ FCLR	CPU Force Clear: Clears IRQ when 1 is written to this bit.

UNDER NDA FOR EASTECH

Parameter Input, Low Byte (0x0004h)
W **Default: N/A**

PILB
15:0

Bit Definitions:

Bits	Name	Description
15:0	PILB	Low byte parameter input CPU data in.

Data Out, Low Byte (0x0004h)
R **Default: N/A**

DOLB
7:0

Bit Definitions:

Bits	Name	Description
7:0	DOLB	Low byte of data output.

Parameter Input, High Byte (0x0005h)
W **Default: N/A**

PIHB
15:0

Bit Definitions:

Bits	Name	Description
15:0	PIHB	High byte parameter input CPU data in.

Data Out, High Byte (0x0005h)
R **Default: N/A**

DOHB
7:0

Bit Definitions:

Bits	Name	Description
70	DOHB	High byte of data output.

RF AFE Address (0x0008h)
W **Default: N/A**

RFPA
31:0

Bit Definitions:

Bits	Name	Description
31:0	RFPA	RF AFE address.

RF AFE Control (0x0008h)
R **Default: N/A)**

SP_DIR	—	SR_TRANS_ON_RF	SLED_IN	TRAY_OPEN_SWITCH	TRAY_CLOSE_SWITCH	DRPOUT
7	6:5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	SP_DIR	Spindle direction (status of external pin).
6:5	—	Reserved
4	SR_TRANS_ON_RF	Serial transmission-on to RF preamp.
3	SLED_IN	Sled home switch status (external pin).
2	TRAY_OPEN_SWITCH	Tray open switch status (external pin).
1	TRAY_CLOSE_SWITCH	Tray close switch status (external pin).
0	DRPOUT	Dropout (defect handling status).

RF AFE Data (0x0009h)
W **Default: N/A**

RFPD
31:0

Bit Definitions:

Bits	Name	Description
31:0	RFPD	RF AFE data.

RF AFE Data (0x0009h)
R **Default: N/A**

RFPD
7:0

Bit Definitions:

Bits	Name	Description
7:0	RFPD	Data returned from RF AFE.

UNDER NDA FOR EASTECH

RF AFE Control (0x000Ah)
W **Default: N/A**

FL MC	PLLOK OUT	RAMMN TYPE	LDON	DVDCD SEL	PAMP ON	TOPN CMD	TCLS CMD
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	FLMC	Flexible Length Microcode: 1 = Allow 0 = Disallow
6	PLLOK OUT	PLL OK Out.
5	RAMMN TYP	RAM Monitor Type.
4	LDON	Laser Diode On/Off. Cleared upon reset.
3	DVDCD SEL	DVD/CD Select: 1 = DVD 0 = CD
2	PAMPON	Power Amplifier On/Off: 1 = Power amp on.
1	TOPN CMD	Tray Open Command: 1 = Tray open.
0	TCLS CMD	Tray Close Command: 1 = Tray close.

VOBS Low Byte (0x000Ch)
R **Default: N/A**

VOBSL
7:0

Bit Definitions:

Bits	Name	Description
7:0	VOBSL	Low byte of video object data returned from RAM monitor.

System Control Data (0x000Dh)
R **Default: N/A**

SCD
7:0

Bit Definitions:

Bits	Name	Description
7:0	SCD	Data returned from System Control register.

VOBS High Byte (0x000Eh)
R **Default: N/A**

VOBSH
7:0

Bit Definitions:

Bits	Name	Description
7:0	VOBSH	High byte of video object data returned from RAM monitor.

System Control Registers

ATAPI and System Interface Registers

This section describes the ATAPI and system interface registers of the ES8381.

SYSTST1_SEL 0x002Fh
W **Default: 00h)**

SYSTS1
7:0

Bit Definitions:

Bits	Name	Description
7:0	SYSTS1	Selects grouping of signals for chip test (write only).

MCUCLK_SET 0x0030h
R/W **Default: 000b)**

—	MCUCLKSPD
7:3	2:0

Bit Definitions:

Bits	Name	Description
7:3	—	Reserved.
2:0	MCU CLK SPD	MCU clock gating for ROM access: 000 = 27MHz 001 = 54MHz 010 = 81MHz 011 = 108MHz 100 = 135MHz 101 = 162MHz 11X = Reserved

UNDER NDA FOR EASTECH

DISK_INFO_DT **0x0031h**
R/W **Default: N/A**

—	SWPDATA	MTYPE
7:4	3	2:0

Bit Definitions:

Bits	Name	Description
7:4	—	Reserved.
3	SWP DATA	Data byte swapping control bit: 1: unswap
2:0	MTYPE	Disk media type setting: 000 = DVD mode 001 = VCD mode 100 = DVD-RAM mode 111 = CDDA mode

PULSE27GEN **0x0032h**
R/W **Default: N/A)**

PULSE27GEN
7:0

Bit Definitions:

Bits	Name	Description
7:0	PULSE27GEN	Divide by number for 27MHz pulse generation.

INTRQ_REASON **0x0033h**
R/W **Default: N/A**

HRST	FIFO	AVBM	PCMD	NPCMD	XDBM	ECCBLK	CRCOK
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	HRST	Host hardware reset interrupt
6	FIFO	ATAPI data transfer complete (data from 8051 to host).
5	AVBM	ATAPI data transfer complete (data from DRAM to host).
4	PCMD	ATAPI packet command reception interrupt.
3	NPCMD	ATAPI non-packet command reception interrupt.
2	XDBM	XDBM interrupt.
1	ECCBLK	ECC block interrupt request (DVD only) interrupt.
0	CRCOK	CRCOK interrupt.

INTRQ_CLEAR **0x0034h**
R/W **Default: N/A)**

Bit Definitions:

INTRQ_MSK **0x0035h**
R/W **Default: N/A)**

Bit Definitions:

UNDER NDA FOR EASTECH

MCU_DRAM_RW_RESET 0x0036h
W Default: N/A)

—	HOSTBUSSEL	RWRST
7:2	1	0

Bit Definitions:

Bits	Name	Description
7:2	—	Reserved
1	HOST BUS SEL	Write only. Host Bus Type Select: 1 = ATAPI 0 = AV Bus
0	RWRST	Read/Write Reset: 1 = MCU DMA interface read/write reset 0 = no reset

SECXFRDC_H 0x0037h
R Default: N/A

SECCNTRH
7:0

Bit Definitions:

Bits	Name	Description
7:0	SEC CNTRH	ATAPI sector transfer down counter, high byte (read only).

SECXFRDC_L 0x0038h
R Default: N/A

SECCNTRL
7:0

Bit Definitions:

Bits	Name	Description
7:0	SEC CNTRL	ATAPI sector transfer down counter, low byte (read only).

BLKXFRDC_H 0x0039h
R Default: N/A

BLKCNTRH
7:0

Bit Definitions:

Bits	Name	Description
7:0	BLK CNTRH	ATAPI block transfer down counter, high byte (read only).

BLKXFRDC_L 0x003Ah
R Default: N/A

BLKCNTRL
7:0

Bit Definitions:

Bits	Name	Description
7:0	BLK CNTRL	ATAPI block transfer down counter, low byte (read only).

MCUTSTDT 0x003Bh
W Default: N/A

MCUTSTDT
7:0

Bit Definitions:

Bits	Name	Description
7:0	MCU TSTDT	MCU's write data to test port.

SVO_TEST_SETUP 0x003Ch
W Default: N/A

GPIOSEL	ADCSEL	EMICLK SEL	SVO REGEN	TSMODE
7	6	5	4	3:0

Bit Definitions:

Bits	Name	Description
7	GPIO SEL	Select signal source to monitor at GPIO pins: 1 = signals from servo or MCU 0 = MCU interrupts
6	ADCSEL	RF ADC Select: 1 = internal ADC 0 = external ADC
5	EMICLK SEL	ECC clock select.
4	SVO REGEN	Servo register enable.

UNDER NDA FOR EASTECH

Bits	Name	Description
3:0	TS MODE	Test Servo Mode: 0000 = Normal mode 0010 = ECC Test 1 0011 = Reserved 0100 = ECC Test 2 0101 = Reserved 0110 = Servo Test 1 0111 = Reserved 1000 = MPEG Test 1001 = Reserved 1010 = Servo Test 2 1011 = Reserved 1100 = RF ADC Test 1101 = Reserved 1110 = Servo test 3 1111 = Reserved

DESCR_OFFSET_H 0x003Dh
W **Default: N/A**

DSCROFSTH
7:0

Bit Definitions:

Bits	Name	Description
7:0	DSCR OFSTH	Address for descrambling DVD data -high byte.

DESCR_OFFSET_L 0x003Eh
W **Default: N/A**

DSCROFSTL
7:0

Bit Definitions:

Bits	Name	Description
7:0	DSCR OFSTL	Address for descrambling DVD data - low byte.

TRSONCTL 0x003Fh
W **Default: N/A**

—	TRSONGCTL
7:1	0

Bit Definitions:

Bits	Name	Description
7:1	—	Reserved.
0	TRSON GCTL	TRSON control for CRCOK interrupt: 1 = gating on 0 = gating off

DRAMMCUCH_STATUS 0x0040h
R/W **Default: N/A**

—	DRAMMCUBSY
7:1	0

Bit Definitions:

Bits	Name	Description
7:1	—	Reserved.
0	DRAM MCU BSY	MCU DRAM channel read/write status: 1 = busy 0 = not busy

DRAMMCU_DATA 0x0041h
R/W **Default: N/A**

MCUDRAMDT
7:0

Bit Definitions:

Bits	Name	Description
7:0	MCU DRAM DT	MCU read/write data from/to DRAM.

AV_OFFSET_L 0x0042h
R/W **Default: N/A**

AVOFSTL
7:0

Bit Definitions:

Bits	Name	Description
7:0	AV OFSTL	AV offset low byte address.

AV_LAST_PAGE_L 0x0043h
R/W **Default: N/A**

AVLPGL
7:0

Bit Definitions:

Bits	Name	Description
7:0	AVLPGL	AV last page low byte.

UNDER NDA FOR EASTECH

AV_LAST_PAGE_H 0x0044h
R/W Default: N/A

—	AVLPGH
7:1	0

Bit Definitions:

Bits	Name	Description
7:1	—	Reserved
0	AVLPGH	AV last page high bit.

AV_START_PAGE_L 0x0045h
R/W Default: N/A

AVSPGL
7:0

Bit Definitions:

Bits	Name	Description
7:0	AVSPGL	AV start page low byte.

AV_START_PAGE_H 0x0046h
R/W Default: N/A

—	AVSPGHBit
7:1	0

Bit Definitions:

Bits	Name	Description
7:1	—	Reserved
0	AVSPGH Bit	AV start page high bit.

XD_OFST 0x0047h
R/W Default: N/A

XDOFST
7:0

Bit Definitions:

Bits	Name	Description
7:0	XDOFST	DRAM offset for XD mode.

AV_CPAG_H 0x0048h
R Default: N/A

—	AVCPH
7:1	0

Bit Definitions:

Bits	Name	Description
7:1	—	Reserved
0	AVCPH	AV current page high bit (read only).

AV_CPAG_L 0x0049h
R Default: N/A

AVCPL
7:0

Bit Definitions:

Bits	Name	Description
7:0	AVCPL	AV current page low byte (read only).

AV_OFFSET_H 0x004Ah
R/W Default: N/A

—	AVOFSTH
7:4	3:0

Bit Definitions:

Bits	Name	Description
7:4	—	Reserved
3:0	AV OFSTH	AV offset - high byte address.

DMA_DESTP 0x004Bh
W Default: N/A

DMA_DESTP
7:0

This register, in conjunction with the registers at addresses 003Dh and 003Eh, is used to specify the DMA descrambling destination address:

DMA descrambling destination address = {DMADP, DSCROFSTH, DSCROFSTL}.

Bit Definitions:

Bits	Name	Description
7:0	DMA_ DESTP	DMA Destination Page for DVD-RAM data descrambling (write only).

ATAPI_DT_FMCU 0x004Ch
W Default: N/A

ATAPIDTMCU
7:0

Bit Definitions:

Bits	Name	Description
7:0	ATAPIDT MCU	MCU data for host transfer (write only).

UNDER NDA FOR EASTECH

IDE_ERROR **0x004Dh**
W **Default: N/A**

AERR
7:0

Bit Definitions:

Bits	Name	Description
7:0	AERR	IDE error register (write only).

ATAPI_CMD_PACKET **0x004Fh**
R **Default: N/A**

APKT
7:0

Bit Definitions:

Bits	Name	Description
7:0	APKT	ATAPI command packet register (read only).

ATAPI_FIFO_STATUS **0x0050h**
R/W **Default: N/A**

AFIFO
7:0

Bit Definitions:

Bits	Name	Description
7:0	AFIFO	ATAPI FIFO status register.

ATAPI_AUTO_DATA_TRANSFER **0x0051h**
R/W **Default: N/A**

AADAT
7:0

Bit Definitions:

Bits	Name	Description
7:0	AADAT	ATAPI automatic data transfer setting register.

ATAPI_DATA_IO_CFG **0x0053h**
R/W **Default: N/A**

AIOCON
7:0

Bit Definitions:

Bits	Name	Description
7:0	AIOCON	ATAPI data I/O configuration register.

IDE_DEVICE_CTRL **0x0054h**
R **Default: N/A**

ADEVCTL
7:0

Bit Definitions:

Bits	Name	Description
7:0	ADEV CTL	IDE device control register (read only).

IDE_ALTERNATE_STATUS **0x0055h**
R **Default: N/A**

AASTA
7:0

Bit Definitions:

Bits	Name	Description
7:0	AASTA	IDE alternate status register (read only).

IDE_CMD **0x0056h**
R **Default: N/A**

ACMD
7:0

Bit Definitions:

Bits	Name	Description
7:0	ACMD	IDE command register.

IDE_STATUS **0x0057h**
W **Default: N/A**

ASTA
7:0

Bit Definitions:0x

Bits	Name	Description
7:0	ASTA	IDE status register.

IDE_DEVICE_HEAD **0x0058h**
R/W **Default: N/A**

ADVH
7:0

Bit Definitions:

Bits	Name	Description
7:0	ADVH	IDE device head register.

UNDER NDA FOR EASTECH

IDE_BYTE_COUNT_HIGH 0x0059h
R/W **Default: N/A**

ABCH
7:0

Bit Definitions:

Bits	Name	Description
7:0	ABCH	IDE byte count register, high byte.

IDE_BYTE_COUNT_LOW 0x005Ah
R/W **Default: N/A**

ABCL
7:0

Bit Definitions:

Bits	Name	Description
7:0	ABCL	IDE byte count register, low byte.

IDE_INTERRUPT_REASON 0x005Bh
R **Default: N/A**

AIRR
7:0

Bit Definitions:

Bits	Name	Description
7:0	AIRR	IDE interrupt reason register.

IDE_FEATURES 0x005Ch
R/W **Default: N/A**

AFEA
7:0

Bit Definitions:

Bits	Name	Description
7:0	AFEA	IDE features register.

GPIO_SELECT1 0x005Dh
W **Default: N/A**

AGPIOS1
7:0

Bit Definitions:

Bits	Name	Description
7:0	AGPIOS1	Test Mode GPIO Select Register 1 (write only).

GPIO_SELECT2 005Eh
W **Default: N/A**

AGPIOS2
7:0

Bit Definitions:

Bits	Name	Description
7:0	AGPIOS2	Test Mode GPIO Select Register 2 (write only).

Digital PLL And ECC Decoder Registers

ECC System Interface Registers

SYS_CONFIG 0x0080h
R/W **Default: N/A**

AFE_DDEN	FIR_EN	MEM_DLY_CFG	EMI_OUT_SEL	TST_PRB_SEL	8051_MEM_ACC_SEL	CB_IN_SEL
7	6	5	4	3:2	1	0

Bit Definitions:

Bits	Name	Description
7	AFE_DDEN	AFE Defect Detection Enable: 1 = enable 0 = disable
6	FIR_EN	FIR Enable: 1 = enable 0 = disable
5	MEM_DLY_CFG	Memory Clock Delay Configuration.
4	EMI_OUT_SEL	EMI Output Select: 1 = Select EMII output. 0 = Select test output.
3:2	TST_PRB_SEL	Test Probe Select: 00 = Probe set 0 (probe_adi) 01 = Probe set 1 (probe_ecc, probe_decd) 10 = Probe set 2 (probe_decc) 11 = Probe set 3 (probe_dma)
1	8051 MEM_ACCSEL	8051 Memory Access Select: 1 = 8051 memory access. 0 = Normal memory access.
0	CB_IN_SEL	Channel Bit Input Select: 1 = Select inserted test channel bit input. 0 = Select normal ADC channel bit input.

UNDER NDA FOR EASTECH

SYS_STATUS 0x0081h
R/W **Default: N/A**

—	DMA_ERR_STATUS
7:1	0

Bit Definitions:

Bits	Name	Description
7:1	—	Reserved
0	DMA_ERR_STATUS	DMA Error Status: 1 = error 0 = no error

FADC_CONFIG 0x0082h
R/W **Default: N/A**

FADC_FRQ_EST_BLK_DIS	FADC_FRC_DFCT	FADC_PWR_DN_ADC	ADI_DC_OUT_CFG	FADC_SLICE_THRESHOLD	—
7	6	5	4:3	2:1	0

Bit Definitions:

Bits	Name	Description
7	FADC_FRQ_EST_BLK_DIS	FADC Frequency Estimate Block Disable: 1 = disable 0 = enable
6	FADC_FRC_DFCT	FADC Force Defect: 1 = force defect 0 = no defect
5	FADC_PWR_DN_ADC	FADC Power Down ADC: 1 = Power down ADC. 0 = Normal ADC operation.
4:3	FADC_DC_OUT_CFG	FADC DC Output Configuration: 00 = delay 1 sample 01 = delay 2 samples 10 = delay 4 samples 11 = delay 8 samples
2:1	FADC_SLICE_THRESHOLD	FADC Slice Threshold: 00 = 0 01 = 4 10 = 8 11 = 16
0	—	Reserved

FADC_STATUS 0x0083h
R/W **Default: N/A**

—	FADC_PLL_EST_REQ
7:1	0

Bit Definitions:

Bits	Name	Description
7:1	—	Reserved
0	FADC_PLL_EST_REQ	FADC PLL Est Request: 1 = Est request 0 = No est request

DECD_CONFIG 0x0084h
R/W **Default: N/A**

DECD_INV_SYNC_TH_SCALE	DECD_PSYNC_TH_SCALE	DECD_ROUND_THRESHOLD	DECD_TEST_PROBE_SEL
7:6	5:4	3:2	1:0

Bit Definitions:

Bits	Name	Description
7:6	DECD_INV_SYNC_TH_SCALE	DECD Invalid Sync Threshold Scale: 00 = no shift 01 = shift 1 bit 10 = shift 2 bit 11 = shift 3 bit
5:4	DECD_PSYNC_TH_SCALE	DECD Pseudo-Sync Threshold Scale: 00 = no shift 01 = shift 1 bit 10 = shift 2 bit 11 = shift 3 bit
3:2	DECD_ROUND_THRESHOLD	DECD Round Threshold: 00 = 12 half row 01 = 14 half row 10 = 16 half row 11 = 18 half row
1:0	DECD_TEST_PROBE_SEL	DECD Test Probe Select: 00 = Select test probe set 0. 01 = Select test probe set 1. 10 = Select test probe set 2. 11 = Select test probe set 3.

UNDER NDA FOR EASTECH

DECD_STATUS
R/W **0x0085h**
Default: N/A

DECD_INV_SYNC_TH	DECD_PSD_SYNC_TH	DECD_FIFO_OVER_RUN	DFF_UNDER_RUN
7:5	4:2	1	0

Bit Definitions:

Bits	Name	Description
7:5	DECD_INV_SYNC_TH	Invalid sync count threshold.
4:2	DECD_PSD_SYNC_TH	Pseudo sync count threshold.
1	DECD_FIFO_OVER_RUN	DECD FIFO Overrun Status: 1 = FIFO overrun occurred. 0 = FIFO normal.
0	DFF_UNDER_RUN	DECD FIFO Underrun Status: 1 = FIFO underrun occurred. 0 = FIFO normal.

EMI_CONFIG
R/W **0x0086h**
Default: N/A

—	EMI_INPUT_SEL
7:2	1:0

Bit Definitions:

Bits	Name	Description
7:2	—	Reserved
1:0	EMI_INPUT_SEL	EMI Input Select: 00 = Select run length error data. 01 = Select channel bit serial data. 10 = Select channel bit parallel data. 11 = Select spindle data.

MEM_ADDR_L
R/W **0x0088h**
Default: N/A

MEM_ADDR_L
15:0

Bit Definitions:

Bits	Name	Description
15:0	MEM_ADDR_L	Memory address, low byte.

MEM_ADDR_H
R/W **0x0089h**
Default: N/A

MEM_ADDR_H
15:0

Bit Definitions:

Bits	Name	Description
15:0	MEM_ADDR_H	Memory address, high byte.

MEM_ROM_DATA
R/W **0x008Ah**
Default: N/A

MEM_ROM_DATA
7:0

Bit Definitions:

Bits	Name	Description
7:0	MEM_ROM_DATA	Memory ROM Data: Valid when sys_config_reg[1] = 1. Read: Write 2 memory address bytes, read one rom data byte.

MEM_ROW_DATA
R/W **0x008Bh**
Default: N/A

MEM_ROW_DATA
7:0

Bit Definitions:

Bits	Name	Description
7:0	MEM_ROW_DATA	MEM Row Data: Valid when sys_config_reg[1] = 1. **Write: Write 2 memory address bytes, write one row data byte.** **Read: Write 2 memory address bytes, read one row data byte.**

UNDER NDA FOR EASTECH

MEM_COLUMN_]DATA_BYTE[3:0] **0x008Ch —0x00 8Fh**
R/W **Default: N/A**

MEM_COLUMN_DATA
31:0

Bit Definitions:

Bits	Name	Description
31:0	MEM_COLUMN_DATA	Memory Column Data Byte [3:0]: Valid if sys_config_reg[1] = 1. **Write: Write 2 memory address bytes, write 4 column data byes, bytes 3:0.** **Read: Write 2 memory address bytes, read 4 column data bytes, bytes 3:0.**

ECC DMA Controller Registers

MODE_SELECT **0x0090h**
R/W **Default: N/A**

—	SYS_SOFT_RESET	—	MODE_CB2	—	DISK_MODE
7	6	5	4	3	2:0

Bit Definitions:

Bits	Name	Description
7	—	Reserved
6	SYS_SOFT_RESET	System Soft Reset: The hardware will clear this bit once the reset is done. 1 = Set by 8051 to reset all RC/ECC hardware logic. 0 = Normal operation.
5	—	Reserved
4	MODE_CB2	Memory Channel Width Select: 1 = 2-bit channel bit stream selected. 0 = 1-bit channel bit stream selected.
3	—	Reserved
2:0	DISK_MODE	Disk Mode: Indicates what type of disk needs to be decoded. All other combinations are reserved. 000 = DVD mode 001 = VCD mode 100 = DVD-RAM mode 111 = CD-DA mode

DMA_REQ_LEVEL_DLY_CTRL **0x0092h**
R/W **Default: N/A**

DMA_REQ_LEVEL_ADJ_DLY
7:0

Bit Definitions:

Bits	Name	Description
7:0	DMA_REQ_LEVEL_ADJ_DLY	DMA Request Level Adjustment Delay Control: 00 = No adjustment. The base DMA request level is programmed by the software and passed to the DMA controller as is. Other values: The base DMA request level is programmed by the software and it will be adjusted up one level every time. The dma_req_level_adj_delay time is expired until the highest DMA request level is reached. Each incremental value in the dma_req_level_adj_delay represents about 200ns of time. This register affects only the DMA channel used for row buffer write.

XDBM_START_ADDR_BYTE[2:0] **0x0093h — 0x0095h**
R/W **Default: N/A**

XDBM_START_ADDR_BYTEx
23:0

Bit Definitions:

Bits	Name	Description
23:0	XDBM_START_ADDR_BYTEx	XDBM Start Address byte 2:0: This address is used by the ECC logic as the base address of its DMA operation. The actual DMA address generated by the ECC logic is the sum of the XDBM Start Address and a 17-bit Dword DMA offset.

FIR_DATA **0x009Bh**
R/W **Default: N/A**

FIR_DATA
7:0

Bit Definitions:

Bits	Name	Description
7:0	FIR_DATA	FIR Data: The FIR data register is used for programming the coefficients in the equalizer, and is addressed indirectly through the Memory Address Low Byte register. To access the coefficient registers, write an address to the Memory Address Low Byte register, and then write or read to the FIR Data register.

UNDER NDA FOR EASTECH

DVD_ROW_COUNT_STATUS0 0x00A8h
R/W **Default: N/A**

DVD_UNCORR_ROW_CNT	DVD_UNRELIABLE_ROW_CNT
7:4	3:0

Bit Definitions:

Bits	Name	Description
7:4	DVD_UNCORR_ROW_CNT	DVD Uncorrectable Row Count: Status is per sector.
3:0	DVD_UNRELIABLE_ROW_CNT	DVD Unreliable Row Count: Status is per sector.

DVD_ROW_COUNT_STATUS1 0x00A9h
R/W **Default: N/A**

—	DVD_SKIP_ROW_CNT
7:4	3:0

Bit Definitions:

Bits	Name	Description
7:4	—	Reserved
3:0	DVD_SKIP_ROW_CNT	DVD Skip Row Count: Status is per sector.

DVD_ROW_ERR_BYTE_CNT 0x00AAh
R/W **Default: N/A**

—	DVD_ROW_ERR_BYTE_CNT
7:6	5:0

Bit Definitions:

Bits	Name	Description
7:6	—	Reserved
5:0	DVD_ROW_ERR_BYTE_CNT	DVD Row Error Byte Count: Total error byte count corrected by row per sector.

DVD_XD_START_PAGE 0x00B0h
R/W **Default: N/A**

—	DVD_XD_START_PAGE
7:5	4:0

The DVD_XD_Start_Page is used by the 8051 to inform the RC/ECC which DVD page in the rate buffer is the first page to which data should first be written. This register should be loaded before setting the NEW_SEARCH_START bit (bit 1) in the DVD RC Control register.

Bit Definitions:

Bits	Name	Description
7:5	—	Reserved
4:0	DVD_XD_START_PAGE	DVD XD Start Page Index: This field is set by the 8051 before initiating a target sector search.

DVD_XD_END_PAGE 0x00B1h
R/W **Default: N/A**

—	DVD_XD_END_PAGE
7:5	4:0

The DVD XD End Page register is used for 8051 to inform the RC/ECC which DVD page in the rate buffer is the last available page. This register should be loaded before setting the NEW_SEARCH_START bit (bit 1) in the DVD RC Control register, and updated as new pages become available. The RC/ECC uses this register to decide when the buffer is full and when to stop the XDBM process.

Bit Definitions:

Bits	Name	Description
7:5	—	Reserved
4:0	DVD_XD_END_PAGE	DVD XD End Page Index: This field is set by the 8051 before initiating a target sector search, and updated when new pages become available.

DVD_XD_CURRENT_PAGE 0x00B2h
R/W **Default: N/A**

—	DVD_XD_CURRENT_PAGE
7:5	4:0

Bit Definitions:

Bits	Name	Description
7:5	—	Reserved
4:0	DVD_XD_CURRENT_PAGE	DVD XD Current Page Index: This field is set by RC/ECC when it starts processing a new page.

UNDER NDA FOR EASTECH

DVD_XD_LATEST_AVAILABLE_PAGE 0x00B3h
R/W **Default: N/A**

—	DVD_XD_LATEST_AVAILABLE_PAGE
7:5	4:0

Bit Definitions:

Bits	Name	Description
7:5	—	Reserved
4:0	DVD_XD_LATEST_AVAILABLE_PAGE	DVD XD Latest Available Page Index: This field is set by RC/ECC and points to the latest available ECC block in the rate buffer.

DVD_XD_WRAP_AROUND_PAGE_CONFIG 0x00B4h
R/W **Default: N/A**

—	DVD_XD_WRAP_AROUND_PAGE_CONFIG
7:5	4:0

The DVD XD Wrap Around Page Configuration register is used by the 8051 to inform the RC/ECC at which DVD page in the rate buffer the ECC DMA should wrap around. The wrap around is always to page 0. This field should be loaded before setting the new_search_start bit (bit 1) in the DVD RC Control register.

Bit Definitions:

Bits	Name	Description
7:5	—	Reserved
4:0	DVD_XD_WRAP_AROUND_PAGE_CONFIG	DVD XD Wrap Around Page Configuration: This field is set by the 8051 before initiating a target sector search.

DVD_LATEST_BLOCK_CRC_STATUS_L 0x00B6h
R/W **Default: N/A**

DVD_LATEST_BLOCK_CRC_STATUS_L
15:0

Bit Definitions:

Bits	Name	Description
15:0	DVD_LATEST_BLOCK_CRC_STATUS_L	DVD Latest Block CRC Status, low byte: CRC Status for sectors within the latest available ECC block, Sector 15 - 0 CRC status. (one bit per sector). 1 = CRC error. 0 = CRC ok.

DVD_LATEST_BLOCK_CRC_STATUS_H 0x00B7h
R/W **Default: N/A**

DVD_LATEST_BLOCK_CRC_STATUS_H
15:0

Bit Definitions:

Bits	Name	Description
15:0	DVD_LATEST_BLOCK_CRC_STATUS_H	DVD Latest Block CRC Status, high byte: CRC Status for sectors within the latest available ECC block, Sector 15 - 0 CRC status. (one bit per sector). 1 = CRC error 0 = CRC ok

DVD_CURRENT_SECTOR_NUMBER_BYTE [3:0] 0x00B8h—0x00BBh
R/W **Default: N/A**

DVD_CURRENT_SECTOR_NUMBER_BYTEx
31:0

The DVD Current Sector Number Bytes 3:0 registers indicate the sector number for which the RC/ECC just finished the IED check, right before the CRCOK interrupt.

Bit Definitions:

Bits	Name	Description
31:0	DVD_CURRENT_SECTOR_NUMBER_BYTEx	DVD Current Sector Number Byte 3:0: Indicates the Current Sector Number. These registers are set to the current sector number only if the IED checksum is correct.

DVD_ECC_ERASURE_CONFIG 0x00BCh
R/W **Default: N/A**

—	MAX_DEG_ERASURE_NUM_RECORD	ERASURE_LIST_SEL
7:5	4:2	1:0

Bit Definitions:

Bits	Name	Description
7:5	—	Reserved
4:2	MAX_DEG_ERASURE_NUM_RECORD	Max Degree for Erasure Number Recording: 000 = 9 111 = 16

UNDER NDA FOR EASTECH

Bits	Name	Description
1:0	ERASURE_LIST_SEL	Selection to store erasure list: 00 = Record skip row(s) only. 01 = Record skip rows(s), uncorrectable row(s). 10 = Record skip rows(s), uncorrectable row(s) and row(s) with 5 bytes errors.

DVD_ECC_CTRL 0x00BDh
R/W **Default: N/A**

—	EARLY_TERM_COL_TIME	—	ECC_TEST
7:6	5:2	1	0

Bit Definitions:

Bits	Name	Description
7:6	—	Reserved
5:2	EARLY_TERM_COL_TIME	Early Termination Column Operation Time for Previous Page.
1	—	Reserved
0	ECC_TEST	ECC Test Mode

DVD_ECC_STATUS 0x00BEh
R/W **Default: N/A**

—	COL_DECD_FAIL	COL_TERM_PREM	ROW_BUF_OVERRUN	SKIP_ROWS_XCD_MAX_ALLOW	ERASE_NUM_XCD_MAX_ALLOW
7:5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:5	—	Reserved
4	COL_DECD_FAIL	Column Decode Fail.
3	COL_TERM_PREM	Premature Column Termination.
2	ROW_BUF_OVERRUN	Row Buffer Overrun.
1	SKIP_ROWS_XCD_MAX_ALLOW	Skip Rows Exceed Maximum Allowed.
0	ERASE_NUM_XCD_MAX_ALLOW	Erasure Number Exceed Maximum Allowed.

DVD_ECC_CHANNEL_REQ_CONFIG 0x00BFh
R/W **Default: N/A**

—	RW_CH_REQ_CONFIG	COL_CH_REQ-CONFIG
7:4	3:2	1:0

Bit Definitions:

Bits	Name	Description
7:4	—	Reserved
3:2	RW_CH_REQ_CONFIG	ECC row data DMA write channel request level configuration: 00 = No request 01 = Request level 1 10 = Request level 2 11 = Request level 3
1:0	COL_CH_REQ CONFIG	ECC Column data DMA read/write channel request level configuration: 00 = No request 01 = Request level 1 10 = Request level 2 11 = Request level 3

ECC VCD Mode Registers

VCD_RC_CTRL 0x00C0h
R/W **Default: N/A**

VCD_XD_END_PAGE_NEW	LEAD_IN_ENABLE	—	RC_ECC_ERROR_CONFIG	NEW_SEARCH_START	XD_ABORT_RESET
7	6	5:4	3:2	1	0

The VCD RC Control register is used by the 8051 to control the interface features of the RC/ECC hardware.

Bit Definitions:

Bits	Name	Description
7	VCD_XD END_PAGE_NEW	VCD XD End Page New: This bit indicates the value of VCD XD End Page Index when it has first been set, and after the 8051 has changed the value of the VCD_XD_End_Page_Index bit. This bit is reset by the hardware after the new value has been picked up.

UNDER NDA FOR EASTECH

Bits	Name	Description
6	LEAD_IN_ENABLE	Lead in Enable: 1 = Enable, search and match MIN:SEC:FRAME. 0 = Disable, search and match AMIN:ASEC:AFRAME.
5:4	—	Reserved
3:2	RC_ECC ERROR_CONFIG	RC/ECC Error Configuration: Indicates the condition that the RC_ECC_ERROR status bit in VCD RC Status register should be set. 00 = 8 consecutive sector ID errors detected. 01 = 16 consecutive sector ID errors detected. 10 = 24 consecutive sector ID errors detected. 11 = 32 consecutive sector ID errors detected.
1	NEW_SEARCH_START	New Search Start: When set, this bit starts searching for a new target sector and writes data to the rate buffer starting at XD Start Page. 1 = Set by 8051 only when new_search_start = 0. 0 = Reset by hardware once the current XDBM process is finished.
0	XD_ABORT_RESET	XD Abort/Reset: Hardware will clear this bit once the reset is done. 1 = Set by 8051 to reset ECC hardware to abort the XDBM process. This bit will not reset RC. 0 = Normal operation.

VCD_RC_STATUS 0x00C1h

R/W **Default: N/A**

ECC_METRIC_SEL	—	XD_DONE	RC_ECC_ERROR
7:5	4:2	1	0

The VCD RC Status register is used by the RC/ECC hardware to indicate to the 8051 the current state of the XDBM process.

Bit Definitions:

Bits	Name	Description
7:5	ECC_METRIC SEL	ECC_Metric_Select: 000 = Number of bytes uncorrectable by both C1 and C2. For audio CD, this is also related to the number of interpolations done. 001 = Number of erased C1 vectors. 010 = Number of bytes corrected by C1. 011 = Number of erased C2 vectors. 100 = Number of bytes corrected by C2.
4:2	—	Reserved
1	XD_DONE	XD Process Done: When set, this bit indicates the requested rate buffer transfer is done. 1 = Set by hardware when XD End Page is reached. 0 = Reset by 8051.
0	RC_ECC_ERROR	RC/ECC Error: 1 = RC/ECC has a fatal error which is defined by the RC_ECC_ERROR_CONDITION_CONFIG bits in the VCD RC Control register. 0 = RC/ECC normal.

VCD_ECC_METRIC_STATUS 0x00C5h

R/W **Default: N/A**

ECC_METRIC_STATUS
7:0

Bit Definitions:

Bits	Name	Description
7:0	ECC_METRIC STATUS	ECC Metric Status.

VCD_TARGET_SECTOR_NUMBER_BYTE[2:0] 0x00D0h—0x00D2h

R/W **Default: N/A**

VCD_TARGET_SECTOR_NUMBER_BYTEx
23:0

The VCD Target Number Byte [2:0] registers are used to communicate to the RC/ECC where the next search should take place. They should be loaded before setting the NEW_SEARCH_START bit (bit 1) in the VCD RC Control register. These registers indicates to the RC/ECC which sector and onward to start writing into the rate buffer, starting at the VCD XD Start Page register.

Bit Definitions:

Bits	Name	Description
23:0	VCD_TARGET SECTOR NUMBER_BYTEx	VCD Target Sector Number Byte2:0: VCD target sector number [23:16, 15:8, 7:0].

UNDER NDA FOR EASTECH

VCD_XD_START_PAGE **0x00D4h**
R/W **Default: N/A**

VCD_XD_START_PAGE
7:0

The VCD_XD_Start_Page is used by the 8051 to inform the RC/ECC which VCD page in the rate buffer is the first page to which data should first be written. This register should be loaded before setting the NEW_SEARCH_START bit (bit 1) in the VCD RC Control register.

Bit Definitions:

Bits	Name	Description
7:0	VCD_XD START_ PAGE	VCD XD Start Page Index: This field is set by the 8051 before initiating a target sector search.

VCD_XD_END_PAGE **0x00D5h**
R/W **Default: N/A**

VCD_XD_END_PAGE
7:0

The VCD XD End Page register is used for 8051 to inform the RC/ECC which VCD page in the rate buffer is the last available page. This register should be loaded before setting the NEW_SEARCH_START bit (bit 1) in the VCD RC Control register, and updated as new pages become available. The RC/ECC uses this register to decide when the buffer is full and when to stop the XDBM process.

Bit Definitions:

Bits	Name	Description
7:0	VCD_XD _END_ PAGE	VCD XD End Page Index: This field is set by the 8051 before initiating a target sector search, and updated when new pages become available.

VCD_XD_LATEST_ AVAILABLE_PAGE **0x00D6h**
R/W **Default: N/A**

VCD_XD_LATEST_AVAILABLE_PAGE
7:0

Bit Definitions:

Bits	Name	Description
7:0	VCD_XD _LATEST AVAIL ABLE_ PAGE	VCD XD Latest Available Page Index: This field is set by RC/ECC and points to the latest available ECC block in the rate buffer.

VCD_XD_WRAP_ AROUND_PAGE_CONFIG **0x00D7h**
R/W **Default: N/A**

VCD_XD_WRAP_AROUND_PAGE_CONFIG
7:0

The VCD XD Wrap Around Page Configuration register is used by the 8051 to inform the RC/ECC at which VCD page in the rate buffer the ECC DMA should wrap around. The wrap around is always to page 0. This field should be loaded before setting the new_search_start bit (bit 1) in the VCD RC Control register.

Bit Definitions:

Bits	Name	Description
7:0	VCD_XD _WRAP_ AROUND _PAGE_ CONFIG	VCD XD Wrap Around Page Configuration: This field is set by the 8051 before initiating a target sector search.

VCD_XD_LATEST_ AVAILABLE_HEADER_BYTE[3:0] **0x00D8h —0x00DBh**
R/W **Default: N/A**

VCD_XD_LATEST_AVAILABLE_HEADER_BYTEx
31:0

The VCD Latest Available Header register is used by RC/ECC to indicate to the 8051 the VCD Header information from the latest available sector that finished processing right before the XDBM interrupt is generated.

Bit Definitions:

Bits	Name	Description
31:0	VCD_XD _LATEST AVAIL ABLE_ HEADER _BYTEx	VCD XD Latest Available Header Bytes 3:0: Indicates the header data for the latest page. Set by RC/ECC before XDBM interrupt.

UNDER NDA FOR EASTECH

VCD_XD_LATEST_AVAILABLE_SUBHEADER_BYTE[3:0] 0x00DCh—0x00DFh
R/W **Default: N/A**

VCD_XD_LATEST_AVAILABLE_SUBHEADER_BYTEx
31:0

Bit Definitions:

Bits	Name	Description
31:0	VCD_XD_LATEST_AVAILABLE_SUBHEADER_BYTEx	VCD XD Latest Available Subheader Bytes 3:0: Indicates the subheader data for the latest page. Set by RC/ECC before XDBM interrupt.

VCD_LATEST_SECTOR_CRC_STATUS 0x00E0h
R/W **Default: N/A**

SUBQ_CRC_STATUS	VCD_CRC_STATUS	VCD_SUBHEADER MISMATCH	—	CD_INTERPOLATION_INDICATOR
7	6	5	4:1	0

VCD_Latest_Sector_CRC_Status_Register indicates the CRC status for both the subQ channel and the VCD sector. The subQ status corresponds to the subQ CRC check completed just before the CRCOK interrupt was generated. The VCD sector corresponds to the most recently available sector that finished right before the XDBM interrupt was generated.

Bit Definitions:

Bits	Name	Description
7	SUBQ_CRC_STATUS	SubQ CRC status for latest subQ sector: 1 = CRC error 0 = CRC ok
6	VCD_CRC_STATUS	VCD CRC Status for Latest Available VCD sector: 1 = CRC error 0 = CRC ok
5	VCD_SUBHEADER MISMATCH	VCD Subheader Mismatch: 1 = First 4 bytes does not match second 4 bytes. 0 = First 4 bytes match second 4 bytes.
4:1	—	Reserved
0	CD_INTERPOLATION_INDICATOR	CD Interpolation Indicator: 1 = interpolation 0 = no interpolation

VCD_RESYNC_PROTECT_WINDOW 0x00E1h
R/W **Default: N/A**

VCD_PROTECTION_WINDOW	VCD_RESYNC_LIMIT
7:4	3:0

Bit Definitions:

Bits	Name	Description
7:4	VCD_PROTECTION_WINDOW	VCD Protection Window.
3:0	VCD_RESYNC_LIMIT	VCD Resync Limit.

VCD_CURRENT_SECTOR_NUMBER_BYTE[2:0] 0x00E4h—0x00E6h
R/W **Default: N/A**

VCD_CURRENT_SECTOR_NUMBER_BYTEx
23:0

The VCD Current Sector Number Byte 2:0 registers indicates the sector number for which the RC/ECC just finished the subQ CRC check, right before the CRCOK interrupt.

Bit Definitions:

Bits	Name	Description
23:0	VCD_CURRENT_SECTOR NUMBER_BYTEx	VCD Current Sector Number Bytes 2:0. Load with current sector number from subQ channel only if subQ checksum is correct.

VCD_SUBQ_DATA_BYTE[9:0] 0x00F0h—0x00F9h
R/W **Default: N/A**

VCD_SUBQ_DATA_BYTEx
79:0

The VCD SubQ Data Byte 9:0 registers are used by the 8051 to retrieve the entire subQ frame.

Bit Definitions:

Bits	Name	Description
79:0	VCD_SUBQ_DATA_BYTEx	VCD SubQ Data Bytes 9:0.

UNDER NDA FOR EASTECH

VCD_MAX_ERASURE_CONTROL **0x00FCh**
R/W **Default: N/A**

MAX_ERAS_ ALLOW_ ENABLE	C1_MAX_ ERAS_ALLOW	C1_ERAS_ DEG_CTRL	C2_MAX_ ERAS_ALLOW	CD_INTER POLATION_ON
7	6:5	4	3:1	0

The VCD Max Erasure Control register is used to limit the number of erasures fed to the C1 Reed-Solomon decoder.

Bit Definitions:

Bits	Name	Description
7	MAX_ ERAS_ ALLOW_ ENABLE	Max Erasure Allow Enable: To enable the logic to perform limitation on the number of erasures fed to the module of Berlekamp-Massey inside of C1 RS decoder. 1 = enabled 0 = disabled
6:5	C1_MAX ERAS_ ALLOW	C1 Max Erasure Allow: This field allows the user to set the desired C1 maximum number of erasures fed to the Berlekamp-Massey module inside the C1 R-S decoder. 00 = 0 01 = 1 10 = 2 11 = 3
4	C1_ ERAS_ DEG_ CTRL	C1 Erasure Degree Control: When set, this bit indicates the availability for C1 to decode based on the combination of the number of erasures and the number of degrees coming out of the Berlekamp-Massey module. This bit controls the A/F portion in the following chart. 1 = fail 0 = available
3:1	C2_MAX ERAS_	

	0 Eras	**1 Eras**	**2 Eras**	**3 Eras**	**4 Eras**	**5 Eras**
0°	A	NA	NA	NA	NA	F
1°	A	A	NA	NA	NA	F
2°	A/F	A	A	NA	NA	F
3°	F	F	A/F	A	NA	F
4°	F	F	F	F	A/F	F

A: available
NA: Not available
F: C1 Fail
A/F: Fail in C1, available in C2

VCD_ECC_CHANNEL_ REQUEST_CONFIG **0x00FFh**
R/W **Default: N/A**

Bit Definitions:

UNDER NDA FOR EASTECH

Digital Servo Controller Registers

RAM Core [1:0] Registers

The registers for RAM Cores 0 and 1 are presented in Table 30 and Table 31. Some addresses are either unused or for internal use only, and have been omitted from this section.

Table 30 RAM Core 0 Registers

Address	Description
0x010 to 0x01C	Reserved
0x01D	Cross correlator gain
0x021	TRD tracking offset (TRD_OFFSET)
0x023 to 0x024	Reserved
0x025	TRV tracking offset (TRV_OFFSET)
0x027 to 0x02A	Reserved
0x02B	FOC_H_HD
0x02C	FOC_Ki1_HD
0x02D	FOC_B_HD
0x02E	FOC_C_HD
0x02F	FOC_E_HD
0x030	Constant: set to 0
0x031	TRK12B_HD
0x032	TRK134_HD
0x033	TRK138_HD
0x034	TRK139_HD
0x035	TRK13A_HD
0x036	TRK13C_HD
0x037	FOC_H_HA
0x038	FOC_Ki1_HA
0x039	FOC_B_HA
0x03A	FOC_C_HA
0x03B	FOC_E_HA
0x03C	TRK12B_HA
0x03D	TRK134_HA
0x03E	TRK138_HA
0x03F	TRK139_HA
0x040	TRK13A_HA
0x041	Reserved.
0x042	TRK13C_HA
0x053 to 0x074	Reserved
0x075	Negative of Playback focus filter gain H (M_H_HAT_PB)
0x076	FOC_H_SK
0x077	FOC_H_BD

Table 30 RAM Core 0 Registers (Continued)

Address	Description
0x078	FOC_H_BA
0x079	Reserved
0x087	Seek sled filter (SEK087)
0x08F	Reserved
0x091	Focus balance start value (0xFF32)
0x092	FOC_B_PB
0x093	FOC_C_PB
0x094	Negative of playback focus gain D.
0x095	Negative of playback focus gain E.
0x096	FOD_BIAS in Focus Filter, (0xFEFE) for Normal operation.
0x097	FBAL_DELTA: Focus balance search delta, (0x0030).
0x098	TBAL_DELTA: Tracking balance search delta, 0x0020.
0x09A	FOC_B_SK
0x09B	FOC_C_SK
0x09D	FOC_E_ SK
0x0A0 to 0x0A5	Reserved
0x0A6	TRK12B_SH
0x0A7	TRK134_SH
0x0A8	TRK138_SH
0x0A9	TRK139_SH
0x0AA	TRK13A_SH
0x0AB	TRK13C_SH
0x0AC	FOC_H_SH
0x0AD	FOC_Ki1_SH
0x0AE	FOC_B_SH
0x0AF	FOC_C_SH
0x0B0	FOC_E_SH
0x0B1	TRK12B_SK
0x0B2	TRK134_SK
0x0B3	TRK138_SK
0x0B4	TRK139_SK
0x0B5	TRK13A _SK
0x0B6	TRK13C _SK
0x0B7	FOC_H_PB
0x0B8	FOC_Ki1_PB
0x0B9	FOC_E_PB
0x0BD	TBAL0:Track Balance Start Value
0x0C7	Reserved
0x0C8	Negative of Focus gain Ki1 for PlayBack.
0x0C9	FOC_KI1_SK
0x0CA	Reserved

UNDER NDA FOR EASTECH

Table 30 RAM Core 0 Registers (Continued)

Address	Description
0x0CB	TRK12B_BD
0x0CC	TRK12B_BA
0x0CD	TRK12B_PB
0x0CE	TRK134_BD
0x0CF	TRK134_BA
0x0D0	TRK134_PB
0x0D1	TRK138_BD
0x0D2	TRK138_BA
0x0D3	TRK138_PB
0x0D4	TRK139_BD
0x0D5	TRK139_BA
0x0D6	TRK139_PB
0x0D7	TRK13A_BD
0x0D8	TRK13A_BA
0x0D9	TRK13A_PB
0x0DA	TRK13C_BD
0x0DB	TRK13C_BA
0x0DC	TRK13C_PB
0x0DE	FOC_B_ BD
0x0DF	FOC_C_ BD
0x0E1	FOC_E_ BD
0x0E3	FOC_Ki1_ BD
0x0E5 to 0x0E9	Reserved
0x0EA	FOC_B_BA
0x0EB	FOC_C_BA
0x0ED	FOC_E_BA
0x0EF	FOC_Ki1_BA
0x0F0	Sled dead band plus.
0x0F1	Sled dead band minus.
0x0F2 to 0x0FF	Reserved

RAM Core 0 Registers

CROSS_CORRELATOR_GAIN 0x01Dh

R/W **Default: N/A**

CROSS_CORRELATOR_GAIN
15:0

Bit Definitions:

Bits	Name	Description
15:0	CROSS_ CORREL ATOR_ GAIN	Cross correlator gain.

TRD_OFFSET 0x021h

R/W **Default: N/A**

TRD_OFFSET
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRD_ OFFSET	Tracking drive offset.

TRV_OFFSET 0x025h

R/W **Default: N/A**

TRV_OFFSET
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRV_ OFFSET	Sled traverse drive offset.

FOC_H_HD 0x02Bh

R/W **Default: N/A**

FOC_H_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_H_ HD	Focus H coefficient host data.

FOC_KI1_HD 0x02Ch

R/W **Default: N/A**

FOC_KI1_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_KI1 HD	Focus KI1 coefficient host data.

UNDER NDA FOR EASTECH

FOC_B_HD **0x02Dh**
R/W **Default: N/A**

FOC_B_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_B_HD	Focus B coefficient host data.

FOC_C_HD **0x02Eh**
R/W **Default: N/A**

FOC_C_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_C_HD	Focus C coefficient host data.

FOC_E_HD **0x02Fh**
R/W **Default: N/A**

FOC_E_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_E_HD	Focus E coefficient host data.

TRK_12B_HD **0x031h**
R/W **Default: N/A**

TRK12B_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK12B_HD	Tracking coefficient 12B host data.

TRK134_HD **0x032h**
R/W **Default: N/A**

TRK134_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK134_HD	Tracking coefficient 134 host data.

TRK_138_HD **0x033h**
R/W **Default: N/A**

TRK138_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK138_HD	Tracking coefficient 138 host data.

TRK139_HD **0x034h**
R/W **Default: N/A**

TRK139_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK139_HD	Tracking coefficient 139 host data.

TRK13A_HD **0x035h**
R/W **Default: N/A**

TRK13A_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13A_HD	Tracking coefficient 13A host data.

UNDER NDA FOR EASTECH

TRK13C_HD **0x036h**
R/W **Default: N/A**

TRK13C_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13C_HD	Tracking coefficient 13C host data.

FOC_B_HA **0x039h**
R/W **Default: N/A**

FOC_B_HA
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_B_HA	Focus coefficient B host address.

TRK13C_HD **0x036h**
R/W **Default: N/A**

TRK13C_HD
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13C_HD	Tracking coefficient 13C host data.

FOC_C_HA **0x03Ah**
R/W **Default: N/A**

FOC_C_HA
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_C_HA	Focus coefficient C host address.

FOC_H_HA **0x037h**
R/W **Default: N/A**

FOC_H_HA
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_H_HA	Focus coefficient H host address.

FOC_E_HA **0x03Bh**
R/W **Default: N/A**

FOC_E_HA
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_E_HA	Focus coefficient E host address.

FOC_KI1_HA **0x038h**
R/W **Default: N/A**

FOC_KI1_HA
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_KI1_HA	Focus coefficient KI1 host address.

TRK_12B_HA **0x03Ch**
R/W **Default: N/A**

TRK12B_HA
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK12B_HA	Tracking coefficient 12B host address.

UNDER NDA FOR EASTECH

TRK134_HA **0x03Dh**
R/W **Default: N/A**

TRK134_HA
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK134_HA	Tracking coefficient 134 host address.

TRK13C_HA **0x042h**
R/W **Default: N/A**

TRK13C_HA
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13C HA	Tracking coefficient 13C host address.

TRK_138_HA **0x03Eh**
R/W **Default: N/A**

TRK138_HA
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK138_HA	Tracking coefficient 138 host address.

M_H_HAT_PB **0x075h**
R/W **Default: N/A**

M_H_HAT_PB
15:0

Bit Definitions:

Bits	Name	Description
15:0	M_H_HAT_PB	Negative of playback focus filter (_PB) gain H.

TRK139_HA **0x03Fh**
R/W **Default: N/A**

TRK139_HA
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK139_HA	Tracking coefficient 139 host address.

FOC_H_SK **0x076h**
R/W **Default: N/A**

FOC_H_SK
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_H_SK	Focus coefficient H long seek (_SK) gain.

TRK13A_HA **0x040h**
R/W **Default: N/A**

TRK13A_HA
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13A_HA	Tracking coefficient 13A host address.

FOC_H_BD **0x077h**
R/W **Default: N/A**

FOC_H_BD
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_H_BD	Focus coefficient H BDO start (_BD) gain.

UNDER NDA FOR EASTECH

FOC_H_BA **0x078h**
R/W **Default: N/A**

FOC_H_BA
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_H_BA	Focus coefficient H BDO end (_BA) gain.

SEEK_SLED_FILTER **0x087h**
R/W **Default: N/A**

SEEK_SLED_FILTER
15:0

Bit Definitions:

Bits	Name	Description
15:0	SEEK_SLED_FILTER	SEK087 gain value.

FOC_BAL_START **0x091h**
R/W **Default: N/A**

FOC_BAL_START
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_BAL_START	Focus balance start value.

FOC_B_PB **0x092h**
R/W **Default: N/A**

FOC_B_PB
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_B_PB	Focus coefficient B playback (_PB) gain.

M_D_HAT_PB **0x094h**
R/W **Default: N/A**

M_D_HAT_PB
15:0

Bit Definitions:

Bits	Name	Description
15:0	M_D_HAT_PB	Negative of playback focus filter (_PB) gain D.

M_E_HAT_PB **0x095h**
R/W **Default: N/A**

M_E_HAT_PB
15:0

Bit Definitions:

Bits	Name	Description
15:0	M_E_HAT_PB	Negative of playback focus filter (_PB) gain E.

FOD_BIAS **0x096h**
R/W **Default: N/A**

FOD_BIAS
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOD_BIAS	Focus drive output adjustment for focus filter.

FBAL_DELTA **0x097h**
R/W **Default: N/A**

FBAL_DELTA
15:0

Bit Definitions:

Bits	Name	Description
15:0	FBAL_DELTA	Change in focus balance search value.

UNDER NDA FOR EASTECH

TBAL_DELTA 0x098h
R/W **Default: N/A**

TBAL_DELTA
15:0

Bit Definitions:

Bits	Name	Description
15:0	TBAL_DELTA	Change in tracking balance search value.

FOC_B_SK 0x09Ah
R/W **Default: N/A**

FOC_B_SK
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_B_SK	Focus coefficient B long seek (_SK) gain.

FOC_C_SK 0x09Bh
R/W **Default: N/A**

FOC_C_SK
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_C_SK	Focus coefficient C long seek (_SK) gain.

FOC_E_SK 0x09Dh
R/W **Default: N/A**

FOC_E_SK
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_E_SK	Focus coefficient E long seek (_SK) gain.

TRK12B_SH 0x0A6h
R/W **Default: N/A**

TRK12B_SH
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK12B_SH	Tracking coefficient 12B shock filter (_SH) gain.

TRK134_SH 0x0A7h
R/W **Default: N/A**

TRK134_SH
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK134_SH	Tracking coefficient 134 shock filter (_SH) gain.

TRK138_SH 0x0A8h
R/W **Default: N/A**

TRK138_SH
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK138_SH	Tracking coefficient 138 shock filter (_SH) gain.

TRK139_SH 0x0A9h
R/W **Default: N/A**

TRK139_SH
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK139_SH	Tracking coefficient 139 shock filter (_SH) gain.

UNDER NDA FOR EASTECH

TRK13A_SH **0x0AAh**
R/W **Default: N/A**

TRK13A_SH
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13A_SH	Tracking coefficient 13A shock filter (_SH) gain.

FOC_B_SH **0x0AEh**
R/W **Default: N/A**

FOC_B_SH
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_B_SH	Focus coefficient B shock filter (_SH) gain.

TRK13C_SH **0x0ABh**
R/W **Default: N/A**

TRK13C_SH
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13C SH	Tracking coefficient 13C shock filter (_SH) gain.

FOC_C_SH **0x0AFh**
R/W **Default: N/A**

FOC_C_SH
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_C_SH	Focus coefficient C shock filter (_SH) gain.

FOC_H_SH **0x0ACh**
R/W **Default: N/A**

FOC_H_SH
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_H_SH	Focus coefficient H shock filter (_SH) gain.

FOC_E_SH **0x0B0h**
R/W **Default: N/A**

FOC_E_SH
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_E_SH	Focus coefficient E shock filter (_SH) gain.

FOC_KI1_SH **0x0ADh**
R/W **Default: N/A**

FOC_KI1_SH
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_KI1_SH	Focus coefficient KI1 shock filter (_SH) gain.

TRK12B_SK **0x0B1h**
R/W **Default: N/A**

TRK12B_SK
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK12B_SK	Tracking coefficient 12B long seek (_SK) gain.

UNDER NDA FOR EASTECH

TRK134_SK 0x0B2h
R/W **Default: N/A**

TRK134_SK
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK134_SK	Tracking coefficient 134 long seek (_SK) gain.

TRK13C_SK 0x0B6h
R/W **Default: N/A**

TRK13C_SK
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13C SK	Tracking coefficient 13C long seek (_SK) gain.

TRK138_SK 0x0B3h
R/W **Default: N/A**

TRK138_SK
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK138_SK	Tracking coefficient 138 long seek (_SK) gain.

TBAL0 0x0BDh
R/W **Default: N/A**

TBAL0
15:0

Bit Definitions:

Bits	Name	Description
15:0	TBAL0	Tracking balance start value.

TRK139_SK 0x0B4h
R/W **Default: N/A**

TRK139_SK
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK139_SK	Tracking coefficient 139 long seek (_SK) gain.

M_KI1_PB 0x0C8h
R/W **Default: N/A**

M_KI1_PB
15:0

Bit Definitions:

Bits	Name	Description
15:0	M_KI1_PB	Negative of focus coefficient Ki1 play back (_PB) gain.

TRK13A_SK 0x0B5h
R/W **Default: N/A**

TRK13A_SK
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13A_SK	Tracking coefficient 13A long seek (_SK) gain.

FOC_KI1_SK 0x0C9h
R/W **Default: N/A**

FOC_KI1_SK
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_KI1_SK	Focus coefficient Ki1 long seek (_SK) gain.

UNDER NDA FOR EASTECH

TRK12B_BD **0x0CBh**
R/W **Default: N/A**

TRK12B_BD
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK12B_BD	Tracking coefficient 12B BDO start (_BD) gain.

TRK134_BA **0x0CFh**
R/W **Default: N/A**

TRK134_BA
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK134_BA	Tracking coefficient 134 BDO end (_BA) gain.

TRK12B_BA **0x0CCh**
R/W **Default: N/A**

TRK12B_BA
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK12B_BA	Tracking coefficient 12B BDO end (_BA) gain.

TRK134_PB **0x0D0h**
R/W **Default: N/A**

TRK134_PB
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK134_PB	Tracking coefficient 134 play back (_PB) gain.

TRK12B_PB **0x0CDh**
R/W **Default: N/A**

TRK12B_PB
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK12B_PB	Tracking coefficient 12B play back (_PB) gain.

TRK138_BD **0x0D1h**
R/W **Default: N/A**

TRK138_BD
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK138_BD	Tracking coefficient 138 BDO start (_BD) gain.

TRK134_BD **0x0CEh**
R/W **Default: N/A**

TRK134_BD
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK134_BD	Tracking coefficient 134 BDO start (_BD) gain.

TRK138_BA **0x0D2h**
R/W **Default: N/A**

TRK138_BA
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK138_BA	Tracking coefficient 138 BDO end (_BA) gain.

UNDER NDA FOR EASTECH

TRV_SLED_SL_K132 0x132h
R/W **Default: N/A**

TRV_SLED_SL_K132
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRV_SLED_SL_K132	Sled traverse filter value SL_K132.

TRK133 0x133h
R/W **Default: N/A**

TRK133
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK133	Coefficient A tracking filter value TRK133.

TRK134 0x134h
R/W **Default: N/A**

TRK134
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK134	Coefficient B tracking filter value TRK134.

TRK135 0x135h
R/W **Default: N/A**

TRK135
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK135	Coefficient C tracking filter value TRK135.

TRK136 0x136h
R/W **Default: N/A**

TRK136
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK136	Coefficient D tracking filter value TRK136.

TRK137 0x137h
R/W **Default: N/A**

TRK137
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK137	Coefficient E tracking filter value TRK137.

TRK138 0x138h
R/W **Default: N/A**

TRK138
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK138	Coefficient F tracking filter value TRK138.

TRK139 0x139h
R/W **Default: N/A**

TRK139
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK139	Coefficient I tracking filter value TRK139.

TRK13A 0x13Ah
R/W **Default: N/A**

TRK13A
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13A	Coefficient H tracking filter value TRK13A.

TRK13C 0x13Ch
R/W **Default: N/A**

TRK13C
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13C	Coefficient G tracking filter value TRK13C.

UNDER NDA FOR EASTECH

TRK13D **0x13Dh**
R/W **Default: N/A**

TRK13D
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK13D	Coefficient H tracking filter value TRK13D.

TRV_SLED_SL_K13E **0x13Eh**
R/W **Default: N/A**

TRV_SLED_SL_K13E
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRV_ SLED_ SL_K13E	Sled traverse filter value SL_K13E.

TRV_SLED_SL_K13F **0x13Fh**
R/W **Default: N/A**

TRV_SLED_SL_K13F
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRV_ SLED_ SL_K13F	Sled traverse filter value SL_K13F.

SEK_PUP_OFFSET **0x140h**
R/W **Default: N/A**

SEK_PUP_OFFSET
15:0

Bit Definitions:

Bits	Name	Description
15:0	SEK_ PUP_ OFFSET	Pickup lens seek offset value.

TRV_SLED_SL_K141 **0x141h**
R/W **Default: N/A**

TRV_SLED_SL_K141
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRV_ SLED_ SL_K141	Sled traverse filter value SL_K141.

TRV_SLED_SL_K143 **0x143h**
R/W **Default: N/A**

TRV_SLED_SL_K143
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRV_ SLED_ SL_K143	Sled traverse filter value SL_K143.

TRV_SLED_SL_K145 **0x145h**
R/W **Default: N/A**

TRV_SLED_SL_K145
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRV_ SLED_ SL_K145	Sled traverse filter value SL_K145.

SEK147 **0x147h**
R/W **Default: N/A**

SEK147
15:0

Bit Definitions:

Bits	Name	Description
15:0	SEK147	Sled coefficient B value SEK147.

UNDER NDA FOR EASTECH

SEK148 **0x148h**
R/W **Default: N/A**

SEK148
15:0

Bit Definitions:

Bits	Name	Description
15:0	SEK148	Sled coefficient C value SEK148.

SEK14A **0x14Ah**
R/W **Default: N/A**

SEK14A
15:0

Bit Definitions:

Bits	Name	Description
15:0	SEK14A	Sled coefficient value SEK14A.

SH_KB **0x14Dh**
R/W **Default: N/A**

SH_KB
15:0

Bit Definitions:

Bits	Name	Description
15:0	SH_KB	Shock filter gain SH_KB.

SH_KC **0x14Eh**
R/W **Default: N/A**

SH_KC
15:0

Bit Definitions:

Bits	Name	Description
15:0	SH_KC	Shock filter gain SH_KC.

SH_KA **0x14Fh**
R/W **Default: N/A**

SH_KA
15:0

Bit Definitions:

Bits	Name	Description
15:0	SH_KA	Shock filter gain SH_KA.

SH_K5 **0x150h**
R/W **Default: N/A**

SH_K5
15:0

Bit Definitions:

Bits	Name	Description
15:0	SH_K5	Shock filter gain SH_K5.

TRK151 **0x151h**
R/W **Default: N/A**

TRK151
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK151	Track filter offset gain value TRK151.

TRK152 **0x152h**
R/W **Default: N/A**

TRK152
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK152	Track filter offset gain value TRK152.

CE_GAIN_TRD **0x15Eh**
R/W **Default: N/A**

CE_GAIN_TRD
15:0

Bit Definitions:

Bits	Name	Description
15:0	CE_ GAIN_ TRD	Center error gain for tracking drive.

UNDER NDA FOR EASTECH

PHASE_ERROR_GAIN **0x16Fh**
R/W **Default: N/A**

PHASE_ERROR_GAIN
15:0

Bit Definitions:

Bits	Name	Description
15:0	PHASE_ERROR_GAIN	Phase error gain for spindle filter in CLV mode.

SEK171 **0x171h**
R/W **Default: N/A**

SEK171
15:0

Bit Definitions:

Bits	Name	Description
15:0	SEK171	Feed forward seek gain value SEK171.

SEEK_TIMEOUT **0x186h**
R/W **Default: N/A**

SEEK_TIMEOUT
15:0

Bit Definitions:

Bits	Name	Description
15:0	SEEK_TIMEOUT	Seek timeout.

SLOW_SEEK_TIMEOUT **0x187h**
R/W **Default: N/A**

SLOW_SEEK_TIMEOUT
15:0

Bit Definitions:

Bits	Name	Description
15:0	SLOW_SEEK_TIME-OUT	Slow seek timeout.

COEFF_B_FF **0x191h**
R/W **Default: N/A**

COEFF_B_FF
15:0

Bit Definitions:

Bits	Name	Description
15:0	COEFF_B_FF	Focus filter coefficient B value.

COEFF_C_FF **0x192h**
R/W **Default: N/A**

COEFF_C_FF
15:0

Bit Definitions:

Bits	Name	Description
15:0	COEFF_C_FF	Focus filter coefficient C value.

COEFF_D_FF **0x193h**
R/W **Default: N/A**

COEFF_D_FF
15:0

Bit Definitions:

Bits	Name	Description
15:0	COEFF_D_FF	Focus filter coefficient D value.

COEFF_E_FF **0x194h**
R/W **Default: N/A**

COEFF_E_FF
15:0

Bit Definitions:

Bits	Name	Description
15:0	COEFF_E_FF	Focus filter coefficient E value.

UNDER NDA FOR EASTECH

COEFF_G_FF 0x195h
R/W **Default: N/A**

COEFF_G_FF
15:0

Bit Definitions:

Bits	Name	Description
15:0	COEFF_G_FF	Focus filter coefficient G value.

SLED_PULLOUT 0x197h
R/W **Default: N/A**

SLED_PULLOUT
15:0

Bit Definitions:

Bits	Name	Description
15:0	SLED_PULL-OUT	Sled pullout time used by C_DSKSRCH.

BDO_TIME_LIMIT 0x1A8h
R/W **Default: N/A**

BDO_TIME_LIMIT
15:0

Bit Definitions:

Bits	Name	Description
15:0	BDO_TIME_LIMIT	Black drop out time limit.

BDO_HOLDOFF_TIME 0x1A9h
R/W **Default: N/A**

BDO_HOLDOFF_TIME
15:0

Bit Definitions:

Bits	Name	Description
15:0	BDO_HOLD-OFF_TIME	Black drop out hold-off time.

FOCUS_JUMP_TIMEOUT 0x1ABh
R/W **Default: N/A**

FOCUS_JUMP_TIMEOUT
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOCUS_JUMP_TIME-OUT	Focus jump timeout value.

HALF_DELAY_CDELAY_H 0x1ADh
R/W **Default: N/A**

HALF_DELAY_CDELAY_H
7:0

Bit Definitions:

Bits	Name	Description
7:0	HALF_DELAY_CDELAY_H	Half delay time for C_DELAY (high byte).

HALF_DELAY_CDELAY_L 0x1AEh
R/W **Default: N/A**

HALF_DELAY_CDELAY_L
7:0

Bit Definitions:

Bits	Name	Description
7:0	HALF_DELAY_CDELAY_L	Half delay time for C_DELAY (low byte).

FOC_SETTLE_DELAY 0x1B6h
R/W **Default: N/A**

FOC_SETTLE_DELAY
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_SETTLE_DELAY	Focus settle delay for C_FOC_CHK.

UNDER NDA FOR EASTECH

FOC_HEALTH_MON **0x1B7h**
R/W **Default: N/A**

FOC_HEALTH_MON
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_HEALTH_MON	Focus health monitor value.

COEFF_KI1_FF **0x1BDh**
R/W **Default: N/A**

COEFF_KI1_FF
15:0

Bit Definitions:

Bits	Name	Description
15:0	COEFF_KI1_FF	Focus filter coefficient KI1 value.

COEFF_KI2_FF **0x1C0h**
R/W **Default: N/A**

COEFF_KI2_FF
15:0

Bit Definitions:

Bits	Name	Description
15:0	COEFF_KI2_FF	Focus filter coefficient KI2 value.

COEFF_KIC_FF **0x1C1h**
R/W **Default: N/A**

COEFF_KIC_FF
15:0

Bit Definitions:

Bits	Name	Description
15:0	COEFF_KIC_FF	Focus filter coefficient KIC value.

TRD_INIT **0x1C6h**
R/W **Default: N/A**

TRD_INIT
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRD_INIT	TRD initialization value during C_ADDA execution.

BDO_INT_HOLDOFF **0x1C7h**
R/W **Default: N/A**

BDO_INT_HOLDOFF
15:0

Bit Definitions:

Bits	Name	Description
15:0	BDO_INT_HOLD-OFF	Black drop out to Interrupt holdoff time.

FOC_PULL_IN_END (FAST) **0x1C8h**
R/W **Default: N/A**

FOC_PULL_IN_END (FAST)
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_PULL_IN_END (FAST)	Focus pull-in scan end point, fast setting.

FOC_PULL_IN_START **0x1C9h**
R/W **Default: N/A**

FOC_PULL_IN_START
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_PULL_IN_START	Focus pull-in scan start point.

UNDER NDA FOR EASTECH

FOC_SW_GAIN **0x1DDh**
R/W **Default: N/A**

FOC_SW_GAIN
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_SW_GAIN	Focus filter sine wave gain.

INT_KILL_BDO **0x1EBh**
R/W **Default: N/A**

INT_KILL_BDO
15:0

Bit Definitions:

Bits	Name	Description
15:0	INT_KILL_BDO	Kill interrupt gain for BDO start.

FBAL_GAIN **0x1DEh**
R/W **Default: N/A**

FBAL_GAIN
15:0

Bit Definitions:

Bits	Name	Description
15:0	FBAL_GAIN	Focus filter balance gain value.

FOC_H_GAIN **0x1ECh**
R/W **Default: N/A**

FOC_H_GAIN
15:0

Bit Definitions:

Bits	Name	Description
15:0	FOC_H_GAIN	Focus filtering coefficient H gain value.

INT_GAIN **0x1E6h**
R/W **Default: N/A**

INT_GAIN
15:0

Bit Definitions:

Bits	Name	Description
15:0	INT_GAIN	Interrupt filtering input gain value.

TRK_CE_GAIN **0x1F0h**
R/W **Default: N/A**

TRK_CE_GAIN
15:0

Bit Definitions:

Bits	Name	Description
15:0	TRK_CE GAIN	Center error gain value for track following.

18T_GAIN **0x1EAh**
R/W **Default: N/A**

18T_GAIN
15:0

Bit Definitions:

Bits	Name	Description
15:0	18T_GAIN	18T filtering input gain value.

UNDER NDA FOR EASTECH

Spindle Configuration Registers

SPCFG 0x0106h
R/W **Default: 0x00000h**

SET 6T	—	SERR FGNG	SRV ATST	—	SERSAT ERR	—
15	14:10	9	8	7:5	4	3:0

The Spindle Configuration register is used to perform spindle configuration at the command level.

Bit Definitions:

Bits	Name	Description
15	SET6T	Force Set To 6T: When set, this bit forcibly sets the spindle motor control flag to 6T mode. 1= Forcibly set to 6T mode.
14:10	—	Reserved
9	SERR FGNG	Servo Error, FG No Good: When set, this bit allows the servo controller of the ES8381 to generate an error report caused by the setting of the FG No Good flag. 1 = Allow servo error report by FG no good.
8	SRV ATST	Servo Attention Status: When set, this bit allows the servo attention status flag to be set by the setting of either the CLV flag or FG No Good flag.
7:5	—	Reserved
4	SERSAT ERR	Servo Error/Servo Attention By Error: When set, this bit allows the spindle motor control system to set either the Servo Error or Servo Attention flag when an error status report is generated. 1 = Allows servo error or servo attention by error status report
3:0	—	Reserved

JITTER_ABNORMAL_LEVEL 0x0280h
R/W **Default: 0xC0B8h**

JABUL
15:8

JABLL
7:0

The Jitter Abnormal Level register is used for comparison with incoming jitter level.

Bit Definitions:

Bits	Name	Description
15:8	JABUL	Jitter abnormal level upper limit.
7:0	JABLL	Jitter abnormal level lower limit.

DATA_ABNORMAL_LEVEL 0x0281h
R/W **Default: 0x1A10h**

18TABN
15:8

6TABN
7:0

Bit Definitions:

Bits	Name	Description
15:8	18TABN	18T or 11T abnormal value for high speed detection.
7:0	6TABN	6T abnormal value for low speed detection.

DATA_CLIP_VALUE 0x0282h
RW **Default: N/A**

DCV
7:0

Bit Definitions:

Bits	Name	Description
7:0	DCV	Data clip value in 18T, 11T, and 6T spindle modes: Used in conjunction with DATA_LIMIT register 0x0289. When data > Data Limit [15:8], set to Data Clip Value [15:8]. When data< Data Limit [7:0], set to Data Clip Value [7:0].

FG_FAST_COUNT_LEVEL 0x0283h
RW **Default: 0x01A0h**

FGFCL
7:0

Bit Definitions:

Bits	Name	Description
7:0	FGFCL	Comparison value for FG period in high speed check, calculated by the equation: (time = setting * SI).

UNDER NDA FOR EASTECH

FG_SLOW_COUNT_LEVEL 0x0284h
RW **Default: 0x1A0Ah**

FGSCL
7:0

Bit Definitions:

Bits	Name	Description
7:0	FGSCL	Comparison value for FG period in slow speed check, calculated by the equation: (time = setting * SI).

BRAKE_TIME 0x0285h
RW **Default: 0x00F0h**

BKTIME
7:0

Bit Definitions:

Bits	Name	Description
7:0	BKTIME	Spindle motor brake time, calculated by the equation: (time = setting * 1.536 msec).

SIZE_CHECK_SPEED 0x0286h
R/W **Default: 0x01FBh**

SCSPD
7:0

Bit Definitions:

Bits	Name	Description
7:0	SCSPD	Spindle drive value for 8cm/12cm disc size determination.

SIZE_CHECK_PERIOD 0x0287h
R/W **Default: 0x0378h**

SCPD
7:0

Bit Definitions:

Bits	Name	Description
7:0	SCPD	Time period for disc size determination, calculated by the equation: (time = setting * SI)

SIZE_CHECK_TIME 0x0288h
RW **Default: 0x1111h**

SCT
7:0

Bit Definitions:

Bits	Name	Description
7:0	SCT	Time period for disc size determination, calculated by the equation: (time = setting * SI)

DATA_LIMIT 0x0289h
RW **Default: 0x2B10h**

DATA_LIMIT_H
15:8

DATA_LIMIT_L
7:0

Bit Definitions:

Bits	Name	Description
15:8	DATA_LIMIT_H	Range of 18T, 11T, or 6T data (high byte). Clip any data out of this range. Use in conjunction with DATA_CLIP_VALUE register 0x0282h.
7:0	DATA_LIMIT_L	Range of 18T, 11T, or 6T data (low byte). Use in conjunction with DATA_CLIP_VALUE register 0x0282h.

DELAY_CNT 0x028Ah
RW **Default: 0x0D0Eh**

DELAY_CNT_H
15:8

DELAY_CNT_L
7:0

Bit Definitions:

Bits	Name	Description
15:8	DELAY_CNT_H	Internal spindle processing busy.
7:0	DELAY_CNT_L	Wait time between mode changes. Keep high byte < low byte. (time = setting * 1.536 ms).

UNDER NDA FOR EASTECH

DATA_QUALITY_CHECK 0x028Bh
RW **Default: 0x0D0Fh**

DATA_QUALITY_CHECK (GOOD)
15:8

DATA_QUALITY_CHECK (BAD)
7:0

Bit Definitions:

Bits	Name	Description
15:8	DATA_QUALITY CHECK_(GOOD)	Data Quality Check, Low Byte: Consecutive frame count of good 18T, 11T, or 6T data. Used for transition to CLV.
7:0	DATA_QUALITY CHECK_(BAD)	Data Quality Check, High Byte: Consecutive frame count of bad 18T, 11T, or 6T data. Used for transition to degraded modes.

PWM0_CONFIG 0x028Ch
R/W **Default: 0x05A0h)**

TODT
15:8

USE PGERR	—	CDDT SEL	REFFRQ SEL	DVDDT SEL	UPGSP CLV	MASK BRK	INVSP POL
7	6	5	4	3	2	1	0

The Pulse Width Modulation 0 Configuration register monitors tracking delay time and spindle drive polarity for the spindle motor control function of the servo controller.

Bit Definitions:

Bits	Name	Description
15:8	TODT	Tracking On Delay Time: This 8-bit field contains the tracking on delay time. The tracking on delay time is calculated as follows: (time = setting x 1.536 ms)
7	USE PGERR	Use PG Error: 1 = Use PG error in DSP calculations.
6	—	Reserved.
5	CDDT SEL	CD Mode Tracking Frame Data Select: When a CD-ROM disk is being played back, this bit controls the type of tracking to be performed on the media. 1 = Use minimum of last four frame data. 0 = Select current value.
4	REFFRQ SEL	Reference Frequency Select.
3	DVDDT SEL	DVD Mode Tracking Frame Data Select: When a DVD disk is being played back, this bit controls the type of tracking to be performed on the media. 1 = Use minimum of last four frame data. 0 = Select current value.
2	UPGSP CLV	Upgrade Spindle Mode To CLV Mode: 1 = Use good conditions to upgrade spindle mode towards CLV.
1	MASK BRK	Mask Brake Enable: 1 = In brake mode, don't use active braking 0 = In brake mode, use active braking.
0	INVSP POL	Invert Spindle Drive Polarity: When set, this bit inverts the spindle drive polarity. 1 = Invert spindle drive polarity.

BRAKE_VAL 0x028Dh
R/W **Default: 0x054Bh**

BRAKE_VAL
7:0

The Brake Value register contains the spindle drive value during braking.

Bit Definitions:

Bits	Name	Description
7:0	BRAKE_VAL	Spindle drive value during braking.

DRIVE_MOTOR_ON_DELAY 0x028Eh
R/W **Default: 0x0100h**

DMD
7:0

The Drive Motor On Delay register is used for establishing the delay time for the DMON command to wait before issuing its interrupt request to the CPU to start the spindle drive motor.

Bit Definitions:

Bits	Name	Description
7:0	DMD	Drive Motor On Delay, calculated by the equation: (time = setting * 1.536 msec).

UNDER NDA FOR EASTECH

INIT_PWM0_VAL **0x028Fh**
R/W **Default: 0x0320**

INIT_PWM0_VAL
15:8

Bit Definitions:

Bits	Name	Description
15:0	INIT_PWM0_VAL	Quiescent value of spindle drive.

Tracking Servo Registers

VELOCITY_REFERENCE_10 **0x0300h**
R/W **Default: N/A**

VR1	VR0
15:8	7:0

Bit Definitions:

Bits	Name	Description
15:8	VR1	Velocity Reference for VR1: This field holds the current velocity reference for VR1.
7:0	VR0	Velocity Reference for VR0: This field holds the current velocity reference for VR0.

VELOCITY_REFERENCE_32 **0x0301h**
R/W **Default: N/A**

VR3	VR2
15:8	7:0

Bit Definitions:

Bits	Name	Description
15:8	VR3	Velocity Reference for VR3: This field holds the current velocity reference for VR3.
7:0	VR2	Velocity Reference for VR2: This field holds the current velocity reference for VR2.

TJMP_BRK_START_PW **0x0306h**
R/W **Default: N/A**

TJMP_BRK_START_H	TJMP_BRK_START_L
15:8	7:0

Bit Definitions:

Bits	Name	Description
15:8	TJMP_BRK_START_H	High byte: tracking servo single jump deceleration end time.
7:0	TJMP_BRK_START_H	Low byte: tracking servo single jump deceleration start time.

TJMP_START **0x0307h**
R/W **Default: N/A**

TJMP_START_H	—
15:8	7:0

Bit Definitions:

Bits	Name	Description
15:8	TJMP_START_H	High byte: tracking servo single jump acceleration pulse time.
7:0	—	Reserved

TRV_TOP **0x030Ch**
R/W **Default: N/A**

—	TRV_TOP	—
15	14:7	6:0

Bit Definitions:

Bits	Name	Description
15	—	Reserved
14:7	TRV_TOP	TRV top value.
6:0	—	Reserved

UNDER NDA FOR EASTECH

TRV_BOT 0x030Dh
R/W Default: N/A

—	TRV_BOT	—
15	14:7	6:0

Bit Definitions:

Bits	Name	Description
15	—	Reserved
14:7	TRV_BOT	TRV bottom value.
6:0	—	Reserved

Focus And Sled Servo Configuration Registers

FOCUS_SYSTEM 0x381h
R/W Default: 00h)

TKCRS	OFTR	—	FOC_PULSE	THM_EN	AS2SRF
15	14	13:12	11	10	9:8

SL_ERR	—	FHM_EN	—
7	6:4	3	2:0

Bit Definitions:

Bits	Name	Description
15	TKCRS	TKCRS Direction Bit.
14	OFTR	OFTR Filtering On.
13:12	—	Reserved
11	FOC_PULSE	Focus Pulse Configuration: 1 = relative 0 = absolute
10	THM_EN	Tracking Health Monitor: 1 = allow 0 = disallow
9:8	AS2SRF	AS2SRF: 00 = Set SRF1 if CD or DVD2. 01 = Expect SRF1 from CPU. 10 = Use AS2SRF and AS2MAX to decide SRF1.
7	SL_ERR	Sled In Error Detection Enable: 1 = Enabled 0 = disabled
6:4	—	Reserved
3	FHM_EN	Focus Health Monitor: 1 = allow 0 = disallow
2:0	—	Reserved

BDO_CONFIG 0x382h
R/W Default: 00h)

BDO_GEN CTRL	DFCT_OFF	INT_GEN_CTRL	MIRR_CTRL	—	HS_DET	EX_START CTRL
15	14	13	12	11:10	9	8

—	INT_CTRL	—	BDO_CTRL	—
7	6	5:3	2	1:0

Bit Definitions:

Bits	Name	Description
15	BDO_GEN_CTRL	Black Drop Out Generation Control: 1 = Use black drop out (BDO) generated by AFE to trigger BDO response. 0 = Pass the BDO from the AFE through averaging process, and apply a focus jump null offset as the threshold to trigger a BDO response.
14	DFCT_OFF	Defect Off Priority: 1 = Either BDO or INT exception decides when to stop its exception handling. 0 = Either BDO or INT exception decides when to continue its exception handling.
13	INT_GEN_CTRL	Interrupt Generation Control: 1:= If MIRR_CTR bit (bit 12) is set at 0, treat MIRR as an interrupt. 0 = Don't treat MIRR as an interrupt.
12	MIRR_CTRL	Mirror Error Control: 1 = Allow mirror error detection. 0 = Disallow mirror error detection.
11:10	—	Reserved
9	HS_DET	High Speed Detection Flag: 1 = Trigger error report when FG period is small. 0 = Ignore short FG period.
8	EX_START CTRL	Exception Start Control: 1 = Assign higher priority to BDO. 0 = Assign priority to current exception being executed.
7	—	Reserved
6	INT_CTRL	Interrupt Control: 1 = Allow interrupt response. 0 = Suppress interrupt response.
5:3	—	Reserved
2	BDO_CTRL	BDO Control: 1 = Allow BDO response. 0 = Suppress BDO response.
1:0	—	Reserved

UNDER NDA FOR EASTECH

FG_SLED_CONFIG **0x383h**
R/W **Default: 00h)**

—	SLED_FEED_FWD_CFG
15:12	11:8

—	IGN_SYNTH_FG	SYNC_SYNTH_FG	SYNTH_FG_REV_WIDTH
7	6	5	4:0

Bit Definitions:

Bits	Name	Description
15:12	—	Reserved
11:8	SLED_FEED_FWD_CFG	Sled Feed Forward Configuration: 1 = Feed-forward term on. 0 = Feed-forward term off.
7	—	Reserved
6	IGN_SYNTH_FG	Ignore Synthetic FG Mode: 1 = Actual FG mode used. 0 = Synthetic FG mode used.
5	SYNC_SYNTH_FG	Sync Synthetic FG Mode With BDO: 1 = Synthetic FG mode synchronized with BDO. 0 = Not synchronized.
4:0	SYNTH_FG_REV_WIDTH	Synthetic FG Revolution Width.

DVD Backend Registers

This section describes the DVD backend registers of the ES8381.

Video Interface Registers

This section describes the video interface registers of the ES8381.

VID_SCN_HSTART **0x20001000h**
W **Default: N/A)**

—	HSTART
15:13	12:0

The write-only video screen horizontal start address register contains the 13-bit horizontal pixel starting address of the active video display.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	HSTART	Horizontal starting address of active window.

VID_SCN_HEND **0x20001004h**
W **Default: N/A)**

—	HEND
15:13	12:0

The write-only video screen horizontal end address register contains the 13-bit horizontal pixel ending address of the active video display.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	HEND	Horizontal ending address of active window.

VID_SCN_VSTART **0x20001008h**
W **Default: N/A**

—	VSTART
15:13	12:0

The write-only video screen vertical start address register contains the 13-bit vertical scan line starting address of the active video display.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	VSTART	Vertical scan line starting address of active window.

VID_SCN_VEND **0x2000100Ch**
W **Default: N/A**

—	VEND
15:13	12:0

The write-only video screen vertical end address register contains the 13-bit vertical scan line ending address of the active video display.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	VEND	Vertical scan line ending address of active window.

UNDER NDA FOR EASTECH

VID_SCN_VERTIRQ **0x20001010h**
W **Default: N/A**

The write-only video screen vertical line interrupt register is selectable by software and contains the line in which a

UNDER NDA FOR EASTECH

VID_SCN_HSYNCPERIOD **0x20001028h**
W **Default: N/A**

—	HSYNCPERIOD
15:13	12:0

The write-only video screen horizontal sync period register contains the 13-bit value for the period of the horizontal sync pulse used by the active video display. It is needed only if sync direction is output.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	HSYNC-PERIOD	Horizontal sync period.

VID_SCN_VSYNCPERIOD **0x2000102Ch**
W **Default: N/A**

—	VSYNCPERIOD
15:13	12:0

The write-only video screen video sync period register contains the 13-bit value for the period of the vertical sync pulse used by the active video display. This register is needed only if sync direction is output.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	VSYNC-PERIOD	Vertical sync pulse period.

VID_SCN_VSYNCPIXEL **0x20001030h**
W **Default: N/A**

—	VSYNCPIXEL
15:13	12:0

The write-only video screen vertical sync pixel register defines which pixel VSYNC will change on for the active video display. The number of pixels delayed from HSYNC that VSYNC will change on either the rising or falling edge of VSYNC. This register is needed only if sync direction is output.

Bit Definitions:.

Bits	Name	Description
15:13	—	Reserved
12:0	VSYNC-PIXEL	Pixel on which VSYNC will change.

VID_SCN_VSYNCWIDTH **0x20001034h**
W **Default: N/A**

—	VSYNCWIDTH
15:6	5:0

The write-only video screen vertical sync pulse width register defines the width of the 6-bit vertical sync pulse. It is needed only if sync direction is output.

Bit Definitions:.

Bits	Name	Description
15:6	—	Reserved
5:0	VSYNC-WIDTH	Vertical sync pulse width.

VID_SCN_VERTCOUNT **0x20001036h**
R **Default: N/A**

—	VERTCOUNT
15:13	12:0

The read-only video screen vertical counter register contains the current line of the vertical counter, and starts its counting at VSYNC line 0. This register is typically used for testing only.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	VERT-COUNT	Current pixel of the vertical counter.

VID_SCN_HORIZCOUNT **0x20001038h**
R **Default: N/A**

—	HORIZCOUNT
15:13	12:0

The read-only video screen horizontal counter register contains the current pixel of the horizontal counter, and starts its counting at HSYNC pixel 0.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	HORIZ-COUNT	Current pixel of the horizontal counter.

UNDER NDA FOR EASTECH

VID_SCN_COUNTER_CTL 0x2000103Ch
W **Default: 0x00h**

—	INVBLNK	—	INVHS	INVVS	MSTR MODE
7:5	4	3	2	1	0

The write-only video screen counter control register contains counter control bits for the inverted blank sync, inverted horizontal sync, and inverted vertical sync functions. This register initializes to 0x00 after reset.

Bit Definitions:

Bits	Name	Description
7:5	—	Reserved
4	INV-BLNK	Inverted Blank Sync: 1 = Blank is active low. 0 = Otherwise.
3	—	Reserved. Set at zero.
2	INVHS	Inverted Horizontal Sync: 1 = Horizontal sync is active-low.
1	INVVS	Inverted Vertical Sync: 1 = Vertical sync is active-low. 0 = Otherwise.
0	MSTR MODE	Master Mode Select: 1 = ES8381 drives sync pins. 0 = Syncs input to ES8381.

VID_SCN_OUTPUTCNTL 0x20001040h
RW **Default: N/A**

—	ZEROB	BYPASS	3TAP _EN	COEF-LDMD	CLAMP _EN	INV-MSB	YUV-8BIT	TS-MODE
15:9	8	7	6	5	4	3:2	1	0

The video screen output control register contains the control logic used to control the clamping and filtering characteristics of the signal being output to the video display.

Bit Definitions:

Bits	Name	Description
15:9	—	Reserved
8	ZEROB	Zero Boundary: 1 = Use zeroes for pixels outside of the border for horizontal filtering. 0 = Use the pixel on the edge.
7	BYPASS	Horizontal Filter Bypass: 1 = Bypass horizontal filter. 0 = Use horizontal filter.
6	3TAP_EN	3/7 Tap Filter Select: 1 = 3-tap horizontal filter selected. 0 = 7-tap horizontal filter selected.
5	COEF-LDMD	0 = UV is selected first. 1 = Y is selected first.
4	CLAMP _EN	Clamp Enable: 1 = Clamp output according to CCIR656/601 min/max values. 0 = No clamping.
3:2	INVMSB	Invert MSB YUV Output: INVMSB[1] = Invert MSB of Y output. INVMSB[0] = Invert MSB of UV output.
1	YUV8BIT	8-bit YUV Output Enable: 1 = 8-bit YUV output enabled. 0 = Invalid.
0	TSMODE	Toggle Select Mode: 1 = Y is first in 8-bit mode. 0 = UV is first in 8-bit mode.

VID_SCN_ITERFACECNTL 0x20001048h
RW **Default: N/A**

—	MM	MBM	INVHS	INVVS	INVB	1PE	EPU	MCK	CLKDIV	IPQ	CK1M
15:12	11	10	9	8	7	6	5	4	3:2	1	0

The video screen interface control register contains the control logic used to determine the signal output characteristics to the video display.

Bit Definitions:

Bits	Name	Description
15:12	—	Reserved
11	MM	Master Mode: 1 = ES8381 drives sync signals. 0 = Slave mode.
10	MBM	Master Blanking Mode: 1 = ES8381 determines blanking region. 0 = Slave mode.
9	INVHS	Invert Horizontal Sync: 1 = Horizontal sync inverted.
8	INVVS	Invert Vertical Sync: 1 = Vertical sync inverted.
7	INVB	Invert Blanking: 1 = Blanking interval inverted.
6	1PE	First Pixel Even: 1 = First pixel of active region is even.
5	EPU	Even Pixel U Select: 1 = Even pixel is U pixel. 0 = Even pixel is V pixel.
4	MCK	Master Pixel Clock Mode: 1 = ES8381 drives master clock.

UNDER NDA FOR EASTECH

Bits	Name	Description
3:2	CLK_DIV	Clock Divider: This field determines which type of video screen clock ES8381 uses for pixel clocks:

CLK_DIV1	CLK_DIV0	Description
0	0	Screen clock depends on CLK1XMOD (default).
0	1	13.5 MHz screen clock is half of input pixel clock.
1	X	6.75 MHz screen clock is one-quarter of input pixel clock.

1	IPQ	Invert PCLKQSCN: 1 = PCLKQSCN pin inverted.
0	CK1M	Clock1X Mode: 1 = Use PCLK2CN or internal 27 MHz PCLK. 0 = Use 13.5 MHz PCLKQSCN.

VID_SCN_RESETS **0x20001050h**
RW **Default: N/A**

—	R_PAN	—	R_Y	R_UV	R_HF	R_CNT	DMAGO
15:8	7	6:5	4	3	2	1	0

The video screen reset register contains the control logic for reset events, including the reset pan and scan, horizontal filtering, and DMA enabling functions. This register is set to 1 on reset.

Bit Definitions:

Bits	Name	Description
15:8	—	Reserved
7	R_PAN	Reset Pan and Scan: 1 = Reset pan and scan function (default).
6:5	—	Reserved - always 1.
4	R_Y	Reset Y FIFO: 1 = Reset Y FIFO (default).
3	R_UV	Reset UV FIFO: 1 = Reset UV FIFO (default).
2	R_HF	Reset Horizontal Filter: 1 = Horizontal filter reset (default).
1	R_CNT	Reset Counter: 1 = Counter reset (default)
0	DMAGO	DMA Enable: 1 = DMA enabled (default).

VID_SCN_STATUS **0x20001058h**
R **Default: N/A**

O_E	BLNK	HS	VS	VACT	ACT	ACTD1	ACTD2
15	14	13	12	11	10	9	8

ACTD3	1P	NL	NF	NP	EP	UP	UPD1
7	6	5	4	3	2	1	0

The video screen status register contains the status bits for the video section.

Bit Definitions:

Bits	Name	Description
15	O_E	VS/HS Odd or Even Field Status: 1 = odd field. 0 = even field.
14	BLNK	Blanking Status.
13	HS	Horizontal Sync Status.
12	VS	Vertical Sync Status.
11	VACT	Vertical Active Status.
10	ACT	Active Screen for FIFO.
9	ACTD1	Active Horizontal Filter Signal: 1 = Horizontal filtering signal active.
8	ACTD2	Active OSD/SPU/Mixer Signal: 1 = OSD/SPU/Mixer signal active.
7	ACTD3	Active Output Port Signal: 1 = Output port signal active.
6	1P	First Active Pixel for FIFO: 1 = First active pixel selected.
5	NL	New Line: 1 = First pixel of new line selected.
4	NF	New Field: 1 = First pixel of new field selected.
3	NP	New Pixel: 1 = One clock cycle of every pixel clock cycle selected.
2	EP	Even Pixel for FIFO. 1 = Current pixel selected for FIFO is even.
1	UP	U Pixel Horizontal Filter Select: 1 = Current pixel uses U for horizontal filtering. 0 = Current pixel uses V for horizontal filtering.
0	UPD1	U Pixel Mixer Select: 1 = Current pixel uses U for OSD/SPU/Mixer. 0 = Current pixel uses V for OSD/SPU/Mixer.

UNDER NDA FOR EASTECH

On-Screen Display Controller Registers

VID_SCN_OSD_HSTART 0x20001110h
RW **Default: N/A**

—	OSD_HSTART
15:13	12:0

The OSD video screen horizontal start address register contains the horizontal starting address value for the OSD, as referenced from the active display window.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	OSD_ HSTART	OSD horizontal starting address value.

VID_SCN_OSD_HEND 0x20001114h
RW **Default: N/A**

—	OSD_HEND
15:13	12:0

The OSD video screen horizontal end address register contains the 13-bit horizontal ending address value for the OSD, as referenced from the active video display.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	OSD_ HEND	OSD horizontal ending address value.

VID_SCN_OSD_VSTART 0x20001118h
RW **Default: N/A**

—	OSD_VSTART
15:13	12:0

The OSD video screen vertical start address register contains the 13-bit vertical starting address value for the OSD, as referenced from the active video display.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	OSD_ VSTART	OSD vertical starting address value.

VID_SCN_OSD_VEND 0x2000111Ch
RW **Default: N/A**

—	OSD_VEND
15:13	12:0

The OSD video screen vertical end address register contains the 13-bit vertical ending address value for the OSD, as referenced from the active video display.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12:0	OSD_ VEND	OSD vertical ending address.

VID_SCN_OSD_MISC 0x20001124h
RW **Default: N/A**

LAT_INT	RESET_OVERLAY	PAL_INDEX	INTEN	LDMD	MODE
7	6	5:4	3	2	1:0

The OSD video screen miscellaneous register contains the control logic and status bits for the OSD controller.

Bit Definitions:

Bits	Name	Description
7	LAT_INT	Latched interrupt (read-only).
6	RESET_ OVERLAY	Reset overlay section (set to 1 at reset).
5:4	PAL_ INDEX	Upper 2 bits of palette address when in 2-bit/pixel mode.
3	INTEN	Interrupt enable.
2	LDMD	Enable palette load.
1:0	MODE	Bits/Pixel Mode: 0 0 = Bypass (initializes to 00 at reset). 0 1 = 2 bit/pixel. 1 0 = 4 bit/pixel. 1 1 = 8 bit/pixel.

VID_SCN_OSD PALETTE 0x20001140h — 0x2000117Ch
RW **Default: N/A**

Y	V	U	BLND_ON/OFF	BLND
15:12	11:8	7:4	3	2:0

These 16 registers contain the OSD palette.

Bit Definitions:

Bits	Name	Description
15:12	Y	Upper 4 bits of luminance data (lower 4 bits are 0).
11:8	V	Upper 4 bits of V chrominance data (lower 4 bits are 0).
7:4	U	Upper 4 bits of U chrominance data (lower 4 bits are 0).

UNDER NDA FOR EASTECH

Bits	Name	Description
3	BLND_ ON/OFF	Blending/Transparency Enable: 1 = Blending off; transparency on. 0 = Blending on; transparency off.
2:0	BLND	Blending Value: finalpixel = blend x palette value + (1 - blend) x original pixel.

Value	Blend	Value	Blend
000	1/8	100	5/8
001	2/8	101	6/8
010	3/8	110	7/8
011	4/8	111	8/8

For mode 3 (8-bit/pixel) the upper 4 bits of the pixel are the blend information, the lower 4 bits are the palette index and the blend information in the palette is ignored.

Digital Video Encoder Registers

This section addresses the digital video encoder registers of the ES8381.

DVECTL0 **0x20001300h**
RW **Default: N/A**

—	DVE_EN
7:1	0

The DVECTL0 register is the control register for the digital video encoder module of the ES8381.

Bit Definitions:

Bits	Name	Description
7:1	—	Reserved
0	DVE_EN	Digital Video Encoder Enable: 1 = encoder enabled 0 = disabled

DVECTL1 **0x20001304h**
RW **Default: N/A**

PORCH	SQPIX_ SEL	DVE_ SETUP	SYN- CLK	FIRE	FMODE	VMODE	—
7	6	5	4	3	2	1	0

The DVECTL1 register controls the NTSC/PAL video mode select function, the square/nonsquare pixel select function, and the horizontal and vertical sync clock function. After reset, this register returns a default value of 0x0000h.

Bit Definitions:

Bits	Name	Description
7	PORCH	Standard Front/Back Porch: 1 = Pixels follow CCIR-624. 0 = Pixels follow nonsquare mode.
6	SQPIX_ SEL	Square Pixels Select: 1 = Square pixels. 0 = Nonsquare pixels (27 MHz CLK2X for both PAL and NTSC).
5	DVE_ SETUP	IRE Setup: 1 = 0.0 IRE in NTSC mode. 0 = 7.5 IRE in NTSC mode.
4	SYNCLK	Sync Slave Mode Enable: 1 = External horizontal/vertical sync. 0 = Internal horizontal/vertical sync.
3	FIRE	Fixed IRE Enable: 1 = Use as much of the DAC dynamic range as possible. 0 = All outputs are set to the same number of codes IRE.
2	FMODE	Filter Mode Select: 1 = Enhanced BW filters. 0 = Normal range for the filters.
1	VMODE	Video Mode Select: 1 = NTSC interlace. 0 = PAL interlace.
0	—	Reserved

DVECTL2 **0x20001308h**
RW **Default: 0x0000h**

TPGEN	INVERT DAC	—	COLOR KILL	TRANSI	IBLANK	DAC TEST	BYPASS
7	6	5	4	3	2	1	0

The DVECTL2 register is primarily used for testing and diagnostic purposes for the video DACs. A test pattern can also be generated in this register to check the blanking, burst and chroma signal outputs of the video encoder. After reset, this register returns a default value of 0x0000h.

Bit Definitions:

Bits	Name	Description
7	TPGEN	Test Pattern Enable: 1 = Test pattern generated.
6	INVERT DAC	Invert DACs: 1 = Data inverted before being applied to DACs.
5	—	Reserved
4	COLOR KILL	Color Kill: 1 = Burst and chroma signals are blanked out at the DACs.
3	TRANSI	Transparency input control.
2	IBLANK	Input Blank Select: 1 = Data on DVE_PD is ignored; screen is blanked. 0 = Normal blanking operation.

UNDER NDA FOR EASTECH

Bits	Name	Description
1	DACTEST	DAC Test Mode Select: 1 = Test mode. 0 = Normal operation.
0	BYPASS	Pipeline Bypass Enable: When this bit is set, input data is passed directly to the output scaling stage before being sent to the video DACs: 1 = DVE disabled.

DVECTL3 **0x2000130Ch**
RW **Default: 0x0000h**

—	DAC_DITH	DTME	PWDNV	PWDNC	PWDNY	PWDNALL
7:6	5	4	3	2	1	0

The DVECTL3 register controls the power down features of the digital video encoder and its DACs. Video DAC dithering can be disabled for diagnostic purposes, while noninterlaced NTSC and PAL scan modes can also be enabled in this register. After reset, this register returns a default value of 0x0000h.

Bit Definitions:

Bits	Name	Description
7:6	—	Reserved
5	DAC_DITH	DAC Dither Disable: 1 = Outputs to the DACs are dithered for use with 10-bit DAC. 0 = Outputs to the DACs are dithered for use with 9-bit DAC.
4	DTME	Noninterlace Mode Select: When this bit is set, this bit produces non-interlace output when in sync-lock to an interlace source: 1 = Noninterlace mode continues to generate 525 lines for NTSC and 625 lines for PAL for two fields, rather than 525 and 626 lines respectively.
3	PWDNV	V Component Video DAC Power Down: 1 = Normal operation. 0 = V component video DACs powered down.
2	PWDNC	C Component Video DAC Power Down: 1 = Normal operation. 0 = C component video DACs powered down.
1	PWDNY	Y Component Video DAC Power Down: 1 = Normal operation. 0 = Y component video DACs powered down.
0	PWDNALL	Master Video DAC Power Down: 1 = Normal operation. 0 = All video DACs powered down.

DVECTL4 **0x20001310h**
RW **Default: 0x0000h**

—	NOVER RIDE	VSYNC	HSYNC	MAT BYPASS	RGB_ DITHER	PHASE_ SH	CBSWAP
7	6	5	4	3	2	1	0

The DVERCTL4 register controls horizontal and vertical sync for the digital video decoder, RGB output select and YUV input select. The DVECTL4 register also controls RGB dithering, YUV bit swapping and RGB-to-YUV matrix conversion operation. After reset, this register returns a default value of 0x0000h.

Bit Definitions:

Bits	Name	Description
7	—	Reserved
6	NOVER RIDE	No Override Enable: 1 = No override enabled.
5	VSYNC	Vertical Sync Output Enable: 1 = Vertical sync output enabled. 0 = Cleared on reset.
4	HSYNC	Horizontal Sync Output Enable: 1 = Horizontal sync output enabled. 0 = Cleared on reset.
3	MAT BYPASS	Matrix Bypass Disable: 1 = Matrix bypass disabled. 0 = Bypass cleared on reset.
2	RGB_ DITHER	RGB Dither Enable: 1 = RGB dithering enabled. 0 = Cleared on reset.
1	PHASE_SH	YUV Phase Input Sync Clock Shift: 1 = Shift sync timing by two 2x clock for non-square formats (odd pixels start at 123).
0	CBSWAP	YUV-YCrCb Input Data Swap: 1 = YUV-YCrCb data not swapped. 0 = Data swapped.

DVECC1 **0x20001324h**
RW) **Default: 0x00h**

—	CCE_GATE	CCE_FLD2	CCE_FLD1
7:3	2	1	0

The DVECC1 register controls closed captioning features of the digital video encoder. The default value is 0x00h.

Bit Definitions:

Bits	Name	Description
7:3	—	Reserved
2	CCE_ GATE	Closed Caption Gate Enable: 1 = Enabled.
1	CCE_FLD2	Closed Caption Field 2 Enable: 1 = Field 2 enabled.
0	CCE_FLD1	Closed Caption Field 1 Enable: 1 = Field 1 enabled.

UNDER NDA FOR EASTECH

VFD_CTL **0x200013CCh**
RW **Default: 0x00h**

—		VFDCLK_FSEL	VFD_MODE	VFDK_SEL	VFD_EN

6(o)-0.4(l)]Tio2930.

The VFD control register contains the control logic for the VFD interface. This register initializes to 0x00h after reset.

Bit Definitions:

IRQ_CTL **0x200013D4h**
RW **Default: 0x00h**

The system interrupt control register contains the control logic for the ES8381. This register initializes to 0x00h after reset.

Bit Definitions:

Subpicture Unit Decoder Registers

This section describes the Subpicture Unit (SPU) decoder registers.

SP_SPCTL **0x20001600h**
RW **Default: 0x000h**

The SPU subpicture control register initializes to 0x000h after reset. Writing a 1 to the corresponding bit masks the applicable interrupt.

Bit Definitions:

UNDER NDA FOR EASTECH

Bits	Name	Description
1	RLIRQ EN	RLFIFO IRQ Enable: 1 = enable 0 = disable
0	DCSIRQ EN	DCSFIFO IRQ Enable: 1 = enable 0 = disable

SP_VCNT **0x20001700h**
RW **Default: 0x07Fh**

—	SP_VCNT
15:10	9:0

The SPU vertical counter value register After reset, this register initializes to 0x07Fh.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SP_VCNT	SPU vertical count value.

SP_VCNTREG **0x20001704h**
RW **Default: 0x7FEh**

—	SP_VCNT_INIT
15:10	9:0

The SPU vertical counter initial value register initializes to 0x7FEh after reset.

Bit Definitions:

Bits	Name	Description
15:11	—	Reserved
10:0	SP_VCNT _INIT	SPU vertical count initial value.

SP_HCNT **0x20001708h**
RW **Default: 0x0h**

—	SP_HCNT
15:11	10:0

The SPU horizontal counter value register initializes to 0x0h after reset.

Bit Definitions:

Bits	Name	Description
15:11	—	Reserved
10:0	SP_HCNT	SPU horizontal count value.

SP_HCNTREG **0x2000170Ch**
RW **Default: 0x000h**

—	SP_HCNT_INIT
15:11	10:0

The SPU horizontal counter initial value register contains the initial 10-bit value for the SPU horizontal counter, and initializes to 0x000h after reset.

Bit Definitions:

Bits	Name	Description
15:11	—	Reserved
10:0	SP_HCNT_ INIT	SPU horizontal count initial value.

SP_VSTART **0x20001710h**
RW **Default: 0x3FFh**

—	SP_VSTART
15:10	9:0

The SPU vertical start address register is the start line of subpicture display area register. After reset, this register initializes to 0x3FFh.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SP_VSTART	SPU vertical start line address value.

SP_VEND **0x20001714h**
RW **Default: 0x3FFh**

—	SP_VEND
15:10	9:0

SP_VEND is the end line of subpicture display area register. After reset, it is initialized to 0x3FFh.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SP_VEND	SPU vertical start line value.

SP_HSTART **0x20001718h**
RW **Default: 0x3FFh**

—	SP_HSTART
15:10	9:0

The contents of the horizontal start pixel of the subpicture display area register. This register initializes to 0x3FFh after reset.

UNDER NDA FOR EASTECH

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SP_HSTART	SPU horizontal start pixel value.

SP_HEND **0x2000171Ch**
RW **Default: 0x3FFh**

—	SP_HEND
15:10	9:0

SP_HEND is the horizontal pixel end of the subpicture display area register. This register initializes to 0x3FFh after reset.

Bit Definitions:.

Bits	Name	Description
15:10	—	Reserved
9:0	SP_ HEND	SPU horizontal end pixel value.

SP_SUBVCNT **0x20001720h**
RW **Default: 0x3FFh**

—	SP_SUBVCNT
15:10	9:0

SP_SUBVCNT is the subpicture vertical count register within the Subpicture display area register. This register initializes to 0x3FFh after reset.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SP_SUB VCNT	SPU subpicture display vertical count value.

SP_SUBHCNT **0x20001724h**
RW **Default: 0x3FFh**

—	SP_SUBHCNT
15:10	9:0

SP_SUBHCNT is the horizontal pixel count within the Subpicture display area register. This register initializes to 0x3FFh after reset.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SP_SUB HCNT	SPU subpicture display horizontal pixel count value.

SP_VCSTART **0x20001728h**
RW **Default: 0x3FFh**

—	SP_VCSTART
15:10	9:0

SP_VCSTART is the start line of current subpicture change register. This register initializes to 0x3FFh after reset.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SP_VC START	SPU current subpicture display vertical start scan line value.

SP_VCEND **0x2000172Ch**
RW **Default: 0x3FFh**

—	SP_VCEND
15:10	9:0

SP_VCEND is the end line of current subpicture change register. This register initializes to 0x3FFh after reset.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SP_ VCEND	SPU current subpicture display vertical end scan line value.

SP_HIVS **0x20001730h**
RW **Default: 0x3FFh**

—	SPU_HIVS
15:10	9:0

SP_HIVS is the current subpicture highlight vertical start line display area register. This register initializes to 0x3FFh after reset.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SPU_HIVS	SPU current subpicture display highlight vertical start scan line value.

UNDER NDA FOR EASTECH

SP_HIVE **0x20001734h**
RW **Default: 0x3FFh**

—	SPU_HIVE
15:10	9:0

SP_HIVE is the current subpicture highlight vertical end line display area register. This register initializes to 0x3FFh after reset.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SPU_HIVE	SPU current subpicture display highlight vertical end scan line value.

SP_HIHS **0x20001738h**
RW **Default: 0x3FFh**

—	SPU_HIHS
15:10	9:0

The SPU highlight horizontal start pixel display area register contains the 10-bit horizontal pixel starting address value for the active SPU window. This register initializes to 0x3FFh after reset.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SPU_HIHS	SPU current subpicture display highlight horizontal pixel start value.

SP_HIHE **(0x2000173Ch**
RW **Default: 0x3FFh**

—	SPU_HIHE
15:10	9:0

SP_HIHE is the current subpicture highlight horizontal end pixel display area register. This register initializes to 0x3FFh after reset.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SPU_HIHE	SPU current subpicture display highlight horizontal pixel end value.

SP_HSTART1-8 **0x20001740h—**
RW **0x200175Ch**
Default: 0x3FFh

—	SPU_HSTART
15:10	9:0

SP_HSTART [1:8] are the pixel number for start of changes 1 through 8 registers. After reset, the contents of these registers are initialized to 0x3FFh. The register bit tables for all these registers are identical to the one shown above.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:0	SPU_ HSTART	SPU current subpicture display highlight horizontal pixel change start value.

SP_VTCTL **(0x20001760h**
RW **Default: 0x0000h**

NUMCHG	CINDEX	CS	CC PAR SEEN	RLEN	CHG VAL ID	HI VAL ID
15:12	11:8	7:4	3	2	1	0

The subpicture display video timing control register initializes to 0x0000h after reset.

Bit Definitions:

Bits	Name	Description
15:12	NUMCHG	Number of changes in current horizontal stripe.
11:8	CINDEX	Code index (current region index).
7:4	CS	Current state of COL/CON state machine (read only).
3	CCPAR SEEN	1 = Start parsing COL/CON data (one clock cycle) (need to set after RISC decodes). 0 = Otherwise.
2	RLEN	1 = Current pixel in subpicture display area. 0 = Otherwise.
1	CHG VAL ID	1 = Current pixel is within a change region (i.e., not default subpicture color/contrast). 0 = Otherwise.
0	HI VAL ID	1 = Current pixel is within the highlight region. 0 = Otherwise.

UNDER NDA FOR EASTECH

SPU Contrast Index Registers

This section describes the contrast index registers in the SPU decoder.

SP_CON0 **(0x200017B0h**
RW **Default: 0x0000h**

D	C	B	A
15:12	11:8	7:4	3:0

SP_CON0 through SP_CON9 are registers containing the contrast index for a particular region and pixel type. SP_CON0 is the default subpicture display start contrast region register. This register initializes to 0x0000h after reset. The register bit tables for all these registers are identical to the one shown above.

Bit Definitions:

Bits	Name	Description
15:12	D	Contrast index for emphasis 2 pixel (type 11).
11:8	C	Contrast index for emphasis 1 pixel (type 10).
7:4	B	Contrast index for pattern pixel (type 01).
3:0	A	Contrast index for background pixel (type 00).

SP_CON1:8 **0x200017B4h–**
RW **0x200017D0h**
Default: 0x0000h

D	C	B	A
15:12	11:8	7:4	3:0

SP_CON0 through SP_CON9 are registers containing the contrast index for a particular region and pixel type. SP_CON1 through SP_CON8 are the change region registers. After reset, each register is initialized to 0x0000h. The register bit tables for all of these registers are identical to the one shown above.

Bits	Name	Description
15:12	D	Contrast index for emphasis 2 pixel (type 11).
11:8	C	Contrast index for emphasis 1 pixel (type 10).
7:4	B	Contrast index for pattern pixel (type 01).
3:0	A	Contrast index for background pixel (type 00).

SP_CON9 **0x200017D4h**
RW **Default: 0x0000h**

D	C	B	A
15:12	11:8	7:4	3:0

SP_CON0 through SP_CON9 are registers containing the contrast index for a particular region and pixel type. SP_CON9 is the highlight region register. After reset, it is initialized to 0x0000h. The register bit tables for all these registers are identical to the one shown above.

Bit Definitions:

Bits	Name	Description
15:12	D	Contrast index for emphasis 2 pixel (type 11).
11:8	C	Contrast index for emphasis 1 pixel (type 10).
7:4	B	Contrast index for pattern pixel (type 01).
3:0	A	Contrast index for background pixel (type 00).

SPU Color Index Registers

This section describes the color index registers in the SPU decoder.

SP_COL0 **0x20001780h**
RW **Default: 0x0000h**

D	C	B	A
15:12	11:8	7:4	3:0

SP_COL0 through SP_COL9 are registers containing color index for a particular region and pixel type. COL0 is the default subpicture display start color region register. This register initializes to 0x0000h after reset. The register bit tables for all these registers are identical to the one shown above.

Bit Definitions:

Bits	Name	Description
15:12	D	Color index for emphasis 2 pixel (type 11).
11:8	C	Color index for emphasis 1 pixel (type 10).
7:4	B	Color index for pattern pixel (type 01).
3:0	A	Color index for background pixel (type 00).

SP_COL1:8 **(0x20001784h–**
RW **0x20017A0h**
Default: 0x0000h

D	C	B	A
15:12	11:8	7:4	3:0

SP_COL0 through SP_COL9 are registers containing color index for a particular region and pixel type. SP_COL1:8 are the change region 1-8 registers. After

UNDER NDA FOR EASTECH

reset, each register is initialized to 0x0000. The register bit tables for all of these registers are identical to the one shown above.

Bit Definitions:

Bits	Name	Description
15:12	D	Contrast index for emphasis 2 pixel (type 11).
11:8	C	Contrast index for emphasis 1 pixel (type 10).
7:4	B	Contrast index for pattern pixel (type 01).
3:0	A	Contrast index for background pixel (type 00).

SP_COL9 (0x200017A4h
RW Default: 0x0000h

D	C	B	A
15:12	11:8	7:4	3:0

SP_COL0 through SP_COL9 are registers containing color index for a particular region and pixel type. SP_COL9 is the highlight region register. This register initializes to 0x0000h after reset. The register bit tables for all these registers are identical to the one shown above.

Bit Definitions:

Bits	Name	Description
15:12	D	Color index for emphasis 2 pixel (type 11).
11:8	C	Color index for emphasis 1 pixel (type 10).
7:4	B	Color index for pattern pixel (type 01).
3:0	A	Color index for background pixel (type 00).

Host Interface RISC Side Registers

This section describes the host interface RISC side registers.

R_HOSTDMAPORT (0x20003000h, R/W)

HOST INTERFACE RISC SIDE DMA PORT
15:0

The RISC Side DMA Port register contains data transferred to and from the host via the DMA port. After reset, this register initializes to 0x0000.

R_HOSTVCXPORT (0x20003004h, R/W)

HOST INTERFACE RISC SIDE COMMAND PORT
7:0

The RISC Side Command Port register contains data transferred to and from the host via the command port. After reset, this register initializes to 0x00.

R_HOSTDBGPORT (0x20003008h, R/W)

HOST INTERFACE RISC SIDE DEBUG PORT
7:0

The RISC Side Debug Port register contains data transferred to and from the host via the debug port. After reset, this register initializes to 0x00.

R_HOSTCTL (0x2000300Ch, R/W)

—	GW2 HST	HST2 XPT	R2H IRQ	CLR HIRQ
31:4	3	2	1	0

The RISC Side Host Control Port register contains data transferred to and from the host via the control port. After reset, this register initializes to 0x10.

Bit Definitions:

Bits	Name	Description
31:4	—	Reserved
3	GW2 HST	Gateway To Host Select: 1 = Allows data transfer from gateway to host. 0 = Allows data transfer from RISC to host.
2	HST2 XPT	Host To Transport Parser Select: 1 = Allows data transfer to transport parser. 0 = Allows data transfer to ESS RISC
1	R2H IRQ	Set RISC to Host IRQ: Writing a 1 to this bit sets the ESS RISC to Host IRQ flag.
0	CLR HIRQ	Clear Host IRQ: Writing a 1 to this bit clears the host to RISC IRQ.

R_HOSTMASK (0x20003010h, R/W)

ENDN_ SEL	DBG_ DW	DBG_ TRE	DMA_ DW	DMA_ TRE	VCX DW	VCXI TRE	H2R IRQ
7	6	5	4	3	2	1	0

The RISC Side Host Mask register contains the masking bits for interrupts from the host to the RISC. After reset, this register initializes to 0x0.

Bit Definitions:

Bits	Name	Description
7	ENDN_ SEL	Big/Little Endian Select: 1 = switch upper/lower bytes when writing to R_HOSTDMAPORT.
6:0	(multi)	Mask bits for interrupts from the host to the RISC.

UNDER NDA FOR EASTECH

R_HOSTIRQSTAT (0x20003014h, R)

—	R2H IRQ	DBG TRE	DBG DW	DMA TRE	DMA DW	VCXI TRE	VCXI DW	H2R IRQ
15:8	7	6	5	4	3	2	1	0

The RISC Side Host Interrupt Status register reads the status of interrupts being sent from the host to the RISC (1 = IRQ present, 0 = no IRQ present).

Bit Definitions:

Bits	Name	Description
15:8	—	Reserved
7	R2HIRQ	Interrupt flag set by the RISC as a signal to the host.
6	DBG TRE	Debug transmit register empty (OK for RISC to send data to the host).
5	DBGDW	Debug data waiting (RISC needs to read data from the host).
4	DMA TRE	DMA transmit register empty (OK for RISC to send data to the host).
3	DMA DW	DMA data waiting (RISC needs to read data from the host).
2	VCXI TRE	VCXI transmit register empty (OK for RISC to send data to the host).
1	VCXI DW	VCXI data waiting (RISC needs to read data from the host).
0	H2RIRQ	Interrupt flag set by the host as a signal to the RISC.

R_IDEDAT (0x20003018h, R/W)

IDE_DATA
15:0

The RISC Side Data register contains IDE bus data being sent and received to and from an ATAPI slave when the ES8381 is operating in master mode. After reset, this register initializes to 0x0000h.

R_IDEADDR (0x2000301Ch, R/W)

—	IDE_ADDR
7:3	2:0

The RISC Side IDE Address register contains the IDE bus address value sent to an ATAPI slave when the ES8381 is in master mode. This register initializes to 0x0 after reset.

Bit Definitions:

Bits	Name	Description
7:3	—	Reserved
2:0	IDE_ ADDR	IDE Address.

R_IDECTL (0x20003020h, R/W)

—	CLR IRQ	IDE 2 XPT	IDE ST	IDE RST	IDE MSK 1	IDE MSK0	IDE CS	HST MODE	IDE _EN	IDE _RW	PIO MODE
15:13	12	11	10	9	8	7	6	5	4	3	2:0

The RISC Side IDE Control register contains the control logic for interfacing with ATAPI-based loaders and other peripherals This register initializes to 0x0000h after reset.

Bit Definitions:

Bits	Name	Description
15:13	—	Reserved
12	CLRIRQ	Write 1 to clear sector-end interrupt from ATAPI slave.
11	IDE2 XPT	In master mode, writing a 1 to this bit enables data transfer from the external ATAPI device to the transport stream parser. The data transfer continues until this bit is reset to 0.
10	IDEST	Write 1 to signal the beginning of the sector. The sector start signal will be reset by the first data valid.
9	IDERST	Write 1 to reset the ATAPI slave, then write 0 to unreset. The ATAPI slave will also be reset at the same time with the ES8381.
8	IDE MSK1	Mask sector-end interrupt from ATAPI to RISC.
7	IDE MSK0	Mask interrupt from ATAPI to RISC.
6	IDECS	IDE Chip Select: 1 = Assert CS3FX#. 0 = Assert CS1FX#.
5	HST MODE	Host Mode: 1 = Master mode. Host will send read/write commands (comply to ATAPI). 0 = Slave mode. Host will receive commands or data from DMP-DSP.
4	IDE_ EN	Enable the host to write/read to/from the ATAPI slave.
3	IDE_ RW	ATAPI Slave Read/Write: 1 = Read from ATAPI slave. 0 = Write to ATAPI slave.
2:0	PIO MODE	Programmable IO Mode Select:

Bit 2	Bit 1	Bit 0	Maximum Transfer Rate
0	0	0	3.33 MB/0
0	0	1	5.22 MB/0
0	1	0	11.11 MB/0

UNDER NDA FOR EASTECH

R_IDESSTAT (0x20003024h, W)

—	IDEIRQ	IDE16	IDEVAL
7:3	2	1	0

The write-only RISC Side IDE Status register contains the status information for the IDE bus interface.

Bit Definitions:

Bits	Name	Description
7:3	—	Reserved
2	IDEIRQ	1 = Sector-end interrupt from ATAPI slave to RISC.
1	IDE16	IDE 16/8-Bit Transfer: (read only) 1 = 16-bit transfer: If reading from ATAPI slave, all 16-bit data of R_IDEDAT are valid. If writing to ATAPI slave, all 16-bit data of R_IDEDAT are received at the ATAPI slave. 0 = 8-bit transfer: If reading from ATAPI slave, only the last 8 bits of R_IDEDAT are valid. If writing to ATAPI slave, only the last 8 bits of R_IDEDAT are received at the ATAPI slave.
0	IDEVAL	1 = PIO cycle is completed. In read mode, read from R_IDEDAT to retrieve the data from the ATAPI slave; write 1 to clear this bit.

R_IDECNT (0x20003028h, R/W)

—	IDE_CNT
15:12	11:0

The RISC Side IDE Bus Counter register contains the counter mechanism for the IDE bus interface of the ES8381 when configured to be in Master Mode. This register initializes to 0x07FFh after reset.

Bit Definitions:

Bits	Name	Description
15:12	—	Reserved
11:0	IDE_ CNT	Reading from this register returns the IDE bus interface count down value.

Host Interface Host Side Registers

This section describes the host interface host side registers of the ES8381.

H_HOSTDMAPORT (0x0, R/W)

HOST INTERFACE (DMA PORT) DATA

15:0

The Host Side DMA Port register contains memory and I/O data transferred to and from the RISC. After reset, this register initializes to 0x0000.

H_HOSTVCXPORT (0x1, R/W)

HOST INTERFACE (COMMAND PORT) DATA

7:0

The Host Side Command Port register contains control and status data transferred to and from the RISC. After reset, this register initializes to 0x00.

H_HOSTDBGPORT (0x2, R/W)

HOST INTERFACE (DEBUG PORT) DATA

7:0

The Host Side Debug Port register transfers data to and from the RISC during debugging. After reset, this register initializes to 0x00.

H_HOSTCTL (0x3, R/W)

H2R_IRQ	OSEL	ISEL	CLR_RIRQ
7	6:4	3:1	0

The Host Side Control register enables and disables the host-to-RISC and RISC-to-host interrupt capabilities of the ES8381. After reset, this register initializes to 0x00.

Bit Definitions:

Bits	Name	Description
7	H2R_IRQ	Host to RISC IRQ Enable: Writing a 1 to this bit sets the host to RISC IRQ flag.
6:4	OSEL	Select which TRE and DW bits are sent to the HRRQ read request pins. HRRQ = (DMA_DW and OSEL_0) or (VCX_DW and OSEL_1) or (DBG_DW and OSEL_2).
3:1	ISEL	Select which TRE and DW bits are sent to the HWRQ (write request) pins. HWRQ = (DMA_TRE and ISEL_0) or (VCX_TRE and ISEL_1) or (DBG_TRE and ISEL_2).

UNDER NDA FOR EASTECH

H_HOSTMASK (0x4, R/W)

ENDN_ SEL	DBG_ TRE	DBG_ DW	DMA_ TRE	DMA_ DW	VCXI _TRE	VCXI _DW	R2R_ IRQ
7	6	5	4	3	2	1	0

The Host Side Interrupt Mask register initializes to 0x00 after reset.

Bit Definitions:

Bits	Name	Description
7	ENDN_ SEL	Host Side Endian Select: When set, this bit switches the upper and lower bytes of data sent as writes to the Host Interface DMA Port register. 1 = switch upper/lower bytes.
6	DBG_ TRE	Host To RISC Debug Transmit Register Empty Flag.
5	DBG_ DW	RISC To Host Debug Data Waiting Flag: 1 = Host ready to read debug data from ESS RISC.
4	DMA_ TRE	Host To RISC DMA Transmit Register Empty Flag: 1 = Host ready to send DMA data to ESS RISC.
3	DMA_ DW	DMA Data Waiting: 1 = Host waiting to read data from ESS RISC.
2	VCXI_ TRE	VCXI Transmit Register Empty: 1 =Host ready to send data to ESS RISC.
1	VCXI_ DW	VCXI Data Waiting: 1 = Host waiting to read data from ESS RISC.
0	R2R_ IRQ	Interrupt Flag: 1 = Set by ESS RISC as Ready To Receive signal to the host.

H_HOSTIRQSTAT (0x5, R)

H2R_IR Q	DBG_ TRE	DBG_ DW	DMA_ TRE	DMA DW	VCXI_ TRE	VCXI_ DW	R2H_ IRQ
7	6	5	4	3	2	1	0

The read-only Host Side Host Interrupt Status register reads the status of Interrupts from the ESS RISC to the host (1 = IRQ present, 0 = No IRQ present).

Bit Definitions:

Bits	Name	Description
7	H2R_ IRQ	Host To RISC Interrupt Flag: Set by the host as a signal to the RISC to generate an interrupt.
6	DBG_ TRE	Host To RISC Debug Transmit Register Empty Flag: When set, host sends data to the RISC.
5	DBG_ DW	Host To RISC Debug Data Waiting Flag: When set, host can read data from the RISC.
4	DMA_ TRE	Host To RISC DMA Transmit Register Empty Flag: When set, host sends data to the RISC.
3	DMA_ DW	Host To RISC DMA Data Waiting Flag: When set, host reads DMA data from the RISC.
2	VCXI_ TRE	VCXI Transmit Register Empty: OK for host to send data to the RISC.
1	VCXI_ DW	VCXI Data Waiting: Host needs to read data from the RISC.
0	R2H_ IRQ	Interrupt Flag: Set by the RISC as a signal to the host.

Host Interface RISC-SRAM Interface Registers

This section describes the RISC-SRAM interface registers associated with the host interface of the ES8381.

RIFACE_WIDTH (0x20004000h, R/W)

—	DBGMODE	CACHEFLS	CACHE DISABLE	DIV	B3W	B2W	B1W	B0W
15:11	10	9	8	7:5	4	3	2	1:0

The RISC-SRAM Interface Width register controls the internal cache.

Bit Definitions:

Bits	Name	Description
15:11	—	Reserved
10	DBGMODE	Debug Mode: 0 = Save power from outside pins toggling. 1 = riscaddr and riscbus are seen from the SRAM address/data. Default is a 1 after reset.
9	CACHEFLS	Cache Flush: When set to 1, the memory cache is flushed. Default is a 1 after reset. 1 = flush cache 0 = normal operation
8	CACHE DISABLE	Cache Disable: 0 = cache enabled 1 = cache bypassed Default is a 1 after reset.
7:5	DIV	Clock Divisor

UNDER NDA FOR EASTECH

Bits	Name	Description
4	B3W	Bank 3 Width: 1 = Reserved 0 = 8 bits wide
3	B2W	Bank 2 Width: 1 = Reserved 0 = 8 bits wide
2	B1W	Bank 1 Width: 1 = Reserved 0 = 8 bits wide
1:0	B0W	Bank 0 Width [1:0]: 00 = 8-bit wide (default) 01 = Reserved 10 = Map Bank 0 to DRAM 11 = Undefined

RIFACE_WAIT_STATE (0x20004004h, R/W)

—	BANK3	BANK2	BANK1	BANK0
31:20	19:15	14:10	9:5	4:0

The RISC-SRAM Interface Wait State register contains the logic for the total number of possible external wait states that can be inserted per access for SRAM banks 3:0. Up to 32 wait states can be inserted if desired. Table 32 gives the hexadecimal value for each number of possible wait states:

Table 32 Hex Values for Wait States

Hex Value	Wait State	Hex Value	Wait State	Hex Value	Wait State	Hex Value	Wait State
1F	1	17	9	0F	17	07	25
1E	2	16	10	0E	18	06	26
1D	3	15	11	0D	19	05	27
1C	4	14	12	0C	20	04	28
1B	5	13	13	0B	21	03	29
1A	6	12	14	0A	22	02	30
19	7	11	15	09	23	01	31
18	8	10	16	08	24	00	32 (default)

RIFACE_AUX1 (0x2000402Ch, R/W)

—	0	T3	T2	P3	P2	P1	P0
15:10	9:6	5	4	3	2	1	0

This register is a general I/O port for interfacing with external devices.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9:6	—	Reserved (always 0)
5:4	T3,T2	Tri-state Controls: 1 = I/O state selected 0 = Tri-state selected
3:2	P3, P2	Tri-stateable pins.
1:0	P1, P0	Open collector pins.

When this register is read, the values read are the values at the pin. The two open collector pins allow I²C bus communication and require an external pull-up resistor. The default value is for P3:P2 to be tri-state, and P1:P0 to be disabled (i.e., P1, P0 = high (logic 1), and T3, T2 = low (logic 0)).

RIFACE_AUX2 (0x20004030h, R/W)

—	T	P
15:8	7:4	3:0

This register is a second general-purpose I/O port with four tri-state channels.

Bit Definitions:

Bits	Name	Description
15:8	—	Reserved
7:4	T	Tri-stateable controls
3:0	P	Tri-stateable pads

When this register is read, the values read are the values at the pin. Default values for tri-state controls are 0 (tri-state) at reset.

I2C Registers

TI2C (0x20005400h, R/W)

TI2C
7:0

Bit Definitions:

Bits	Name	Description
7:0	TI2C	TI²C

MADR (0x20005404h, R/W)

MADR
7:0

Bit Definitions:

Bits	Name	Description
7:0	MADR	MADR

UNDER NDA FOR EASTECH

MBCR (0x20005408h, R/W)

MBCR
7:0

Bit Definitions:

Bits	Name	Description
7:0	MBCR	MBCR.

MBDR8 (0x2000541Ch, R/W)

MBDR8
7:0

Bit Definitions:

Bits	Name	Description
7:0	MBDR8	MBDR8.

MBSR (0x2000540Ch, R/W)

MBSR
7:0

Bit Definitions:

Bits	Name	Description
7:0	MBSR	MBSR.

MBDR12 (0x20005420h, R/W)

MBDR12
7:0

Bit Definitions:

Bits	Name	Description
7:0	MBDR12	MBDR12.

MBNR (0x20005410h, R/W)

MBNR
7:0

Bit Definitions:

Bits	Name	Description
7:0	MBNR	MBNR.

MBMR (0x20005424h, R/W)

MBMR
7:0

Bit Definitions:

Bits	Name	Description
7:0	MBMR	MBMR.

MBDR0 (0x20005414h, R/W)

MBDR0
7:0

Bit Definitions:

Bits	Name	Description
7:0	MBDR0	MBDR0.

I2C_CTL (0x20005500h, R/W)

I2C_CTL
7:0

Bit Definitions:

Bits	Name	Description
7:0	I2C_CTL	I2C Control.

MBDR4 (0x20005418h, R/W)

MBDR4
7:0

Bit Definitions:

Bits	Name	Description
7:0	MBDR4	MBDR4.

UNDER NDA FOR EASTECH

SD Registers

SD_CMD_DAT (0x2000560Ch, R/W)

SD_CMD_DAT
7:0

Bit Definitions:

Bits	Name	Description
7:0	SD_CMD_DAT	SD Command Data.

SD_RES_TO (0x20005610h, R/W)

SD_RES_TO
7:0

Bit Definitions:

Bits	Name	Description
7:0	SD_RES_TO	SD Resend TO.

SD_RCVD_TO (0x20005614h, R/W)

SD_RCVD_TO
7:0

Bit Definitions:

Bits	Name	Description
7:0	SD_RCVD_TO	SD Received TO.

SD_BLK_LEN (0x20005618h, R/W)

RD_BLK_LEN	WR_BLK_LEN
7:4	3:0

Bit Definitions:

Bits	Name	Description
7:4	RD_BLK_LEN	Read Block Length: This field contains the maximum length of the read data block.
3:0	WR_BLK_LEN	Write Block Length: This field contains the maximum length of the write data block.

SD_NO_BLKS (0x2000561Ch, R/W)

SD_NO_BLKS
7:0

Bit Definitions:

Bits	Name	Description
7:0	SD_NO_BLKS	SD No Blocks.

SD_INT_MSK (0x20005620h, R/W)

SD_INT_MSK
7:0

Bit Definitions:

Bits	Name	Description
7:0	SD_INT_MSK	SD Interrupt Mask.

SD_CMD_0 (0x20005624h, R/W)

SD_CMD_0
7:0

Bit Definitions:

Bits	Name	Description
7:0	SD_CMD_0	SD Command 0.

SD_CMD_1 (0x20005628h, R/W)

SD_CMD_1
7:0

Bit Definitions:

Bits	Name	Description
7:0	SD_CMD_1	SD Command 1.

UNDER NDA FOR EASTECH

SD_CMD_2 (0x2000562Ch, R/W)

SD_CMD_2
7:0

Bit Definitions:

Bits	Name	Description
7:0	SD_CMD_2	SD Command 2.

SD_BUF_RDY (0x20005630h, R/W)

SD_BUF_RDY
7:0

Bit Definitions:

Bits	Name	Description
7:0	SD_BUF_RDY	SD Buffer Ready.

SD_RES_REG (0x20005634h, R/W)

SD_RES_REG
7:0

Bit Definitions:

Bits	Name	Description
7:0	SD_RES_REG	SD Resend Register.

SD_STATUS (0x20005640h, R/W)

SD_STATUS
7:0

Bit Definitions:

Bits	Name	Description
7:0	SD_STATUS	SD Status.

UART Port Registers

IOPORT_UART_ADDR (0x20005880h, R/W)

IOPORT_UART_ADDR
7:0

Bit Definitions:

Bits	Name	Description
7:0	IOPORT UART_ADDR	I/O Port UART Address.

IOPORT_UART_ADDR (0x20005884h, R/W)

IOPORT_UART_ADDR
7:0

Bit Definitions:

Bits	Name	Description
7:0	IOPORT UART_ADDR	I/O Port UART Address.

IOPORT_UART_CONFIG (0x20005888h, R/W)

BHL	IEDL	IDFIFO	LCR	MCR	LSR	MSR	SCR
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	BHL	Buffer/Hold/Divisor Latch (Low):

R/W	Name	Abbr.
R	Receive Buffer Register	RBR
W	Transmit Holding Register	THR
R/W	Divisor Latch (Low)	DLL

Bits	Name	Description
6	IEDL	Interrupt Enable/Divisor Latch (High):

R/W	Name	Abbr.
R/W	Interrupt Enable Register	RBR
R/W	Divisor Latch (High)	DLH

Bits	Name	Description
5	IDFIFO	Interrupt Identity/FIFO Control:

R/W	Name	Abbr.
R	Interrupt Identity Register	IIR
W	FIFO Control Register	FCR

Bits	Name	Description
4	LCR	Line Control Register.
3	MCR	Modem Control Register.
2	LSR	Line Status Register.
1	MSR	Modem Status Register.
0	SCR	Scratch Register.

UNDER NDA FOR EASTECH

Bus Controller Registers

Bus Controller (Video Processor) Registers

This section describes the video processor registers of the bus controller module in detail.

BUSCON_VP_CONTROL **0x20008000h**
RW **Default: N/A**

—	DVE_108	LOAD_VP	VP_RST#
15:3	2	1	0

The bus controller video processor control register contains the control logic for the video processor core.

Bit Definitions:

Bits	Name	Description
15:3	—	Reserved
2	DVE_108	Video PLL frequency Select: 1 = 108 MHz frequency selected 0 = 54 MHz frequency selected (default)
1	LOAD_VP	Load Video Processor Microcode: 1 = load microcode 0 = don't load
0	VP_RST#	Video Processor Reset: 1 = enabled 0 = reset

BUSCON_VP_STATUS **0x20008004h**
R **Default: N/A**

—	SEQ	TRD	IOSM	CMDQ_ST
15:5	4	3	2	1:0

The read-only bus controller video processor status register provides status information on the core components of the video processor, including the I/O state machine, the sequencer, and the command queue.

Bit Definitions:

Bits	Name	Description
15:5	—	Reserved
4	SEQ	Sequencer status.
3	TRD	Transfer ready status.
2	IOSM	I/O State machine status.
1:0	CMDQ_ST	Command queue status.

Bus Controller (Memory Controller) Registers

This section describes the memory controller registers of the bus controller module in detail.

BUSCON_DRAM_CONTROL **(0x20008100h, R/W)**

—	SEL_SCLKEN
31:17	16

SD64M	SD8BIT	BIGEDO	SDCF	SREFEN	REFEN
15	14	13	12:11	10	9

—	RASPRE	RASDEL	SPDEDO
8:6	5:4	3:2	1:0

The bus controller DRAM control register contains the control logic for the video memory interface. This register initializes to 0x0000h after reset.

Bit Definitions:

Bits	Name	Description
31:17	—	Reserved
16	SEL SCLK EN	DRAM Clock Enable: 1 = Pin 70 is SDSCLKEN. 0 = Pin 70 is DOE#.
15	SD64M	DRAM Type Select: 1 = Use 64 Mb DRAM. 0 = Use 16 Mb DRAM.
14	SD8 BIT	DRAM 8-bit Select: 1 = DRAM type is x8. 0 = DRAM type is x16. **Note:** If the memory used is of 128 Mb type (16 MB total memory), set SD8BIT to 1.
13	BIG EDO	EDO DRAM Select: 1 = EDO is 1M x 16. 0 = EDO is 256K x 16.
12:11	SDCF	Memory Configuration:

Mem Size (MB)	SD 64M	SD 8BIT	SD CFG1	SD CFG0	Memory Configuration (Mb per pc)
2	0	0	0	1	1 pc: 512kx16x2 (16 Mb)
4	0	0	0	0	2 pc: 512kx16x2 (16 Mb)
4	0	1	0	1	2 pc: 1Mx8x2 (16 Mb)
8	0	1	0	0	4 pc: 1Mx8x2 (16 Mb)
8	1	0	—	—	1 pc: 1Mx16x4 (64 Mb)
16	1	0	—	—	2 pc: 1Mx16x4 (64 Mb)
16	1	1	—	—	2 pc: 2Mx8x4 (64 Mb)
16	1	1	—	—	1 pc: 2Mx16x4 (128 Mb)

UNDER NDA FOR EASTECH

Bits	Name	Description
10	SREF EN	DRAM Refresh Enable: 1 = Refresh logic for DRAM enabled.
9	REF EN	EDO Refresh Enable: 1 = Refresh logic for EDO DRAM enabled.
8:6	—	Reserved
5:4	RAS PRE	RAS precharge time control for EDO.
3:2	RAS DEL	RAS to CAS delay time.
1:0	SPD EDO	EDO DRAM speed select.

BUSCON_DRAM_SREFTIME (0x20008114h
RW Default: N/A

INTVAL
7:0

The bus controller DRAM refresh time register controls the DRAM refresh period for the system, and contains the refresh interval value. After reset, it is not initialized.

Bit Definitions:

Bits	Name	Description
7:0	INTVAL	DRAM refresh interval value.

Bus Controller (Command Queue) Registers

This section describes the command queue registers of the bus controller module in detail.

BUSCON_CMDQUE_
VPDMASETUP 0x20008200h
W Default: N/A

—	BK	DIR	HINT	DWS	DB	WX	DWS	DELY	DELX
31:25	24	23	22	20	19	18	17:16	15:9	8:0

The BUSCON_CMDQUE_VPDMASETUP register takes the video processor DMA access requests directed to the command queue and prioritizes the DMA requests.

Bit Definitions:

Bits	Name	Description
31:25	—	Reserved
23	BK	Break: When set, this bit sends the BREAK# signal to the VP at the end of a line.
23	DIR	Data Transfer Direction: 1 = Memory to VP. 0 = VP to memory.
22	HINT	VP Hint Block: When set, this bit blocks the DMA arbitration to the extent that the next VP DMA request will be granted over requests at the same level or below the current request level for a back-to-back VP DMA transaction.
20	DWS	Select DMA Width Enable: 1 = DMA Width select feature enabled. 0 = Disabled.
19	DB	Double DMA Width Select: 1 = Double DMA width selected. 0 = Single DMA width selected.
18	WX	Select Delta X as DMA Width Register: 1 = Use DMA Width register. 0 = Use DELX as DMA Width register.
17:16	DWS	DMA Width Register Select: This 2-bit field permits the selection of up to one of eight possible DMA width registers, depending on the DMA width selected by DB bit (bit 19) of this register. Four single DMA width registers and four double DMA width registers are available to support the desired DMAs for the memory configuration implemented in the design.
15:9	DELY	Transfer Y longwords
8:0	DELX	Transfer X scan lines.

GMC/QPEL Block Registers

This section describes the GMC/QPEL registers.

EXECUTE_CMD (0x20009E00h, R/W)

SFGO	—	ST_ADDR1
31	30:25	24:16

SFRST	—	ST_ADDR0
15	14:9	8:0

This register contains the GQH commands and program starting addresses.

Bit Definitions:

Bits	Name	Description
31	SFGO	Software Go Command: Writing a ‘1’ to this bit will trigger an execution. This bit is *self clearing*.
30:25	—	Reserved
24:16	ST_ADDR1	Starting Address - Program 1 [8:0]
15	SFRST	Software Reset Command: Writing a ‘1’ to this bit will do a software reset on the hardware. This bit is *self clearing*.
14:9	—	Reserved
8:0	ST_ADDR0	Starting Address - Program 0 [8:0]

UNDER NDA FOR EARLY TEST

DATAFMT (0x20009E48h, R/W)

TBK	DMAWSEL	—	REF-MODE	BLK-MODE	DP BYTE
31	30:28	27:22	21:20	19:18	17:16

DI INV	DIORD	DO INV	DOORD	DOQY	DOQX
15	14:12	11	10:8	7:4	3:0

This register contains the GQH data format control.

Bit Definitions:

Bits	Name	Description
31	TBK	Two Breaks: There are two breaks per one horizontal input data line: 0 no break suppression 1 suppress the first break
30:28	DMAWSEL	DMA Width Register Select [2:0]: These bits select the appropriate DMA Width register: 0 0 0 - DMA Width register 0 0 0 1 - DMA Width register 1 0 1 0 - DMA Width register 2 0 1 1 - DMA Width register 3 1 0 0 - DMA Width register 4 1 0 1 - DMA Width register 5 1 1 0 - DMA Width register 6 1 1 1 - DMA Width register 7
27:22	—	Reserved
21:20	REFMODE	Reference Mode [1:0]: These bits select the number of reference bk/mb: 0 0 - no reference bk/mb 0 1 - one reference bk/mb 1 0 - two reference bk/mb 1 1 - reserved
19:18	BLKMODE	Block Mode [1:0]: These bits select the transfer size of the video data block: 0 0 - 8x8 0 1 - 16x16 1 0 - 16x8 1 1 - reserved
17:16	DPBYTE	Bytes Dropped [1:0]: These bits select the number of bytes to be dropped when reading in from DMA on DW boundary: 0 0 - no drop 0 1 - drop 1 byte 1 0 - drop 2 bytes 1 1 - drop 3 bytes
15	DIINV	Data Input Invert: Writing a '1' to this bit inverts bit 7 of the data input.
14:12	DIORD	Data Input Reformat [2:0]: When the original data order is A, B, C, D: 0 0 0 - A B C D 0 0 1 - B A D C 0 1 0 - C D A B 0 1 1 - D C B A 1 0 0 - A C B D 1 0 1 - C A D B 1 1 0 - B D A C 1 1 1 - D B C A
11	DOINV	Data Output Invert: Writing a '1' to this bit inverts bit 7 of the data output.
10:8	DOORD	Data Output Reformat [2:0]: When the original data order is A, B, C, D: 0 0 0 - A B C D 0 0 1 - B A D C 0 1 0 - C D A B 0 1 1 - D C B A 1 0 0 - A C B D 1 0 1 - C A D B 1 1 0 - B D A C 1 1 1 - D B C A
7:4	DOQY	Y Output Number of Lines [3:0]: These bits select the number of lines to output at Y (vertical) direction. This number must be in multiples of four. 0 - 4 lines 1 - 8 lines : n - (n+1) x 4 lines
3:0	DOQX	X Output Number of Bytes [3:0]: These bits select the number of bytes to output at X (horizontal) direction. This number must be in multiples of four. 0 - 4 bytes 1 - 8 bytes : n - (n+1) x 4 bytes

UNDER NDA FOR EASTECH

DMA_SETUP (0x20009E50h, R/W)

DELTY	DELTX
31:26	25:22

DMA_ADDR
21:0

This register contains the address and DELTY and DELTX data for DMA setup.

Bit Definitions:

Bits	Name	Description
31:26	DELTY	Delta Y [5:0]: These bits indicate the number of lines of vertical direction.
25:22	DELTX	Delta X [3:0]: These bits indicate the number of pixels of horizontal direction in dword.
21:0	DMA_ADDR	DMA DRAM Address [21:0]: These bits are the DRAM address for DMA.

CMD_CONTROL (0x20009EFCh, R/W)

CMQ RST	CMQ EMTY	CMQ FULL	—	CMQLVL
15	14	13	12:6	5:0

This register contains the command queue control bits.

Bit Definitions:

Bits	Name	Description
15	CMQRST	Command Queue Software Reset: Writing a '1' to this bit will cause a software reset of the command queue.
14	CMQEMTY	Command Queue Empty: A '1' for this bit indicates that the command queue is empty.
13	CMQFULL	Command Queue Full: A '1' for this bit indicates that the command queue is full.
12:6	—	Reserved
5:0	CMQLVL	Command Queue Level [5:0]: These bits represent the number of commands left in the queue.

HDMI_MUX 0x2000C400h
RW Default: 0x00h

—	H_MUX	—
15:10	9	8:0

This register controls the muxing of the HDMI signals. After reset, it is initialized to 0x00.

Bit Definitions:

Bits	Name	Description
15:10	—	Reserved
9	H_MUX	HDMI 12-bit Mux Select. When this bit is set, the lower HDMI 12-bit data and control signals are output as follows:

Signal Name	Muxed To
HDMI_D0	YUV0 (pin 52)
HDMI_D1	YUV1 (pin 53)
HDMI_D2	YUV2 (pin 118)
HDMI_D3	YUV3 (pin 117)
HDMI_D4	YUV4 (pin 167)
HDMI_D5	YUV5 (pin 166)
HDMI_D6	YUV6 (pin 165)
HDMI_D7	YUV7 (pin 164)
HDMI_D8	MSD0 (pin 67)
HDMI_D9	MSD1 (pin 66)
HDMI_D10	SIN (pin 32)
HDMI_D11	HDMI_D11 (pin 31)
HDMI_CLK	PCLKQSCN (pin 163)
HDMI_ACT	HRDQ# (pin 244)
HDMI_HSYNC	HWRQ# (pin 243)
HDMI_VSYNC	VSYNC (pin 41)

0 = Muxing disabled.

8:0	—	Reserved

UNDER NDA FOR EASTECH

CFG **0x2000C404h**
RW **Default: 0x00h**

—	USB_EN	—
31:28	27	26:24

—	PLL_USB USB_A_PD	PLL_HD PD	—	PLL_HD_DIV
23	22	21	20:17	16

PLL_HD_DIV	PLL_HD_ DUTY_SEL	PLL_HD_ DELAY_SEL	SD_ SRESET	SD_EN
15:14	13:12	11:10	9	8

CLKHD_SEL	BYPASS_8051	—
7	6	5:0

This control register enables the corresponding functions and clocks. After reset, it is initialized to 0x00.

Bit Definitions:

Bits	Name	Description
31:28	—	Reserved
27	USB_EN	USB Enable: 1 = Enable USB. 0 = Disable USB
26:23	—	Reserved
22	PLL_ USB_ USB_A _PD	PLL_USB and USB_A Power Down: 1 = Power down PLL_USB and USB_A. 0 = Power on PLL_USB and USB_A.
21	PLL_ HD_PD	PLL_HD Power Down: 1 = Power down PLL_HD. 0 = Power on PLL_HD.
20:17	—	Reserved
16:14	PLL_HD_ DIV	PLL HD Divider Select:

SS2	SS1	SS0	DIV_NUM	Freq (MHz)
0	0	0	18	121.5
0	0	1	20	135
0	1	0	14	Bypass
0	1	1	16	108.0
1	0	0	17	114.75
1	0	1	19	128.25
1	1	0	22	148.5
1	1	1	24	162.0

Bits	Name	Description
13:12	PLL_HD DUTY_ SEL	PLL HD Duty Select:

SS2	SS1	SS0	DIV_NUM	Duty Cycle
0	0	0	18	8/10
0	0	1	20	8/12
0	1	0	14	6/8
0	1	1	16	8/8
1	0	0	17	8/9
1	0	1	19	8/11
1	1	0	22	8/14
1	1	1	24	8/15

11:10	PLL_HD_ DELAY_ SEL	PLL_HD Delay Select.
9	SD_ SRESET	Secure Digital Soft Reset: 1 = Assert SD software reset. 0 = Reset deasserted.
8	SD_EN	Secure Digital Enable: 1 = Secure Digital function enabled. 0 = Disabled.
7	CLKHD_ SEL	HD Clock Select: 1 = Select system clock as HD-DVE clock. 0 = Select PLL_HD clock as HD-DVE clock.
6	BYPASS _8051	Bypass 8051: 1 = Enable bypass_8051. 0 = Disable bypass_8051.
5:0	—	Reserved

CLKSEL **0x2000C420h**
RW **Default: 0x00h**

SLICER_MAX	SLICER_MIN
31:24	23:16

SLICER_ EN	UART1 _EN	—	SEL_CS1	UART_ HISPD	USBCK_ SEL	PLLUSB_ ON	EXT_HST _MST
15	14	13	12	11	10	9	8

—	UART_EN	—	YUV_OUT_SEL	—	DIS_HST_IO	—	CLK33M_OUT
7	6	5	4	3	2	1	0

This control register enables the corresponding functions and clocks. After reset, it is initialized to 0x00.

Bit Definitions:

Bits	Name	Description
31:24	SLICER_ MAX	Maximum Slicer Value.
23:16	SLICER_ MIN	Minimum Slicer Value.

UNDER NDA FOR EASTECH

Bits	Name	Description
15	SLICER_EN	Slicer Enable: 1 = Enabled.
14	UART1_EN	UART 1 Enable: 1 = uart_sin and uart_sout mapped to AUX7-6. 0 = Mapping disabled.
13	—	Reserved
12	SEL_CS1	CS1 Select: 1 = Select SD_CS1 as DRAS1# out. 0 = Select original RAS0 # as DRAS1# out.
11	UART_HISPD	UART High Speed Clock Select: 1 = Select system clock / 3 as UART input clock. 0 = Select system clock / 4 as UART input clock.
10	USBCK_SEL	PLL USB Clock Select: 1 = 148.5 MHz selected for PLL USB clock. 0 = 162.0 MHz selected.
9	PLLUSB_ON	PLL USB On: 1 = PLL USB powered down. 0 = PLL USB power on.
8	EXT_HST_MST	External Host Master: 1 = External host mastering enabled. 0 = Disabled.
7	—	Reserved
6	UART_EN	UART Enable: 1 = Enable UART. 0 = Disabled.
5	—	Reserved
4	YUV_OUT_SEL	YUV Output Select: 1 = Enable YUV data to pads. 0 = Disabled.
3	—	Reserved
2	DIS_HST_IO	Disable Host I/O: 1 = Disable host I/O. 0 = Enable host I/O.
1	—	Reserved
0	CLK33M_OUT	CLK33M Out: 1 = Send CLK33M to SPDIF_OUT. 0 = Don't send.

Audio Interface Registers

This section describes all the registers controlling the audio section, and serves as a reference for both hardware and firmware engineers who need to understand the internal workings of the ES8381.

AUDIOCTL **0x2000D008h**
RW **Default: 0x00h**

AIEN	AMS	AREN	AXEN	ABEN	DM	SRST	—
7	6	5	4	3	2	1	0

This audio control register enables the corresponding functions and clocks. After reset, it is initialized to 0x00.

Bit Definitions:

Bits	Name	Description
7	AIEN	Audio Interrupt Enable: The corresponding port must be enabled for proper interrupt status. 0 = disabled 1 = enabled
6	AMS	Audio Master Clock Selection: 0 = external MCLK 1 = internal MCLK
5	AREN	Audio Receive Enable: 0 = disabled 1 = enabled
4	AXEN	Audio Transmit Enable: The DMA must be started before enabling the transmit port: 1 = Audio transmit enabled. 0 = Audio transmit disabled.
3	ABEN	Audio bit clock generator enable (used only when internal MCLK is selected).
2	DM	Data input (either from pri_bus or risc) Debug Mode: 0 = data from pri_bus. 1 = data from risc_bus.
1	SRST	Soft reset: This bit will self-reset when a 1 is written.
0	—	Reserved

UNDER NDA FOR EASTECH

AUDIOXMT **0x2000D00Ch**
RW **Default: 0x0000h**

TLSB	TDGE	TDFS	TDM	TCF	TFM	ITFS	TBCS	AM	TBCF
15	14	13	12:10	9:8	7:6	5	4	3:2	1:0

This audio transmit format register is used for setting up the format for the transmit port. After reset, the register is initialized to 0x0000h.

Bit Definitions:

Bits	Name	Description
15	TLSB	Transmit LSB Select: 1 = LSB first 0 = MSB first
14	TDGE	Transmit Bit Clock Edge Select: 1 = Output data on falling edge of clock. 0 = Output data on rising edge of clock.
13	TDFS	Transmit Data Frame Sequence Select: 1 = Last bit sent on last cycle. 0 = First bit sent on first cycle.
12:10	TDM	Transmit Data Frame Mode Select: 000 = 16-bit data frame 001 = 18-bit data frame 010 = 20-bit data frame 011 = 24-bit data frame 100 = 32-bit data frame 101 = Reserved 11x = Reserved
9:8	TCF	Transmit Cycle Frame: 00 = 16-bit cycle frame 01 = 24-bit cycle frame 10 = 32-bit cycle frame 11 = Reserved
7:6	TFM	Transmit Frame Mode: 00 = normal mode 01 = Left justified mode 10 = right justified mode 11 = Reserved
5	ITFS	Inverse Audio Transmit Frame Sync: 1 = enabled 0 = disabled
4	TBCS	Audio Bit Clock Select: 1 = Use internal bit clock and output bit clock. 0 = Use external bit clock.
3:2	AM	Audio Mode Select: 00 = Stereo L-R channel 01 = Dolby Digital (5.1 channel) 10 = MPEG-2 audio (7.1 channel) 11 = Reserved
1:0	TBCF	Audio Transmit Bit Clock Frequency Select: 00 = MCLK/8 01 = MCLK/4 10 = MCLK/2 11 = MCLK/16

AUDIORCV **0x2000D010h**
RW **Default: 0x0000h**

RLSB	RDGE	RDFS	—	RDM	RCF	RFM	IRFS	RBCS	—	RBCF
15	14	13	12	11:10	9:8	7:6	5	4	3:2	1:0

This is the audio receive format register. After reset, it is initialized to 0x0000h.

Bit Definitions:

Bits	Name	Description
15	RLSB	Receive LSB Select: 1 = LSB first 0 = MSB first
14	RDGE	Receive Data Bit Clock Edge Select: 1 = Input data sampled on falling edge. 0 = Input data sampled on rising edge.
13	RDFS	Receive Data Frame Sequence: 1 = Last bit sent on last cycle. 0 = First bit sent on first cycle.
12	—	Reserved
11:10	RDM	Receive Data Frame Select: 00 = 16-bit data frame 01 = Reserved 10 = Reserved 11 = Reserved
9:8	RCF	Receive Cycle Frame Select: 00 = 16-bit cycle frame 01 = 24-bit cycle frame 10 = Reserved 11 = Reserved
7:6	RFM	Receive Frame Mode Select: 00 = normal mode 01 = left justified mode 10 = right justified mode 11 = Reserved
5	IRFS	Inverse Receive Frame Sync Select: 1 = enabled 0 = disabled
4	RBCS	Receive Bit Clock Select: 1 = Use internal bit clock and output bit clock to pin. 0 = Use external bit clock.
3:2	—	Reserved
1:0	RBCF	Receive Bit Clock Frequency Select: 00 = MCLK/8 01 = MCLK/4 10 = MCLK/2 11 = MCLK/1

UNDER NDA FOR EASTECH

AUDIOAPLLM **0x2000D014h**
RW **Default: 0x4Ah**

M
7:0

This register is the analog PLL frequency divider register. After reset, it is initialized to 0x4Ah.

Bit Definitions:

Bits	Name	Description
7:0	M	Audio frequency divider M.

AUDIOAPLLN **0x2000D018h,**
RW **Default: 0x1Fh**

FS	OD	M8	N
7	6	5	4:0

This register is the analog PLL frequency multiplier register. After reset, it is initialized to 0x1Fh.

Bit Definitions:

Bits	Name	Description
7	FS	Sampling Frequency Select: 1 = 384 sample frequency selected. 0 = 256 sample frequency selected.
6	OD	Output divider.
5	M8	Bit 8 of M Divider value.
4:0	N	Audio frequency multiplier N.

S/PDIF Output Interface Registers

This section describes the S/PDIF audio output interface registers.

SPDIF_CTL **0x2000D01Ch**
RW **Default: 0x00h**

—	SPDIF_RST	SPDIF_CLK	SPDIF_ SFRMV	SFRMDB	—	SOE
7	6	5:4	3	2	1	0

The S/PDIF control register contains the control logic for the S/PDIF output function of the ES8381. This register initializes to 0x00h after reset.

Bit Definitions:

Bits	Name	Description
7	—	Reserved
6	SPDIF_ RST	S/PDIF Soft reset.
5:4	SPDIF_ CLK	S/PDIF Bit Clock Frequency Select: 00 = SPMCLK/8 (n=8) 01 = SPMCLK/4 (n=2) 10 = SPMCLK/2 (n=4) 11 = SPMCLK/16 (n=16)
3	SPDIF_ SFRMV	S/PDIF Subframe validity select.
2	SFRM DB	User data bit for subframe.
1	—	Reserved (always 0).
0	SOE	SPDIF Output Enable: 1 = enabled 0 = disabled

SPDIF_CSD1:6 **0x2000D020h—**
RW **0x2000D034h**
Default: 0x0000h

CSD1:6
31:0

The S/PDIF channel status 1:6 registers initialize to 0x0000h after reset.

Bit Definitions:

Bits	Name	Description
31:0	CSD1:6	SPDIF Channel status data 1 through 6.

Audio ADC Registers

This section describes the audio ADC registers.

REGVOCAL **0x2000D080h,**
RW **Default: 0x00h**

CURRENT_PEAK_VOCAL_VALUE
7:0

This register keeps the peak value of the current sample which its most significant bit [bit 15] is zero. Each read to this register will reset the internal register value to zero to re-capture the peak value after read.

Bit Definitions:

Bits	Name	Description
7:0	CUR RENT_ PEAK_ VOCAL_ VALUE	Current sample of the peak vocal value.

UNDER NDA FOR EASTECH

REG_ADCEN 0x2000D084h
RW Default: 0x00h

—	ADC_CLK27_EN	ADC_EN
7:2	1	0

Bit Definitions:

Bits	Name	Description
7:2	—	Reserved
1	ADC_CLK27_EN	ADC Block Clock Enable: 1 = enable ADC 27MHz clock 0 = disable ADC 27MHz clock for power saving
0	ADC_EN	ADC Block Enable: 1 = enable ADC block 0 = reset ADC block

ADCCTRL 0x2000D088h
RW Default: 0x0080h

—	ADC_TLSB	ADC_ATFS_INV	SFW	DSAMPLE	COFF	ADC 3898_DIV	FBW
15:12	11	10	9:6	5	4	3:2	1:0

Bit Definitions:

Bits	Name	Description
15:12	—	Reserved
11	ADC_TLSB	ADC Transmit LSB First: 1 = LSB first 0 = MSB first
10	ADC_ATFS_INV	Invert ADC Audio Transmit Frame Sync: 1 = enabled (inverse ATFS) 0 = disabled
9:6	SFW	Select ADC Clock Sample Frequency Width: SFW[3]: Select sample clock is 2Fs or Fs, which is used by ADC. ACLK must be in the range of 32k-192kHz. Fs is the sample rate audio DAC is using. In ADC, Fs indicates 1 channel (left or right). 1 = 2 Fs ACLK. 0 = Fs ACLK. SFW[2:0]: Divide ACLK further to get appropriate output sample rate. This is used by parallel to serial conversion divide factor. 000 = 1 001 = 2 010 = 4 011 = 8 100 = 16 101 = 32
5	DSAMPLE	Select 256 or 384Fs MCLK input: By selecting either 256fs or 384fs, a different divider to get 2Fs clock for the ADC is realized. 1 = 384Fs 0 = 256Fs
4	COFF	Compression Off: 1 = compression off 0 = compression on
3:2	ADC3898_DIV	ADC3898 Clock Divider. ADC can run lower than 27MHz clock. 00 = divide by 1 01 = divide by 2 10 = divide by 4 11 = divide by 8
1:0	FBW	Bandwidth Control Select: 00 = nominal (20kHz for CLK=27MHz) 01 = half frequency (10kHz) 1X = quarter frequency (5kHz)

DACEN 0x2000D08Ch
RW Default: 0x0000h

—	DAC_CLK_EN
15:9	8

PWM4_EN	PWM3_EN	PWM2_EN	PWM1_EN	PWM1_PADEN	PWM2_PADEN	PWM3_PADEN	PWM4_PADEN
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:9	—	Reserved
8	DAC_CLK_EN	PWM Block Clock Enable: 1 = enabled 0 = disabled for power saving
7	PWM4_EN	PWM4 L/R Block Enable: 1= enable PWM generation. 0 = disabled
6	PWM3_EN	PWM3 L/R Block Enable: 1= enable PWM generation 0 = disabled
5	PWM2_EN	PWM2 L/R Block Enable: 1= enable PWM generation 0 = disabled
4	PWM1_EN	PWM1 L/R Block Enable: 1= enable PWM generation 0 = disabled
3	PWM1_PADEN	PWM1 Pad Output Enable: 1 = output enable 0 = disabled

UNDER NDA FOR EASTECH

Bits	Name	Description
2	PWM2_ PADEN	PWM2 Pad Output Enable: 1 = output enable 0 = disabled
1	PWM3_ PADEN	PWM3 Pad Output Enable: 1 = output enable 0 = disabled.
0	PWM4_ PADEN	PWM4 Pad Output Enable: 1 = output enable 0 = disabled

DACCTRL **0x2000D090h**
RW **Default: 0x0001h**

—	DAC_CKDBL
15:9	8

LR_ SWITCH1	LR_ SWITCH2	LR_ SWITCH3	LR_ SWITCH4	SD4	SD3	SD2	SD1
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:9	—	Reserved
8	DAC_ CKDBL	DAC Clock Double Control: 1 = DAC select 54MHz clock 0 = DAC select 27MHz clock
7	LR_ SWITCH 1	Left/Right Channel 1 Switching Control: 1= switch 0 = no switch
6	LR_ SWITCH 2	Left/Right Channel 2 Switching Control: 1= switch 0 = no switch
5	LR_ SWITCH 3	Left/Right Channel 3 Switching Control: 1= switch 0 = no switch
4	LR_ SWITCH 4	Left/Right Channel 4 Switching Control: 1= switch 0 = no switch
3	SD4	Reserved.
2	SD3	Disable High-Pass Filter In ADC: (For testing only.) 1 = disable filtering 0 = enable filtering
1	SD2	Disable Soft Start: (For testing only.) 1 = disable soft start 0 = enable soft start
0	SD1	Soft Start Input: 1 = begin shutdown sequence 0 = normal operation

S/PDIF Receiver Registers

This section describes the S/PDIF receiver registers.

SPDIF_RCV_CS1:6 **(0x2000E080h—**
R **0x000E094h**
Default: N/A

CS1:6
31:0

The SPDIF receiver channel status registers default value is 0x0000h. SPDIF_RCV_CS1 through SPDIF_RCV_CS6 contains 192 bits of channel status data. Each bit comes from the channel status bit of subframe A (B or M preceding states) of a frame.

Bit Definitions:

Bits	Name	Description
31:0	CS1:6	Channel status data 1 through 3.

SPDIF_RCV_CSIRQ **0x000E098h**
W **Default: 0x0002h**

—	CSIRQ
31:3	2:0

The SPDIF receiver channel interrupt select register default value is 0x0002h. SPDIF_RCV_CSIRQ contains the selected CS register number to generate the interrupt whenever CS data fills up to this register.

Bit Definitions:

Bits	Name	Description
31:3	—	Reserved
2:0	CSIRQ	SPDIF Channel status interrupt request.

SPDIF_RCV_UD1:3 **0x2000E09Ch—**
R **0x000E0A4h**
Default: 0x0000h

UD1:3
31:0

The SPDIF receiver user data register default value is 0x0000h. SPDIF_RCV_UD1 through SPDIF_RCV_UD3 contains 96 bits of sub code data. The sub code (Q, R, S, T, U, V, W) is selected by SPDIF_RCV_SUBSEL.

Bit Definitions:

Bits	Name	Description
31:0	UD1:3	User data.

UNDER NDA FOR EASTECH

SPDIF_RCV_SUBSEL 0x000E0A8h
W Default: 0x0000h

—	SUBSEL
31:3	2:0

The SPDIF receiver sub code select register default value is 0x0000h. SPDIF_RCV_SUBSEL selects which sub code would be stored in SPDIF_RCV_UD[3:1] registers.

Bit Definitions:

Bits	Name	Description
31:3	—	Reserved
2:0	SUBSEL	Receiver Sub Code Select: 001 = Sub_Q. 010 = Sub_R. 011 = Sub_S. 100 = Sut_T. 101 = Sub_U. 110 = Sub_V. 111 = Sub_W.

SPDIF RCV_IRQ 0x2000E0ACh
RW Default: 0x0000h

—	IRQ
31:8	7:0

The SPDIF receiver interrupt register default value is 0x0000h. The interrupt bits would be cleared when writing 1 back to these bits.

Bit Definitions:

Bits	Name	Description
31:8	—	Reserved
7	IRQ	= 1 when parity error.
6	IRQ	= 1 when data is valid (locked or data invalid = 0).
5	IRQ	= 1 when unlocked or data invalid bit in subframe is high.
4	IRQ	= 1 when finish filling SPDIF_RCV_UB3.
3	IRQ	= 1 when finish filling SPDIF_RCV_UB1.
2	IRQ	= 1 when the CS register number

SPDIF RCV_MASK (0x2000E0B0h, R/W)

The SPDIF receiver interrupt mask register default value is 0x0000h. Read back the value has been written.

Bit Definitions:

SPDIF RCV_JITER 0x2000E0B4h
RW Default: 0x0000h

The SPDIF receiver jitter window setting register default value is 0x0000h.

Bit Definitions:

UNDER NDA FOR EASTECH

SPDIF RCV_APLLM **0x2000E0B8h**
W **Default: 0x0000h**

—	APLLM
31:8	7:0

The SPDIF receiver new APLL M number setting register default value is 0x0000h. The new APLL M value applies to APLL when APLL mode = 01 or 10 (SPDIF_RVC_MASK).

Bit Definitions:

Bits	Name	Description
31:8	—	Reserved
7:0	APLLM	SPDIF receiver APLL M value.

SPDIF RCV_APLLN **0x2000E0BCh**
W **Default: 0x0000h**

—	APLLN
31:8	7:0

The SPDIF receiver new APLL N number setting register default value is 0x0000h. The new APLL N value applies to APLL when APLL mode = 01 or 10 (SPDIF_RVC_MASK).

Bit Definitions:

Bits	Name	Description
31:8	—	Reserved
7:0	APLLN	SPDIF receiver APLL N value.

UNDER NDA FOR EASTECH

TIMING DIAGRAMS

Audio Interface Timing

The audio transmit and receive timing diagrams for the ES8381 are shown in Figure 31 through Figure 35.

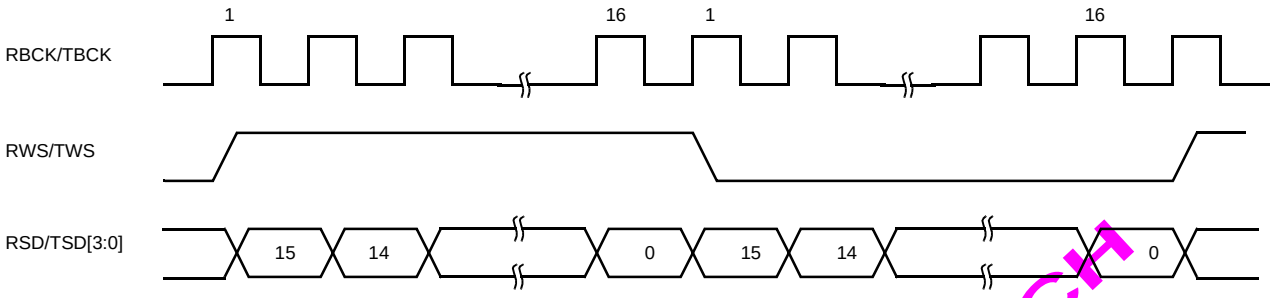


Figure 31 Right Justified Mode / 16-Bit Cycle Frame / 16-Bit Data Frame / MSB First

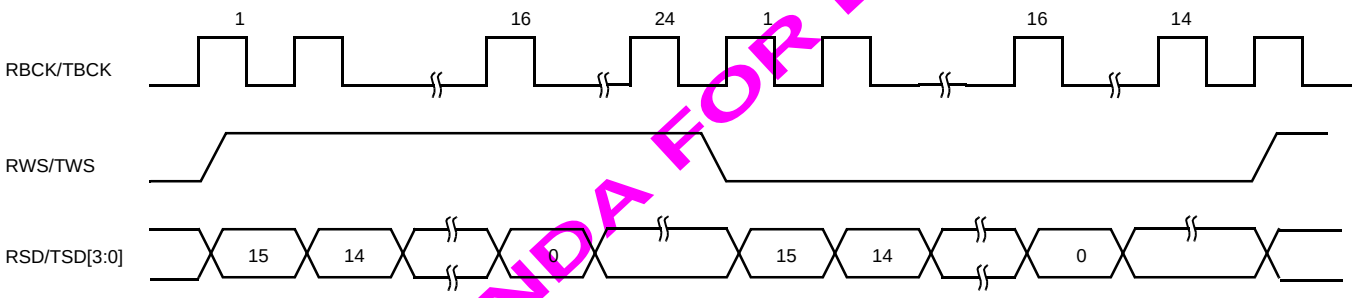


Figure 32 Right Justified Mode / 24-Bit Cycle Frame / 16-Bit Data Frame / MSB First

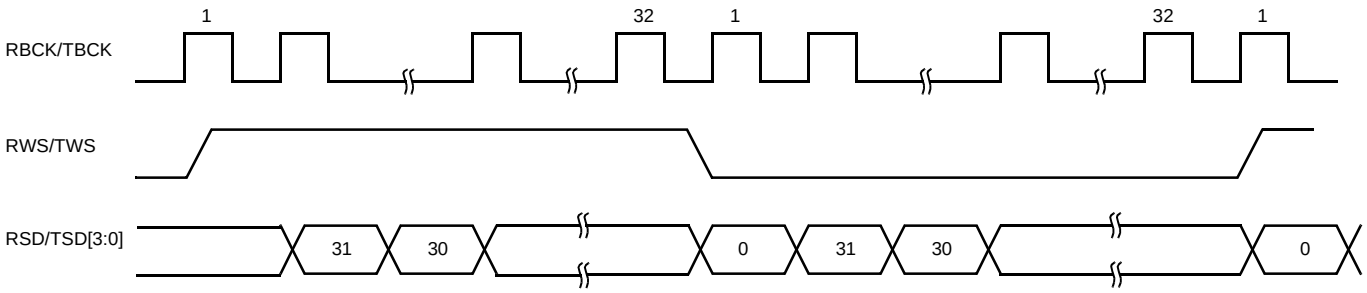


Figure 33 Right Justified Mode / 32-Bit Cycle Frame / 24-Bit Data Frame / LSB First

UNDER NDA FOR EASTECH

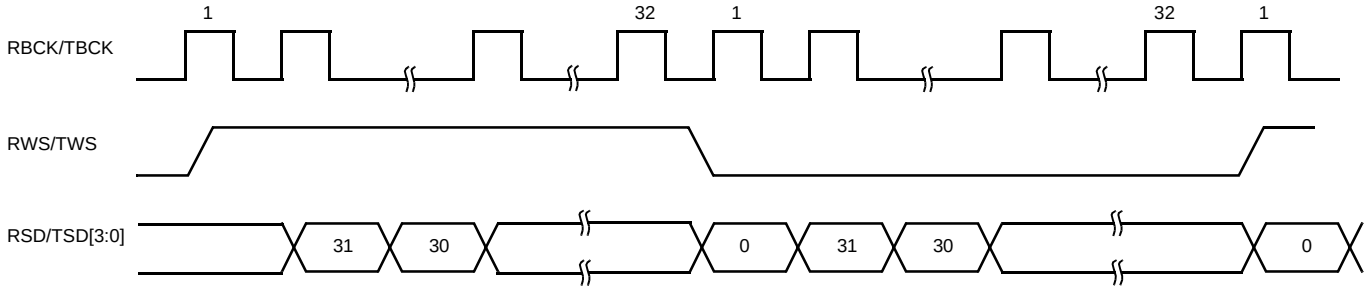


Figure 34 Left Justified Mode / 32-Bit Cycle Frame / 24-Bit Data Frame / MSB First

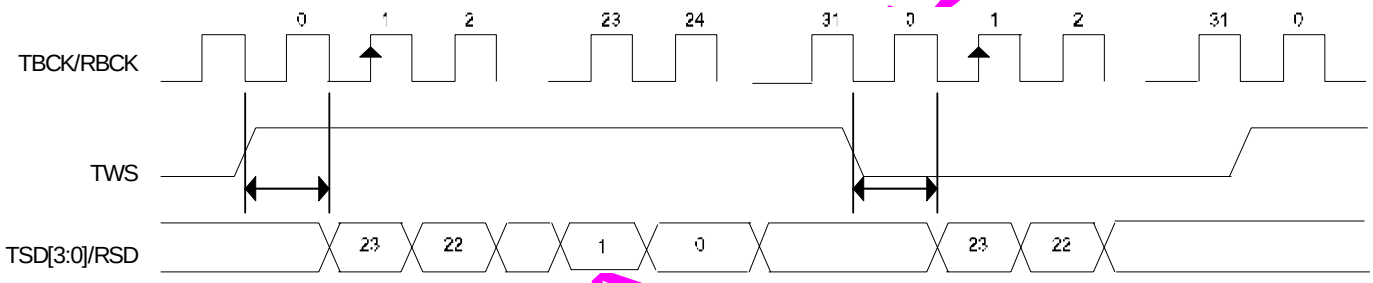


Figure 35 I²S Mode

UNDER NDA STECH

Compact Flash Interface Timing

The Compact Flash interface timing diagrams for the ES8381 appear from Figure 36 to Figure 37.

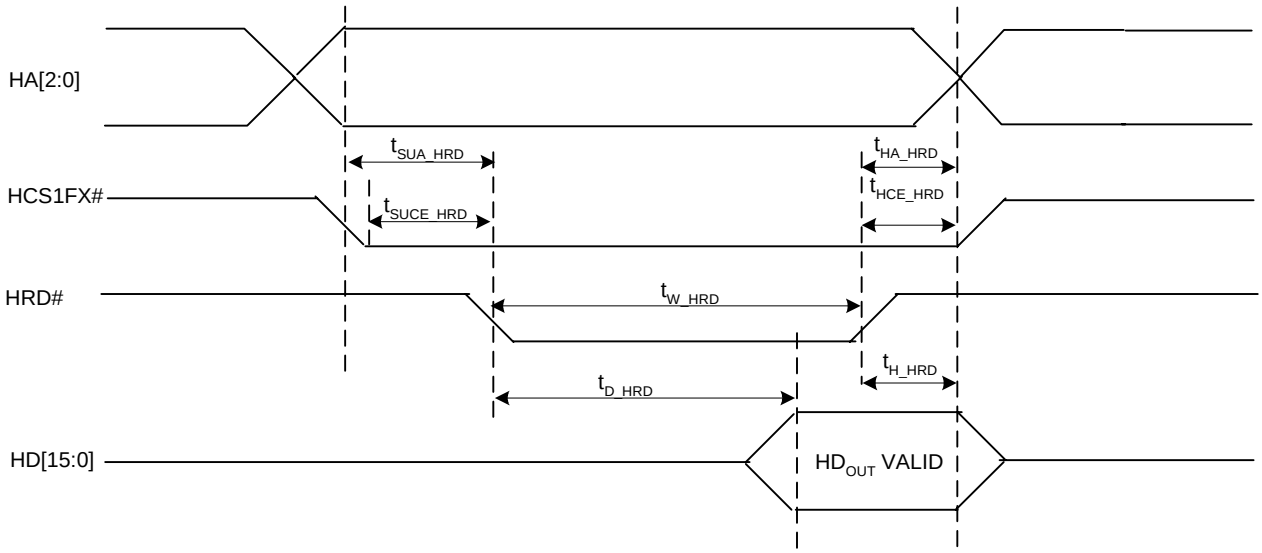


Table 33 Compact Flash True IDE Mode I/O Read Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{D_HRD}	Data delay after HRD#.	—	—	100	ns
t_{H_HRD}	Data hold following HRD#.	0	—	—	
t_{W_HRD}	HRD# width time.	165	—	—	
t_{SUA_HRD}	Address setup before HRD#.	70	—	—	
t_{HA_HRD}	Address hold following HRD#.	20	—	—	
t_{SUCE_HRD}	CE# setup before HRD#.	5	—	—	
t_{HCE_HRD}	CE# hold following HRD#.	20	—	—	

Figure 36 Compact Flash True IDE Mode I/O Read Timing

UNDER NDA FOR E

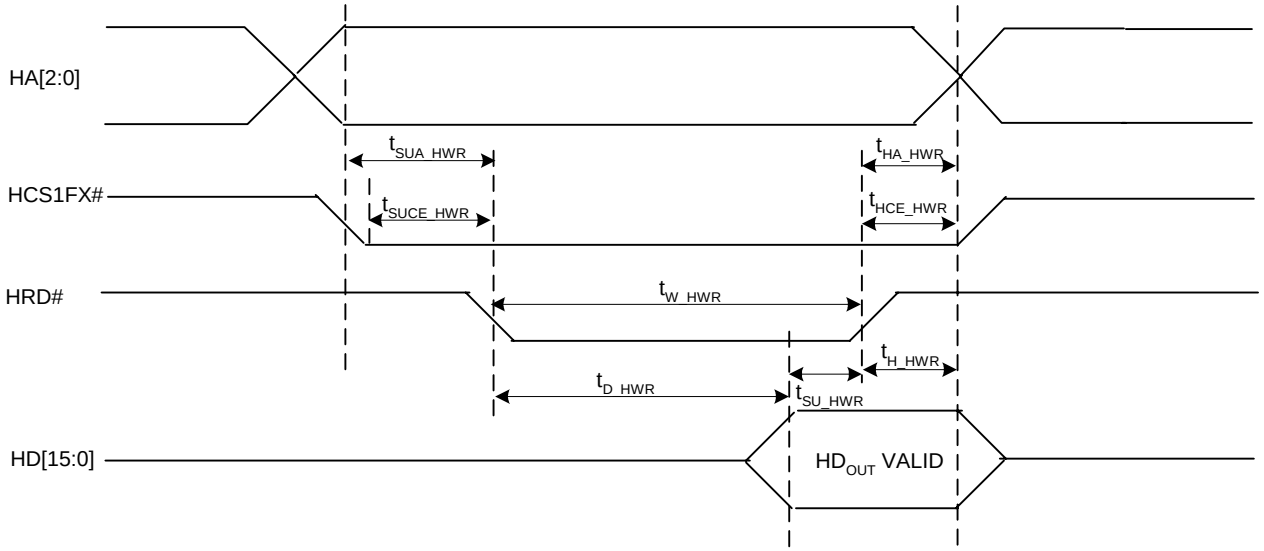


Table 34 Compact Flash True IDE Mode I/O Write Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{SU_HWR}	Data setup before HWR#.	60	—	—	ns
t_{H_HWR}	Data hold following HWR#.	30	—	—	
t_{W_HWR}	HWR# width time.	165	—	—	
t_{SUA_HWR}	Address setup before HWR#.	70	—	—	
t_{HA_HWR}	Address hold following HWR#.	20	—	—	
t_{SUCE_HWR}	CE# setup before HWR#.	5	—	—	
t_{HCE_HWR}	CE# hold following HWR#.	20	—	—	

Figure 37 Compact Flash True IDE Mode I/O Write Timing

UNDER NDA FOR EAS

Host Interface Timing

The host interface timing diagrams for the ES8381 are shown in Figure 38 and Figure 39.

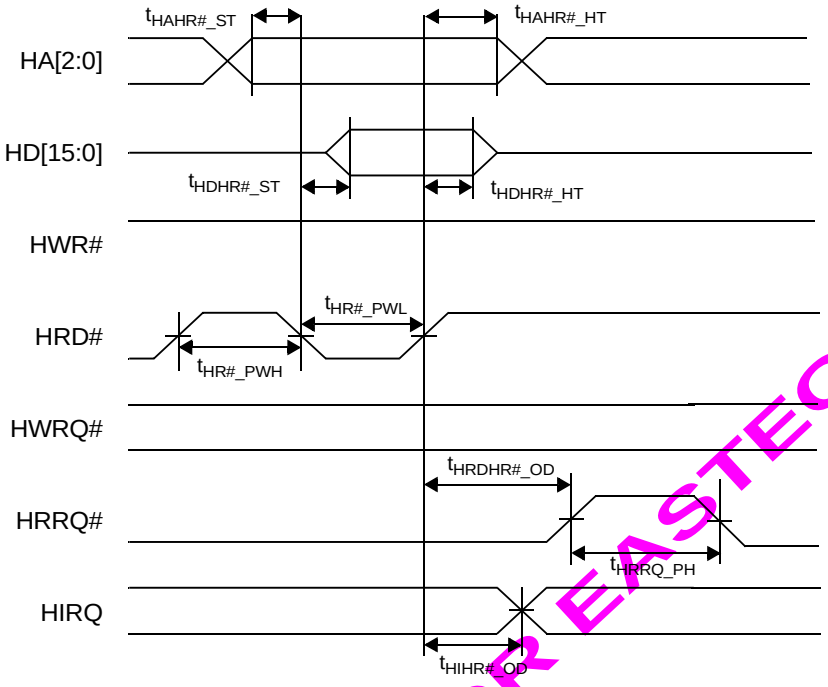


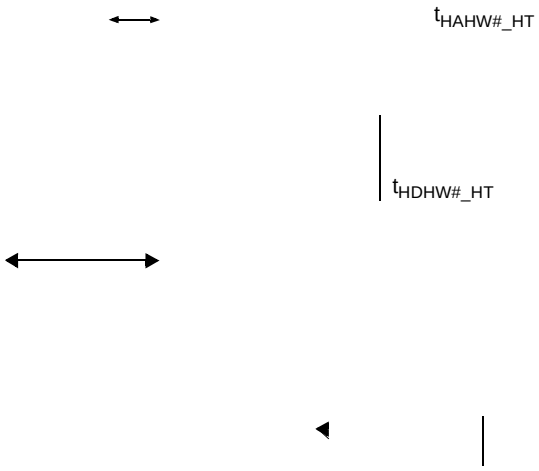
Table 35 Host Bus Read Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$t_{HAHR\#_ST}$	HA to HRD# setup time	4	—	—	ns
$t_{HAHR\#_HT}$	HA to HRD# hold time	2	—	—	
$t_{HDHR\#_ST}$	HD to HRD# setup time	0	—	4	
$t_{HDHR\#_HT}$	HD to HRD# hold time	2	—	—	
$t_{HR\#_PWH}$	HRD# pulse width high	30	—	—	
$t_{HR\#_PWL}$	HRD# pulse width low	30	—	—	
$t_{HRDHR\#_OD}$	HRRQ# to HRD# output delay	0	—	8	
$t_{HIHR\#_OD}$	HIRQ to HRD# output delay	0	—	8	
t_{HRRQ_PH}	HRRQ# pulse width high (See note)	75	—	—	

NOTE: HRRQ# is defined as a minimum value.

Figure 38 Host Bus Read Timing

UNDER NDA FOR EASTECH



UNDER NDA FOR EASTECH

Figure 39 Host Bus Write Timing

Memory Stick Interface Timing

The Memory Stick interface timing diagrams for the ES8381 appear from Figure 40 to Figure 41.

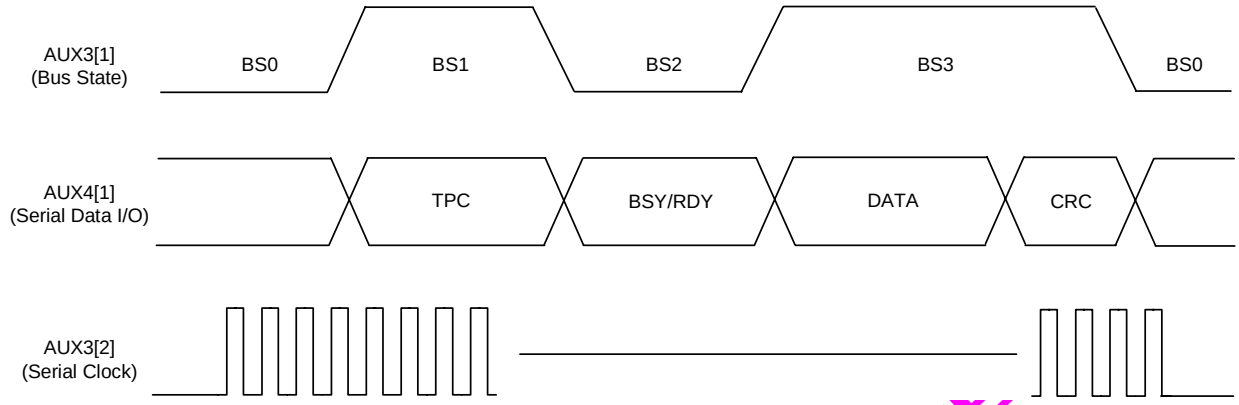


Figure 40 Memory Stick Read Timing

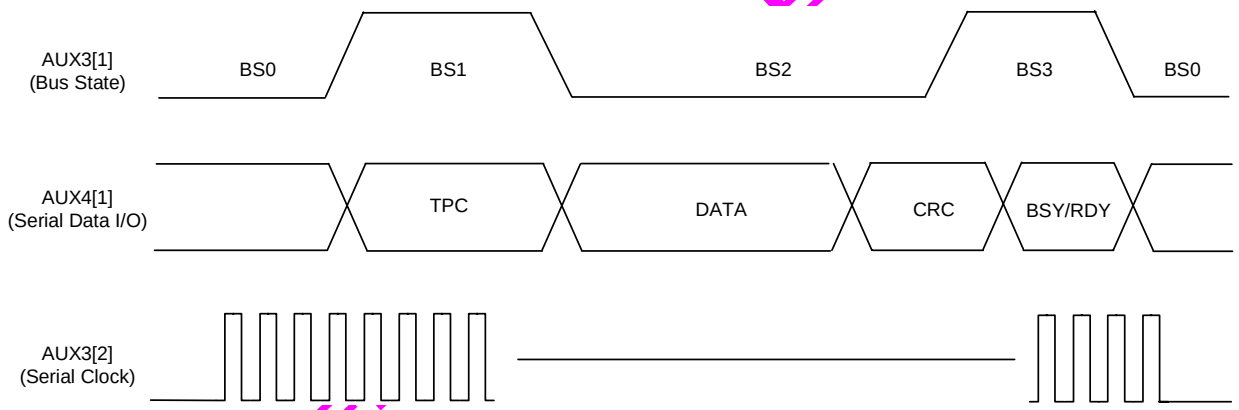


Figure 41 Memory Stick Write Timing

SDRAM Interface Timing

The SDRAM read and write timing diagrams for the ES8381 are shown in Figure 42 through Figure 45.

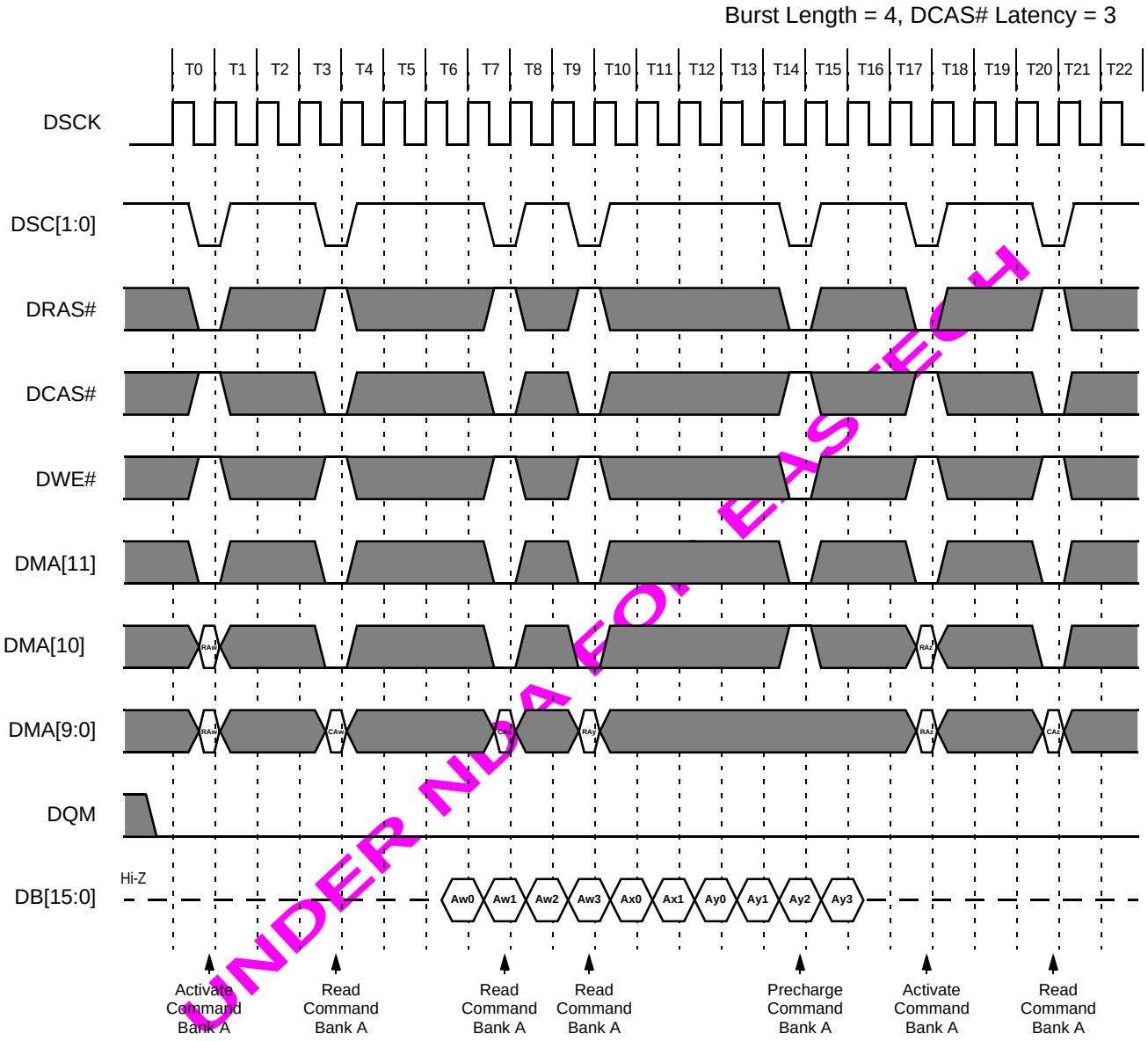
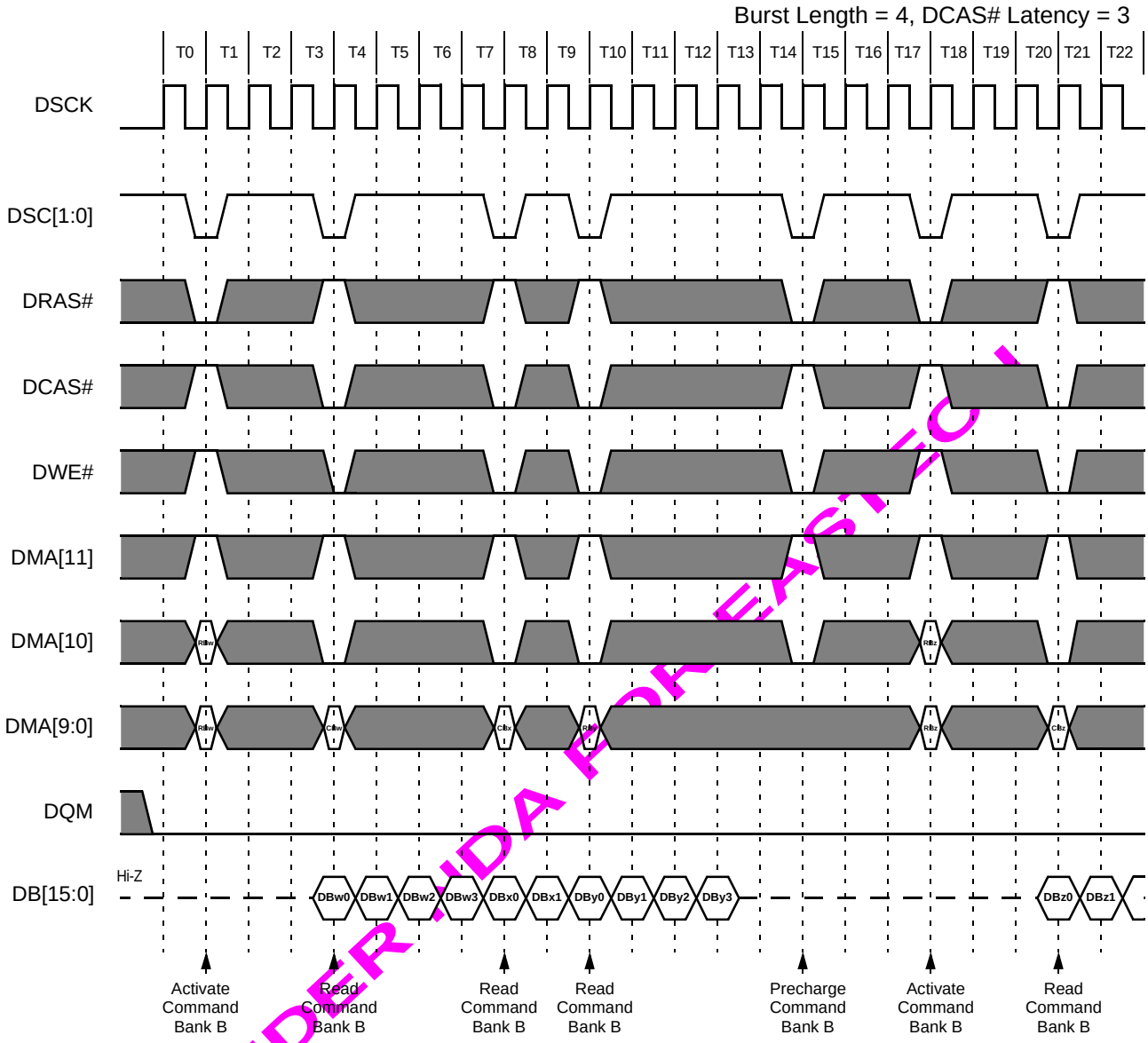
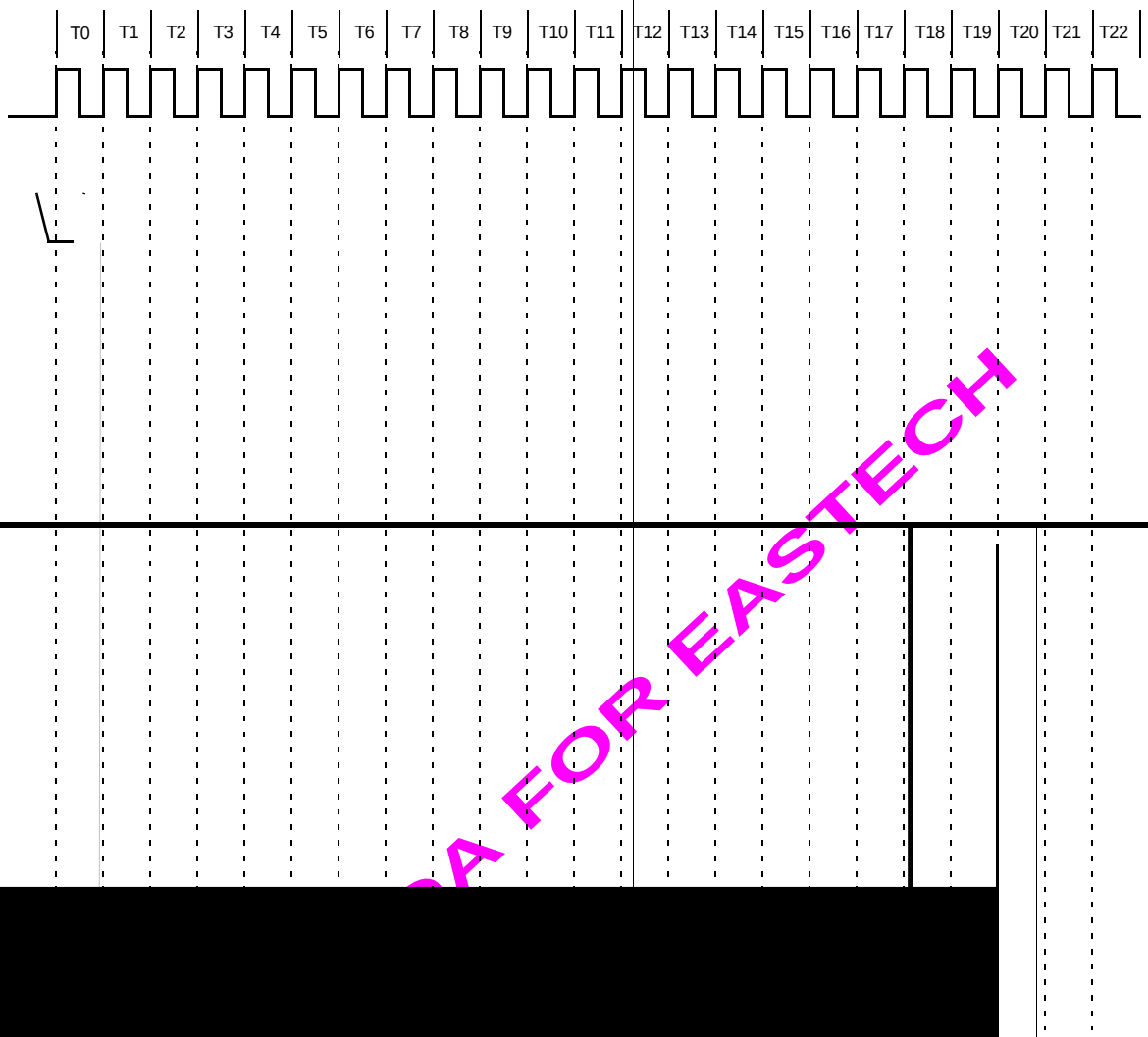


Figure 42 SDRAM Random Column Read Timing

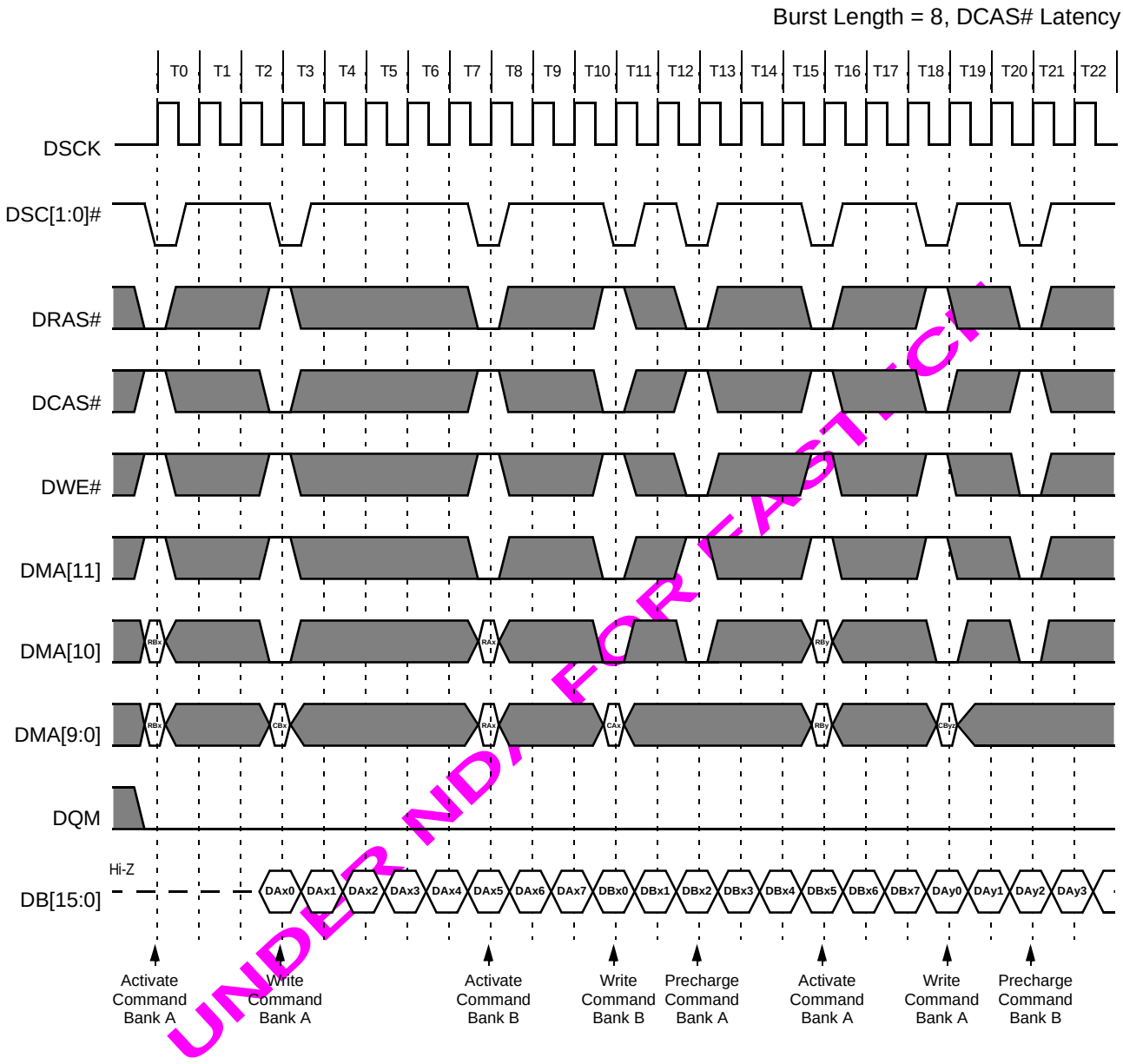


UNDER NDA FOR EASTECH

Figure 43 SDRAM Random Column Write Timing



A FOR EASTECH



UNDER NDA FOR FAST-CH

Figure 45 SDRAM Random Row Write Timing

Table 37 SDRAM Interface Timing

Symbol	Parameter (CAS Latency = 3)	Minimum	Maximum	Unit
t_{RRD}	Row active to Row Active Delay	2	—	CLK
t_{RCD}	DRAS# to DCAS# Delay	3	—	
t_{RP}	Row precharge time	3	—	
t_{RAS}	Row active time	6	200	
t_{RC}	Row cycle time	10	—	
t_{CDL}	Last data in to new column address delay	1	—	
t_{RDL}	Last data in to row precharge	1	—	
t_{BDL}	Last data in to burst stop	1	—	
t_{CCD}	Column address to column address delay	1	—	

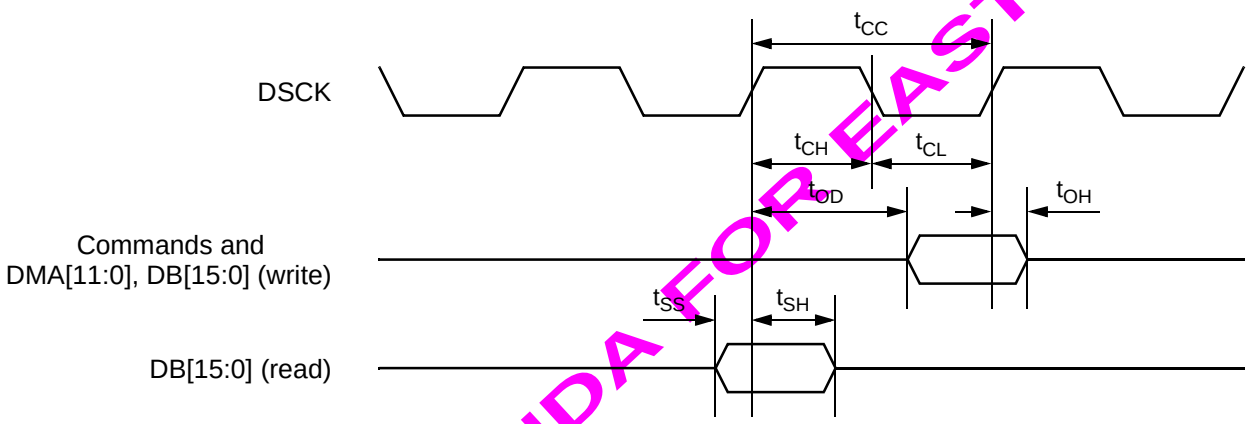


Figure 46 ES8381 SDRAM Read and Write Timing

UNDER NDA FOR EASTECH

Table 38 SDRAM Read and Write Timing

Symbol	Parameter (CAS Latency = 3)	Minimum	Maximum	Unit
t_{CC}	CLK cycle time	7.5	—	ns
t_{OD}	CLK to valid output delay	—	6	ns
t_{OH}	Output data hold time	2	—	ns
t_{CH}	CLK high pulse width	3	—	ns
t_{CL}	CLK low pulse width	3	—	ns
t_{SS}	Input setup time	1.0	—	ns
t_{SH}	Input hold time	0.5	—	ns
t_{SLZ}	CLK to output in low-Z	1	—	ns
t_{SHZ}	CLK to output in Hi-Z	—	6	ns

SRAM Interface Timing

The SRAM interface read and write timing diagrams for the ES8381 are shown in Figure 47 and Figure 48.

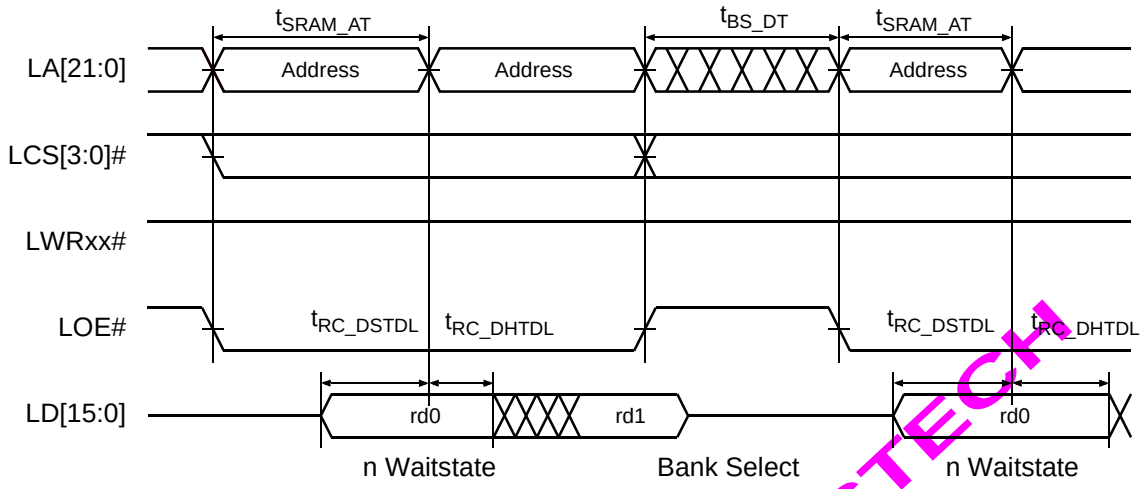


Table 39 SRAM Read Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{DRAM_IOSS}	DRAM interface output signal skew	0	—	3	ns
t_{RC_DSTDL}	Read cycle data setup time to data latch	6	—	—	ns
t_{RC_DHTDL}	Read cycle data hold time to data latch	2	—	—	ns
t_{SRAM_AT}	SRAM access time	2	—	33	Internal CPU clock cycle
t_{BS_DT}	Bank Select delay time	0	—	3	Internal CPU clock cycle

Figure 47 SRAM Read Timing

UNDER NDA FOR EASTECH

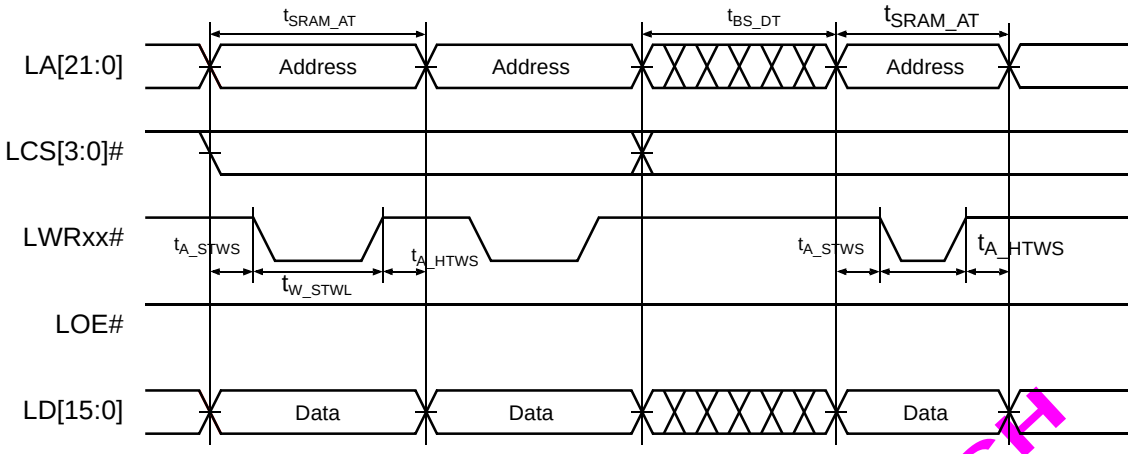


Table 40 SRAM Write Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{SRAM_IOSS}	SRAM interface output signal skew	0	—	3	ns
t_{SRAM_AT}	SRAM access time	2	—	33	Internal CPU clock cycle
t_{BS_DT}	Bank Select delay time	0	—	3	Internal CPU clock cycle
t_{A_STWS}	Address setup time to write strobe	0.5	—	0.5	Internal CPU clock cycle
t_{A_HTWS}	Address hold time to write strobe	0.5	—	0.5	Internal CPU clock cycle
t_{W_STWL}	Write strobe pulse width low	1	—	31.5	Internal CPU clock cycle

Figure 48 SRAM Write Timing

UNDER NDA FOR EASTECH

UNDER NDA FOR

USB Interface Timing

The USB interface timing diagram for the ES8381 is shown in Figure 50.

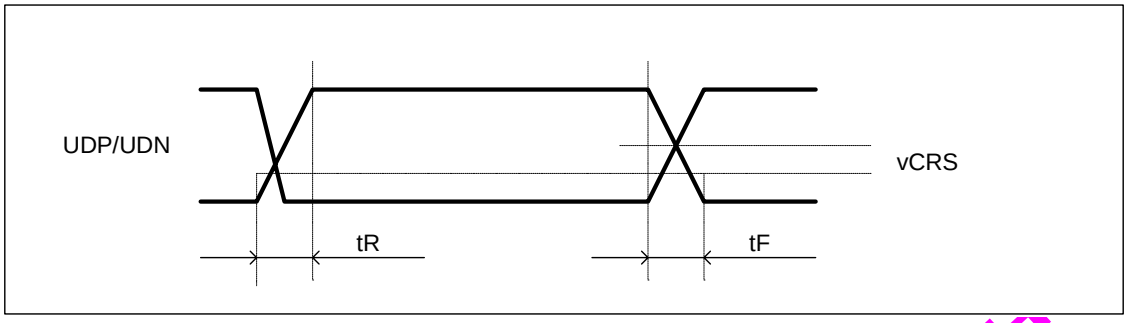


Table 42 USB Full-Speed Mode Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_R	Rise time	4		20	ns
t_F	Fall time	4		20	
t_{RFM}	Rise/Fall output	90		111	%
v_{CRS}	Cross level	1.3		2.0	V

Table 43 USB Low-Speed Mode Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_R	Rise time	75		300	ns
t_F	Fall time	75		300	
t_{RFM}	Rise/Fall output	80		125	%
v_{CRS}	Cross level	1.3		2.0	V

Figure 50 USB Full Speed and Low Speed Timing

UNDER NDA FOR EASTECH

Video Timing

The video timing diagrams for the ES8381 are shown in Figure 51 through Figure 58.

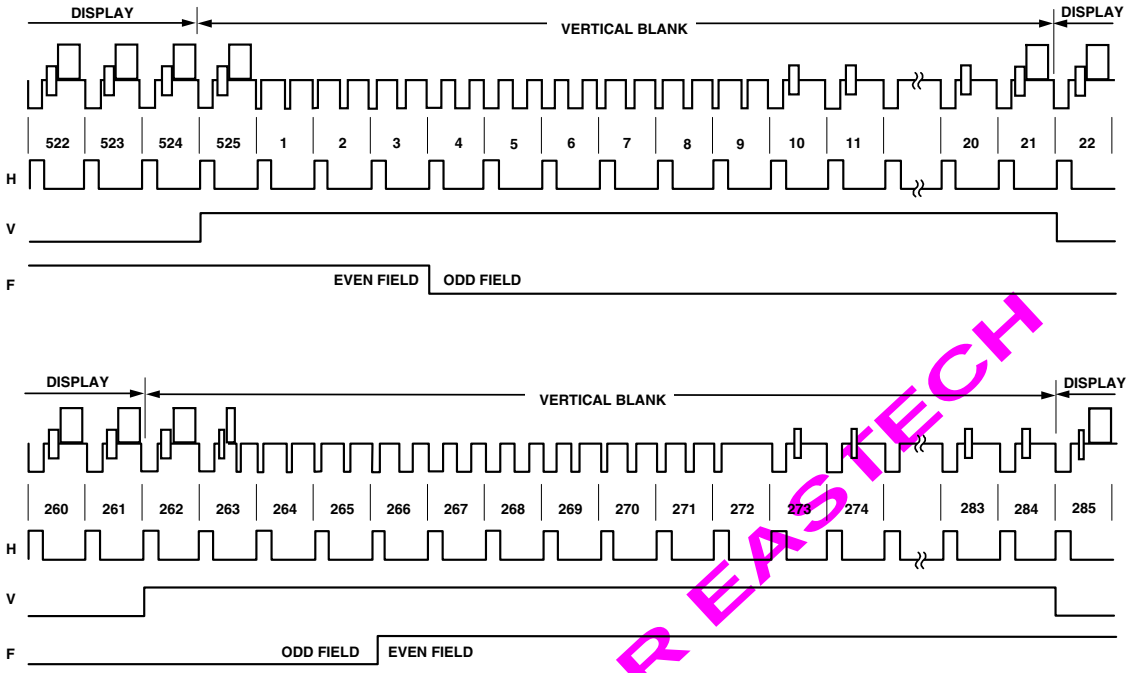


Figure 51 NTSC Timing

A FOR EASTECH

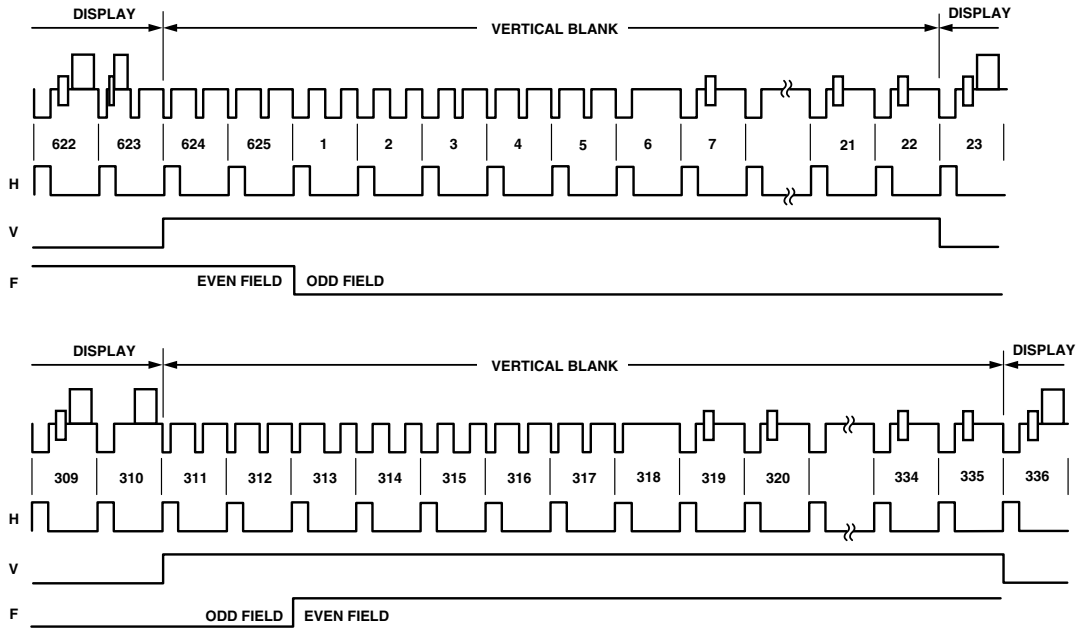


Figure 52 PAL Timing

PREAMBLE ADDRESS CODES

	Row 1	Row 2	Row 3	Row 4	Row 5	Row 6	Row 7	Row 8	Row 9	Row 10	Row 11	Row 12	Row 13	Row 14	Row 15
First byte of code pair:															
Data Channel 1	11	11	12	12	15	15	16	16	17	17	10	13	13	14	14
Data Channel 2	19	19	1A	1A	1D	1D	1E	1E	1F	1F	18	1B	1B	1C	1C
Second byte of code pair:															
White	40	60	40	60	40	60	40	60	40	60	40	40	60	40	60
White Underline	41	61	41	61	41	61	41	61	41	61	41	41	61	41	61
Green	42	62	42	62	42	62	42	62	42	62	42	42	62	42	62
Green Underline	43	63	43	63	43	63	43	63	43	63	43	43	63	43	63
Blue	44	64	44	64	44	64	44	64	44	64	44	44	64	44	64
Blue Underline	45	65	45	65	45	65	45	65	45	65	45	45	65	45	65
Cyan	46	66	46	66	46	66	46	66	46	66	46	46	66	46	66
Cyan Underline	47	67	47	67	47	67	47	67	47	67	47	47	67	47	67
Red	48	68	48	68	48	68	48	68	48	68	48	48	68	48	68
Red Underline	49	69	49	69	49	69	49	69	49	69	49	49	69	49	69
Yellow	4A	6A	4A	6A	4A	6A	4A	6A	4A	6A	4A	4A	6A	4A	6A
Yellow Underline	4B	6B	4B	6B	4B	6B	4B	6B	4B	6B	4B	4B	68	4B	6B
Magenta	4C	6C	4C	6C	4C	6C	4C	6C	4C	6C	4C	4C	6C	4C	6C
Magenta Underline	4D	6D	4D	6D	4D	6D	4D	6D	4D	6D	4D	4D	6D	4D	6D
White Italics	4E	6E	4E	6E	4E	6E	4E	6E	4E	6E	4E	4E	6E	4E	6E
White Italics Underline	4F	6F	4F	6F	4F	6F	4F	6F	4F	6F	4F	4F	6F	4F	6F
Indent 0	50	70	50	70	50	70	50	70	50	70	50	50	70	50	70
Indent 0 Underline	51	71	51	71	51	71	51	71	51	71	51	51	71	51	71
Indent 4	52	72	52	72	52	72	52	72	52	72	52	52	72	52	72
Indent 4 Underline	53	73	53	73	53	73	53	73	53	73	53	53	73	53	73
Indent 8	54	74	54	74	54	74	54	74	54	74	54	54	74	54	74
Indent 8 Underline	55	75	55	75	55	75	55	75	55	75	55	55	75	55	75
Indent 12	56	76	56	76	56	76	56	76	56	76	56	56	76	56	76
Indent 12 Underline	57	77	57	77	57	77	57	77	57	77	57	57	77	57	77
Indent 16	58	78	58	78	58	78	58	78	58	78	58	58	78	58	78
Indent 16 Underline	59	79	59	79	59	79	59	79	59	79	59	59	79	59	79
Indent 20	5A	7A	5A	7A	5A	7A	5A	7A	5A	7A	5A	5A	7A	5A	7A
Indent 20 Underline	5B	7B	5B	7B	5B	7B	5B	7B	5B	7B	5B	5B	7B	5B	7B
Indent 24	5C	7C	5C	7C	5C	7C	5C	7C	5C	7C	5C	5C	7C	5C	7C
Indent 24 Underline	5D	7D	5D	7D	5D	7D	5D	7D	5D	7D	5D	5D	7D	5D	7D
Indent 28	5E	7E	5E	7E	5E	7E	5E	7E	5E	7E	5E	5E	7E	5E	7E
Indent 28 Underline	5F	7F	5F	7F	5F	7F	5F	7F	5F	7F	5F	5F	7F	5F	7F

NOTE: All indent codes (second byte equals 50h±5fh, 70th±7fh) assign white as the color attribute.

Figure 53 Line 21 Preamble Address Codes (Same As FCC Part 15.119)

UNDER NDA FOR EASTECH

DVE NTSC SQ Simulation

Code	V	IRE
954	1.233	172.7
774	1.001	140.1
715	0.924	129.4
476	0.616	86.2
336	0.434	60.8
263	0.340	47.6
221	0.286	40.0
106	0.138	19.3
83	0.108	15.1
0	0.000	0.0

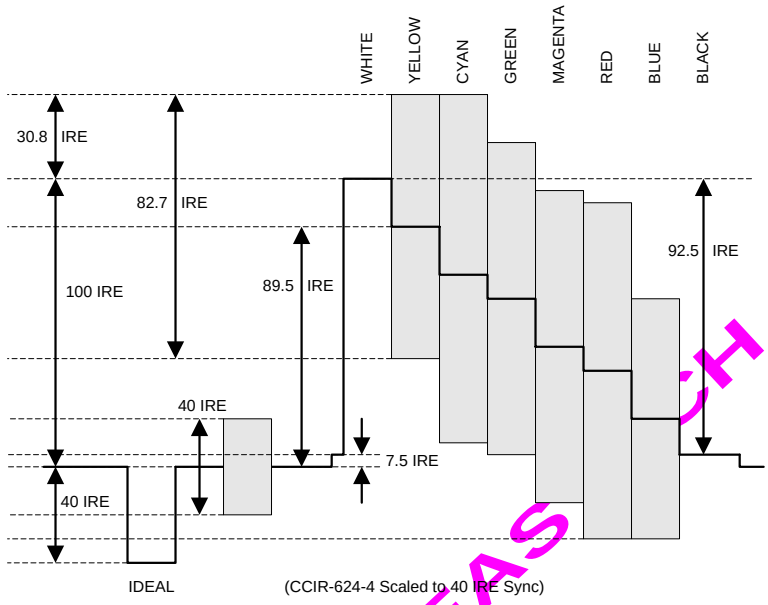


Figure 54 NTSC Composite (VDAC) Line Output Waveform

DVE PAL SQ Simulation

Code	V	IRE
960	1.241	173.8
774	1.001	140.1
712	0.921	128.9
464	0.600	84.0
349	0.451	63.1
232	0.300	42.0
115	0.149	20.8
46	0.060	8.4
0	0.000	0.0

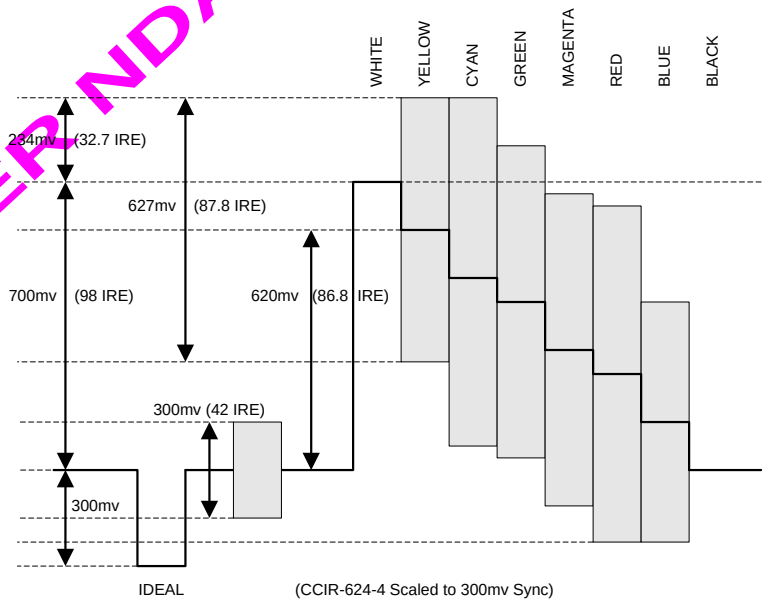


Figure 55 PAL Composite (VDAC) Line Output Waveform

UNDER NDA FOR EASTECH

DVE NTSC SQ Simulation

Code	V	IRE
387	1.001	140.1
716	0.926	129.6
476	0.615	86.2
322	0.416	58.3
263	0.340	47.6
221	0.286	40.0
0	0.000	0.0

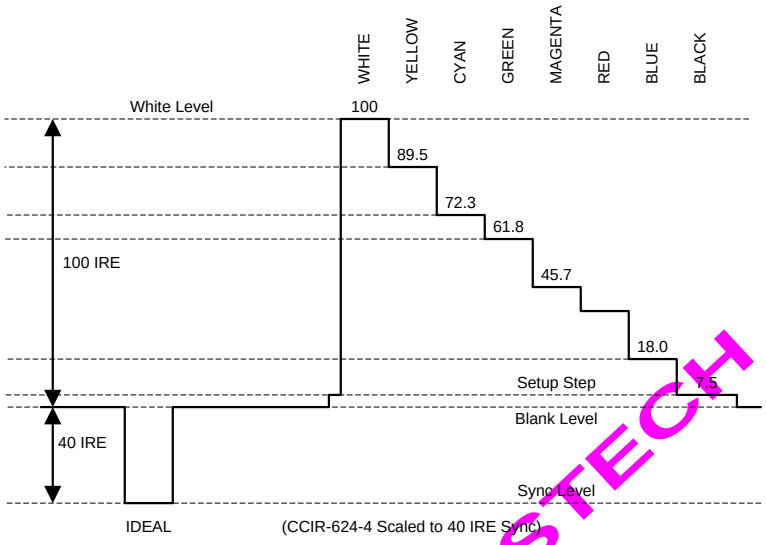
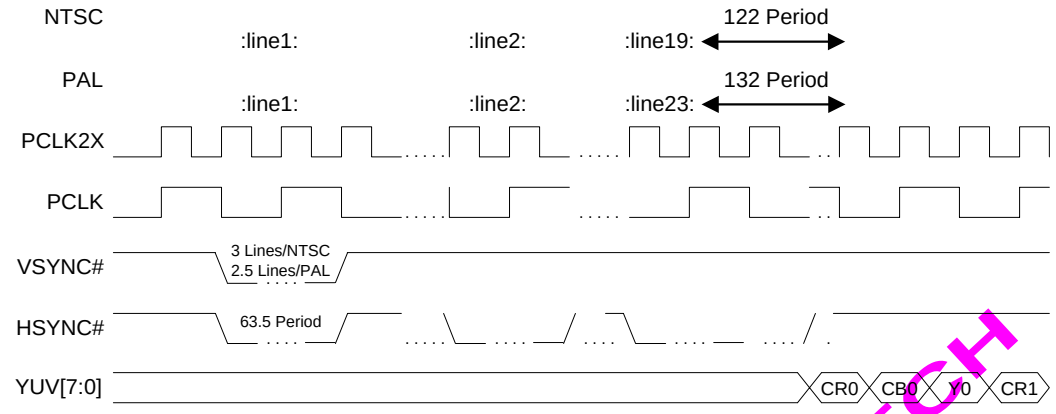


Figure 56 Luma (YDAC) Line Output Waveform

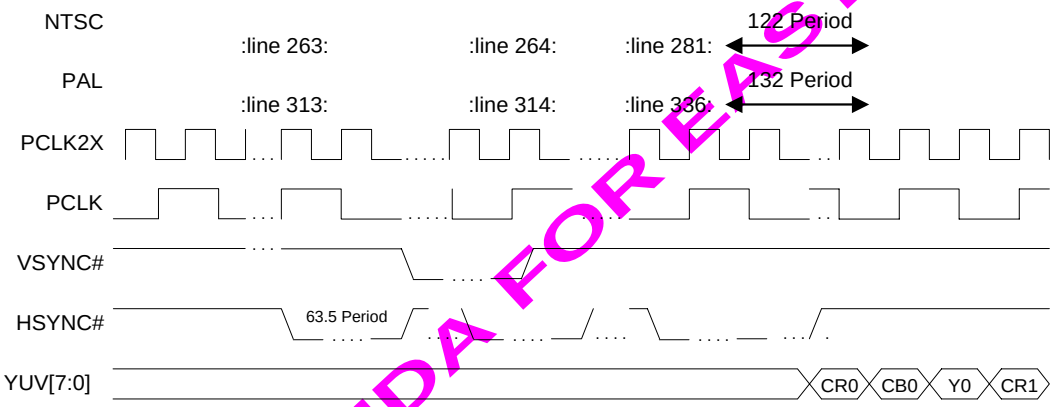
UNDER NDA FOR EASTECH

Figure 57 Chroma (CDAC) Line Output Waveform

Field 1



Field 2



1 Period = 1 Pixel Clock

Figure 58 Sync and Pixel Clock Timings

UNDER NDA FOR EASTECH

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Storage temperature range	–65° C to 150° C
Operating temperature range	0° C (ambient) to 85° C (case)
Voltage range for 5V tolerant input pins	–0.5 V to +5.5 V
Voltage range on all other pins	–0.5 V to (VD33 +0.5 V)

Recommended Operating Conditions

Operating temperature range	0° C (ambient) to 85° C (case)
Supply voltage VDD / DVCC	TBD
Supply voltage VD33 / AVDD33	TBD
Supply voltage VD33_DAC	TBD
Supply voltage VD33PLL	TBD

Power Dissipation

Power dissipation	TBD

WARNING: Stress beyond those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section of this specification is not implied. Exposure to the Absolute Maximum Ratings conditions for extended periods may affect device reliability. For case temperatures exceeding 85° C, a heatsink may be required.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

Electrical characteristics for the ES8381 are listed in Table 44 through Table 47.

UNDER NDA FOR EASTECH

DC Electrical Characteristics

Table 44 DC Electrical Characteristics

Symbol	Parameter	Minimum	Maximum	Unit	Comments
V_{IH}	High-level input voltage	2.0	VD33	V	All inputs TTL levels except CLK and 5V tolerant input pins
		2.0	5.5	V	All 5V tolerant inputs
V_{IL}	Low-level input voltage	–0.3	0.8	V	All inputs TTL levels except CLK
V_{CLKH}	CLK high-level input	2.0	VD33 +0.25	V	TTL level input
V_{CLKL}	CLK low-level input	–0.3	0.8	V	
V_{OH}	High-level output voltage	3.0	—	V	I_{OH} = 1 mA
V_{OL}	Low-level output voltage	—	0.45	V	I_{OL} = 4 mA
I_{LI}	Input leakage current	—	±15	µA	
I_{LO}	Output leakage current	—	±15		
C_{IN}	Input capacitance	—	10	pF	fc = 1 MHz
C_O	Input/output capacitance	—	12		
C_{CLK}	CLK capacitance	—	20	pF	fc = 1 MHz

Table 45 Video DAC DC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
DAC resolution	—	10	—	bits
Integral linearity (INL)	—	±2	±2	LSB
Differential linearity error (DNL)	—	±0.5	±1	LSB
Gain error	—	—	±5	%
DAC output impedance	—	20K	—	Ω
Output current-DAC	33.5	35.2	36.5	mA
Internal reference voltage (V_{REF})	1.17	1.235	1.29	V
Output load	34	37.5	42	Ω
Output capacitance	—	—	40	pF

AC Electrical Characteristics

Table 46 Video DAC AC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
D/A Input Clock Rate	—	—	15	ns
Clock to Valid Output	—	—	15	
Analog Output Skew	—	—	30	
Output Rise and Fall Time	—	8	10	
Output Settling Time	—	—	12	
Glitch Energy	—	150	300	pYs
Power Dissipation	TBD	—	TBD	mW
SLX On to Output Sleep	—	—	165	ns
SLX Off to Output Awake	—	—	1550	
SL On to Output Sleep	—	—	1665	
SL Off to Output Awake	—	—	62.2	ms

UNDER NDA FOR EASTECH

Table 47 VFD Interface Characteristics

Parameter	Minimum	Typical	Maximum	Unit
VFD Clock Frequency	—	—	10	MHz
VFD Clock Pulse Width	500	—	—	ns
VFD Data Setup	50	—	—	
VFD Data Hold	50	—	—	
VFD Data Output Delay	—	—	5	

Audio Performance

Table 48 lists the audio performance characteristics of the digital audio processor of the ES8381 under normal operating conditions.

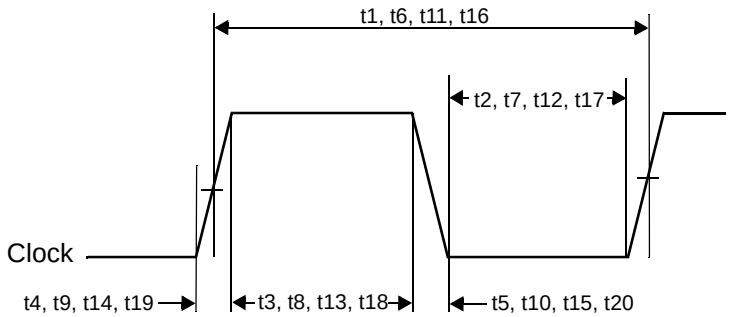
Table 48 Audio Performance

Parameter	Minimum	Typical	Maximum	Unit
ADC Resolution	TBD	—	TBD	Bit
ADC Data Sample Rate	TBD	—	TBD	KHz
ADC Dynamic Range	TBD	TBD	—	dB
ADC THD	—	TBD	TBD	%
DAC Resolution	TBD	—	TBD	Bit
DAC Sample Rate	TBD	—	TBD	KHz
DAC THD+Noise	TBD	TBD	TBD	dB
DAC Dynamic Range	TBD	TBD	TBD	dB
DAC Bandwidth	TBD	—	TBD	KHz

UNDER NDA FOR EASTECH

Device Clock Characteristics

Device clock characteristics for the ES8381 are shown in Figure 59.



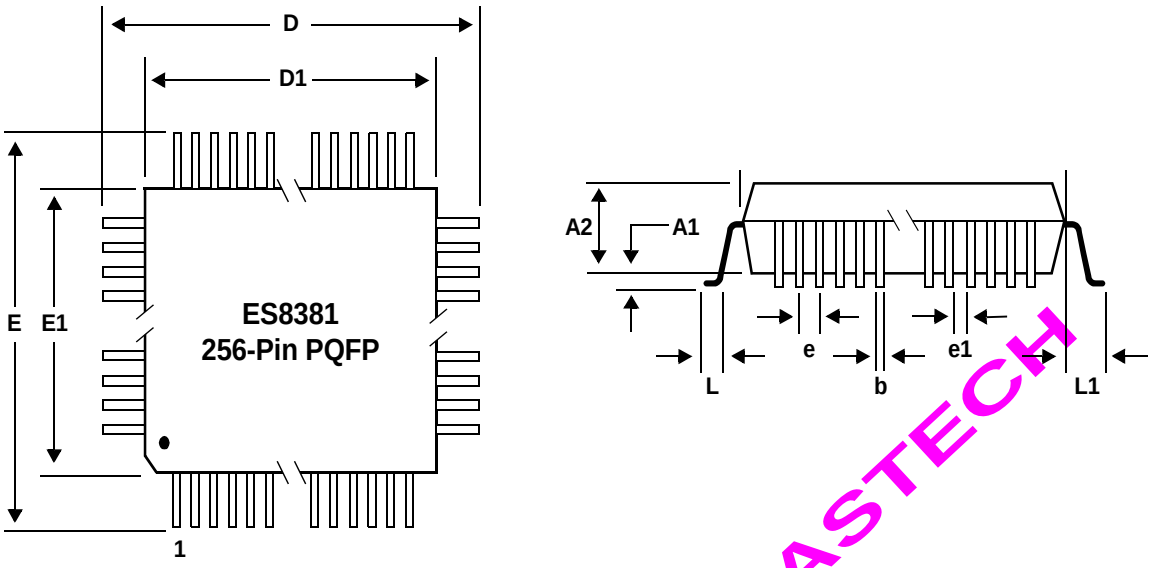
Symbol		Parameter	Minimum	Typical	Maximum	Unit	Comments
Pixel Clock Timing							
t1	t_{CLK_P}	Clock period	30	—	100	ns	
t2	t_{CLK_LT}	Clock low time	15	—	—	ns	
t3	t_{CLK_HT}	Clock high time	15	—	—	ns	
t4	t_{CLK_RT}	Clock rise time	—	—	6	ns	
t5	t_{CLK_FT}	Clock fall time	—	—	6	ns	
Doubled Pixel Clock Timing							
t6	t_{PCLK_P}	Pixel clock period	33	—	—	ns	
t7	t_{PCLK_LT}	Pixel clock low time	15	—	—	ns	
t8	t_{PCLK_HT}	Pixel clock high time	15	—	—	ns	
t9	t_{PCLK_RT}	Pixel clock rise time	—	—	4	ns	
t10	t_{PCLK_FT}	Pixel clock fall time	—	—	4	ns	
Audio Master Clock Timing							
t11	t_{ACLK_P}	Audio clock period	40	—	—	ns	T = 1/192 kHz X 128
t12	t_{ACLK_LT}	Audio clock low time	9	—	—	ns	
t13	t_{ACLK_HT}	Audio clock high time	9	—	—	ns	
t14	t_{ACLK_RT}	Audio clock rise time	—	—	6	ns	
t15	t_{ACLK_FT}	Audio clock fall time	—	—	6	ns	
TDM Clock Timing							
t16	t_{TDMCLK_P}	TDM clock period	40	—	—	ns	T = 1/96 kHz X 256
t17	t_{TDMCLK_LT}	TDM clock low time	14	—	—	ns	
t18	t_{TDMCLK_HT}	TDM clock high time	14	—	—	ns	
t19	t_{TDMCLK_RT}	TDM clock rise time	—	—	6	ns	
t20	t_{TDMCLK_FT}	TDM clock fall time	—	—	6	ns	

UNDER NDA FOR ESS TECH

Figure 59 Pixel, Doubled Pixel, TDM and Audio Master Clock Timing

MECHANICAL DIMENSIONS

The mechanical dimensions for the ES8381 are shown in Figure 60.



Symbol	Descriptions	Millimeters		
		Minimum	Nominal	Maximum
D	Lead to lead, X-axis	—	30.60	—
D1	Package's outside, X-axis	—	28.00	—
E	Lead to lead, Y-axis	—	30.60	—
E1	Package's outside, Y-axis	—	28.00	—
A1	Board standoff	0.25	0.33	0.42
A2	Package thickness	3.20	3.32	3.60
b	Lead width	0.13	0.16	0.23
e	Lead pitch	—	0.40	—
e1	Lead gap	0.17	0.24	0.27
L	Foot length	0.45	0.60	0.75
L1	Lead length	—	1.30	—
—	Foot angle	0°	—	7°
—	Coplanarity	—	—	0.102
—	Number of leads in X-axis	—	64	—
—	Number of leads in Y-axis	—	64	—
—	Total number of leads	—	256	—
—	Package type	—	PQFP	—

For lead-free devices, the solder paste and PCB finish/plating must be 100% lead-free in order to ensure proper solderability. (Cu = Copper, Sn = Tin, Bi = Bismuth).

Figure 60 256-pin Plastic Quad Flat Package (PQFP)

UNDER NDA FOR EASTECH

This page is intentionally left blank.

UNDER NDA FOR EASTECH

ORDERING INFORMATION

Part Number	Description	Package
ES8381CC	Phoenix DVD SOC, Progressive scan, MPEG-4, DivX, DTS, audio DAC, and TV encoder.	256-pin PQFP
ES8381CD	Phoenix DVD SOC, Progressive scan, MPEG-4, DivX, DTS, Class-D audio, and TV encoder.	256-pin PQFP
ES8381CE	Phoenix DVD SOC, Progressive scan, MPEG-4, DivX, DTS, DVD Audio, audio DAC, and TV encoder.	256-pin PQFP
ES8381CF	Phoenix DVD SOC, Progressive scan, MPEG-4, DivX, DTS, DVD Audio, Class-D audio, and TV encoder.	256-pin PQFP

Other Phoenix DVD Processors

Part Number	Description	Package

UNDER NDA FOR EASTECH

ESS Technology, Inc.
48401 Fremont Blvd.
Fremont, CA 94538
Tel: (510) 492-1088
Fax: (510) 492-1898

No part of this publication may be reproduced, stored in a retrieval system, transmitted, or translated in any form or by any means, electronic, mechanical, manual, optical, or otherwise, without the prior written permission of ESS Technology, Inc.

ESS Technology, Inc. makes no representations or warranties regarding the content of this document.

All specifications are subject to change without prior notice.

ESS Technology, Inc. assumes no responsibility for any errors contained herein.

U.S. patents pending.

MPEG is the Moving Picture Experts Group of the ISO/IEC. References to MPEG in this document refer to the ISO/IEC JTC1 SC29 committee draft ISO 11172 dated January 9, 1992.

Vibratto, SmartBright, SmartLogo, SmartColor, and Music Slideshow are trademarks of ESS Technology, Inc.

Dolby is a trademark of Dolby Laboratories, Inc.

Trusurround, Trusurround XT, SRS, and (o) symbol are trademarks of SRS Labs., Inc.

All other trademarks are trademarks of their respective companies and are used for identification purposes only.