# ES8396

## Low Power Stereo Audio CODEC

## FEATURES

System

- High performance and low power multi-bit delta-sigma stereo ADC and DAC
- Two independent I$^2$S/PCM master or slave serial data port
- Three pairs of analog input
- Four pairs of analog output
- 2x0.9W stereo or 1.8W mono class D speaker driver
- Ground centered headphone driver
- Mono ear speaker driver
- 256/384Fs, USB 12/24 MHz, fractional PLL for wide range of system clocks
- Sophisticated analog input and output routing, mixing and gain
- Support analog and digital microphone
- GPIO
- I$^2$C interface

ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 95 dB dynamic range, 95 dB signal to noise ratio, -85 dB THD+N
- Low noise pre-amplifier
- Auto level control (ALC) and noise gate
- Microphone bias

DAC

- 24-bit, 8 to 96 kHz sampling frequency
- 95 dB dynamic range, 95 dB signal to noise ratio, -85 dB THD+N
- Digital peak limiter (DPL)
- Pop and click noise suppression

DSP

- Flexible digital signal routing and mixing
- Asynchronous sample rate conversion
- Six programmable digital filters for PEQ and noise reduction
- Stereo enhancement
- Support u/A law

Low Power

- 1.8V to 3.3V operation
- 7 mW playback; 16 mW playback and record

## APPLICATIONS

- MID/Phoblet
- Smart Phone
- Digital amplifier

## ORDERING INFORMATION

ES8396 -40°C ~ +85°C
QFN-48

## 1. BLOCK DIAGRAM

MCLK

SCL
SDA

GPIO1/DMIC_SCL1
GPIO2/DMIC_SCL2

BCLK1
LRCK1
DACDAT1
ADCDAT1
BCLK2
LRCK2
DACDAT2
ADCDAT2

| PLL Clock Mgr | I²C | GPIO | I²S/PCM 1 | I²S/PCM 2 |

DSP
ASRC
Mixing
ADC ALC
DAC DPL
Programmable Filters
PEQ
SE
u/A Law

L/R Line Mixer Out
L/R Aux Mixer Out
L/R Mono Mixer Out

PGA

Stereo ADC

Stereo DAC

L/R ADC PGA Out

L/R DAC Out

AINL/AINR
MONOP/MONON

Line Mixer
Aux Mixer
Mono Mixer
HP Mixer
SPK Mixer

L/R Line Mixer Out
L/R Aux Mixer Out
L/R Mono Mixer Out
L/R HP Mixer Out
L/R, P/N SPK Mixer Out

Line Driver
Aux Driver
Mono Driver
HP Driver
SPK Driver

LOUT1/ROUT1 (LOUT1N)

MONOUTP/MONOUTN

HPLOUT/HPROUT

SPKLOUTP/SPKLOUTN

SPKROUTP/SPKROUTN

AINL/AINR
MONOP/MONON
MIC1P/MIC1N
MIC2P/MIC2N

MICP/MICN

D2S Preamp

Charge Pump

Mic Bias

Analog Reference

Power Supply and LDO

CPVSSP
CPBOT
CPTOP
CPGND
CPVDD

MICBIAS

VMID
DACVRP
ADCVRP

SPKGND
SPKLDO
SPKVDD2
SPKVDD1
AGND
AVDDLDO
AVDD
DGND
DPVDD
DCVDD

## 2. PIN OUT AND DESCRIPTION

```
                SPKRROUTP
                 SPKVDD2
                SPKRROUTN
                SPKLOUTN
                 SPKVDD1
                SPKLOUTP
                  SPKGND
                  SPKLDO
                  HPLOUT
                  HPROUT
                   CPBOT
                   CPGND

                48  47  46  45  44  43  42  41  40  39  38  37

      GPIO1  | 1                                              36 |  CPVSSP
    DACDAT1  | 2                                              35 |  CPTOP
    ADCDAT1  | 3                                              34 |  CPVDD
      BCLK1  | 4               ES8396                         33 |  DACVRP
      LRCK1  | 5                                              32 |  MONOUTN
        SDA  | 6               QFN 48                         31 |  MONOUTP
        SCL  | 7                                              30 |  AVDDLDO
      DPVDD  | 8                                              29 |  AVDD
       DGND  | 9                                              28 |  AGND
      DCVDD  | 10                                             27 |  VMID
       MCLK  | 11                                             26 |  ADCVRP
      GPIO2  | 12                                             25 |  MICN

                13  14  15  16  17  18  19  20  21  22  23  24

                 BCLK2
                 LRCK2
                DACDAT2
                ADCDAT2
                   ROUT
                   LOUT
                 MICBIAS
                  MONOP
                  MONON
                   AINR
                   AINL
                   MICP
```

| Name | Type | Description |
|------|------|-------------|
| MCLK | DI | Master clock |
| SDA | DIO | I$^2$C data |
| SCL | DI | I$^2$C clock |
| GPIO1 | DIO | GPIO (digital mic clock, ADC LRCK, etc) |
| GPIO2 | DIO | GPIO (digital mic clock, ADC LRCK, etc) |
|  |  |  |
| ADCDAT1/AD0 | DIO | I$^2$S/PCM serial data out; Also used as I$^2$C address |
| DACDAT1 | DI | I$^2$S/PCM serial data in |
| LRCK1 | DIO | I$^2$S/PCM left and right clock |
| BCLK1 | DIO | I$^2$S/PCM bit clock |
| ADCDAT2 | DIO | I$^2$S/PCM serial data out |
| DACDAT2 | DI | I$^2$S/PCM serial data in |
| LRCK2 | DIO | I$^2$S/PCM left and right clock |
| BCLK2 | DIO | I$^2$S/PCM bit clock |
|  |  |  |
| AINL/JD1 | AI | Left analog line input or jack detect 1 |
| AINR/JD2 | AI | Right analog line input or jack detect 2 |
| MONOP | AI | Mono positive input or left analog line input |
| MONON | AI | Mono negative input or right analog line input |
| MICP | AI | Mic positive input or left analog line input |
| MICN/DMIC_SDA | AI | Mic negative input or right analog line input or digital mic data |

| | | |
|---|---|---|
| LOUT | AO | Left line out |
| ROUT/LOUTN | AO | Right line out or negative left line out |
| MONOUTP | AO | Mono positive output |
| MONOUTN | AO | Mono negative output |
| HPLOUT | AO | Left headphone out |
| HPROUT | AO | Right headphone out |
| SPKLOUTP | AO | Positive left speaker out |
| SPKLOUTN | AO | Negative left speaker out |
| SPKROUTP | AO | Positive right speaker out |
| SPKROUTN | AO | Negative right speaker out |
| | | |
| CPVDD | | Charge pump power supply |
| CPGND | | Charge pump ground |
| CPTOP | | Charge pump capacitor top |
| CPBOT | | Charge pump capacitor bottom |
| CPVSSP | | Charge pump filtering |
| | | |
| MICBIAS | AO | Mic bias |
| | | |
| ADCVRP | | ADC reference filtering |
| DACVRP | | DAC reference filtering |
| VMID | | Common mode filtering |
| | | |
| DCVDD | | Digital core power supply |
| DPVDD | | Digital IO power supply |
| DGND | | Digital ground |
| AVDD | | Analog power supply |
| AVDDLDO | | Analog LDO power supply |
| AGND | | Analog ground |
| SPKVDD1 | | Speaker driver power supply |
| SPKVDD2 | | Speaker driver power supply |
| SPKLDO | | Speaker driver LDO power supply |
| SPKGND | | Speaker driver ground |

## 3. TYPICAL APPLICATION CIRCUIT
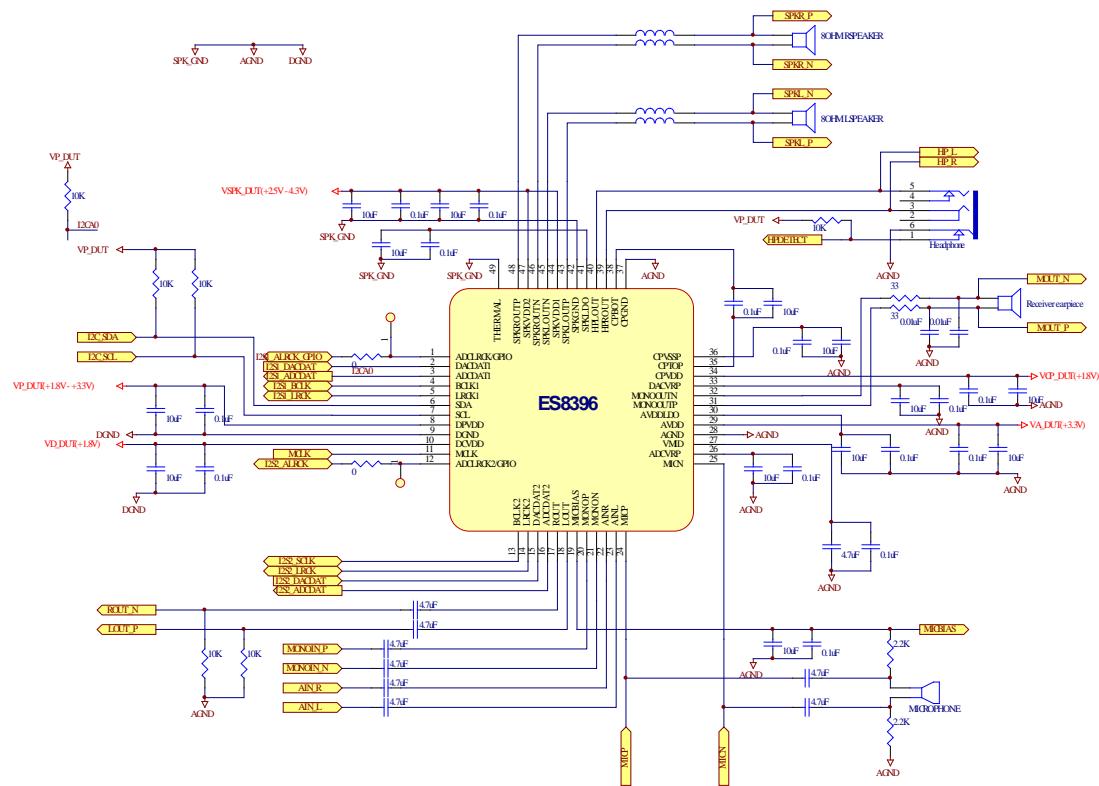
## 4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports three types of clocking: standard audio clocks (256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and an on-chip 22-bit fractional PLL clock.

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

## 5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard $I^2C$ micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

$I^2C$ interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 100 kbps.
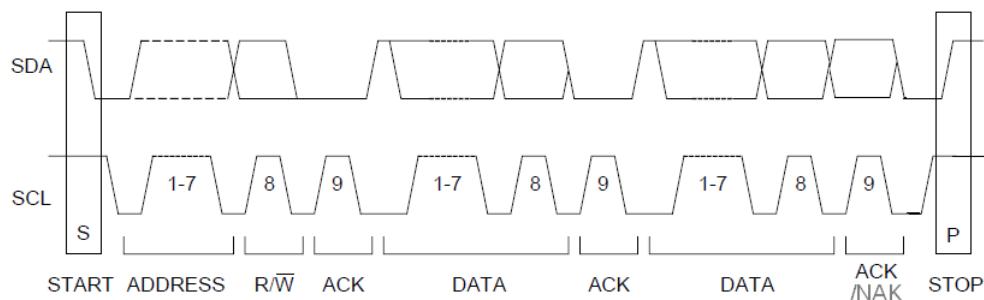


Figure 1 Data Transfer for $I^2C$ Interface

A master controller initiates the transmission by sending a "start" signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals AD0. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a "stop" signal, which is defined as a low-to-high transition at SDA while SCL is high.

In I$^2$C interface mode, the registers can be written and read. The formats of "write" and "read" instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register. There are no acknowledge bit after data to be written or read, this is the only difference from the I$^2$C protocol.

Table 1 Write Data to Register in I$^2$C Interface Mode

| Chip Address | | R/W | | Register Address | | Data to be written |
|---|---|---|---|---|---|---|
| 001000 | AD0 | 0 | ACK | RAM | ACK | DATA |

Table 2 Read Data from Register in I$^2$C Interface Mode

| Chip Address | | R/W | | Register Address |
|---|---|---|---|---|
| 001000 | AD0 | 0 | ACK | RAM |
| Chip Address | | R/W | | Data to be read |
| 001000 | AD0 | 1 | ACK | Data |

## 6. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, BCLK (SCLK) and DACDAT/ADCDAT pins. These formats are I$^2$S, left justified, right justified, DSP/PCM and TDM mode. DAC input DACDAT is sampled by the device on the rising edge of SCLK. ADC data is out at ADCDAT on the falling edge of SCLK. The relationship of SDATA (DACDAT/ADCDAT), SCLK and LRCK with these formats are shown through Figure 2 to Figure 6.
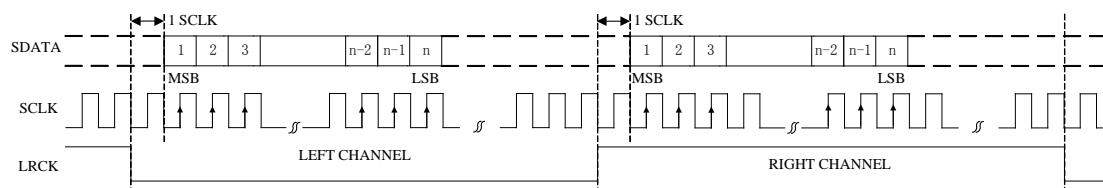


Figure 2 I$^2$S Serial Audio Data Format Up To 24-bit
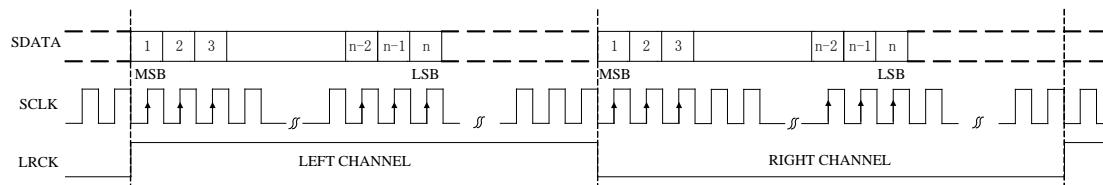


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit
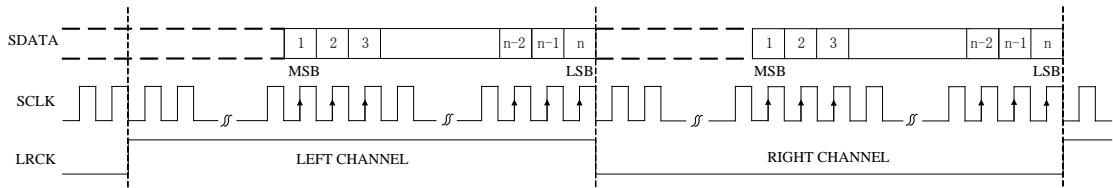
Figure 4 Right Justified Serial Audio Data Format Up To 24-bit
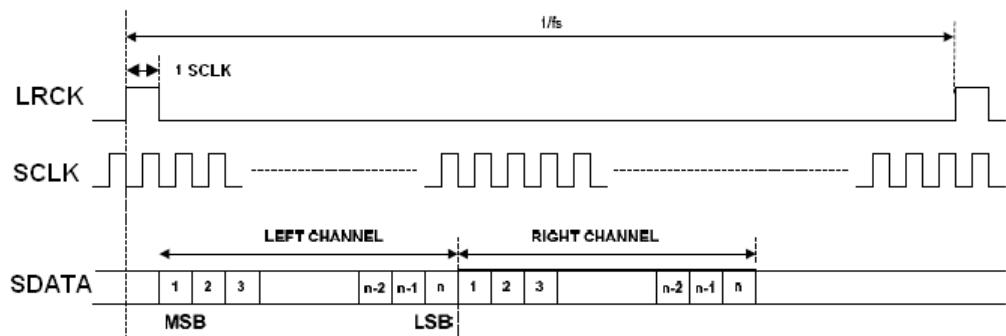


Figure 5 DSP/PCM Mode A
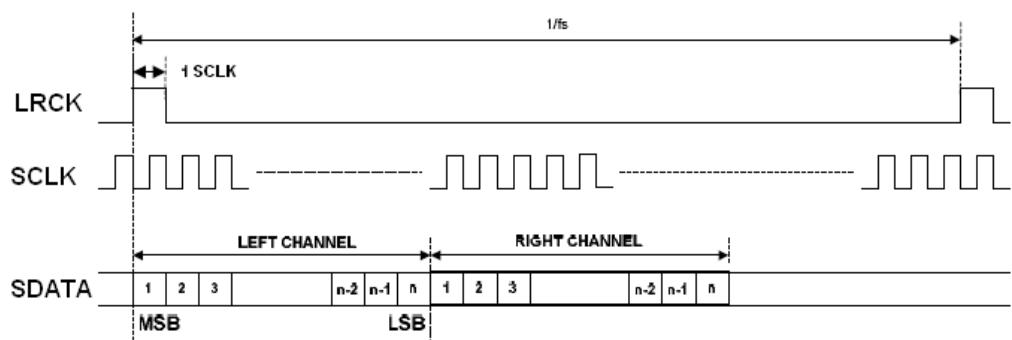


Figure 6 DSP/PCM Mode B

## 7. ELECTRICAL CHARACTERISTICS

*ABSOLUTE MAXIMUM RATINGS*

Continuous operation at or beyond these conditions may permanently damage the device.

| PARAMETER | MIN | MAX |
|---|---|---|
| Analog Supply Voltage Level | -0.3V | +4.5V |
| Digital Supply Voltage Level | -0.3V | +5.0V |
| Input Voltage Range | DGND-0.3V | DVDD+0.3V |
| Operating Temperature Range | -40°C | +85°C |
| Storage Temperature | -65°C | +150°C |

*RECOMMENDED OPERATING CONDITIONS*

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Analog Supply Voltage Level | 2.0 | 3.3 | 3.6 | V |
| Analog Supply Voltage Level – Class D | 2.5 | 4.0 | 4.3 | V |
| Digital Supply Voltage Level – DCVDD | 1.6 | 1.8 | 2.0 | V |
| Digital Supply Voltage Level – DPVDD | 1.6 | 1.8 | 3.6 | V |

*ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS*

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DCVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| ADC Performance | | | | |
| Signal to Noise ratio (A-weigh) | 85 | 95 | 98 | dB |
| THD+N | -88 | -85 | -75 | dB |
| Channel Separation (1KHz) | 80 | 85 | 90 | dB |
| Interchannel Gain Mismatch | | 0.1 | | dB |
| Gain Error | | | ±5 | % |
| Filter Frequency Response – Single Speed | | | | |
| Passband | 0 | | 0.4535 | Fs |
| Stopband | 0.5465 | | | Fs |
| Passband Ripple | | | ±0.05 | dB |
| Stopband Attenuation | 50 | | | dB |
| Filter Frequency Response – Double Speed | | | | |
| Passband | 0 | | 0.4167 | Fs |
| Stopband | 0.5833 | | | Fs |
| Passband Ripple | | | ±0.005 | dB |
| Stopband Attenuation | 50 | | | dB |
| Analog Input | | | | |
| Full Scale Input Level | | AVDD/3.3 | | Vrms |
| Input Impedance | | 20 | | KΩ |

*DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS*

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DCVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| DAC Performance | | | | |
| Signal to Noise ratio (A-weigh) | 83 | 96 | 98 | dB |
| THD+N | -85 | -83 | -75 | dB |
| Channel Separation (1KHz) | 80 | 85 | 90 | dB |
| Interchannel Gain Mismatch | | 0.05 | | dB |
| Filter Frequency Response – Single Speed | | | | |
| Passband | 0 | | 0.4535 | Fs |
| Stopband | 0.5465 | | | Fs |
| Passband Ripple | | | ±0.05 | dB |
| Stopband Attenuation | 40 | | | dB |
| Filter Frequency Response – Double Speed | | | | |
| Passband | 0 | | 0.4167 | Fs |
| Stopband | 0.5833 | | | Fs |
| Passband Ripple | | | ±0.005 | dB |
| Stopband Attenuation | 40 | | | dB |
| De-emphasis Error at 1 KHz (Single Speed Mode Only) | | | | |
| Fs = 32KHz<br>Fs = 44.1KHz<br>Fs = 48KHz | | | 0.002<br>0.013<br>0.0009 | dB |
| Analog Output | | | | |
| Full Scale Output Level | | AVDD/3.3 | | Vrms |

*POWER CONSUMPTION CHARACTERISTICS*

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Normal Operation Mode | | | | |
| DVDD=1.8V, AVDD=1.8V:<br>Play back<br>Play back and record<br>DVDD=3.3V, AVDD=3.3V:<br>Play back<br>Play back and record | | <br>7<br>16<br><br>31<br>59 | | mW |
| Power Down Mode | | | | |
| DVDD=1.8V, AVDD=1.8V<br>DVDD=3.3V, AVDD=3.3V | | TBD<br>TBD | | mW |

*SERIAL AUDIO PORT SWITCHING SPECIFICATIONS*

| PARAMETER | Symbol | MIN | MAX | UNIT |
|---|---|---|---|---|
| MCLK frequency | | | 51.2 | MHz |
| MCLK duty cycle | | 40 | 60 | % |
| LRCK frequency | | | 200 | KHz |

| | | | | |
|---|---|---|---|---|
| LRCK duty cycle | | 40 | 60 | % |
| SCLK frequency | | | 26 | MHz |
| SCLK pulse width low | TSCLKL | 15 | | ns |
| SCLK Pulse width high | TSCLKH | 15 | | ns |
| SCLK falling to LRCK edge | TSLR | −10 | 10 | ns |
| SCLK falling to SDOUT valid | TSDO | 0 | | ns |
| SDIN valid to SCLK rising setup time | TSDIS | 10 | | ns |
| SCLK rising to SDIN hold time | TSDIH | 10 | | ns |
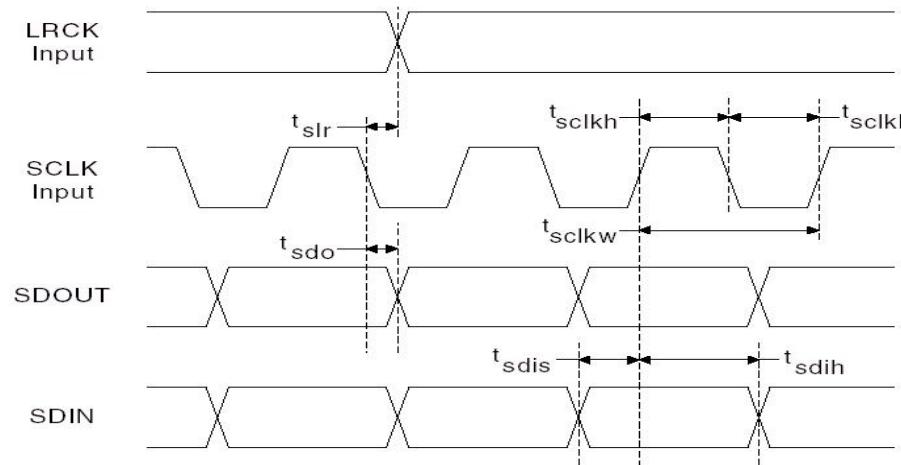


Figure 8 Serial Audio Port Timing

## $I^2C$ SWITCHING SPECIFICATIONS

| PARAMETER | Symbol | MIN | MAX | UNIT |
|---|---|---|---|---|
| SCL Clock Frequency | FSCL | | 100 | KHz |
| Bus Free Time Between Transmissions | TTWID | 4.7 | | us |
| Start Condition Hold Time | TTWSTH | 4.0 | | us |
| Clock Low time | TTWCL | 4.0 | | us |
| Clock High Time | TTWCH | 4.0 | | us |
| Setup Time for Repeated Start Condition | TTWSTS | 4.7 | | us |
| SDA Hold Time from SCL Falling | TTWDH | 0.1 | | us |
| SDA Setup time to SCL Rising | TTWDS | 100 | | ns |
| Rise Time of SCL | TTWR | | 25 | us |
| Fall Time SCL | TTWF | | 25 | ns |
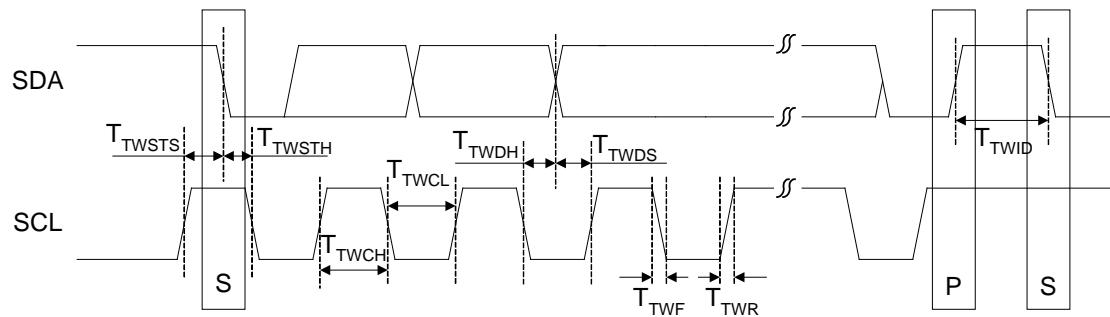
Figure 10 I$^2$C Timing

## 8. CONFIGURATION REGISTER DEFINITION

*ADDRESS 0X00, RESET*

| Bit Name | Bit | R/W | Default | Description |
|---|---|---|---|---|
| seq_dis | 1 | R/W | 0 | Automatic power up sequence<br>0 – sequence enable<br>1 – sequence disable |
| rst_reg | 0 | R/W | 0 | Reset all registers to default values.<br>This bit will auto clear to '0' after reset. |

*ADDRESS 0X01, CLOCK SCHEME*

| Bit Name | Bit | R/W | Default | Description |
|---|---|---|---|---|
| mclk_div2 | 4 | R/W | 0 | 0 – MCLK no divide<br>1 – MCLK divide by 2 |
| clk2_src | 3:2 | R/W | 0 | clk2 source<br>0 – 0<br>1 – MCLK (MCLK/2 if mclk_div2 is '1')<br>2 – 1<br>3 – BCLK1 |
| clk1_src | 1:0 | R/W | 0 | clk1 source<br>0 – MCLK (MCLK/2 if mclk_div2 is '1')<br>1 – 1<br>2 – 0<br>3 – BCLK1 |

*ADDRESS 0X02, CLOCK SCHEME*

| Bit Name | Bit | R/W | Default | Description |
|---|---|---|---|---|
| pll_pdn | 7 | R/W | 1 | 0 – enable PLL analog<br>1 – power down PLL analog |
| pll_rb | 6 | R/W | 0 | 0 – reset PLL digital<br>1 – PLL digital on |
| plldith_mag | 4:2 | R/W | 0 | PLL DSM divider dither<br>0 – dither off<br>1 – minimum dither<br>…<br>7 – maximum dither<br><br>This register reuse as calibration control<br>plldith_mag[2] – pll_cal_short :<br>0 – pll calibrate 64 data<br>1 – pll calibrate 32 data<br>plldith_mag[1:0] – pll_vco_wait[1:0] :<br>0 – wait 2 MCLK cycles for vco stable<br>1 – wait 4 MCLK cycles for vco stable<br>2 – wait 8 MCLK cycles for vco stable<br>3 – wait 16 MCLK cycles for vco stable |
| pllout_sel | 1:0 | R/W | 0 | PLL output select<br>0 – PLL clock in (PLL bypass)<br>1 – vcoout divide by 8<br>2 – vcoout divide by 4 |

| | | | | 3 – vcoout divide by 2 |
|---|---|---|---|---|

### ADDRESS 0X03, CLOCK SCHEME

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pll_lp | 7 | R/W | 0 | 0 – normal<br>1 – PLL analog low power mode |
| pll_cp | 6:4 | R/W | 0 | |
| pll_supsel | 3:2 | R/W | 0 | 0 – 1.8V |
| pll_kvco | 1:0 | R/W | 0 | |

### ADDRESS 0X04, CLOCK SCHEME

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pll_n | 3:0 | R/W | 0 | Integer part of PLL input/output frequency ratio<br>Use value greater than 5 and less than 13 |

### ADDRESS 0X05, CLOCK SCHEME

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pll_k[21:16] | 5:0 | R/W | 0 | Fractional part of PLL input/output frequency ratio (treat as one 22-bit binary number); fraction= pll_k/0.65735982222960 |

### ADDRESS 0X06, CLOCK SCHEME

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pll_k[15:8] | 7:0 | R/W | 0 | Fractional part of PLL input/output frequency ratio (treat as one 22-bit binary number) |

### ADDRESS 0X07, CLOCK SCHEME

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pll_k[7:0] | 7:0 | R/W | 0 | Fractional part of PLL input/output frequency ratio (treat as one 22-bit binary number) |

### ADDRESS 0X08, CLOCK SCHEME

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| clk_adc_dis | 7 | R/W | 0 | 0 – enable adc clock divider<br>1 – disable adc clock divider |
| clk_dac_dis | 6 | R/W | 1 | 0 – enable dac clock divider<br>1 – disable dac clock divider |
| clk_cp_dis | 5 | R/W | 0 | 0 – enable charge pump clock divider<br>1 – disable charge pump clock divider |
| clk_clsd_dis | 4 | R/W | 1 | 0 – enable class D clock divider<br>1 – disable class D clock divider |
| clk_adc_src | 3 | R/W | 0 | adc clock divider source<br>0 – from clk1<br>1 – from clk2 |
| clk_dac_src | 2 | R/W | 0 | dac clock divider source<br>0 – from clk1<br>1 – from clk2 |
| clk_cp_src | 1 | R/W | 0 | charge pump clock divider source<br>0 – from clk1<br>1 – from clk2 |

| | | | | |
|---|---|---|---|---|
| clk_clsd_src | 0 | R/W | 0 | class D clock divider source<br>0 – from clk1<br>1 – from clk2 |

### *ADDRESS 0X09, CLOCK SCHEME*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| div_adc[7:0] | 7:0 | R/W | 0x04 | adc clock divider ratio; default adc clock is MCLK divide by 4; ratio "0" will hold adc clock divider |

### *ADDRESS 0X0A, CLOCK SCHEME*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| div_dac[7:0] | 7:0 | R/W | 0x00 | dac clock divider ratio; ratio "0" will hold dac clock divider |

### *ADDRESS 0X0B, CLOCK SCHEME*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| div_cp[5:0] | 5:0 | R/W | 0x20 | Charge pump clock divider ratio; for example, clk1=12.288MHz, default clk_cp is 12.288M/32=384K |

### *ADDRESS 0X0C, CLOCK SCHEME*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| div_clsd[5:0] | 5:0 | R/W | 0x20 | Class D clock divider ratio; for example, clk1=12.288MHz, default clk_cp is 12.288M/32=384K |

### *ADDRESS 0X0D, CLOCK SCHEME*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| dll_pwd | 6 | R/W | 0 | 0 – DLL on<br>1 – DLL power down |
| dll_ana_pwd | 5 | R/W | 0 | 0 – DLL analog clock in enable<br>1 – DLL analog clock in disable |
| dllbypass | 4 | R/W | 0 | 0 – DLL enable<br>1 – DLL bypass |
| dac_mclk_sel | 0 | R/W | 0 | 0 – dac mclk from ADC<br>1 – dac mclk from dac clock divider |

### *ADDRESS 0X0E, CLOCK SCHEME*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| bclk_inv_m1 | 6 | R/W | 0 | bclk_m1 inversion<br>0 – normal<br>1 – inversion | |
| mclk_src_m1 | 5 | R/W | 0 | bclk_m1 clock divider clock source<br>0 – from clk1<br>1 – from clk2 | |
| bclk_div_m1[4:0] | 4:0 | R/W | 0 | bclk_m1 clock divider ratio | |
| | | | | 0~18 – divide by bclk_div_m1<br>19 – divide by 20<br>20 – divide by 22<br>21 – divide by 24<br>22 – divide by 25<br>23 – divide by 30 | 25 – divide by 33<br>26 – divide by 34<br>27 – divide by 36<br>28 – divide by 44<br>29 – divide by 48<br>30 – divide by 66 |

| | | | | 24 – divide by 32 | 31 – divide by 72 |
|---|---|---|---|---|---|

### ADDRESS 0X0F, CLOCK SCHEME

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| bclk_inv_m2 | 6 | R/W | 0 | bclk_m2 inversion<br>0 – normal<br>1 – inversion | |
| mclk_src_m2 | 5 | R/W | 0 | bclk_m2 clock divider clock source<br>0 – from clk1<br>1 – from clk2 | |
| bclk_div_m2[4:0] | 4:0 | R/W | 0 | bclk_m2 clock divider ratio | |
| | | | | 0~18 – divide by bclk_div_m2<br>19 – divide by 20<br>20 – divide by 22<br>21 – divide by 24<br>22 – divide by 25<br>23 – divide by 30<br>24 – divide by 32 | 25 – divide by 33<br>26 – divide by 34<br>27 – divide by 36<br>28 – divide by 44<br>29 – divide by 48<br>30 – divide by 66<br>31 – divide by 72 |

### ADDRESS 0X10, CLOCK SCHEME

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| mclk_src_m3 | 5 | R/W | 0 | lrck_m3 clock divider clock source<br>0 – from clk1<br>1 – from clk2 | |
| mclk_ratio_m3[4:0] | 4:0 | R/W | 0 | lrck_m3 clock divider ratio | |
| | | | | 00000 – 128<br>00001 – 192<br>00010 – 256<br>00011 – 384<br>00100 – 512<br>00101 – 576<br>00110 – 768<br>00111 – 1024<br>01000 – 1152<br>01001 – 1408<br>01010 – 1536<br>01011 – 2112<br>01100 – 2304 | 10000 – 125<br>10001 – 136<br>10010 – 250<br>10011 – 272<br>10100 – 375<br>10101 – 500<br>10110 – 544<br>10111 – 750<br>11000 – 1000<br>11001 – 1088<br>11010 – 1496<br>11011 – 1500<br>Other – Reserved |

### ADDRESS 0X11, CLOCK SCHEME

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| mclk_src_m4 | 5 | R/W | 0 | lrck_m4 clock divider clock source<br>0 – from clk1<br>1 – from clk2 | |
| mclk_ratio_m4[4:0] | 4:0 | R/W | 0 | lrck_m4 clock divider ratio | |
| | | | | 00000 – 128<br>00001 – 192<br>00010 – 256<br>00011 – 384<br>00100 – 512 | 10000 – 125<br>10001 – 136<br>10010 – 250<br>10011 – 272<br>10100 – 375 |

| | | | | 00101 – 576 | 10101 – 500 |
|---|---|---|---|---|---|
| | | | | 00110 – 768 | 10110 – 544 |
| | | | | 00111 – 1024 | 10111 – 750 |
| | | | | 01000 – 1152 | 11000 – 1000 |
| | | | | 01001 – 1408 | 11001 – 1088 |
| | | | | 01010 – 1536 | 11010 – 1496 |
| | | | | 01011 – 2112 | 11011 – 1500 |
| | | | | 01100 – 2304 | Other – Reserved |

### ADDRESS 0X12, PAD MUX

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| lrck1_adc_src | 7:6 | R/W | 0 | SDP1 out LRCK select<br>0/3 – from LRCK1<br>1 – from ADCLRCK<br>2 – from ADCLRCK2 |
| lrck1_dir | 5 | R/W | 0 | LRCK1 direction select<br>0 – LRCK1 is input<br>1 – LRCK1 is output |
| lrck1_src | 4:3 | R/W | 0 | LRCK1 source<br>0 – from lrck_m3<br>1 – from lrck_m4<br>2 – 0<br>3 – 1 |
| bclk1_dir | 2 | R/W | 0 | BCLK1 direction select<br>0 – BCLK1 is input<br>1 – BCLK1 is output |
| bclk1_src | 1:0 | R/W | 0 | BCLK1 source<br>0 – from bclk_m1<br>1 – from bclk_m2<br>2 – 0<br>3 – 1 |

### ADDRESS 0X13, PAD MUX

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| lrck2_adc_src | 7:6 | R/W | 0 | SDP2 out LRCK select<br>0/3 – from LRCK2<br>1 – from ADCLRCK<br>2 – from ADCLRCK2 |
| lrck2_dir | 5 | R/W | 0 | LRCK2 direction select<br>0 – LRCK2 is input<br>1 – LRCK2 is output |
| lrck2_src | 4:3 | R/W | 0 | LRCK2 source<br>0 – from lrck_m3<br>1 – from lrck_m4<br>2 – 0<br>3 – 1 |
| bclk2_dir | 2 | R/W | 0 | BCLK2 direction select<br>0 – BCLK2 is input<br>1 – BCLK2 is output |
| bclk2_src | 1:0 | R/W | 0 | BCLK2 source<br>0 – from bclk_m1 |

| | | | | 1 – from bclk_m2<br>2 – 0<br>3 – 1 |
|---|---|---|---|---|

### *ADDRESS 0X14, PAD MUX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| lrck3_adc_src | 7:6 | R/W | 0 | SDP3 out LRCK select<br>0/3 – from LRCK3<br>1 – from ADCLRCK<br>2 – from ADCLRCK2 |
| lrck3_dir | 5 | R/W | 0 | LRCK3 direction select<br>0 – LRCK3 is input<br>1 – LRCK3 is output |
| lrck3_src | 4:3 | R/W | 0 | LRCK3 source<br>0 – from lrck_m3<br>1 – from lrck_m4<br>2 – 0<br>3 – 1 |
| bclk3_dir | 2 | R/W | 0 | BCLK3 direction select<br>0 – BCLK3 is input<br>1 – BCLK3 is output |
| bclk3_src | 1:0 | R/W | 0 | BCLK3 source<br>0 – from bclk_m1<br>1 – from bclk_m2<br>2 – 0<br>3 – 1 |

### *ADDRESS 0X15, PAD MUX*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| adclrck2_dir | 7 | R/W | 0 | ADCLRCK2 direction select<br>0 – ADCLRCK2 is input<br>1 – ADCLRCK2 is output | |
| adclrck2_src | 6:4 | R/W | 0 | ADCLRCK2 source | |
| | | | | 0 – lrck_m3<br>1 – lrck_m4<br>2 – DMIC_SCL<br>3 – int2_out | 4 – divclk<br>5 – clk_cp<br>6 – lrck_eq_out<br>7 – int1_out |
| adclrck_dir | 3 | R/W | 0 | ADCLRCK direction select<br>0 – ADCLRCK is input<br>1 – ADCLRCK is output | |
| adclrck _src | 2:0 | R/W | 0 | ADCLRCK source | |
| | | | | 0 – lrck_m3<br>1 – lrck_m4<br>2 – DMIC_SCL<br>3 – int1_out | 4 – adc_mclk<br>5 – dac_mclk<br>6 – clk_clsd<br>7 – int2_out |

### *ADDRESS 0X16, GPIO*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| int1_en | 7 | R/W | 0 | 0 – interrupt1 disable<br>1 – interrupt1 enable |

| int1_pol | 6 | R/W | 0 | interrupt1 polarity<br>0 – high active<br>1 – low active |
| int2_en | 5 | R/W | 0 | 0 – interrupt2 disable<br>1 – interrupt2 enable |
| int2_pol | 4 | R/W | 0 | interrupt2 polarity<br>0 – high active<br>1 – low active |
| int1_src | 1 | R/W | 0 | interrupt1 source<br>0 – from AINL pin<br>1 – from AINR pin |
| int2_src | 0 | R/W | 0 | interrupt2 source<br>0 – from AINL pin<br>1 – from AINR pin |

### *ADDRESS 0X17, GPIO*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| gpio_bclk2 | 7 | R | 0 | Show BCLK2 level |
| gpio_bclk3 | 6 | R | 0 | Show BCLK3 level |
| gpio_lrck2 | 5 | R | 0 | Show LRCK2 level |
| gpio_lrck3 | 4 | R | 0 | Show LRCK3 level |
| gpio_adclrck | 3 | R | 0 | Show ADCLRCK level |
| gpio_adclrck2 | 2 | R | 0 | Show ADCLRCK2 level |
| gpio_ainl | 1 | R | 0 | Show AINL level |
| gpio_ainr | 0 | R | 0 | Show AINR level |

### *ADDRESS 0X18, DIGITAL MIXER*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| dmix_l_src | 6:4 | R/W | 0 | Left digital mixer source | |
| | | | | 0 – from left SDP1 in<br>1 – from left SDP2 in<br>2 – from left SDP3 in<br>3 – from left ADC | 4 – from right SDP1 in<br>5 – from right SDP2 in<br>6 – from right SDP3 in<br>7 – from right ADC |
| dmix_r_src | 2:0 | R/W | 0 | Right digital mixer source | |
| | | | | 0 – from right SDP1 in<br>1 – from right SDP2 in<br>2 – from right SDP3 in<br>3 – from right ADC | 4 – from left SDP1 in<br>5 – from left SDP2 in<br>6 – from left SDP3 in<br>7 – from left ADC |

### *ADDRESS 0X19, DIGITAL MIXER*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| eq_l_src | 6:4 | R/W | 0 | Left 3-band EQ source | |
| | | | | 0 – from left SDP1 in<br>1 – from left SDP2 in<br>2 – from left SDP3 in<br>3 – from left ADC | 4 – from right SDP1 in<br>5 – from right SDP2 in<br>6 – from right SDP3 in<br>7 – from right ADC |
| eq_r_src | 2:0 | R/W | 0 | Right 3-band EQ source | |

| | | | | 0 – from right SDP1 in<br>1 – from right SDP2 in<br>2 – from right SDP3 in<br>3 – from right ADC | 4 – from left SDP1 in<br>5 – from left SDP2 in<br>6 – from left SDP3 in<br>7 – from left ADC |
|---|---|---|---|---|---|

### *ADDRESS 0X1A, DIGITAL MIXER*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| dac_l_src | 6:4 | R/W | 0 | DAC source | |
| | | | | 0 – from SDP1 in<br>1 – from SDP2 in<br>2 – from SDP3 in<br>3 – from ADC | 4 – from 3-band EQ stereo out<br>5 – from 3-band EQ left out<br>6 – from 3-band EQ right out |
| sdp1_r_src | 2:0 | R/W | 0 | SDP1 output source | |
| | | | | 0 – from ADC<br>1 – from SDP1 in<br>2 – from SDP2 in<br>3 – from SDP3 in | 4 – from 3-band EQ stereo out<br>5 – from 3-band EQ left out<br>6 – from 3-band EQ right out |

### *ADDRESS 0X1B, DIGITAL MIXER*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| sdp2_l_src | 6:4 | R/W | 0 | SDP2 output source | |
| | | | | 0 – from ADC<br>1 – from SDP1 in<br>2 – from SDP2 in<br>3 – from SDP3 in | 4 – from 3-band EQ stereo out<br>5 – from 3-band EQ left out<br>6 – from 3-band EQ right out |
| sdp3_r_src | 2:0 | R/W | 0 | SDP1 output source | |
| | | | | 0 – from ADC<br>1 – from SDP1 in<br>2 – from SDP2 in<br>3 – from SDP3 in | 4 – from 3-band EQ stereo out<br>5 – from 3-band EQ left out<br>6 – from 3-band EQ right out |

### *ADDRESS 0X1C, DIGITAL MIXER*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| eqclk_sel | 5:4 | R/W | 0 | 3-band EQ clock select | |
| | | | | 0 – from dac_mclk<br>1 – from adc_mclk | 2 – from clk1<br>3 – from clk2 |
| eq_osr | 2:0 | R/W | 0 | 3-band EQ oversample rate | |
| | | | | 0 – 1x FS<br>1 – 2x FS<br>2 – 3x FS | 3 – 4x FS<br>4 – 5x FS<br>5 – 6x FS |

### *ADDRESS 0X1D, DIGITAL MIXER*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| share_wr_mode | 7 | R/W | 0 | Share register write mode<br>0 – auto address increase write mode<br>1 – manual write mode |
| share_addr | 6:0 | R/W | 0 | Share register address<br>share_addr will increase 1 automatically at auto address<br>increase write mode when a write operation to share_data |

### ADDRESS 0X1E, DIGITAL MIXER

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| share_data | 7:0 | R/W | 0 | Share register data |

SHARE REGISTER MAP:

| share_addr | share_data | share_addr | share_data | share_addr | share_data | share_addr | share_data |
|---|---|---|---|---|---|---|---|
| 0x03 | eq1_b0[29:24] | 0x02 | eq1_b0[23:16] | 0x01 | eq1_b0[15:8] | 0x00 | eq1_b0[7:0] |
| 0x07 | eq1_b1[29:24] | 0x06 | eq1_b1[23:16] | 0x05 | eq1_b1[15:8] | 0x04 | eq1_b1[7:0] |
| 0x0B | eq1_b2[29:24] | 0x0A | eq1_b2[23:16] | 0x09 | eq1_b2[15:8] | 0x08 | eq1_b2[7:0] |
| 0x0F | eq1_a1[29:24] | 0x0E | eq1_a1[23:16] | 0x0D | eq1_a1[15:8] | 0x0C | eq1_a1[7:0] |
| 0x13 | eq1_a2[29:24] | 0x12 | eq1_a2[23:16] | 0x11 | eq1_a2[15:8] | 0x10 | eq1_a2[7:0] |
| 0x17 | eq2_b0[29:24] | 0x16 | eq2_b0[23:16] | 0x15 | eq2_b0[15:8] | 0x14 | eq2_b0[7:0] |
| 0x1B | eq2_b1[29:24] | 0x1A | eq2_b1[23:16] | 0x19 | eq2_b1[15:8] | 0x18 | eq2_b1[7:0] |
| 0x1F | eq2_b2[29:24] | 0x1E | eq2_b2[23:16] | 0x1D | eq2_b2[15:8] | 0x1C | eq2_b2[7:0] |
| 0x23 | eq2_a1[29:24] | 0x22 | eq2_a1[23:16] | 0x21 | eq2_a1[15:8] | 0x20 | eq2_a1[7:0] |
| 0x27 | eq2_a2[29:24] | 0x26 | eq2_a2[23:16] | 0x25 | eq2_a2[15:8] | 0x24 | eq2_a2[7:0] |
| 0x2B | eq3_b0[29:24] | 0x2A | eq3_b0[23:16] | 0x29 | eq3_b0[15:8] | 0x28 | eq3_b0[7:0] |
| 0x2F | eq3_b1[29:24] | 0x2E | eq3_b1[23:16] | 0x2D | eq3_b1[15:8] | 0x2C | eq3_b1[7:0] |
| 0x33 | eq3_b2[29:24] | 0x32 | eq3_b2[23:16] | 0x31 | eq3_b2[15:8] | 0x30 | eq3_b2[7:0] |
| 0x37 | eq3_a1[29:24] | 0x36 | eq3_a1[23:16] | 0x35 | eq3_a1[15:8] | 0x34 | eq3_a1[7:0] |
| 0x3B | eq3_a2[29:24] | 0x3A | eq3_a2[23:16] | 0x39 | eq3_a2[15:8] | 0x38 | eq3_a2[7:0] |
| 0x3F | eq4_b1[29:24] | 0x3E | eq4_b1[23:16] | 0x3D | eq4_b1[15:8] | 0x3C | eq4_b1[7:0] |
| 0x43 | eq4_a1[29:24] | 0x42 | eq4_a1[23:16] | 0x41 | eq4_a1[15:8] | 0x40 | eq4_a1[7:0] |
| 0x47 | eq5_b1[29:24] | 0x46 | eq5_b1[23:16] | 0x45 | eq5_b1[15:8] | 0x44 | eq5_b1[7:0] |
| 0x4B | eq5_a1[29:24] | 0x4A | eq5_a1[23:16] | 0x49 | eq5_a1[15:8] | 0x48 | eq5_a1[7:0] |
| 0x4F | eq6_b1[29:24] | 0x4E | eq6_b1[23:16] | 0x4D | eq6_b1[15:8] | 0x4C | eq6_b1[7:0] |
| 0x53 | eq6_a1[29:24] | 0x52 | eq6_a1[23:16] | 0x51 | eq6_a1[15:8] | 0x50 | eq6_a1[7:0] |
| 0x57 | offset1_r[11:8] | 0x56 | offset1_r[7:0] | 0x55 | offset1_l[11:8] | 0x54 | offset1_l[7:0] |
| 0x5B | offset2_r[11:8] | 0x5A | offset2_r[7:0] | 0x59 | offset2_l[11:8] | 0x58 | offset2_l[7:0] |

### ADDRESS 0X1F, SERIAL AUDIO INTERFACE

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| sdp1_in_mute | 6 | R/W | 0 | SDP1 in mute<br>0 – unmute<br>1 – mute |
| sdp1_in_fmt | 5:4 | R/W | 0 | SDP1 in audio data format<br>0 – I$^2$S<br>1 – LJ<br>2 – RJ<br>3 – DSP mode |
| sdp1_in_lrp | 3 | R/W | | SDP1 in LRCK polarity<br>I$^2$S/LJ/RJ case:<br>0 – L/R invert polarity<br>    Left/Right=Low/High (LJ, RJ) |

| | | | | Left/Right=High/Low (I2S) |
|---|---|---|---|---|
| | | | | 1 – L/R normal polarity |
| | | | | Left/Right=High/Low (LJ, RJ) |
| | | | | Left/Right=Low/High (I2S) |
| | | | | DSP mode case: |
| | | | | 0 – mode A, MSB is available on 2$^{nd}$ SCLK rising edge after LRCK rising edge |
| | | | | 1 – mode B, MSB is available on 1$^{st}$ SCLK rising edge after LRCK rising edge |
| sdp1_in_wl | 2:0 | R/W | 0 | SDP1 in data word length |
| | | | | 000 – 24-bit |
| | | | | 001 – 20-bit |
| | | | | 010 – 18-bit |
| | | | | 011 – 16-bit |
| | | | | 100 – 32-bit |

### ADDRESS 0X20, SERIAL AUDIO INTERFACE

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| sdp1_out_mute | 6 | R/W | 0 | SDP1 out mute |
| | | | | 0 – unmute |
| | | | | 1 – mute |
| sdp1_out_fmt | 5:4 | R/W | 0 | SDP1 out audio data format |
| | | | | 0 – I$^2$S |
| | | | | 1 – LJ |
| | | | | 2 – RJ |
| | | | | 3 – DSP mode |
| sdp1_out_lrp | 3 | R/W | | SDP1 out LRCK polarity |
| | | | | I$^2$S/LJ/RJ case: |
| | | | | 0 – L/R invert polarity |
| | | | | Left/Right=Low/High (LJ, RJ) |
| | | | | Left/Right=High/Low (I2S) |
| | | | | 1 – L/R normal polarity |
| | | | | Left/Right=High/Low (LJ, RJ) |
| | | | | Left/Right=Low/High (I2S) |
| | | | | DSP mode case: |
| | | | | 0 – mode A, MSB is available on 2$^{nd}$ SCLK rising edge after LRCK rising edge |
| | | | | 1 – mode B, MSB is available on 1$^{st}$ SCLK rising edge after LRCK rising edge |
| sdp1_out_wl | 2:0 | R/W | 0 | SDP1 out data word length |
| | | | | 000 – 24-bit |
| | | | | 001 – 20-bit |
| | | | | 010 – 18-bit |
| | | | | 011 – 16-bit |
| | | | | 100 – 32-bit |

### ADDRESS 0X21, SERIAL AUDIO INTERFACE

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| sdp1_in_gain | 5:4 | R/W | 0 | SDP1 in gain |
| | | | | 0 – 1x |
| | | | | 1 – 1/2 |

| | | | | 2 – 1/4 |
| | | | | 3 – 2x |
| sdp1_out_tdm | 3 | R/W | 0 | SDP1 out TDM control |
| | | | | 0 – TDM disable |
| | | | | 1 – TDM enable |
| sdp1_out_tdm_chan | 2 | R/W | 0 | SDP1 out TDM channel |
| | | | | 0 – data on slot 0 |
| | | | | 1 – data on slot 1 |
| sdp1_in_tdm | 3 | R/W | 0 | SDP1 in TDM control |
| | | | | 0 – TDM disable |
| | | | | 1 – TDM enable |
| sdp1_in_tdm_chan | 2 | R/W | 0 | SDP1 in TDM channel |
| | | | | 0 – data on slot 0 |
| | | | | 1 – data on slot 1 |

### ADDRESS 0X22, SERIAL AUDIO INTERFACE

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| sdp2_in_mute | 6 | R/W | 0 | SDP2 in mute |
| | | | | 0 – unmute |
| | | | | 1 – mute |
| sdp2_in_fmt | 5:4 | R/W | 0 | SDP2 in audio data format |
| | | | | 0 – $I^2S$ |
| | | | | 1 – LJ |
| | | | | 3 – DSP mode |
| sdp2_in_lrp | 3 | R/W | | SDP2 in LRCK polarity |
| | | | | $I^2S$/LJ case: |
| | | | | 0 – L/R invert polarity |
| | | | |     Left/Right=Low/High (LJ) |
| | | | |     Left/Right=High/Low (I2S) |
| | | | | 1 – L/R normal polarity |
| | | | |     Left/Right=High/Low (LJ) |
| | | | |     Left/Right=Low/High (I2S) |
| | | | | DSP mode case: |
| | | | | 0 – mode A, MSB is available on 2nd SCLK rising edge after LRCK rising edge |
| | | | | 1 – mode B, MSB is available on 1st SCLK rising edge after LRCK rising edge |
| sdp2_in_wl | 2:0 | R/W | 0 | SDP2 in data word length |
| | | | | 000 – 24-bit |
| | | | | 001 – 20-bit |
| | | | | 010 – 18-bit |
| | | | | 011 – 16-bit |
| | | | | 100 – 32-bit |

### ADDRESS 0X23, SERIAL AUDIO INTERFACE

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| sdp2_out_mute | 6 | R/W | 0 | SDP2 out mute |
| | | | | 0 – unmute |
| | | | | 1 – mute |
| sdp2_out_fmt | 5:4 | R/W | 0 | SDP2 out audio data format |
| | | | | 0 – $I^2S$ |

| | | | | 1 – LJ |
| --- | --- | --- | --- | --- |
| | | | | 3 – DSP mode |
| sdp2_out_lrp | 3 | R/W | | SDP2 out LRCK polarity |
| | | | | I$^2$S/LJ case: |
| | | | | 0 – L/R invert polarity |
| | | | |     Left/Right=Low/High (LJ) |
| | | | |     Left/Right=High/Low (I2S) |
| | | | | 1 – L/R normal polarity |
| | | | |     Left/Right=High/Low (LJ) |
| | | | |     Left/Right=Low/High (I2S) |
| | | | | DSP mode case: |
| | | | | 0 – mode A, MSB is available on 2$^{nd}$ SCLK rising edge after LRCK rising edge |
| | | | | 1 – mode B, MSB is available on 1$^{st}$ SCLK rising edge after LRCK rising edge |
| sdp2_out_wl | 2:0 | R/W | 0 | SDP2 out data word length |
| | | | | 000 – 24-bit |
| | | | | 001 – 20-bit |
| | | | | 010 – 18-bit |
| | | | | 011 – 16-bit |
| | | | | 100 – 32-bit |

***ADDRESS 0X24, SERIAL AUDIO INTERFACE***

| Bit Name | Bit | R/W | default | Description |
| --- | --- | --- | --- | --- |
| sdp3_in_mute | 6 | R/W | 0 | SDP3 in mute |
| | | | | 0 – unmute |
| | | | | 1 – mute |
| sdp3_in_fmt | 5:4 | R/W | 0 | SDP3 in audio data format |
| | | | | 0 – I$^2$S |
| | | | | 1 – LJ |
| | | | | 3 – DSP mode |
| sdp3_in_lrp | 3 | | | SDP3 in LRCK polarity |
| | | | | I$^2$S/LJ case: |
| | | | | 0 – L/R invert polarity |
| | | | |     Left/Right=Low/High (LJ) |
| | | | |     Left/Right=High/Low (I2S) |
| | | | | 1 – L/R normal polarity |
| | | | |     Left/Right=High/Low (LJ) |
| | | | |     Left/Right=Low/High (I2S) |
| | | | | DSP mode case: |
| | | | | 0 – mode A, MSB is available on 2$^{nd}$ SCLK rising edge after LRCK rising edge |
| | | | | 1 – mode B, MSB is available on 1$^{st}$ SCLK rising edge after LRCK rising edge |
| sdp3_in_wl | 2:0 | R/W | 0 | SDP3 in data word length |
| | | | | 000 – 24-bit |
| | | | | 001 – 20-bit |
| | | | | 010 – 18-bit |
| | | | | 011 – 16-bit |
| | | | | 100 – 32-bit |

*ADDRESS 0X25, SERIAL AUDIO INTERFACE*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| sdp3_out_mute | 6 | R/W | 0 | SDP3 out mute<br>0 – unmute<br>1 – mute |
| sdp3_out_fmt | 5:4 | R/W | 0 | SDP3 out audio data format<br>0 – I$^2$S<br>1 – LJ<br>3 – DSP mode |
| sdp3_out_lrp | 3 | R/W | | SDP3 out LRCK polarity<br>I$^2$S/LJ case:<br>0 – L/R invert polarity<br>    Left/Right=Low/High (LJ)<br>    Left/Right=High/Low (I2S)<br>1 – L/R normal polarity<br>    Left/Right=High/Low (LJ)<br>    Left/Right=Low/High (I2S)<br>DSP mode case:<br>0 – mode A, MSB is available on 2$^{nd}$ SCLK rising edge after LRCK rising edge<br>1 – mode B, MSB is available on 1$^{st}$ SCLK rising edge after LRCK rising edge |
| sdp3_out_wl | 2:0 | R/W | 0 | SDP3 out data word length<br>000 – 24-bit<br>001 – 20-bit<br>010 – 18-bit<br>011 – 16-bit<br>100 – 32-bit |

*ADDRESS 0X26, SPKMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LD2LSPKMX | 7 | R/W | 0 | Left DAC to left SPK mixer<br>0 – disable<br>1 – enable |
| LLN2LSPKMX | 6 | R/W | 0 | LLN to left SPK mixer<br>0 – disable<br>1 – enable |
| LAX2LSPKMX | 5 | R/W | 0 | Left AX to left SPK mixer<br>0 – disable<br>1 – enable |
| LSPKMX_MUTE | 4 | R/W | 1 | Left SPK mixer mute<br>0 – unmute<br>1 – mute (-30dB) |
| RD2RSPKMX | 3 | R/W | 0 | Right DAC to right SPK mixer<br>0 – disable<br>1 – enable |
| RLN2RSPKMX | 2 | R/W | 0 | RLN to right SPK mixer<br>0 – disable<br>1 – enable |
| RAX2RSPKMX | 1 | R/W | 0 | Right AX to right SPK mixer<br>0 – disable |

| | | | | |
|---|---|---|---|---|
| | | | | 1 – enable |
| RSPKMX_MUTE | 0 | R/W | 1 | Right SPK mixer mute<br>0 – unmute<br>1 – mute (-30dB) |

### *ADDRESS 0X27, SPKMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LSPKMX_HI | 7 | R/W | 0 | Left SPK mixer gain HI |
| LSPKMX_LO0 | 6 | R/W | 0 | Left SPK mixer gain LO0 |
| LSPKMX_LO1 | 5 | R/W | 0 | Left SPK mixer gain LO1 |
| LSPKMX_LO2 | 4 | R/W | 0 | Left SPK mixer gain LO2 |
| RSPKMX_HI | 3 | R/W | 0 | Right SPK mixer gain HI |
| RSPKMX_LO0 | 2 | R/W | 0 | Right SPK mixer gain LO0 |
| RSPKMX_LO1 | 1 | R/W | 0 | Right SPK mixer gain LO1 |
| RSPKMX_LO2 | 0 | R/W | 0 | Right SPK mixer gain LO2 |

### *ADDRESS 0X28, SPKMIX*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| LSPKMXVol | 7:4 | R/W | 0 | Left SPK mixer volume | |
| | | | | 0000 – -12dB<br>0001 – -10.5dB<br>0010 – -9dB<br>0011 – -7.5dB<br>0100 – -6dB | 1000 – -4.5dB<br>1001 – -3dB<br>1010 – -1.5dB<br>1011 – 0dB |
| RSPKMXVol | 3:0 | R/W | 0 | Right SPK mixer volume | |
| | | | | 0000 – -12dB<br>0001 – -10.5dB<br>0010 – -9dB<br>0011 – -7.5dB<br>0100 – -6dB | 1000 – -4.5dB<br>1001 – -3dB<br>1010 – -1.5dB<br>1011 – 0dB |

### *ADDRESS 0X29, SPKMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| SPKmix_ref2 | 2 | R/W | 1 | SPK mixer ref2 |
| SPKmix_ref1 | 1 | R/W | 0 | SPK mixer ref1 |
| LPSPKMX | 0 | R/W | 0 | SPK mixer low power mode<br>0 – normal<br>1 – low power |

### *ADDRESS 0X2A, HPMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LD2LHPMIX | 7 | R/W | 0 | LDAC to LHP mixer selection<br>0 – disable<br>1 – enable |
| LLN2LHPMIX | 6 | R/W | 0 | Left LINE to LHP mixer selection<br>0 – disable<br>1 – enable |
| LAX2LHPMIX | 5 | R/W | 0 | Left AX to LHP mixer selection<br>0 – disable |

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| | | | | 1 – enable |
| RD2RHPMIX | 3 | R/W | 0 | RDAC to RHP mixer selection<br>0 – disable<br>1 – enable |
| RLN2RHPMIX | 2 | R/W | 0 | Right LINE to RHP mixer selection<br>0 – disable<br>1 – enable |
| RAX2RHPMIX | 1 | R/W | 0 | Right AX to RHP mixer selection<br>0 – disable<br>1 – enable |

### ADDRESS 0X2B, HPMIX

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LHPMIX_HI | 7 | R/W | 0 | LHP mixer gain HI |
| LHPMIX_LO | 6 | R/W | 0 | LHP mixer gain LO |
| LHPMIX_MUTE | 5 | R/W | 1 | LHP mixer gain MUTE |
| pdnLHPMix | 4 | R/W | 1 | Power down LHP mixer |
| RHPMIX_HI | 3 | R/W | 0 | RHP mixer gain HI |
| RHPMIX_LO | 2 | R/W | 0 | RHP mixer gain LO |
| RHPMIX_MUTE | 1 | R/W | 1 | RHP mixer gain MUTE |
| pdnRHPMix | 0 | R/W | 1 | Power down RHP mixer |

### ADDRESS 0X2C, HPMIX

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| LHPMIXVol | 7:4 | R/W | 0 | LHP mixer volume | |
| | | | | 0000 – -12dB<br>0001 – -10.5dB<br>0010 – -9dB<br>0011 – -7.5dB<br>0100 – -6dB | 1000 – -4.5dB<br>1001 – -3dB<br>1010 – -1.5dB<br>1011 – 0dB |
| RHPMIXVol | 3:0 | R/W | 0 | RHP mixer volume | |
| | | | | 0000 – -12dB<br>0001 – -10.5dB<br>0010 – -9dB<br>0011 – -7.5dB<br>0100 – -6dB | 1000 – -4.5dB<br>1001 – -3dB<br>1010 – -1.5dB<br>1011 – 0dB |

### ADDRESS 0X2D, HPMIX

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| HPmix_ref2 | 2 | R/W | 1 | HP mixer ref2 |
| HPmix_ref1 | 1 | R/W | 0 | HP mixer ref1 |
| LPHPMix | 0 | R/W | 0 | HP mixer low power mode<br>0 – normal<br>1 – low power |

### ADDRESS 0X2E, AXMIX

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LAX2LMIXAX | 7 | R/W | 0 | Left AX to LAX mixer selection<br>0 – disable |

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| | | | | 1 – enable |
| LVXP2LMIXAX | 6 | R/W | 0 | Left VXP to LAX mixer selection<br>0 – disable<br>1 – enable |
| LMIC2P2LMIXAX | 5 | R/W | 0 | LMIC2P to LAX mixer selection<br>0 – disable<br>1 – enable |
| LMICPDFSE2LAX | 4 | R/W | 0 | LMICPDFSE to LAX mixer selection<br>0 – disable<br>1 – enable |
| RAX2RMIXAX | 3 | R/W | 0 | Right AX to RAX mixer selection<br>0 – disable<br>1 – enable |
| RVXN2RMIXAX | 2 | R/W | 0 | Right VXN to RAX mixer selection<br>0 – disable<br>1 – enable |
| RMIC2N2RMIXAX | 1 | R/W | 0 | RMIC2N to RAX mixer selection<br>0 – disable<br>1 – enable |
| RMICNDFSE2RAX | 0 | R/W | 0 | RMICNDFSE to RAX mixer selection<br>0 – disable<br>1 – enable |

### *ADDRESS 0X2F, AXMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LAXMIX_HI | 7 | R/W | 0 | LAX mixer gain HI |
| LAXMIX_BOOST | 5 | R/W | 0 | LAX mixer gain BOOST |
| pdnLAXMIX | 4 | R/W | 1 | Power down LAX mixer |
| RAXMIX_HI | 3 | R/W | 0 | RAX mixer gain HI |
| RAXMIX_BOOST | 1 | R/W | 0 | RAX mixer gain BOOST |
| pdnRAXMIX | 0 | R/W | 1 | Power down RAX mixer |

### *ADDRESS 0X30, AXMIX*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| LAXMIXVol | 7:4 | R/W | 0 | LAX mixer volume | |
| | | | | 0000 – -12dB<br>0001 – -10.5dB<br>0010 – -9dB<br>0011 – -7.5dB<br>0100 – -6dB | 1000 – -4.5dB<br>1001 – -3dB<br>1010 – -1.5dB<br>1011 – 0dB |
| RAXMIXVol | 3:0 | R/W | 0 | RAX mixer volume | |
| | | | | 0000 – -12dB<br>0001 – -10.5dB<br>0010 – -9dB<br>0011 – -7.5dB<br>0100 – -6dB | 1000 – -4.5dB<br>1001 – -3dB<br>1010 – -1.5dB<br>1011 – 0dB |

### *ADDRESS 0X31, AXMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| AXMIX_ref2 | 2 | R/W | 1 | AX mixer ref2 |

| AXMIX_ref1 | 1 | R/W | 0 | AX mixer ref1 |
| LPAXMix | 0 | R/W | 0 | AX mixer low power mode<br>0 – normal<br>1 – low power |

### *ADDRESS 0X32, LNMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LAIX2LMIXLN | 7 | R/W | 0 | Left AX to left LINE mixer selection<br>0 – disable<br>1 – enable |
| LLN2LMIXLN | 6 | R/W | 0 | Left LINE to left LINE mixer selection<br>0 – disable<br>1 – enable |
| LMIC1P2LMIXLN | 5 | R/W | 0 | LMIC1P to left LINE mixer selection<br>0 – disable<br>1 – enable |
| LMICPDFSE2LLN | 4 | R/W | 0 | LMICPDFSE to left LINE mixer selection<br>0 – disable<br>1 – enable |
| RAIX2RMIXLN | 3 | R/W | 0 | Right AX to right LINE mixer selection<br>0 – disable<br>1 – enable |
| RLN2RMIXLN | 2 | R/W | 0 | Right LINE to right LINE mixer selection<br>0 – disable<br>1 – enable |
| RMIC1N2RMIXLN | 1 | R/W | 0 | RMIC1N to right LINE mixer selection<br>0 – disable<br>1 – enable |
| RMICNDFSE2RLN | 0 | R/W | 0 | RMICNDFSE to right LINE mixer selection<br>0 – disable<br>1 – enable |

### *ADDRESS 0X33, LNMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LLNMIX_HI | 7 | R/W | 0 | Left LINE mixer gain HI |
| LLNMIX_BOOST | 5 | R/W | 0 | Left LINE mixer gain BOOST |
| pdnLLNMIX | 4 | R/W | 1 | Power down Left LINE mixer |
| RLNMIX_HI | 3 | R/W | 0 | Right LINE mixer gain HI |
| RLNMIX_BOOST | 1 | R/W | 0 | Right LINE mixer gain BOOST |
| pdnRLNMIX | 0 | R/W | 1 | Power down Right LINE mixer |

### *ADDRESS 0X34, LNMIX*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| LLNMIXVol | 7:4 | R/W | 0 | Left LINE mixer volume | |
| | | | | 0000 – -12dB<br>0001 – -10.5dB<br>0010 – -9dB<br>0011 – -7.5dB<br>0100 – -6dB | 1000 – -4.5dB<br>1001 – -3dB<br>1010 – -1.5dB<br>1011 – 0dB |

| RLNMIXVol | 3:0 | R/W | 0 | Right LINE mixer volume | |
|---|---|---|---|---|---|
| | | | | 0000 – -12dB | 1000 – -4.5dB |
| | | | | 0001 – -10.5dB | 1001 – -3dB |
| | | | | 0010 – -9dB | 1010 – -1.5dB |
| | | | | 0011 – -7.5dB | 1011 – 0dB |
| | | | | 0100 – -6dB | |

### *ADDRESS 0X35, LNMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LNMIX_ref2 | 2 | R/W | 1 | LINE mixer ref2 |
| LNMIX_ref1 | 1 | R/W | 0 | LINE mixer ref1 |
| LPLNMix | 0 | R/W | 0 | LINE mixer low power mode<br>0 – normal<br>1 – low power |

### *ADDRESS 0X36, MNMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LDAC2LMIXMN | 7 | R/W | 0 | Left DAC to left mono mixer selection<br>0 – disable<br>1 – enable |
| LVXP2LMIXMN | 6 | R/W | 0 | Left VXP to left mono mixer selection<br>0 – disable<br>1 – enable |
| LAIX2LMIXMN | 5 | R/W | 0 | Left AX to left mono mixer selection<br>0 – disable<br>1 – enable |
| RDAC2RMIXMN | 3 | R/W | 0 | Right DAC to right mono mixer selection<br>0 – disable<br>1 – enable |
| RVXN2RMIXMN | 2 | R/W | 0 | Right VXN to right mono mixer selection<br>0 – disable<br>1 – enable |
| RMIC1N2RMIXMN | 1 | R/W | 0 | RMIC1N to right mono mixer selection<br>0 – disable<br>1 – enable |

### *ADDRESS 0X37, MNMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LMNMIX_HI | 7 | R/W | 0 | Left mono mixer gain HI |
| LMNMIX_BOOST | 5 | R/W | 0 | Left mono mixer gain BOOST |
| pdnLMNMIX | 4 | R/W | 1 | Power down Left mono mixer |
| RMNMIX_HI | 3 | R/W | 0 | Right mono mixer gain HI |
| RMNMIX_BOOST | 1 | R/W | 0 | Right mono mixer gain BOOST |
| pdnRMNMIX | 0 | R/W | 1 | Power down Right mono mixer |

### *ADDRESS 0X38, MNMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LMNMIXVol | 7:4 | R/W | 0 | Left mono mixer volume |

| | | | | 0000 – -12dB | 1000 – -4.5dB |
|---|---|---|---|---|---|
| | | | | 0001 – -10.5dB | 1001 – -3dB |
| | | | | 0010 – -9dB | 1010 – -1.5dB |
| | | | | 0011 – -7.5dB | 1011 – 0dB |
| | | | | 0100 – -6dB | |
| RMNMIXVol | 3:0 | R/W | 0 | Right mono mixer volume | |
| | | | | 0000 – -12dB | 1000 – -4.5dB |
| | | | | 0001 – -10.5dB | 1001 – -3dB |
| | | | | 0010 – -9dB | 1010 – -1.5dB |
| | | | | 0011 – -7.5dB | 1011 – 0dB |
| | | | | 0100 – -6dB | |

### *ADDRESS 0X39, MNMIX*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| MNMIX_ref2 | 2 | R/W | 1 | Mono mixer ref2 |
| MNMIX_ref1 | 1 | R/W | 0 | Mono mixer ref1 |
| LPMNMix | 0 | R/W | 0 | Mono mixer low power mode<br>0 – normal<br>1 – low power |

### *ADDRESS 0X3A, SPKD*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| EN_SPKLSCP | 7 | R/W | 0 | |
| PDN_SPKLBiasgen | 6 | R/W | 1 | |
| LM2SPKLOUT | 5 | R/W | 0 | |
| RM2SPKLOUT | 4 | R/W | 0 | |
| EN_SPKRSCP | 3 | R/W | 0 | |
| PDN_SPKRBiasgen | 2 | R/W | 1 | |
| LM2SPKROUT | 1 | R/W | 0 | |
| RM2SPKROUT | 0 | R/W | 0 | |

### *ADDRESS 0X3B, SPKD*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| EN_SPKL | 7 | R/W | 0 | | |
| SPKLVol | 6:4 | R/W | 0 | SPKL volume | |
| | | | | 000 – | 100 – |
| | | | | 001 – | 101 – |
| | | | | 010 – | 110 – |
| | | | | 011 – | 111 – |
| EN_SPKR | 3 | R/W | 0 | | |
| SPKRVol | 2:0 | R/W | 0 | SPKR volume | |
| | | | | 000 – | 100 – |
| | | | | 001 – | 101 – |
| | | | | 010 – | 110 – |
| | | | | 011 – | 111 – |

### *ADDRESS 0X3C, SPKD*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| EN_OTP | 7 | R/W | 0 | |

| SPK_MONOOUT | 6 | R/W | 0 | | |
|---|---|---|---|---|---|
| pdn_SPKLDO | 5 | R/W | 1 | | |
| BPCap_SPKLDOB | 4 | R/W | 0 | | |
| SPK_LDOLVL | 2:0 | R/W | 0 | SPK LDO level | |
| | | | | 000 –<br>001 –<br>010 –<br>011 – | 100 –<br>101 –<br>110 –<br>111 – |

### ADDRESS 0X3D, SPKD

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| SPK_TRI_TSEL0 | 7 | R/W | 0 | |
| SPK_TRI_TSEL1 | 6 | R/W | 0 | |
| SPK_TRI_TSEL2 | 5 | R/W | 0 | |
| SPK_TRI_TSEL3 | 4 | R/W | 0 | |
| SPKL_DT | 3 | R/W | 0 | |
| SPKR_DT | 2 | R/W | 0 | |
| SPKL_ILOSEL | 1 | R/W | 0 | |
| SPKR_ILOSEL | 0 | R/W | 0 | |

### ADDRESS 0X3E, CPHP

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| HPL_iCal | 7:0 | R/W | 0 | HPL ical value; the result of reading this register is the actual ical when auto ical enable. |

### ADDRESS 0X3F, CPHP

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| HPR_iCal | 7:0 | R/W | 0 | HPR ical value; the result of reading this register is the actual ical when auto ical enable. |

### ADDRESS 0X40, CPHP

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| EnHPL | 6 | R/W | 0 | HPL enable<br>0 – disable<br>1 – enable |
| HPL_outen | 5 | R/W | 0 | HPLout output enable<br>0 – disable<br>1 – enable |
| HPLcal | 4 | R/W | 0 | HPL calibration<br>0 – off<br>1 – on |
| EnRefr_HP | 3 | R/W | 0 | HP Refr enable<br>0 – disable<br>1 – enable |
| EnHPR | 2 | R/W | 0 | HPR enable<br>0 – disable<br>1 – enable |
| HPR_outen | 1 | R/W | 0 | HPRout output enable<br>0 – disable |

| | | | | 1 – enable |
|---|---|---|---|---|
| HPRcal | 0 | R/W | 0 | HPR calibration<br>0 – off<br>1 – on R calibra |

### ADDRESS 0X41, CPHP

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pdn_Lical | 7 | R/W | 1 | Power down Lical<br>0 – power on<br>1 – power down |
| HPL_iCal_sw | 6 | R/W | 0 | |
| HPLVol | 5:4 | R/W | 0 | HPL Volume<br>0 – 0dB<br>1 – -12dB<br>2 – -24dB<br>3 – -48dB |
| pdn_Rical | 3 | R/W | 1 | power down Rical<br>0 – power on<br>1 – power down |
| HPL_iCal_sw | 2 | R/W | 0 | |
| HPRVol | 1:0 | R/W | 0 | HPR Volume<br>0 – 0dB<br>1 – -12dB<br>2 – -24dB<br>3 – -48dB |

### ADDRESS 0X42, CPHP

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| HPL_zcen | 7 | R/W | 0 | HPL zero cross enable |
| HPR_zcen | 6 | R/W | 0 | HPR zero cross enable |
| pdn_CPHP | 5 | R/W | 1 | Power down CPHP<br>0 – power on<br>1 – power down |
| VROI_HP | 3 | R/W | 0 | |
| LPHP | 2 | R/W | 0 | HP low power mode<br>0 – normal<br>1 – low power mode |
| hp_ref2 | 1 | R/W | 0 | HP ref2 |
| hp_ref1 | 1 | R/W | 0 | HP ref1 |

### ADDRESS 0X43, CPHP

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pdn_cp | 7 | R/W | 1 | Power down charge pump<br>0 – power on<br>1 – power down |
| cp_HIPWR | 6 | R/W | 0 | Charge pump high power mode<br>0 – normal<br>1 – high power mode |
| LPCPNLDO | 4 | R/W | 0 | |
| cpn_swcomp_en | 3 | R/W | 0 | |

| cp_swdly_auto | 2 | R/W | 0 | |
|---|---|---|---|---|
| cp_swdly_reg | 1 | R/W | 1 | |
| cp_clkdly_en | 1 | R/W | 0 | |

### ADDRESS 0X44, CPHP

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| vhp_ldolvl | 7:6 | R/W | 0 | |
| cpn_ldolvl | 5:4 | R/W | 0 | |
| cpn_swlvl | 3:2 | R/W | 0 | |
| pdn_CPNLDO | 1 | R/W | 1 | |
| pdn_cpvncomp | 0 | R/W | 1 | |

### ADDRESS 0X45, MONOHP

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| EnRefr_mono | 7 | R/W | 1 | Mono EnRefr enable<br>0 – disable<br>1 – enable |
| VROI_mono | 6 | R/W | 0 | |
| pdnVrefBuf_mono | 5 | R/W | 1 | |
| Mono_ref2 | 3 | R/W | 0 | Mono out ref2 |
| Mono_ref1 | 2 | R/W | 0 | Mono out ref1 |
| LPvrefBuf_mono | 1 | R/W | 0 | Mono vrefbuf low power mode<br>0 – normal<br>1 – low power mode |
| LPMono | 0 | R/W | 0 | Mono out low power mode<br>0 – normal<br>1 – low power mode |

### ADDRESS 0X46, MONOHP

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LMIXMN2MonoN | 7 | R/W | 0 | Left mono mixer to MonoN out selection<br>0 – disable<br>1 – enable |
| RMIXHP2MonoN | 6 | R/W | 0 | Right HP mixer to MonoN out selection<br>0 – disable<br>1 – enable |
| RINV2MonoN | 5 | R/W | 0 | Right mono out inversion to MonoN out selection<br>0 – disable<br>1 – enable |
| LMIXLN2MonoN | 4 | R/W | 0 | Left LINE mixer to MonoN out selection<br>0 – disable<br>1 – enable |
| LMIXAX2MonoN | 3 | R/W | 0 | Left AX mixer to MonoN out selection<br>0 – disable<br>1 – enable |

### ADDRESS 0X47, MONOHP

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LMIXHP2MonoP | 7 | R/W | 0 | Left HP mixer to MonoP out selection |

| | | | | 0 – disable |
|---|---|---|---|---|
| | | | | 1 – enable |
| RMIXHP2MonoP | 6 | R/W | 0 | Right HP mixer to MonoP out selection |
| | | | | 0 – disable |
| | | | | 1 – enable |
| RMIXMN2MonoP | 5 | R/W | 0 | Right mono mixer to MonoP out selection |
| | | | | 0 – disable |
| | | | | 1 – enable |
| RMIXAX2MonoP | 4 | R/W | 0 | Right AX mixer to MonoP out selection |
| | | | | 0 – disable |
| | | | | 1 – enable |
| LMIXLN2MonoP | 3 | R/W | 0 | Right LINE mixer to MonoP out selection |
| | | | | 0 – disable |
| | | | | 1 – enable |

### *ADDRESS 0X48, MONOHP*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| EnMonoP | 7 | R/W | 0 | |
| MonoPCAL | 6 | R/W | 0 | MonoP calibration enable |
| | | | | 0 – calibration off |
| | | | | 1 – calibration on |
| MonoP_gainN1 | 5 | R/W | 0 | |
| MonoP_HI | 4 | R/W | 0 | |
| MonoP_LO | 3 | R/W | 0 | |
| MonoP_attn | 2 | R/W | 0 | |
| MonoP_boost | 1 | R/W | 0 | |
| MonoP_MUTE | 0 | R/W | 1 | MonoP mute |
| | | | | 0 – unmute |
| | | | | 1 – mute |

### *ADDRESS 0X49, MONOHP*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| EnMonoN | 7 | R/W | 0 | |
| MonoNCAL | 6 | R/W | 0 | MonoN calibration enable |
| | | | | 0 – calibration off |
| | | | | 1 – calibration on |
| MonoN_gainN1 | 5 | R/W | 0 | |
| MonoN_HI | 4 | R/W | 0 | |
| MonoN_LO | 3 | R/W | 0 | |
| MonoN_attn | 2 | R/W | 0 | |
| MonoN_boost | 1 | R/W | 0 | |
| MonoN_MUTE | 0 | R/W | 1 | MonoN mute |
| | | | | 0 – unmute |
| | | | | 1 – mute |

### *ADDRESS 0X4A, LNOUT*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| EnRefr_LN1 | 7 | R/W | 1 | LN1 EnRefr |
| | | | | 0 – enable |
| | | | | 1 – disable |

| EnLout1 | 6 | R/W | 0 | Lout1 enable<br>0 – disable<br>1 – enable |
| LDAC2LOUT1 | 5 | R/W | 0 | LDAC to Lout1 selection<br>0 – disable<br>1 – enable |
| LMIXAX2LOUT1 | 4 | R/W | 0 | |
| LMIXLN2LOUT1 | 3 | R/W | 0 | |
| LMIXMN2LOUT1 | 2 | R/W | 0 | |
| LS2LOUT1 | 1 | R/W | 0 | |
| L1CAL | 0 | R/W | 0 | L1 calibration enable<br>0 – calibration off<br>1 – calibration on |

### *ADDRESS 0X4B, LNOUT*

| Bit Name | Bit | R/W | default | Description |
| --- | --- | --- | --- | --- |
| EnRefr_RN1 | 7 | R/W | 1 | RN1 EnRefr<br>0 – enable<br>1 – disable |
| EnRout1 | 6 | R/W | 0 | Rout1 enable<br>0 – disable<br>1 – enable |
| RDAC2ROUT1 | 5 | R/W | 0 | RDAC to Rout1 selection<br>0 – disable<br>1 – enable |
| RMIXAX2ROUT1 | 4 | R/W | 0 | |
| RMIXLN2ROUT1 | 3 | R/W | 0 | |
| RMIXMN2ROUT1 | 2 | R/W | 0 | |
| RS2ROUT1 | 1 | R/W | 0 | |
| R1CAL | 0 | R/W | 0 | R1 calibration enable<br>0 – calibration off<br>1 – calibration on |

### *ADDRESS 0X4C, LNOUT*

| Bit Name | Bit | R/W | default | Description |
| --- | --- | --- | --- | --- |
| EnRefr_LN2 | 7 | R/W | 1 | LN2 EnRefr<br>0 – enable<br>1 – disable |
| EnLout2 | 6 | R/W | 0 | Lout2 enable<br>0 – disable<br>1 – enable |
| LDAC2LOUT2 | 5 | R/W | 0 | LDAC to Lout2 selection<br>0 – disable<br>1 – enable |
| LMIXAX2LOUT2 | 4 | R/W | 0 | |
| LMIXLN2LOUT2 | 3 | R/W | 0 | |
| LMIXMN2LOUT2 | 2 | R/W | 0 | |
| LS2LOUT2 | 1 | R/W | 0 | |
| L2CAL | 0 | R/W | 0 | L2 calibration enable<br>0 – calibration off |

| | | | | 1 – calibration on |
|---|---|---|---|---|

### *ADDRESS 0X4D, LNOUT*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| EnRefr_RN2 | 7 | R/W | 1 | RN2 EnRefr<br>0 – enable<br>1 – disable |
| EnRout2 | 6 | R/W | 0 | Rout2 enable<br>0 – disable<br>1 – enable |
| RDAC2ROUT2 | 5 | R/W | 0 | RDAC to Rout2 selection<br>0 – disable<br>1 – enable |
| RMIXAX2ROUT2 | 4 | R/W | 0 | |
| RMIXLN2ROUT2 | 3 | R/W | 0 | |
| RMIXMN2ROUT2 | 2 | R/W | 0 | |
| RS2ROUT2 | 1 | R/W | 0 | |
| R2CAL | 0 | R/W | 0 | R2 calibration enable<br>0 – calibration off<br>1 – calibration on |

### *ADDRESS 0X4E, LNOUT*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| Lout1_gainN1 | 7 | R/W | 1 | |
| Lout1_HI | 6 | R/W | 0 | |
| Lout1_LO | 5 | R/W | 0 | |
| Lout1_boost | 4 | R/W | 0 | |
| Lout1_attn | 3 | R/W | 0 | |
| Lout1_MUTE | 2 | R/W | 1 | Lout1 mute enable<br>0 – unmute<br>1 – mute |
| LPLout1 | 0 | R/W | 0 | Lout1 low power<br>0 – normal mode<br>1 – low power mode |

### *ADDRESS 0X4F, LNOUT*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| Rout1_gainN1 | 7 | R/W | 1 | |
| Rout1_HI | 6 | R/W | 0 | |
| Rout1_LO | 5 | R/W | 0 | |
| Rout1_boost | 4 | R/W | 0 | |
| Rout1_attn | 3 | R/W | 0 | |
| Rout1_MUTE | 2 | R/W | 1 | Rout1 mute enable<br>0 – unmute<br>1 – mute |
| line1_ref2 | 0 | R/W | 0 | line1 ref2 |
| line1_ref1 | 0 | R/W | 0 | line1 ref1 |

### ADDRESS 0X50, LNOUT

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| Lout2_gainN1 | 7 | R/W | 1 | |
| Lout2_HI | 6 | R/W | 0 | |
| Lout2_LO | 5 | R/W | 0 | |
| Lout2_boost | 4 | R/W | 0 | |
| Lout2_attn | 3 | R/W | 0 | |
| Lout2_MUTE | 2 | R/W | 1 | Lout2 mute enable<br>0 – unmute<br>1 – mute |
| LPLout2 | 0 | R/W | 0 | Lout2 low power<br>0 – normal mode<br>1 – low power mode |

### ADDRESS 0X51, LNOUT

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| Rout2_gainN1 | 7 | R/W | 1 | |
| Rout2_HI | 6 | R/W | 0 | |
| Rout2_LO | 5 | R/W | 0 | |
| Rout2_boost | 4 | R/W | 0 | |
| Rout2_attn | 3 | R/W | 0 | |
| Rout2_MUTE | 2 | R/W | 1 | Rout2 mute enable<br>0 – unmute<br>1 – mute |
| line2_ref2 | 0 | R/W | 0 | line2 ref2 |
| line2_ref1 | 0 | R/W | 0 | line2 ref1 |

### ADDRESS 0X52, LNOUT

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| EnRefr_LN | 7 | R/W | 1 | LINE Enrefr<br>0 – disable<br>1 – enable |
| pdn_vrefBuf_LN | 6 | R/W | 1 | |
| VROI_LN | 5 | R/W | 0 | |
| LPvrefrBuf_LN | 4 | R/W | 0 | |

### ADDRESS 0X53, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pdn_adc_csm | 7 | R/W | 1 | ADC FSM power down control<br>0 – ADC FSM on<br>1 – ADC FSM power down |
| pdn_adc_dig | 6 | R/W | 0 | ADC digital power down<br>0 – ADC digital on<br>1 – Reset ADC digital blocks |
| adc_mute | 5 | R/W | 0 | mute ADC digital output<br>0 – normal<br>1 – mute |
| adc_fsmode | 2 | R/W | 0 | ADC Fs mode<br>0 – single speed mode |

| | | | | 1 – double speed mode |
|---|---|---|---|---|
| adc_osr | 1:0 | R/W | 0 | ADC OSR mode<br>0 – ADC at 64FS mode<br>1 – ADC at 50FS mode<br>2 – ADC at 68FS mode |

### ADDRESS 0X54, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| dmic_l_src | 7:6 | R/W | 0 | Left digital microphone source<br>0 – disable left digital microphone<br>1 – from DMIC_SDA1 when DMIC_SCL high<br>2 – from DMIC_SDA2 when DMIC_SCL high<br>3 – from DMIC_SDA1 when DMIC_SCL low |
| dmic_r_src | 5:4 | R/W | 0 | Right digital microphone source<br>0 – disable right digital Microphone<br>1 – from DMIC_SDA1 when DMIC_SCL low<br>2 – from DMIC_SDA2 when DMIC_SCL low<br>3 – from DMIC_SDA2 when DMIC_SCL high |
| adc_aeb | 3 | R/W | 0 | ADC volume control mode<br>0 – normal<br>1 – both channel volume is set by left volume control register |
| adc_ramp | 2:0 | R/W | 0 | ADC ramp control<br>0xx – ramp disable<br>100 – 0.5 dB per 4LRCK ramp<br>101 – 0.5 dB per 8LRCK ramp<br>110 – 0.5 dB per 16LRCK ramp<br>111 – 0.5 dB per 32LRCK ramp |

### ADDRESS 0X55, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| adc_invl | 7 | R/W | 0 | ADC left channel polarity inverted<br>0 – normal<br>1 – inverted |
| adc_invr | 6 | R/W | 0 | ADC right channel polarity inverted<br>0 – normal<br>1 – inverted |
| adc_hpf_l | 5 | R/W | 0 | ADC left channel high pass filter enable<br>0 – high pass filter disable<br>1 – high pass filter enable |
| adc_hpf_r | 4 | R/W | 0 | ADC right channel high pass filter enable<br>0 – high pass filter disable<br>1 – high pass filter enable |
| adc_comp | 3 | R/W | 0 | ADC data companding control<br>0 – disable<br>1 – enable |
| adc_compmode | 2 | R/W | 0 | ADC data companding type<br>0 – u-law<br>1 – A-law |
| adc_datsel | 1:0 | R/W | 0 | ADC data mixer<br>00 – left data=left ADC, right data=right ADC<br>01 – left data=left ADC, right data=left ADC |

| | | | | 10 – left data=right ADC, right data=right ADC |
| | | | | 11 – left data=right ADC, right data=left ADC |

### ADDRESS 0X56, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| adc_volumel | 7:0 | R/W | C0 | ADC left channel volume<br>00000000 – 0 dB<br>00000001 – -0.5 dB<br>00000010 – -1 dB<br>…<br>11000000 – -96 dB |

### ADDRESS 0X57, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| adc_volumer | 7:0 | R/W | C0 | ADC right channel volume<br>00000000 – 0 dB<br>00000001 – -0.5 dB<br>00000010 – -1 dB<br>…<br>11000000 – -96 dB |

### ADDRESS 0X58, ADC

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| alc_sel | 7:6 | R/W | 0 | ALC function select<br>00 – ALC off<br>01 – right channel ALC only<br>10 – left channel ALC only<br>11 – stereo ALC<br>Note: ensure that left and right channel PGA setting are the same before entering this mode | |
| alc_zc | 5 | R/W | 0 | ALC uses zero cross detection circuit<br>0 – disable<br>1 – enable | |
| alc_mode | 4 | R/W | 0 | Determines the ALC mode of operation<br>0 – ALC mode<br>1 – limiter mode | |
| alc_lvl | 3:0 | R/W | 1011 | ALC target level | |
| | | | | 0000 – -16.5 dB<br>0001 – -15 dB<br>0010 – -13.5 dB<br>…… | 0111 – -6 dB<br>1000 – -4.5 dB<br>1001 – -3 dB<br>1010-1111 – 1.5 dB (1011 default) |

### ADDRESS 0X59, ADC

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| alc_dcy | 7:4 | R/W | 0011 | ALC decay (gain ramp up) time, ALC mode: | |
| | | | | 0000 – 410 us<br>0001 – 820 us<br>0010 – 1.64 ms | …… (time doubles with every step)<br>1001 – 210 ms<br>1010 or higher – 420 ms |
| alc_atk | 3:0 | R/W | 0010 | ALC attack (gain ramp down) time, ALC mode/limiter mode: | |

| | | | | 0000 – 104 us/22.7 us | …… (time doubles with very step) |
| | | | | 0001 – 208 us/45.4 us | 1001 – 53.2 ms/11.6 ms |
| | | | | 0010 – 416 us/90.8 us | 1010 or higher – 106 ms/23.2 ms |

### ADDRESS 0X5A, ADC

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| alc_timout | 4 | R/W | 0 | Zero Cross time out<br>0 – disable<br>1 – enable | |
| alc_hld | 3:0 | R/W | 0 | ALC hold time before gain is increased | |
| | | | | 0000 – 0 ms | …… (time doubles with every step) |
| | | | | 0001 – 2.67 ms | 1001 – 0.68 s |
| | | | | 0010 – 5.33 ms | 1010 or higher – 1.36 s |

### ADDRESS 0X5B, ADC

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| alc_winsize[4:3] | 6:5 | R/W | 00 | Windows size for peak detector，set the window size to N*16 samples<br>00110 – 96 samples (default)<br>00111 – 102 samples<br>…..<br>11111 – 496 samples | |
| alc_maxgain | 4:0 | R/W | 11111 | Set maximum gain of PGA | |
| | | | | 00000 – -6.5 dB | 01111 – +16 dB |
| | | | | 00001 – -5 dB | 10000 – +17.5 dB |
| | | | | 00010 – -3.5 dB | 10001 – +19 dB |
| | | | | 00011 – -2 dB | 10010 – +20.5 dB |
| | | | | 00100 – -0.5 dB | 10011 – +22 dB |
| | | | | 00101 – +1 dB | 10100 – +23.5 dB |
| | | | | 00110 – +2.5 dB | 10101 – +25 dB |
| | | | | 00111 – +4 dB | 10110 – +26.5 dB |
| | | | | 01000 – +5.5 dB | 10111 – +28 dB |
| | | | | 01001 – +7 dB | 11000 – +29.5 dB |
| | | | | 01010 – +8.5 dB | 11001 – +31 dB |
| | | | | 01011 – +10 dB | 11010 – +32.5 dB |
| | | | | 01100 – +11.5 dB | 11011 – +34 dB |
| | | | | 01101 – +13 dB | others – +35.5 dB |
| | | | | 01110 – +14.5 dB | |

### ADDRESS 0X5C, ADC

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| alc_winsize[2:0] | 7:5 | R/W | 110 | Windows size for peak detector，set the window size to N*16 samples<br>00110 – 96 samples (default)<br>00111 – 102 samples<br>…..<br>11111 – 496 samples | |
| alc_mingain[4:0] | 4:0 | R/W | 00000 | Set minimum gain of PGA | |
| | | | | 00000 – -12 dB | 01111 – +10.5 dB |
| | | | | 00001 – -10.5 dB | 10000 – +12 dB |

| | | | 00010 – -9 dB | 10001 – +13.5 dB |
|---|---|---|---|---|
| | | | 00011 – -7.5 dB | 10010 – +15 dB |
| | | | 00100 – -6 dB | 10011 – +16.5 dB |
| | | | 00101 – -4.5 dB | 10100 – +18 dB |
| | | | 00110 – -3 dB | 10101 – +19.5 dB |
| | | | 00111 – -1.5 dB | 10110 – +21 dB |
| | | | 01000 – 0 dB | 10111 – +22.5 dB |
| | | | 01001 – +1.5 dB | 11000 – +24 dB |
| | | | 01010 – +3 dB | 11001 – +25.5 dB |
| | | | 01011 – +4.5 dB | 11010 – +27 dB |
| | | | 01100 – +6 dB | 11011 – +28.5 dB |
| | | | 01101 – +7.5 dB | others – +30 dB |
| | | | 01110 – +9 dB | |

### ADDRESS 0X5D, ADC

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| alc_ngth[4:0] | 7:3 | R/W | 00000 | Noise gate threshold | |
| | | | | 00000 – -76.5 dB<br>00001 – -75 dB<br>…… | 11110 – -31.5 dB<br>11111 – -30 dB |
| alc_ngat | 2 | R/W | 0 | Noise gate function enable<br>0 – disable<br>1 – enable | |
| alc_ngg[1:0] | 1:0 | R/W | 00 | Noise gate type<br>x0 – PGA gain held constant<br>01 – mute ADC output<br>11 – reserved | |

### ADDRESS 0X5E, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pdn_adcVrefgen | 7 | R/W | 1 | ADC Vref gen<br>0 – normal<br>1 – power down |
| pdn_adcBiasgen | 6 | R/W | 1 | ADC Bias gen<br>0 – normal<br>1 – power down |
| Pdn_adcPGAR | 5 | R/W | 1 | ADC right PGA<br>0 – normal<br>1 – power down |
| Pdn_adcPGAL | 4 | R/W | 1 | ADC left PGA<br>0 – normal<br>1 – power down |
| Pdn_adcModR | 3 | R/W | 1 | ADC right Mod<br>0 – normal<br>1 – power down |
| Pdn_adcModL | 2 | R/W | 1 | ADC left PGA<br>0 – normal<br>1 – power down |
| adc_syncMode | 1 | R/W | 0 | |
| rst_adc | 0 | R/W | 0 | |

### ADDRESS 0X5F, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LPadcInt1 | 7 | R/W | 0 | |
| LPadcFlash | 6 | R/W | 0 | |
| LPadcVcmMod | 5 | R/W | 0 | |
| LPADCVrp | 4 | R/W | 0 | |
| LPadcPGA | 3 | R/W | 0 | |
| adc_mref2 | 1 | R/W | 1 | |
| adc_mref1 | 0 | R/W | 0 | |

### ADDRESS 0X60, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LPGA_MicBoost | 5:4 | R/W | 00 | |
| RPGA_MicBoost | 1:0 | R/W | 00 | |

### ADDRESS 0X61, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| LPGA_LinVol | 6:4 | R/W | 000 | |
| RPGA_RinVol | 2:0 | R/W | 000 | |

### ADDRESS 0X62, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| RMIXLNOUT2LPGA | 7 | R/W | 0 | Right LINE mixer to left PGA<br>0 – disable<br>1 – enable |
| RMIXAXOUT2LPGA | 6 | R/W | 0 | Right AX mixer to left PGA<br>0 – disable<br>1 – enable |
| RMIXMNOUT2LPGA | 5 | R/W | 0 | Right Mono mixer to left PGA<br>0 – disable<br>1 – enable |
| LMIXMNOUT2LPGA | 4 | R/W | 0 | Left Mono mixer to left PGA<br>0 – disable<br>1 – enable |
| LMIXLNOUT2LPGA | 3 | R/W | 0 | Left LINE mixer to left PGA<br>0 – disable<br>1 – enable |
| adc_Rmono | 1 | R/W | 0 | |
| adc_Lmono | 0 | R/W | 0 | |

### ADDRESS 0X63, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| RMIXLNOUT2RPGA | 7 | R/W | 0 | Right LINE mixer to right PGA<br>0 – disable<br>1 – enable |
| RMIXAXOUT2RPGA | 6 | R/W | 0 | Right AX mixer to right PGA<br>0 – disable<br>1 – enable |
| RMIXMNOUT2RPGA | 5 | R/W | 0 | Right Mono mixer to right PGA |

| | | | | 0 – disable<br>1 – enable |
|---|---|---|---|---|
| LMIXMNOUT2RPGA | 4 | R/W | 0 | Left Mono mixer to right PGA<br>0 – disable<br>1 – enable |
| LMIXAXOUT2RPGA | 3 | R/W | 0 | Left AX mixer to right PGA<br>0 – disable<br>1 – enable |
| adc_RDCM | 1 | R/W | 0 | |
| adc_LDCM | 0 | R/W | 0 | |

### ADDRESS 0X64, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| AIR2RLNMUX | 7 | R/W | 0 | 0 – disable<br>1 – enable |
| VXN2RLNMUX | 6 | R/W | 0 | 0 – disable<br>1 – enable |
| LPGAP2RLNMUX | 5 | R/W | 0 | 0 – disable<br>1 – enable |
| RPGAP2RLNMUX | 4 | R/W | 0 | 0 – disable<br>1 – enable |
| AIL2LLNMUX | 3 | R/W | 0 | 0 – disable<br>1 – enable |
| VXP2LLNMUX | 2 | R/W | 0 | |
| LPGA2LLNMUX | 1 | R/W | 0 | |
| RPGAP2LLNMUX | 0 | R/W | 0 | |

### ADDRESS 0X65, ADC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| AIR2RAXMUX | 7 | R/W | 0 | 0 – disable<br>1 – enable |
| VXN2RAXMUX | 6 | R/W | 0 | 0 – disable<br>1 – enable |
| LPGAP2RAXMUX | 5 | R/W | 0 | 0 – disable<br>1 – enable |
| RPGAP2RAXMUX | 4 | R/W | 0 | 0 – disable<br>1 – enable |
| AIL2LAXMUX | 3 | R/W | 0 | 0 – disable<br>1 – enable |
| VXP2LAXMUX | 2 | R/W | 0 | |
| LPGA2LAXMUX | 1 | R/W | 0 | |
| RPGAP2LAXMUX | 0 | R/W | 0 | |

### ADDRESS 0X66, DAC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pdn_dac_csm | 7 | R/W | 1 | 0 – normal<br>1 – reset DAC digital and DAC CSM reset to power down |
| pdn_dac_dig | 6 | R/W | 0 | 0 – normal<br>1 – reset DAC digital (default) |
| dac_aeb | 3 | R/W | 0 | 0 – normal |

| | | | | 1 – both channel volume is set by left volume control register |
|---|---|---|---|---|
| clickfree | 2 | R/W | 0 | 0 – disable digital click free power up and down |
| | | | | 1 – enable digital click free power up and down (default) |
| dac_auto_mute | 1 | R/W | 0 | 0 – disable auto mute |
| | | | | 1 – enable auto mute |
| dac_mute | 0 | R/W | 0 | 0 – normal |
| | | | | 1 – mute for both channels |

### *ADDRESS 0X67, DAC*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| dac_invl | 7 | R/W | 0 | 0 – DAC left channel output no phase inversion |
| | | | | 1 – DAC left channel output 180 degree phase inversion |
| dac_invr | 6 | R/W | 0 | 0 – DAC right channel output no phase inversion |
| | | | | 1 – DAC right channel output 180 degree phase inversion |
| dac_zerol | 5 | R/W | 0 | 0 – normal |
| | | | | 1 – DAC Left Channel output all zero |
| dac_zeror | 4 | R/W | 0 | 0 – normal |
| | | | | 1 – DAC Right Channel output all zero |
| dac_mono | 3 | R/W | 0 | 0 – stereo |
| | | | | 1 – mono (L+R)/2 into DACL and DACR |
| dac_ramp | 2:0 | R/W | 0 | DAC ramp |
| | | | | 0xx – ramp disable |
| | | | | 100 – 0.5 dB per 4 LRCKs (default) |
| | | | | 101 – 0.5 dB per 32 LRCKs |
| | | | | 110 – 0.5 dB per 64 LRCKs |
| | | | | 111 – 0.5 dB per 128 LRCKs |

### *ADDRESS 0X68, DAC*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| dac_swap | 6 | R/W | 0 | 0 – normal |
| | | | | 1 – left and right channel data swap |
| vpp_scale | 5:4 | R/W | 0 | 00 – Vpp set at 3.5V (0.7 modulation index) |
| | | | | 01 – Vpp set at 4.0V |
| | | | | 10 – Vpp set at 3.0V |
| | | | | 11 – Vpp set at 2.5V |
| dither_off | 3 | R/W | 0 | DAC DSM dither |
| | | | | 0 – dither on |
| | | | | 1 – dither off |
| dac_se | 2:0 | R/W | 0 | SE strength |
| | | | | 000 – 0 |
| | | | | …… |
| | | | | 111 – 7 |

### *ADDRESS 0X69, DAC*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| jd_sw | 7:6 | R/W | 0 | Jack detect control |
| | | | | 00 – JD not active |
| | | | | 01 – spk/hp switch |
| | | | | 10 – mn/hp switch |
| | | | | 11 – spk+mn/hp switch |

| jdsw_pol | 5 | R/W | 0 | jack detect level polarity<br>0 – normal<br>1 – active level invert |
|---|---|---|---|---|
| jdsw_src | 4 | R/W | 0 | Jack Detect source<br>0 – from AINL<br>1 – from AINR |
| dac_fsmode | 2 | R/W | 0 | 0 – single speed mode<br>1 – double speed mode |
| dac_comp | 1 | R/W | 0 | DAC data companding control<br>0 – disable<br>1 – enable |
| dac_compmode | 0 | R/W | 0 | DAC data companding type<br>0 – u-law<br>1 – A-law |

### ADDRESS 0X6A, DAC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| dac_volumel | 7:0 | R/W | C0 | Digital volume control attenuates the signal in 0.5 dB incremental from 0 to -96 dB.<br>00000000 – 0 dB<br>00000001 – -0.5 dB<br>00000010 – -1 dB<br>…<br>11000000 – -96 dB (default) |

### ADDRESS 0X6B, DAC

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| dac_volumer | 7:0 | R/W | C0 | Digital volume control attenuates the signal in 0.5 dB incremental from 0 to -96 dB.<br>00000000 – 0 dB<br>00000001 – -0.5 dB<br>00000010 – -1 dB<br>…<br>11000000 – -96 dB (default) |

### ADDRESS 0X6C, DAC

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| lim_en | 7 | R/W | 0 | Enable the DAC digital limiter:<br>0 – disable<br>1 – enable | |
| lim_lvl[2:0] | 6:4 | R/W | 0 | Programmable signal threshold level (determines level at which the limiter starts to operate) | |
| | | | | 000 – -1 dB<br>001 – -2 dB<br>010 – -3 dB | 011 – -4 dB<br>100 – -5 dB<br>101 to 111 – -6 dB |
| lim_boost[3:0] | 3:0 | R/W | 0 | Limiter volume boost (can be used as a standalone volume boost when LIMEN = 0): | |

| | | | | 0000 – 0 dB<br>0001 – +1 dB<br>0010 – +2 dB<br>…(1 dB steps) | 1011 – +11 dB<br>1100 – +12 dB<br>1101 to 1111 – reserved |
|---|---|---|---|---|---|

### *ADDRESS 0X6D, DAC*

| Bit Name | Bit | R/W | default | Description | |
|---|---|---|---|---|---|
| lim_dcy[3:0] | 7:4 | R/W | 0 | Limiter decay time (per 6dB gain change) for 44.1kHz sampling. Note that these are proportionally related to sample rate. | |
| | | | | 0000 – 544 us<br>0001 – 1.088 ms<br>0010 – 2.177 ms<br>0011 – 4.354 ms (default)<br>0100 – 8.707 ms<br>0101 – 17.414 ms | 0110 – 34.829 ms<br>0111 – 69.658 ms<br>1000 – 139.315 ms<br>1001 – 278.63 ms<br>1010 – 557.26 ms<br>1011 to 1111 – 1.11 s |
| lim_atk[3:0] | 3:0 | R/W | 0 | Limiter attack time (per 6dB gain change) for 44.1kHz sampling. Note that these are proportionally related to sample rate. | |
| | | | | 0000 – 68 us<br>0001 – 136 us<br>0010 – 272 us<br>0011 – 544 us<br>0100 – 1.088 ms<br>0101 – 2.177 ms | 0110 – 4.354 ms<br>0111 – 8.707 ms<br>1000 – 17.414 ms<br>1001 – 34.829 ms<br>1010 – 69.658 ms<br>1011 to 1111 – 139.315 ms |

### *ADDRESS 0X6E, DAC*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| PdnDacL | 7 | R/W | 1 | |
| PdnDacR | 6 | R/W | 1 | |
| LPDacL | 5 | R/W | 0 | |
| LPDacR | 4 | R/W | 0 | |
| pdnDacVrefgen | 3 | R/W | 1 | |
| LPDacVrp | 2 | R/W | 0 | |
| dac_ibias_sw | 1 | R/W | 0 | |

### *ADDRESS 0X6F, DAC*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| offset_con[1:0] | 7:6 | R/W | 0 | Offset control<br>00 – offset auto detection<br>01 – user configure offset<br>1x – offset disable |
| ical_fixed | 5 | R/W | 0 | Fixed ical<br>0 – auto detect for HPL_ical/HPR_ical<br>1 – user configure HPL_ical/HPR_ical |
| offset_act | 4 | R/W | 0 | Offset active channel<br>0 – use offset1<br>1 – use offset2 |
| offset_sel | 2:0 | R/W | 0 | Select offset channel, offset1 - offset2 |

| | | | | 000 – ICAL_HP - MN |
|---|---|---|---|---|
| | | | | 001 – ICAL_HP - LN1 |
| | | | | 010 – ICAL_HP - LN2 |
| | | | | 011 – MN - LN1 |
| | | | | 100 – MN - LN2 |
| | | | | 101 – LN1 - LN2 |
| | | | | 110 – ICAL_HP only |
| | | | | 111 – HP only |

### *ADDRESS 0X70, SYSTEM*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pdn_ana | 7 | R/W | 1 | Analog power down<br>0 – normal<br>1 – power down |
| pdn_vddaLDO | 6 | R/W | 1 | Power down VDDA LDO<br>0 – VDDA LDO on<br>1 – VDDA LDO power down |
| stb_VDDALDO | 5 | R/W | 0 | |
| BPCap_VDDALDOB | 4 | R/W | 1 | |
| vddaLDO_fsOnOff | 3 | R/W | 0 | |
| vddaLDO_lvl | 2:0 | R/W | 011 | |

### *ADDRESS 0X71, SYSTEM*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| vx1Sel | 7 | R/W | 1 | |
| EnRef | 6 | R/W | 0 | |
| vref2to1 | 5 | R/W | 0 | |
| SUPPLYSEL | 4 | R/W | 1 | |
| vmidlo | 3:2 | R/W | 00 | |
| vmidSel | 1:0 | R/W | 00 | |

### *ADDRESS 0X72, SYSTEM*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| vsel1 | 7:0 | R/W | 0 | |

### *ADDRESS 0X73, SYSTEM*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| vsel2 | 7:0 | R/W | 0 | |

### *ADDRESS 0X74, SYSTEM*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| pdn_MicBias1 | 7 | R/W | 1 | Power down MIC bias1<br>0 – MIC bias1 on<br>1 – power down |
| micBias1_sel | 6:4 | R/W | 000 | |
| pdn_MicBias2 | 3 | R/W | 1 | Power down MIC bias2<br>0 – MIC bias2 on<br>1 – power down |
| micBias2_sel | 2:0 | R/W | 0 | |

*ADDRESS 0X75, SYSTEM*

| Bit Name | Bit | R/W | default | Description |
|---|---|---|---|---|
| ibiasgen_pdn | 7 | R/W | 1 | Power down ibiasgen<br>0 – ibiasgen on<br>1 – power down |
| ibiasgen_pdn2 | 6 | R/W | 1 | Power down ibiasgen2<br>0 – ibiasgen2 on<br>1 – power down |
| ibiasgen_sw | 5 | R/W | 0 | |
| ibiasgen_sw2 | 4 | R/W | 0 | |
| MIC1DFEN | 2 | R/W | 0 | |
| MIC2DFEN | 1 | R/W | 0 | |
| pdn_MICDF2SE | 0 | R/W | 1 | Power down MICDF2SE<br>0 – MICDF2SE on<br>1 – power down |

## 9. PACKAGE



| SYMBOL | MILLIMETER | |
|---|---|---|
| | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | — | 0.05 |
| b | 0.15 | 0.25 |
| c | 0.18 | 0.23 |
| D | 5.90 | 6.10 |
| D2 | 3.70 | 3.90 |
| e | 0.40BSC | |
| Ne | 4.40BSC | |
| Nd | 4.40BSC | |
| E | 5.90 | 6.10 |
| E2 | 3.70 | 3.90 |
| K | 0.20 | — |
| L | 0.35 | 0.45 |
| h | 0.30 | 0.40 |
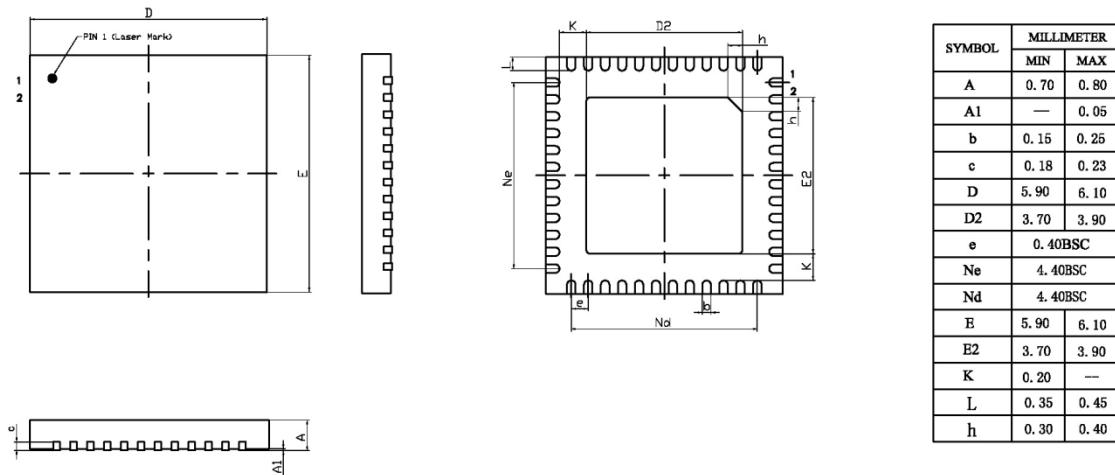
QFN 48L(0606X0.75-0.40)(B)

## 10.CORPORATE INFORMATION

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