DDA002C

High Performance Switch-Mode Power Supply Controller for Backlight and LLC Converters

The DDA002C controller hosts a high performance circuitry dedicated to driving half−bridge topologies, such as lamp ballasts for backlighting applications or resonant converters like the LLC circuit. The controller includes everything needed to build a reliable and rugged converter, including a pre−heating period and various protections such as an adjustable brown−out, for instance. Both, minimum and maximum switching frequencies, are adjustable by single pull down resistor, offering the ability to operate between 30 kHz and 500 kHz.

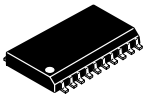
The controller includes a high−voltage driver that simplifies the design of the half−bridge configuration due to direct connection to the upper−side MOSFET. To avoid large shoot−through currents, the circuit includes a deadtime generator whose duration can be easily adjusted externally. Finally, two additional ground−referenced outputs allow the implementation of full−bridge applications.

Features

- High−Frequency Operation from 30 kHz up to 500 kHz
- Selectable Minimum Switching Frequency
- Adjustable Deadtime from 100 ns to 2 μs
- 100 ms Delayed Startup for PFC Stage Stabilization
- Adjustable Preheating Timer via External Capacitor
- Startup Sequence via Adjustable Soft−Start
- 600 V High−Voltage Floating Drivers
- Synchronized Low−Current Outputs for Full Bridge Applications
- Adjustable Maximum On−Time Clamp for Synchronization Outputs
- Brown−Out Protection for Easier PFC Association
- Delayed Open−Loop Protection
- Latched Input for Severe Fault Conditions, e.g. Over Current
- Secondary Latched Input for Over Temperature Protection
- Auto−Recovery Enable Input
- V_{CC} Operation up to 20 V
- Low Startup Current of 300 μA
- 0.5 A / 0.25 A Peak Current Sink / Source Drive Capability, Respectively
- Internal Temperature Shutdown
- SO19W package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

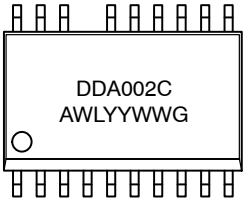
Typical Applications

- Flat Panel Display Power Converters
- LLC Converters Control for LCD/Plasma TVs
- HCFL / CCFL Backlight Inverters



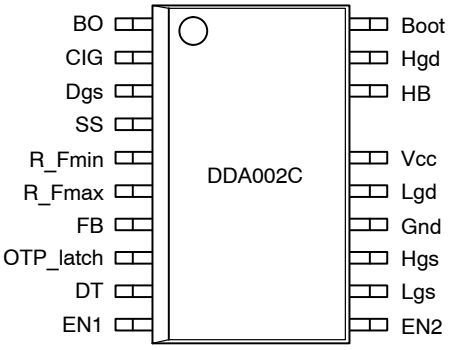
SOIC−19, LESS PIN 17
D SUFFIX
CASE 752AA

MARKING DIAGRAMS



DDA002C = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 26 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

July, 2009 − Rev. 0

Publication Order Number:
DDA002C/D

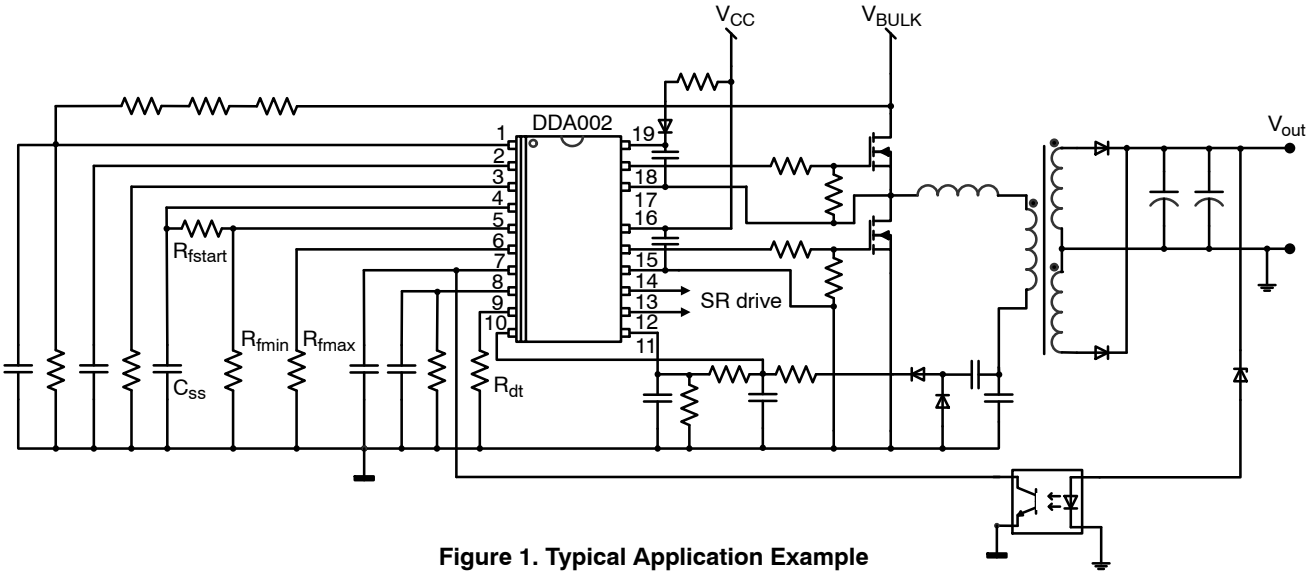


Figure 1. Typical Application Example

Pin Function Description

Pin No.	Pin Name	Function	Pin Description
1	BO	Brown−out	Detects low input voltage conditions and stops the controller. An internal current source sets the hysteresis.
2	CIG	Warm−up time	A capacitor connected to ground sets the pre−heat time for ballast applications.
3	DGS	Synchronous output clamp	A resistor connected between this pin and ground adjusts the maximum on−time available on Lgs and Hgs pins.
4	SS	Soft−start	Monitors the soft−start capacitor voltage to recognize end of the soft−start period, discharges the soft−start capacitor during any IC restart.
5	R_Fmin	Minimum frequency resistor	Connecting a resistor between this pin and ground, sets the minimum oscillator frequency reached for $V_{FB} \geq 5.1$ V
6	R_Fmax	Maximum frequency resistor	A resistor connected between this pin and ground sets the maximum frequency excursion reached for $V_{FB} \leq 1.2$ V
7	FB	Optocoupler connection	An optocoupler connected (by collector) between this pin and ground (by emitter) changes the converter operating frequency. The switching frequency increases when optocoupler pulls the FB pin down to ground.
8	OTP_latch	OTP latch input	If the voltage on this pin decreases below 1.5 V, the circuit latches off. This pin sources 170 μA current so an NTC resistor can be connected directly to this pin.
9	DT	Dead time	A resistor connected between this pin and ground sets the deadtime between drivers.
10	EN1	Enable input 1	When the voltage level on this pin exceeds a reference level for more than 50 μs, all pulses are stopped and the circuit permanently latches off.
11	EN2	Enable input 2	When the voltage level on this pin exceeds a reference voltage, the circuit stops pulsing. The IC auto−restarts via full startup sequence (PFC delay, pre−heat, soft−start) when EN2 is released.
12	Lgs	Lower gate signal	Duplicates the lower gate signal for synchronization purposes. On time is limited based on the Rdgs resistor value.
13	Hgs	Upper gate signal	Duplicates the upper gate signal for synchronization purposes. On time is limited based on the Rdgs resistor value.
14	GND	Ground	The controller ground
15	Lgd	Low−side driver	Drives the low−side half−bridge MOSFET
16	Vcc	Controller Supply	Energizing the controller. This pin accepts voltage up to 20 Vdc
17	HB	Half−Bridge	Connects to the half−bridge output
18	Hgd	High−side driver	Drives the high−side half−bridge MOSFET
19	Boot	High side driver supply line	This pin supplies the internal high−side driver

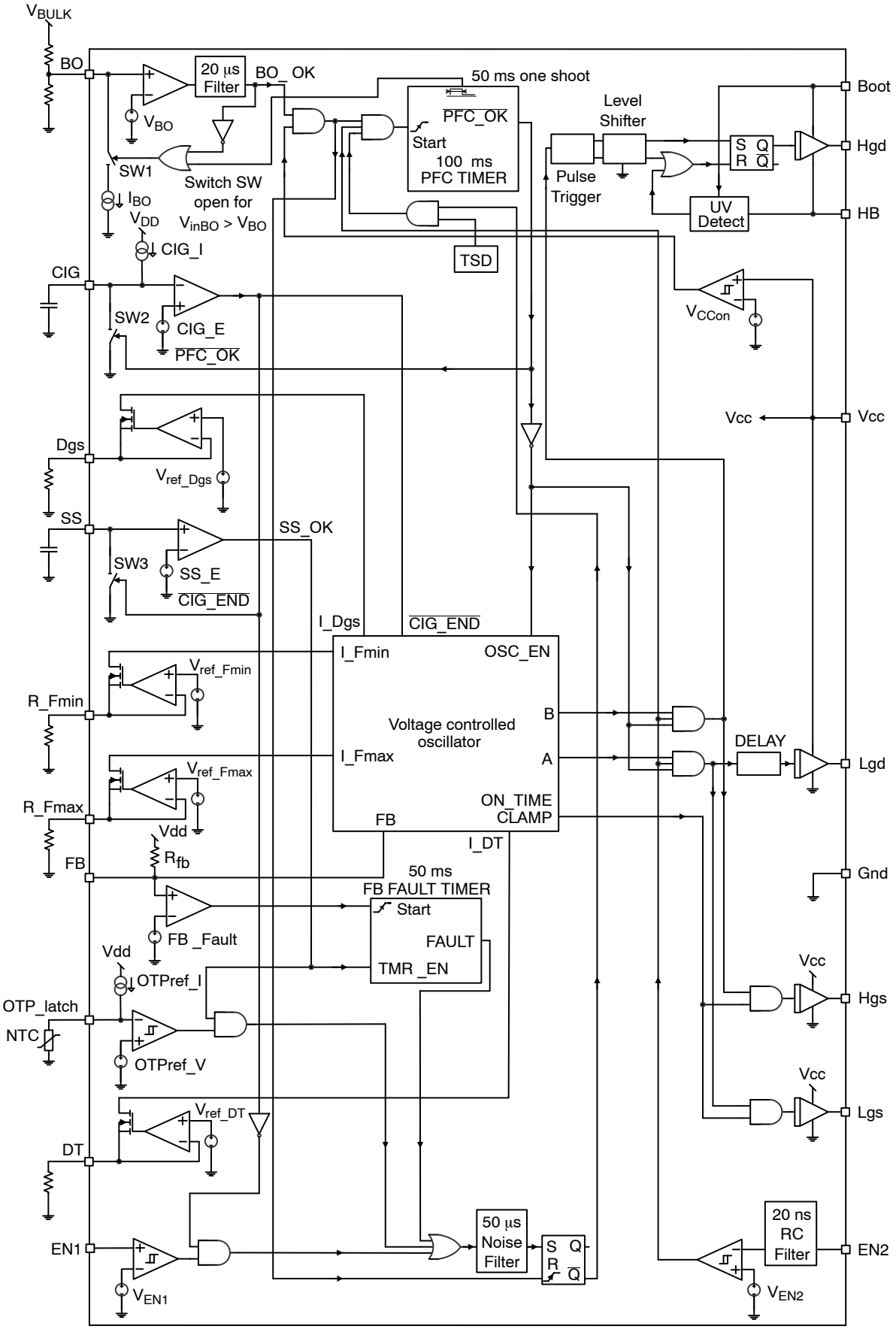


Figure 2. Internal Architecture

Maximum Ratings

Symbol	Rating	Value	Unit
V_{HB}	Continuous voltage on the bridge pin, pin 17	−1 to 600	V
Q_{max}	Maximum injected charge into the HB pin (Note 3)	11	nC
$V_{BOOT}-V_{HB}$	Floating supply voltage, pin 17 and 19	−0.3 to 20	V
V_{Hgd}	High side output voltage, pin 18	VHB−0.3 to VBOOT+0.3	V
V_{Lgd}	Low side output voltage, pin 15	−0.3 to Vcc+0.3	V
dV_{HB}/dt	Maximum slew rate on the HB pin, pin 17	±50	V/ns
Vcc	Power Supply voltage, pin 16	−0.3 to 20	V
	pin voltage, all pins (except pin 3, 6, 15, 16, 17, 18, and 19)	−0.3 to 10	V
V_{Dgs}	Synchronous clamp pin voltage, pin 3	−0.3 to 5	V
V_{R_Fmax}	Maximum frequency adjust pin voltage, pin 6	−0.3 to 5	V
$R_{\theta J-A}$	Thermal Resistance Junction−to−Ambient, (Soldered on traces with total area of 50 mm^2, 1 oz copper) Thermal Resistance Junction−to−Ambient, (Soldered on recommended layout, 1 oz copper)	137 117	°C/W
	Storage Temperature Range	−60 to +150	°C
T_{Jmax}	Maximum Junction Temperature	+150	°C
	ESD Capability, HBM model (Except all HV pins i.e., HB, Hgd and Boot) (Note 1)	2	kV
	ESD Capability, Machine Model	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests: Human Body Model 2000 V per JEDEC (22A114C − Human Body Model and 22A115A Machine Model)
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
3. The maximum injected charge corresponds to the injected current integrated over time into the half−bridge pin. Please refer to Figure 60 and related notes.

Electrical Characteristics
(For typical values T_j = 25°C, for min/max values T_j = −40°C to +125°C, Vcc = 15 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
VCC_{ON}	Turn−on threshold level, Vcc going up	16	11	12	13	V
$VCC_{(min)}$	Minimum operating voltage after turn−on (Note 4)	16	8.5	9.5	10.5	V
$Vboot_{ON}$	Startup voltage on the floating section	19,17	8	9	10	V
$Vboot_{(min)}$	Cutoff voltage on the floating section	19,17	7.4	8.4	9.4	V
Istartup	Startup current, Vcc < VCC_{ON}	16	–	–	300	μA
I_{CC1}	Internal IC consumption, no output load on pin 18/17 − 15/14, Fsw = 300 kHz (Note 5)	16	–	5	–	mA
I_{CC2}	Internal IC consumption, 1 nF output load on pin 18/17 − 15/14, Fsw = 300 kHz (Note 5)	16	–	14	–	mA
I_{CC3}	Internal IC consumption in fault mode (All drivers disabled, V_{CC} > $V_{CC(min)}$)	16	–	2.5	–	mA
VOLTAGE CONTROL OSCILLATOR (VCO)						
Fsw min	Minimum switching frequency, R_Fmin = 41 kΩ on pin 5, Vpin 7 > 5.5 V, DT = 300 ns (Notes 19 and 21)	5	58	60	62	kHz
Fsw max	Maximum switching frequency, R_Fmax = 2.5 kΩ on pin 6, Vpin 7 < 1.2 V, DT = 100 ns, Rt = 41 kΩ (Notes 20 and 21)	6	450	500	550	kHz
SVCO	Maximum VCO conversion slope, Δf / ΔVfb (Note 6)	–	–	120	–	kHz / V
FBSW min	Feedback pin swing above which Δf = 0, Fsw = Fmin, DC = 50%	7	–	5.1	–	V
FBSW max	Feedback pin swing below which Δf = 0, Fsw = Fmax, DC = 50% (Note 6)	7	–	1.2	–	V
DCsl, DCsh	Operating duty−cycle symetry, 5.5 V> Vpin 7 > 0.5 V (Note 7)	18,17; 15,14	48	50	52	%
Min T_{on}	Minimum On time	18,17; 15,14	–	880	–	ns
VFB_DC_0	Skip comparator threshold on the feedback pin (Note 8)	7	–	1.2	–	V
VFB_DC_0_ Hyste	Hysteresis on the skip comparator	7	–	50	–	mV
VREF	Reference voltage for Fmin current generation	5	–	2	–	V
FEEDBACK SECTION						
Rfb	Internal pull−up resistor	7	–	10	–	kΩ
Vfb_O	Open−loop voltage on the feedback pin, no optocoupler connection	7	–	7.3	–	V

4. $V_{CC(min)}$ = $V_{CCreset}$
5. Outputs Lgs and Hgs (pin 9/10) are unloaded.
6. Guaranteed by design.
7. DCsh = (DChs/(DChs + DCls)) * 100%, DCsl = (DCls/(DChs + DCls)) * 100%
8. The VFB_DC_0 is the FB voltage below which are all outputs disabled.
   The FB voltage has to increases to VFB_DC_0 + VFB_DC_0_Hyste to re−enable all outputs of the controller.
9. Low impedance source and sink $R_{DS(on)}$ are designed to respectively deliver 0.5 A and −1 A at Tj = 100°C.
10. Pins 17, 18 and 19 are on the same potencial during IHV_LEAK measurements
11. On−time on synchro outputs wont be longer than on−time on power outputs.
12. The soft start pin is pulled down by an internal switch until the CIG timer ending voltage is reached
13. FB timer is disabled until the soft−start ending voltage is reached
14. EN1 input is blanked until the preheat period (CIG) ends. The OTP input is blanked during full startup sequence made of: PFC_del + CIG_t + SS_t
15. The FB timeout circuit starts to operate at the end of PFC_del + CIG_t + SS_t period.
16. An NTC resistor of 8.8 kΩ @ T_A = 110°C is connected to ground.
17. The EN1 and EN2 input voltages have to go 50 mV below VEN1, VEN2 to release these inputs.
18. The OTP input voltage has to go 50 mV above OTPref_V to release this input.
19. The R_Fmin pin do not accept any bypass capacitor
20. Maximum acceptable capacitance connected to the pin is 100 pF
21. Measured for V_{CC} = 10.5 V

Electrical Characteristics
(For typical values T_j = 25°C, for min/max values T_j = −40°C to +125°C, Vcc = 15 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
LOW IMPEDANCE DRIVE OUTPUTS (HGD, LGD)						
T_r – Hgd	Output voltage rise−time @ C_L = 1 nF, 10−90% of output signal	18, 17	–	80	–	ns
T_f – Hgd	Output voltage fall−time @ C_L = 1 nF, 10−90% of output signal	18, 17	–	40	–	ns
R_{OH} – Hgd	Source resistance – (Note 9)	18, 17	–	30	–	Ω
R_{OL} – Hgd	Sink resistance – (Note 9)	18, 17	–	15	25	Ω
T_r – Lgd	Output voltage rise−time @ C_L 1 nF, 10−90% of output signal	15, 14	–	80	–	ns
T_f – Lgd	Output voltage fall−time @ C_L = 1 nF, 10−90% of output signal	15, 14	–	40	–	ns
R_{OH} – Lgd	Source resistance (Note 9)	15, 14	–	30	–	Ω
R_{OL} – Lgd	Sink resistance (Note 9)	15, 14	–	15	25	Ω
T_dead−min	Minimum dead−time, R_{DT} = 2.7 kΩ from pin 9 to GND (Notes 20 and 21)	9	–	100	–	ns
T_dead−nom	Nominal dead−time with R_{DT} = 10 kΩ from pin 9 to GND (Notes 20 and 21)	9	245	300	355	ns
T_dead−max	Maximum dead−time with R_{DT} = 82 kΩ from pin 9 to GND (Notes 20 and 21)	9	–	2	–	μs
IHV_LEAK	Leakage current on high voltage pins to GND (Note 10)	17, 18, 19	–	–	5	μA
SYNCHRONIZATION DRIVE OUTPUTS (LGS AND HGS)						
R_{OH} – S	Source resistance	12, 13, 14	–	60	–	Ω
R_{OL} – S	Sink resistance	12, 13, 14	–	60	–	Ω
DGS (SYNCHRONOUS OUTPUT CLAMP)						
Tdgs	Clamped on−time duration, Rdgs = 48 kΩ, Fsw < 24 kHz, DT = 300 ns (Notes 11, 20 and 21)	3, 12, 13	17.1	17.9	18.7	μs
Iduty_min	Minimum on−time duration, Rdgs = 12 kΩ, Fsw = Fmin (Notes 11, 20 and 21)	3, 12, 13	4.45	4.66	4.87	μs
Iduty_nom	Minimum on−time duration, Rdgs = 26 kΩ, Fsw < 24 kHz (Notes 11, 20 and 21)	3, 12, 13	9.65	10	10.35	μs
TIMERS						
CIG_I	CIG timer charging current	2	–	10	–	μA
CIG_E	CIG timer ending voltage (Note 12)	2	–	5	–	V
CIG_t	Typical CIG duration for a 0.22 μF capacitor on CIG pin	2	–	110	–	ms
SS_E	Soft−start ending voltage (Note 13)	4	–	1.9	–	V

4. $V_{CC(min)} = V_{CCreset}$
5. Outputs Lgs and Hgs (pin 9/10) are unloaded.
6. Guaranteed by design.
7. DCsh = (DChs/(DChs + DCls)) * 100%, DCsl = (DCls/(DChs + DCls)) * 100%
8. The VFB_DC_0 is the FB voltage below which are all outputs disabled.
   The FB voltage has to increases to VFB_DC_0 + VFB_DC_0_Hyste to re−enable all outputs of the controller.
9. Low impedance source and sink $R_{DS(on)}$ are designed to respectively deliver 0.5 A and −1 A at Tj = 100°C.
10. Pins 17, 18 and 19 are on the same potencial during IHV_LEAK measurements
11. On−time on synchro outputs wont be longer than on−time on power outputs.
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14. EN1 input is blanked until the preheat period (CIG) ends. The OTP input is blanked during full startup sequence made of: PFC_del + CIG_t + SS_t
15. The FB timeout circuit starts to operate at the end of PFC_del + CIG_t + SS_t period.
16. An NTC resistor of 8.8 kΩ @ T_A = 110°C is connected to ground.
17. The EN1 and EN2 input voltages have to go 50 mV below VEN1, VEN2 to release these inputs.
18. The OTP input voltage has to go 50 mV above OTPref_V to release this input.
19. The R_Fmin pin do not accept any bypass capacitor
20. Maximum acceptable capacitance connected to the pin is 100 pF
21. Measured for V_{CC} = 10.5 V

Electrical Characteristics
(For typical values T_j = 25°C, for min/max values T_j = −40°C to +125°C, Vcc = 15 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
TIMERS						
PFC_del	Internal delay timer after brown−out confirmation, EN2 released or Vcc restart	−	−	100	−	ms
PROTECTIONS						
VEN1	Reference voltage for the enable 1 input (latch), (Note 14), (Note 17)	10	0.95	1	1.05	V
VEN2	Reference voltage for the enable 2 input (Note 17)	11	0.95	1	1.05	V
HysteENX	Hysteresis for EN1, EN2 inputs	10, 11	−	50	−	mV
VdelEN1	Delay before latch confirmation on EN1 input (Note 14)	10	−	50	−	μs
VdelEN2	Delay between the EN2 activation and driver disable	11	−	80	120	ns
VBO	Brown−Out level	1	0.95	1	1.05	V
IBO	Hysteresis current, Vpin 1 = 0.9 V, 0°C < T_J < 125°C −40°C < T_J < 125°C	1	17.85 16.31	21 21	24.15 24.15	μA
IBObias	Brown−Out input bias current	1	−	0.02	−	μA
OTPref_I	OTP Reference current (Note 16), 0°C < T_J < 125°C −40°C < T_J < 125°C	8	155.7 143.7	173 173	190.3 190.3	μA
OTPref_V	OTP reference voltage (Note 14), (Note 18)	8	1.425	1.5	1.575	V
OTP_hyste	OTP comparator hysteresis	8	−	50	−	mV
OTPnoise	Noise filter on the OTP output (Note 14)	8	−	50	−	μs
FB_Fault	Above this level, the FB fault timer is activated (Note 15)	7	−	6	−	V
FB_timer	FB timeout duration (Note 15)	7	−	50	−	ms
TSD	Temperature shutdown threshold	−	140	−	−	°C
TSDhyste	Temperature shutdown hysteresis	−	−	30	−	°C

4. $V_{CC(min)} = V_{CCreset}$
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7. DCsh = (DChs/(DChs + DCls)) * 100%, DCsl = (DCls/(DChs + DCls)) * 100%
8. The VFB_DC_0 is the FB voltage below which are all outputs disabled.
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21. Measured for V_{CC} = 10.5 V

TYPICAL CHARACTERISTICS

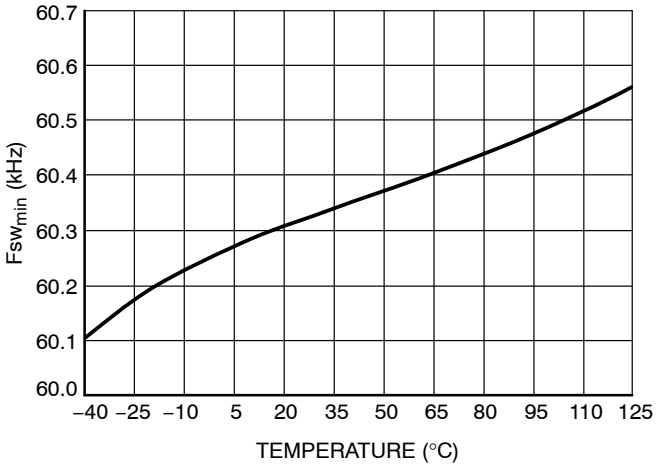


Figure 3. Fsw$_{min}$ vs. Temperature

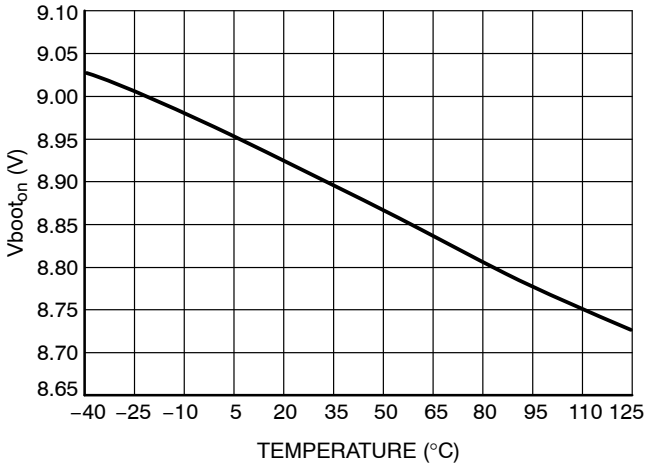


Figure 4. Vboot$_{on}$ vs. Temperature

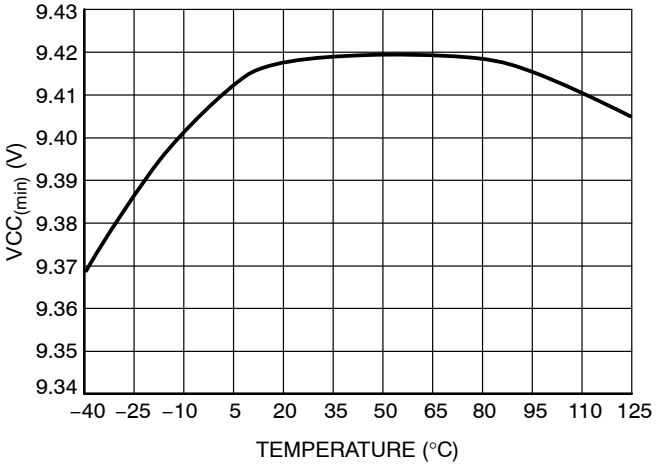


Figure 5. VCC$_{(min)}$ vs. Temperature

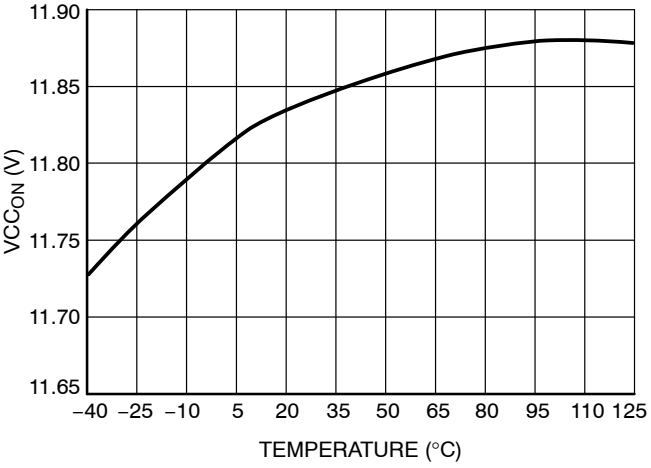


Figure 6. VCC$_{ON}$ vs. Temperature

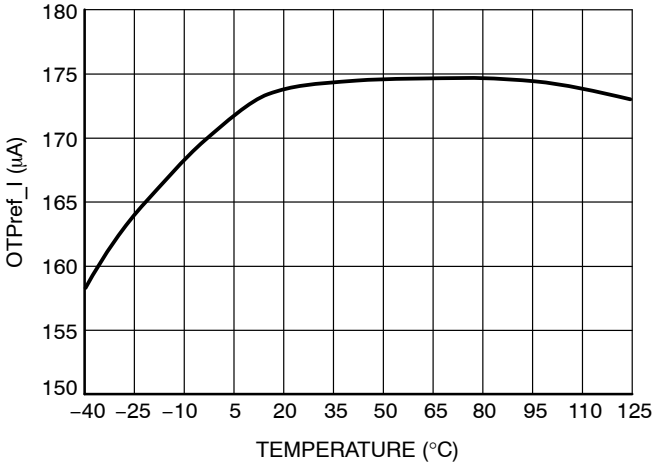


Figure 7. OTPref_I vs. Temperature

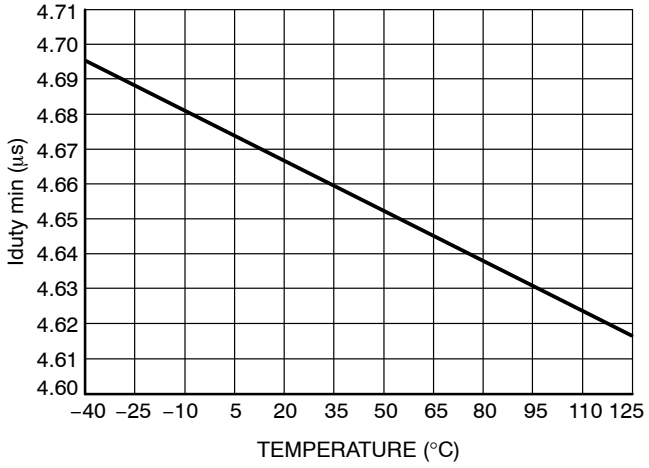


Figure 8. Iduty min vs. Temperature

TYPICAL CHARACTERISTICS

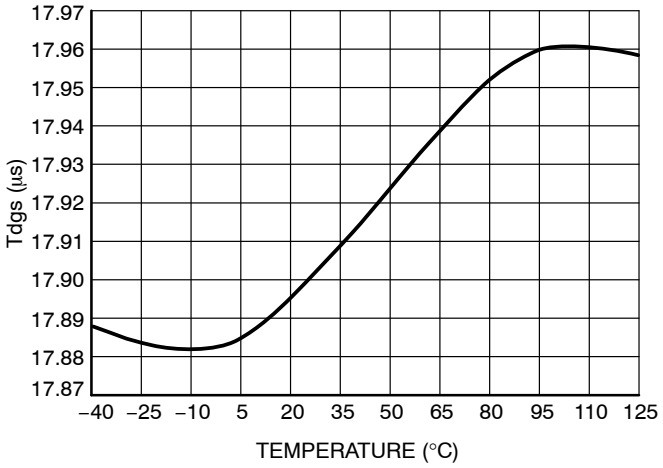


Figure 9. Tdgs vs. Temperature

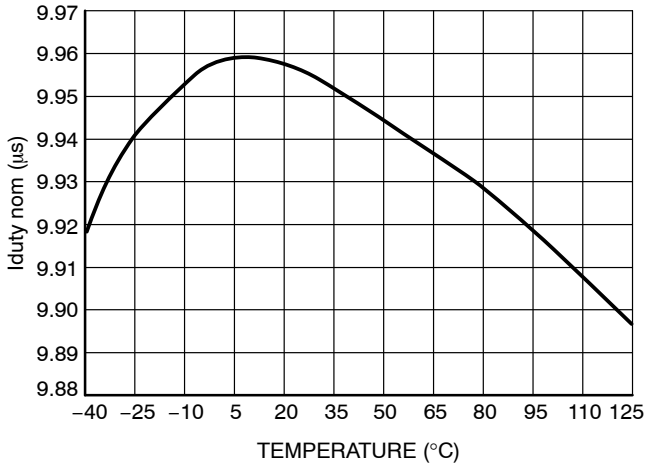


Figure 10. Iduty nom vs. Temperature

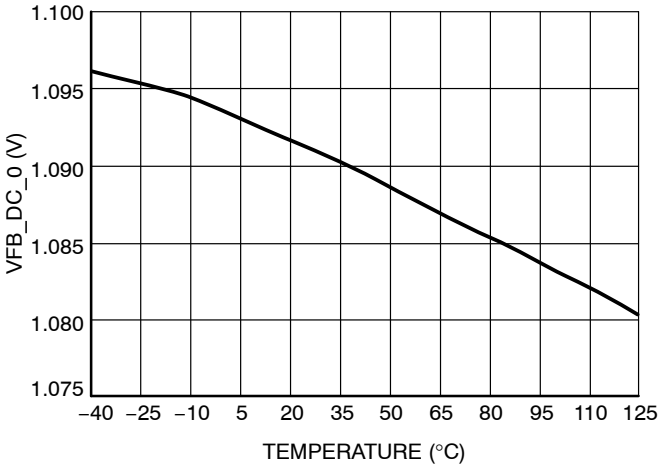


Figure 11. VFB_DC_0 vs. Temperature

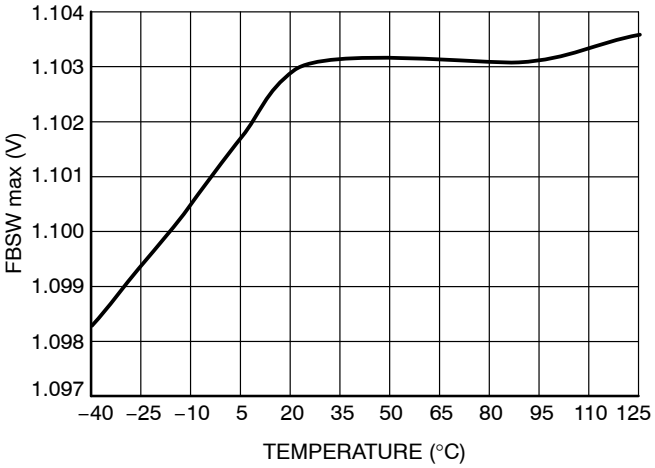


Figure 12. FBSW max vs. Temperature

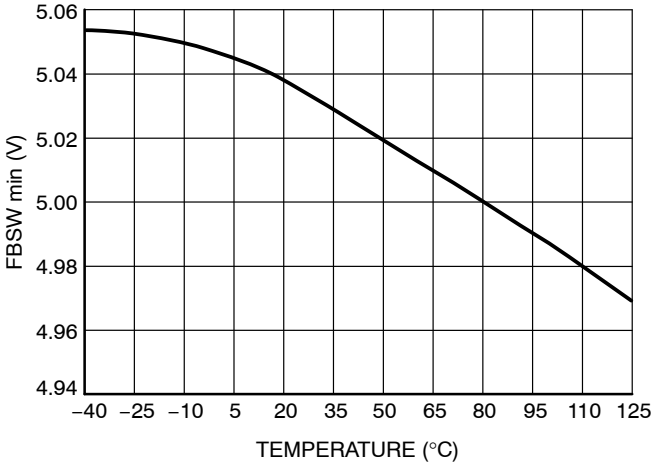


Figure 13. FBSW min vs. Temperature

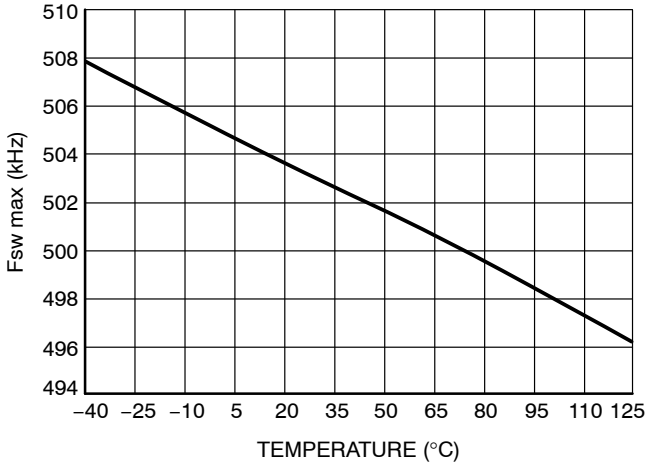


Figure 14. Fsw max vs. Temperature

TYPICAL CHARACTERISTICS

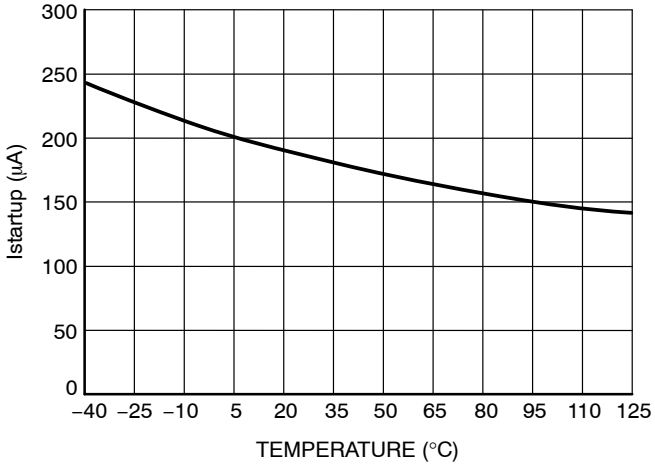


Figure 15. Istartup vs. Temperature

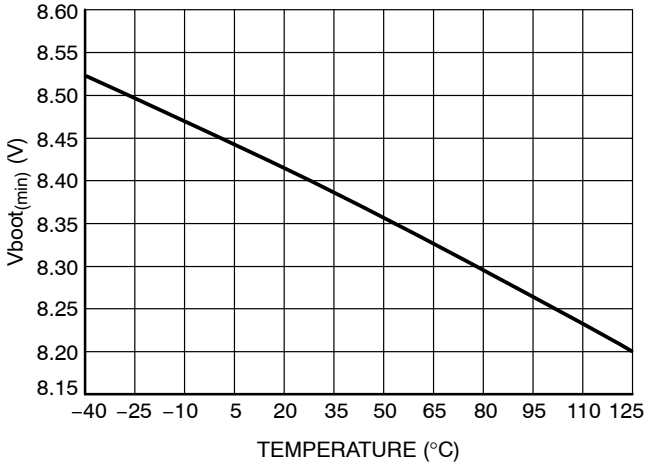


Figure 16. Vboot$_{(min)}$ vs. Temperature

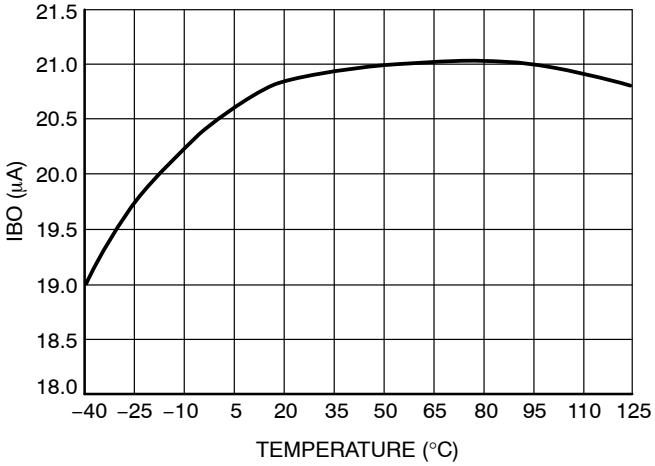


Figure 17. IBO vs. Temperature

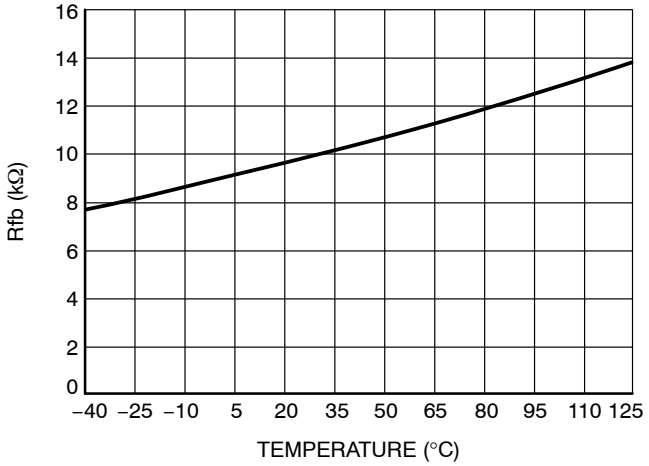


Figure 18. Rfb vs. Temperature

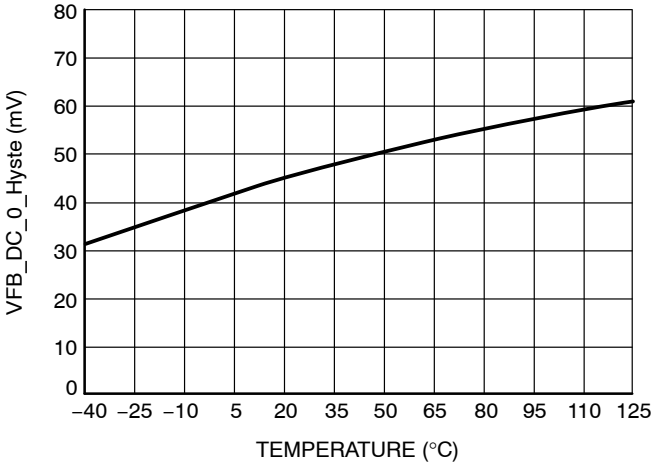


Figure 19. VFB_DC_0_Hyste vs. Temperature

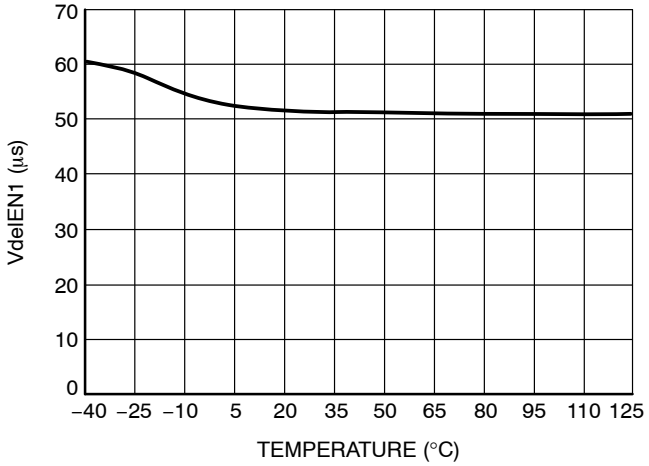


Figure 20. VdelEN1 vs. Temperature

TYPICAL CHARACTERISTICS

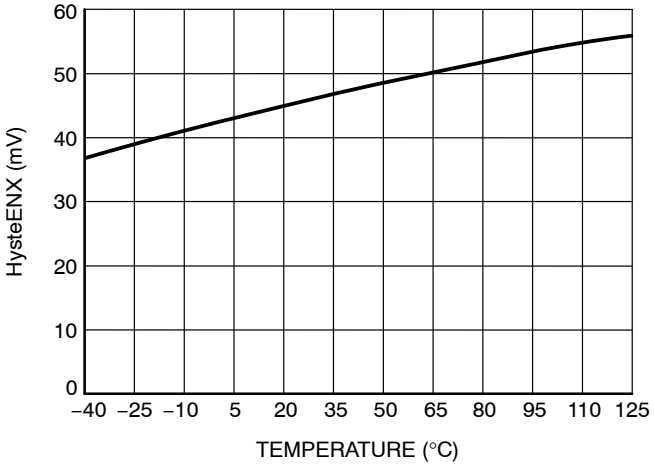


Figure 21. HysteENX vs. Temperature

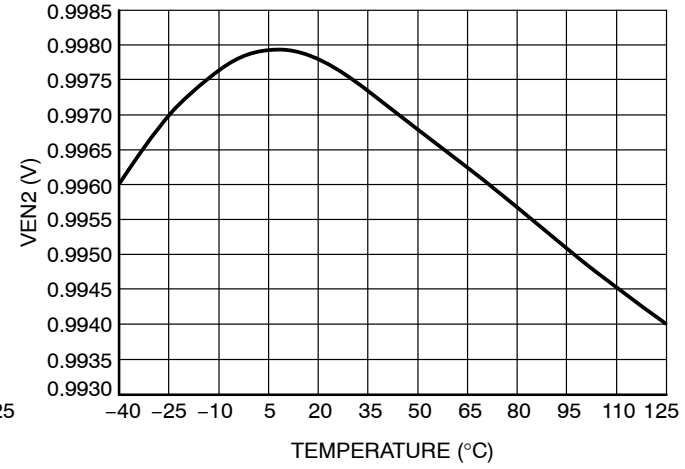


Figure 22. VEN2 vs. Temperature

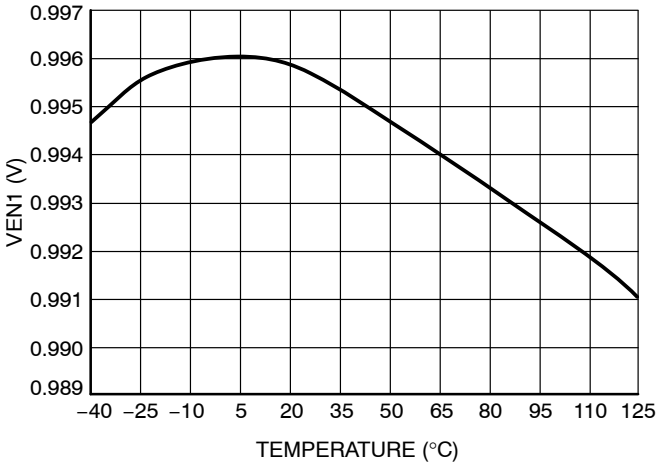


Figure 23. VEN1 vs. Temperature

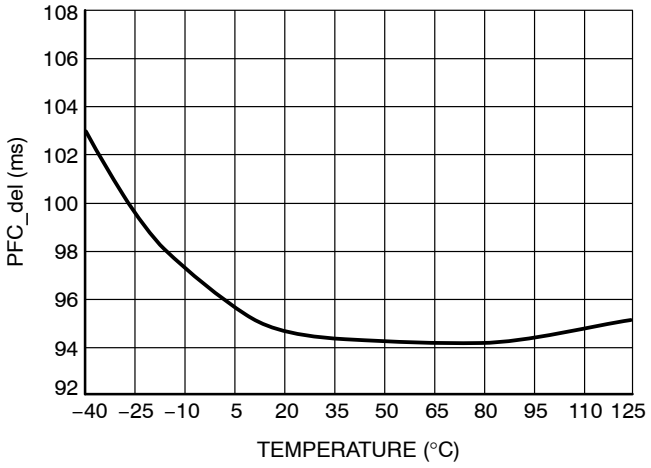


Figure 24. PFC_del vs. Temperature

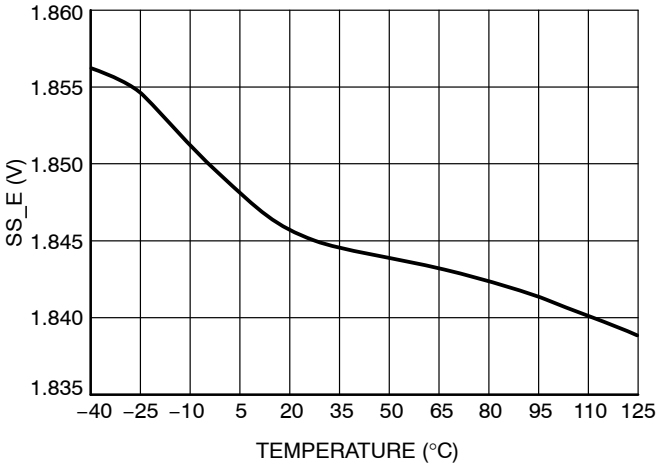


Figure 25. SS_E vs. Temperature

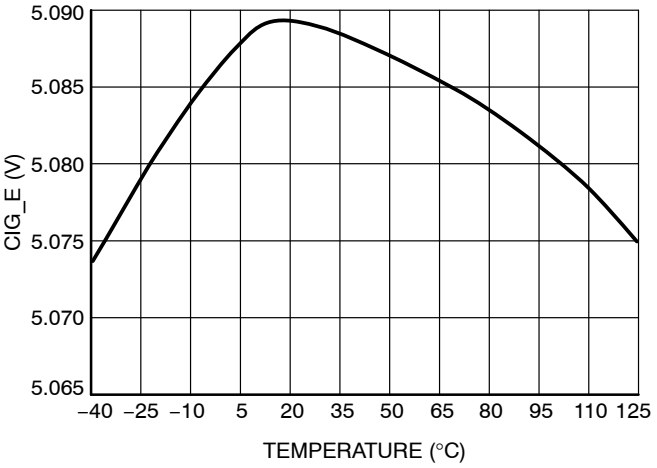


Figure 26. CIG_E vs. Temperature

TYPICAL CHARACTERISTICS

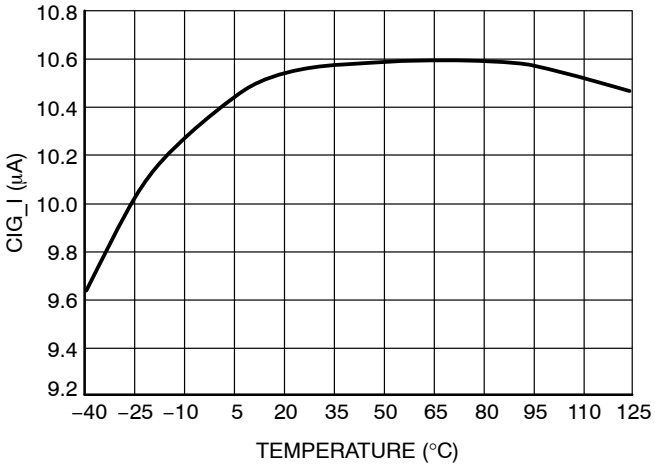


Figure 27. CIG_I vs. Temperature

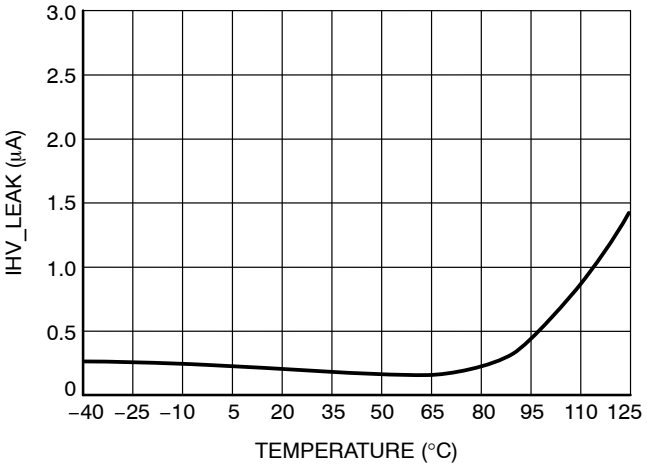


Figure 28. IHV_LEAK vs. Temperature

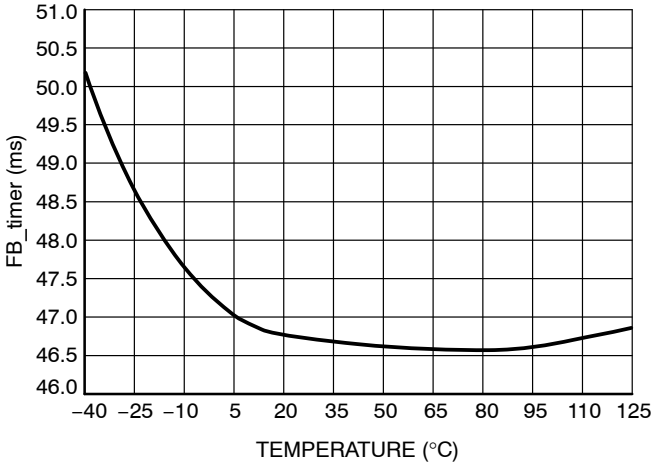


Figure 29. FB_timer vs. Temperature

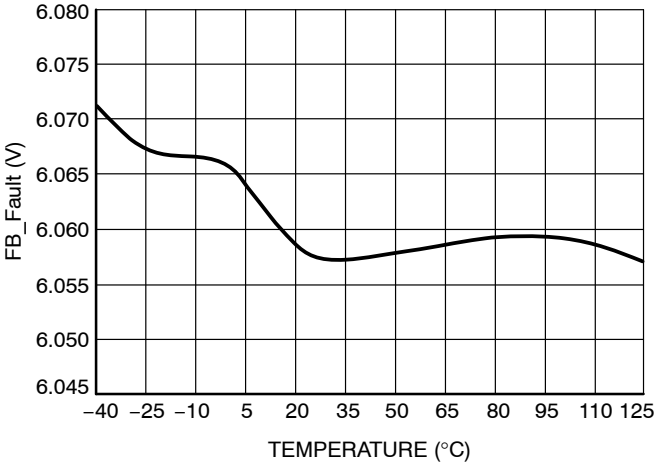


Figure 30. FB_Fault vs. Temperature

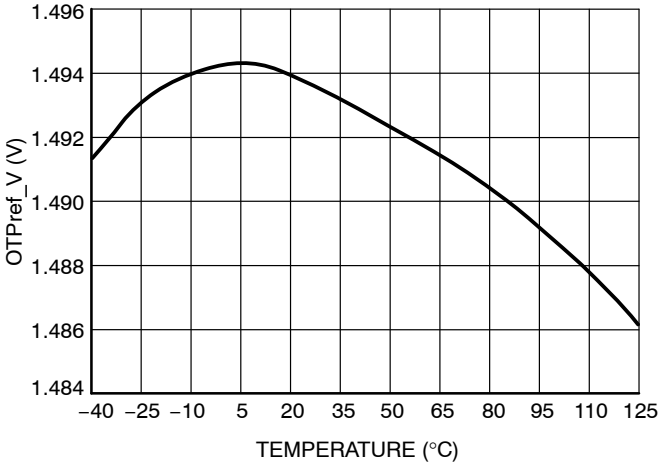


Figure 31. OTPref_V vs. Temperature

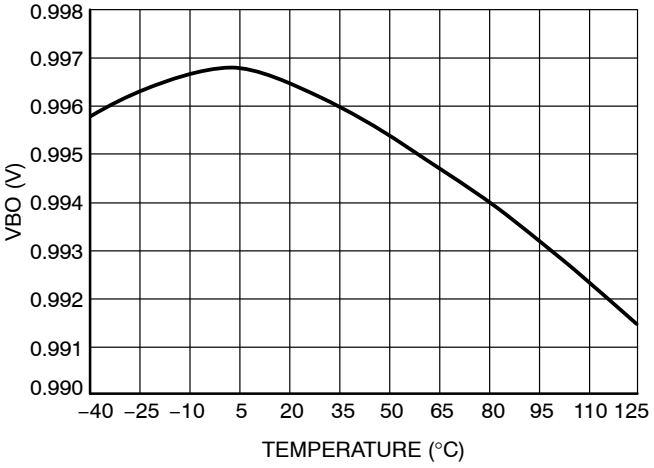


Figure 32. VBO vs. Temperature

TYPICAL CHARACTERISTICS

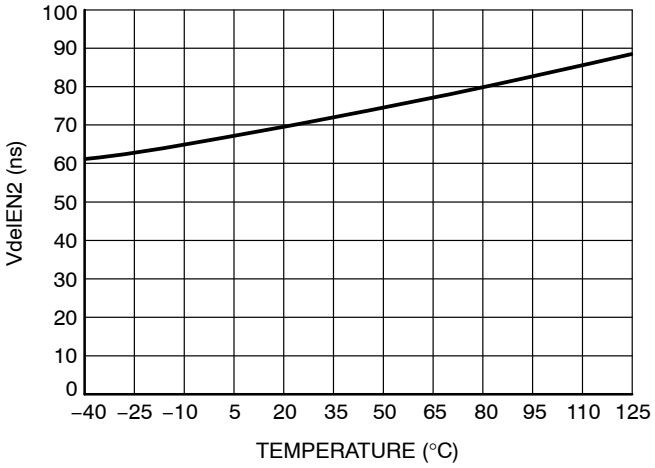


Figure 33. VdelEN2 vs. Temperature

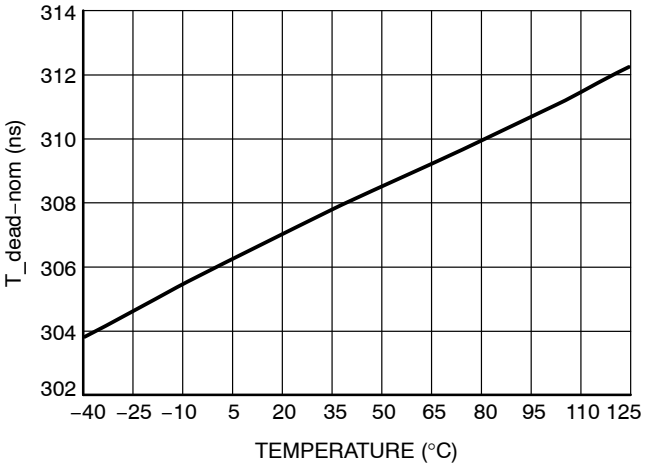


Figure 34. T_dead−nom vs. Temperature

Application Information

The DDA002C includes all necessary features that help building a rugged and safe switch−mode power converter for an LCD TV backlighting or LLC resonant SMPS applications. The bullets below detail the benefits brought by implementing the DDA002C controller:

- **High−voltage drivers:** thanks to the ON Semiconductor proprietary technology, the DDA002C controller can directly drive the upper−side transistor of a half−bridge configuration biased up to 600 V.
- **Wide frequency range:** a high−speed Voltage Control Oscillator allows operating frequency excursion from 30 kHz up to 500 kHz on the Lgd and Hgd outputs, with a 50% duty−cycle. These two outputs are available as synchronization signals via two ground−referenced low−current outputs (Lgs and Hgs).
- **Internal skip comparator:** all drivers are disabled when feedback voltage goes below 1.2 V level. The skip comparator includes 50 mV hysteresis.
- **PFC−delay:** the controller includes a fixed 100 ms delay to allow bulk voltage stabilization after the PFC stage has been started. The PFC timer is reset at power−on, when a brown−out condition occurs and when the EN2 input is released. The controller is ready (VREF is OK) but no pulses are delivered by the outputs during this delay period.
- **Pre−heat period:** once the PFC delay has elapsed, the circuit starts to pulse with start up frequency to pre−heat the lamps (in HCFL ballast applications). This period is also called CIG period.
- **Adjustable soft−start:** at the end of the pre−heat period, the soft−start sequence takes place. The controller starts pulsing with F_{start} and reduces its frequency down to F_{min}. The feedback loop is supposed to take over during this period. The F_{start} frequency is dictated by the parallel combination of R_{fstart} and Rf_{min} resistors, the soft−start length is given by a capacitor connected to the ground. The soft−start sequence is activated after every controller restart.
- **Open−Loop detection:** the controller starts to monitor the feedback voltage at the end of the soft−start period. If it remains stuck above 6 V (it means the feedback loop is not closed) the internal timer starts the countdown. The controller latches off if this situation lasts longer than 50 ms.
- **Adjustable dead−time:** using a single resistor wired to the ground, the user has ability to include needed dead−time that helps to fight cross−conduction between the upper and lower bridge transistors.
- **Adjustable minimum and maximum frequency excursion:** in resonant applications, it is important to stay away from the resonating peak to keep the converter operating in the right region (ZVS). It is also needed, for ballast applications, to keep the F_{min} accuracy high since it dictates maximum lamp power. Thanks to a single external resistor, the designer can program its lowest frequency point, obtained due to a lack of feedback voltage (during the startup sequence or in short−circuit conditions). Internally trimmed capacitor offers a ±3.3 % precision on the selection of the minimum switching frequency. The adjustable upper frequency limit is less precise (±10%).
- **Low startup current:** the device requires only 300 μA start−up current. This feature decreases the power dissipation and/or shortening of the start−up time when the controller is powered from an auxiliary winding and starts using a startup resistor connected directly to the bulk voltage.
- **Brown−Out detection:** the IC incorporates a brown out comparator, which prevents the outputs from switching in case the high−voltage rail is not within the right boundaries. The turn on and off levels of the bulk voltage can be adjusted independently thanks to the internal current sink IBO.
- **Enable1 input:** when a voltage above 1 V is applied to this pin, for a time longer than 50 μs, the controller permanently latches−off. The latch resets when Vcc is cycled below Vcc(min) or when there is a brown−out event detected. The EN1 input is blanked during the PFC delay and preheat periods.
- **Enable2 input:** when a voltage higher than 1 V is applied to this pin, the controller immediately stops all pulses. The controller restores operation (including PFC delay, preheat and soft−start) when enable 2 input voltage decreases down again.
- **OTP latch input:** by connecting an NTC resistor between ground and the OTP_latch input, the designer has ability to latch−off the controller in an over−temperature condition. The OTP input is blanked during the PFC delay, preheat and soft−start periods.
- **Synchronization outputs:** two low−current ground referenced outputs (Lgs and Hgs) are available to implement a full−bridge converter in higher power configurations. A resistor connected to the Dgs pin sets the maximum allowable on−time that is delivered by these two outputs when used for synchronization purpose.

Voltage−Controlled Oscillator

The VCO section features a high−speed circuitry allowing operation from 60 kHz up to 1 MHz. However, as there is an internal division by two, it creates Q and $\overline{Q}$ outputs. The final effective signal on the outputs Lgd, Hgd, Lgs and Hgs therefore switches between 30 kHz and 500 kHz. The VCO is configured in such a way that if the feedback pin voltage goes down, the switching frequency goes up. Figure 35 shows simplified architecture of the VCO.

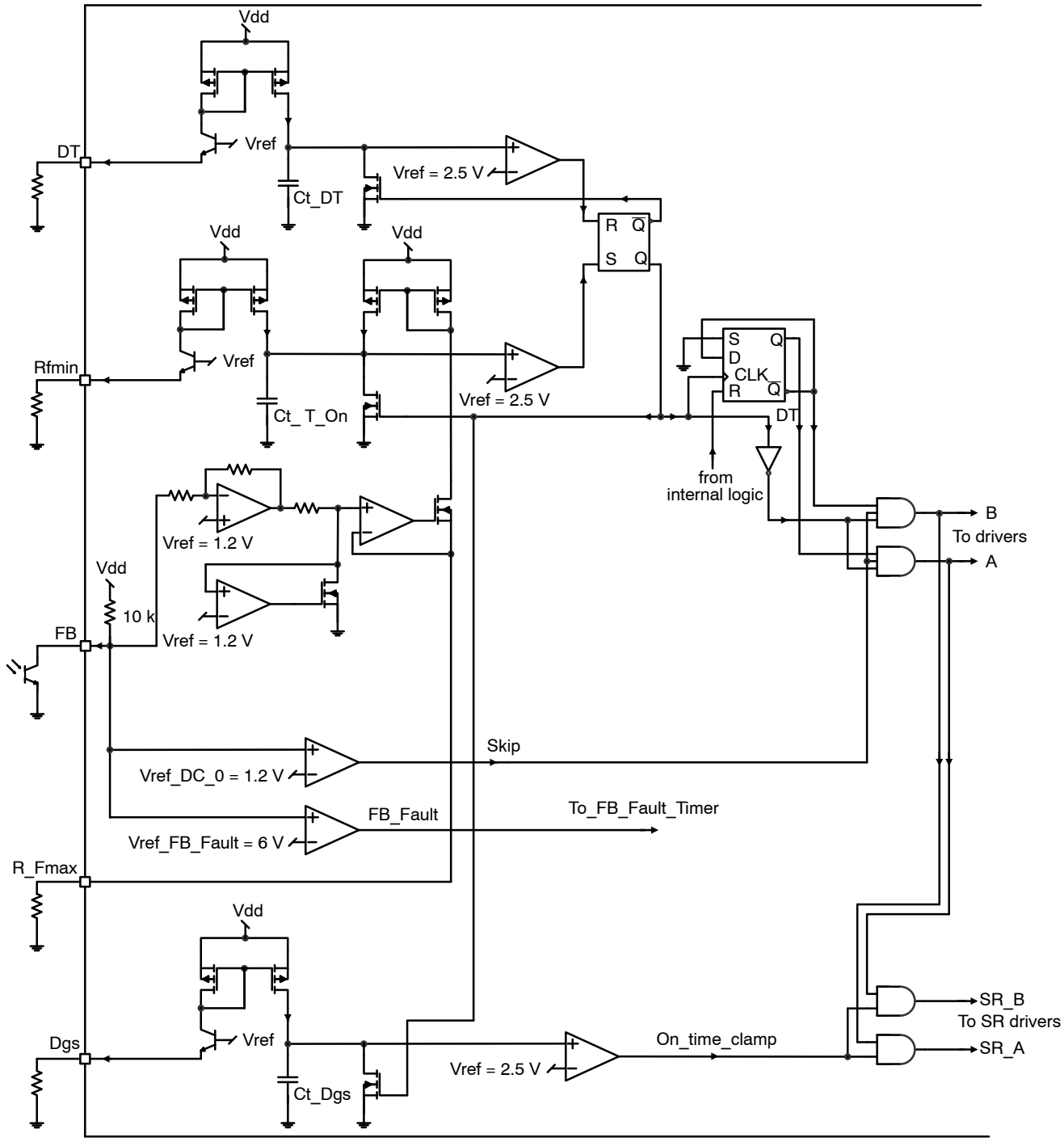


Figure 35. Simplified VCO Architecture

The VCO conversion characteristic is shown in Figure 36. The FB fault is detected in case the feedback voltage is higher than 6 V. This will happen if the converter is overloaded or the feedback path is not closed i.e. a broken optocoupler. The internal fault timer starts to count once the FB fault is detected and it latches off the controller if the fault lasts more than 50 ms. To overcome triggering of the FB fault protection during the application start, the FB timer is disabled until the soft−start period ends (V_{SS} > 1.9 V).

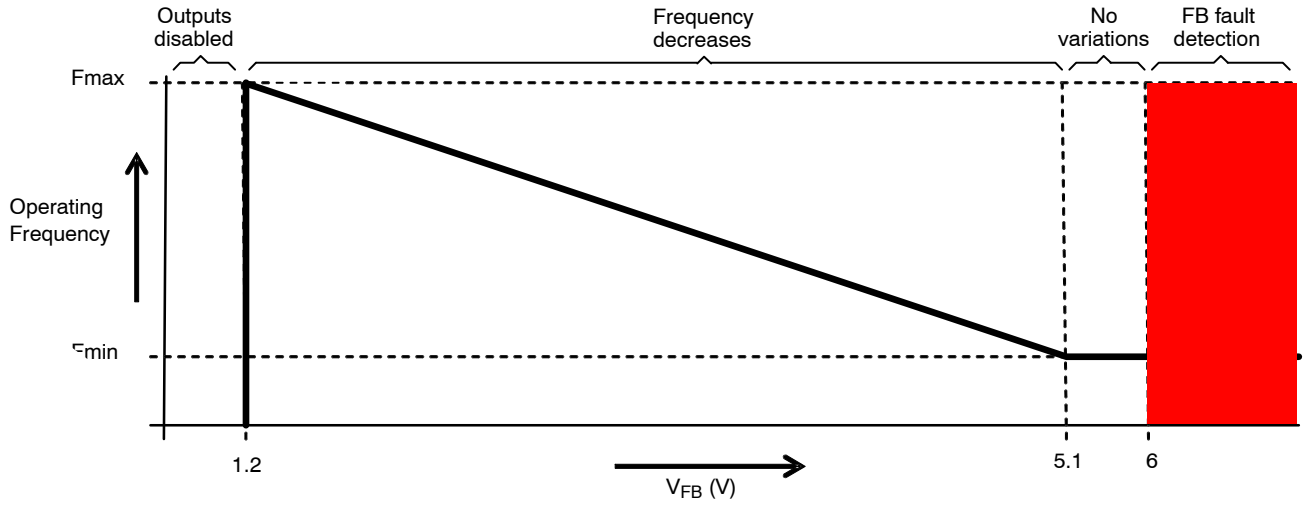


Figure 36. VCO Transfer Characteristic

The output frequency remains at Fmin and the duty cycle is at its maximum value (50% − deadtime) when the FB pin voltage ranges between 5.1 and 6 V. The frequency of the converter varies between F_{min} and F_{max} values if the feedback voltage changes from 5.1 to 1.2 V. If the feedback voltage further decreases, the operating frequency stays constant and is given by the R_fmax resistor value. The IC disables all drivers once the feedback voltage goes below 1.2 V threshold − skip mode. Please refer also to typical VCO operating waveforms in Figure 37.

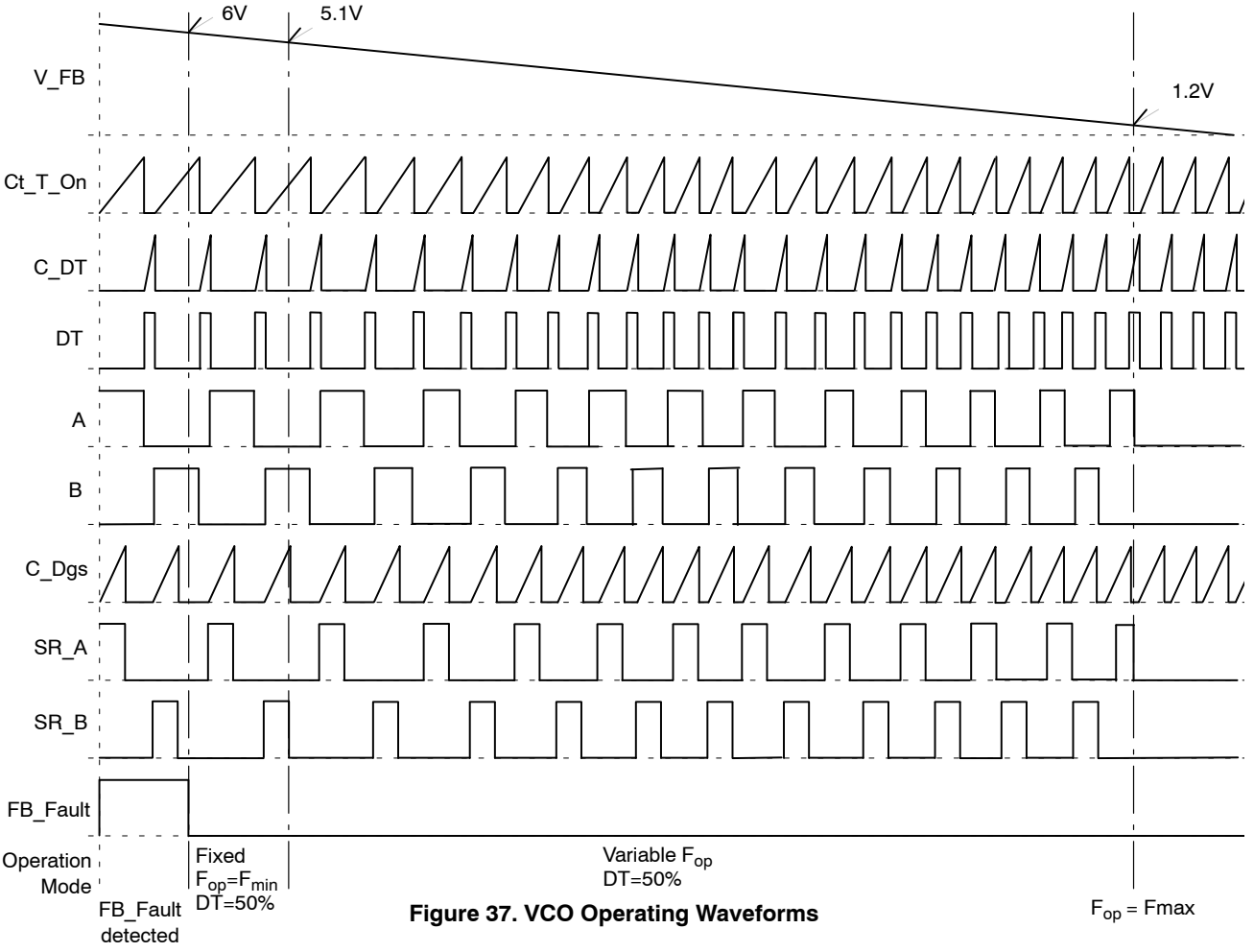


Figure 37. VCO Operating Waveforms

The selection of the three setting resistors (F_{max}, F_{min} and deadtime) require the usage of the selection charts displayed below:

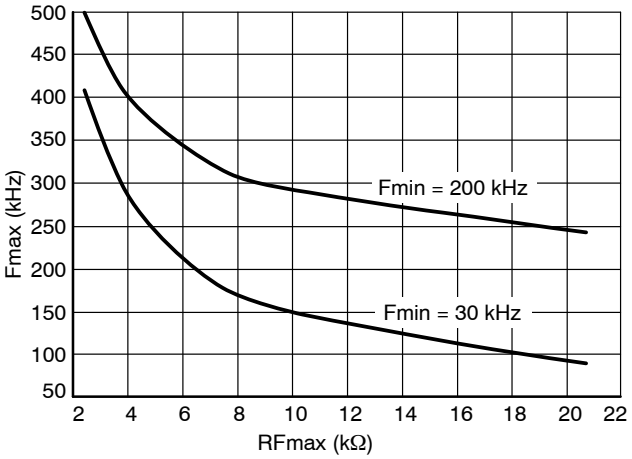


Figure 38. Maximum Switching Frequency Resistor Selection Depending on the Adopted Minimum Switching Frequency

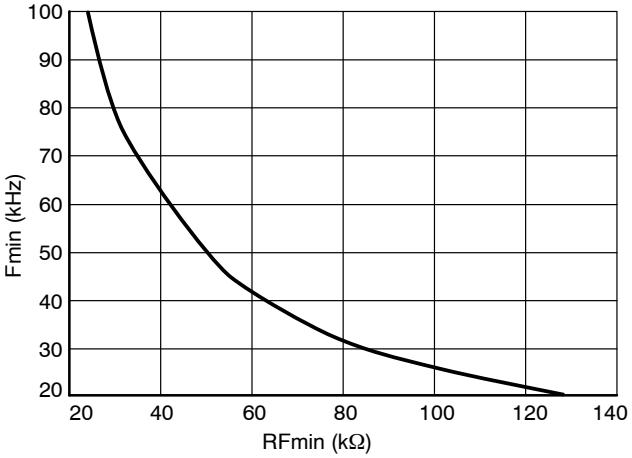


Figure 39. Minimum Switching Frequency Resistor Selection (Fmin = 20 kHz to 100 kHz)

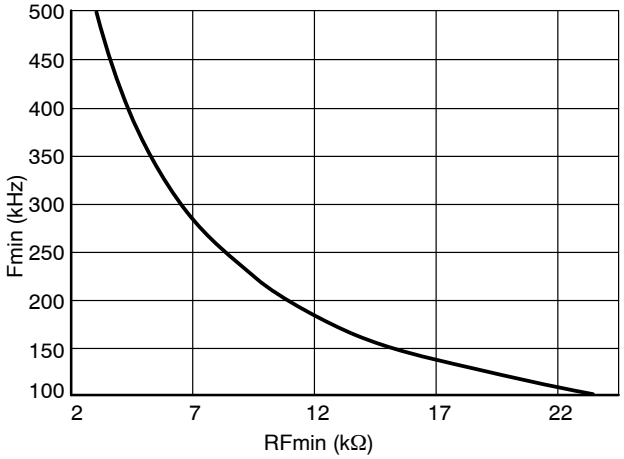


Figure 40. Minimum Switching Frequency Resistor Selection (Fmin = 100 kHz to 500 kHz)

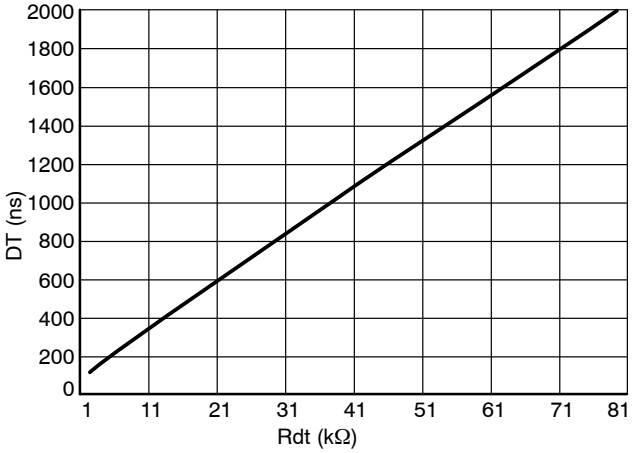


Figure 41. Deadtime Resistor Selection

Deadtime Control

Deadtime control is an absolute necessity when the half−bridge configuration comes into play. The deadtime technique consists of including a time period during which both high and low side switches are off. Of course, the deadtime amount should be different depending on the switching frequency, hence the ability to adjust it on this controller. The option ranges between 100 ns and 2 μs. The deadtime is actually made by the internal timer which is a part of the VCO. Please refer to Figures 35 and 37 for more details. During the C_{t_DT} capacitor charge time, the internal latch is set and invalidates the AND gates: all outputs are low. When the comparator goes back to the low level, A and B outputs are validated, while the timing capacitor $C_{t\_T\_On}$ recharges. By connecting a resistor R_{DT} to the ground, it creates a current whose image serves to charge the C_{t_DT} capacitor − we control the deadtime. It typically ranges between 100 ns (R_{DT} = 2.7 kΩ) and 2 μs (R_{DT} = 70 kΩ).

100 ms PFC Timer

The DDA002C device features an internal digital timer that prolongs the device start by 100 ms after the controller is enabled by Vccon and/or a BO event. This fixed delay allows the PFC stage to fully stabilize the bulk voltage before the resonant power stage is activated. The PFC delay also occurs when the EN2 input is released.

Adjustable Preheat Period − CIG Timer

As this IC is tailored not only for the resonant SMPS applications but also to drive HCFL lamp ballasts, it includes an adjustable preheat timer that allows the designer to accurately setup needed filament preheat time. The timer uses an external capacitor ($C_{preheat}$) that is charged from an internal current source (CIG_I). The IC outputs are forced (via VCO) to operate at the frequency that is given by the parallel combination of resistors R_{fmin} and R_{fstart} until the $C_{preheat}$ capacitor voltage reaches 5 V. Figure 42 shows the internal arrangement of the GIC timer.

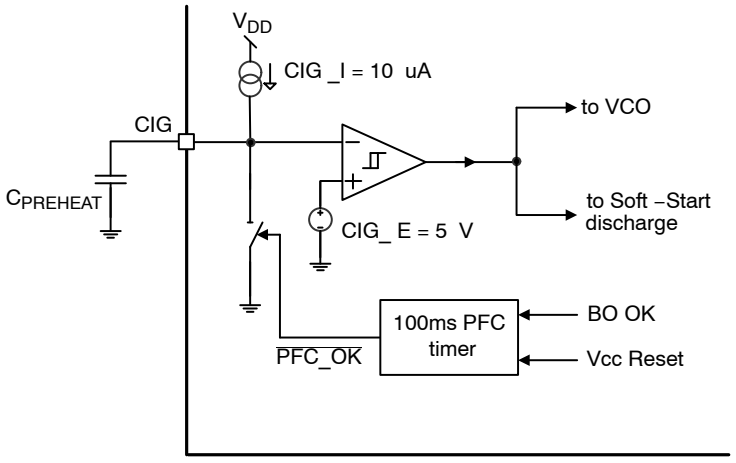


Figure 42. CIG Timer Internal Connection

The preheat time can be easily calculated using Equation 1:

$$T_{CIG} = C_{Preheat} \cdot 0.5 \qquad \text{(eq. 1)}$$

Where:

T_{CIG} is the preheat period time in seconds

$C_{Preheat}$ is the preheat capacitor value in μF

Note that the PFC delay period takes place prior to preheat period. Soft−start period starts immediately after the preheat capacitor voltage is higher than 5 V. If using this IC to drive a resonant SMPS or another application that does not require preheating, use 100 nF capacitor on the CIG pin to overcome false triggering by external noise.

Soft−start Sequence

In resonant converters, a soft−start is needed to avoid suddenly applying the full current into the resonant tank. The soft−start is fully controlled by the external component values when using DDA002C controller − refer to Figure 43.

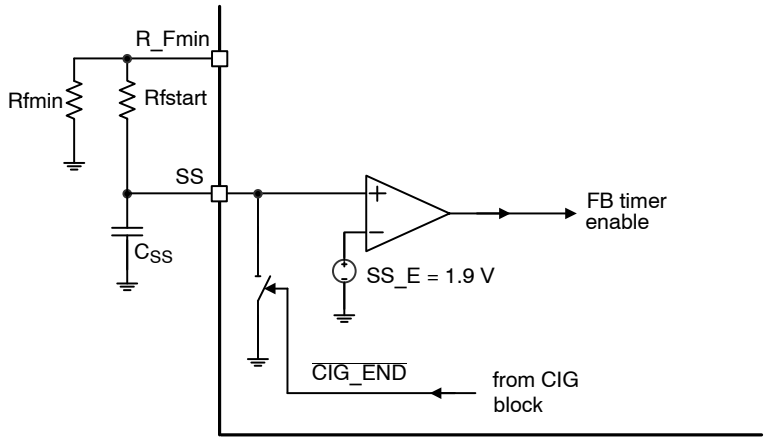


Figure 43. Soft−start Block Internal Connection

The soft−start capacitor is discharged by an internal switch before the soft−start period begins. The discharging path is released at the end of the CIG period. The switching frequency is then given by the parallel combination of resistors R_{fmin} and R_{fstart}. Since the soft−start capacitor charges from the R_Fmin reference voltage, via the R_{fstart} resistor, the current driven from the R_Fmin pin exponentially decreases, as does the switching frequency. In case the feedback path does not take control, the switching frequency will reach a value that is given by the R_{fmin} resistor. The feedback fault timer is disabled during the PFC delay, preheat, and soft−start periods in order to overcome unwanted controller operation interruption. This is accomplished by an internal comparator that monitors the soft−start capacitor voltage. The feedback fault timer is enabled when the soft−start capacitor voltage reaches 1.9 V. Please note that the soft−start sequence is activated after any controller restart. The PFC delay and preheat periods always precede the soft start action. The typical startup sequence of the DDA002C can be seen in Figure 44.

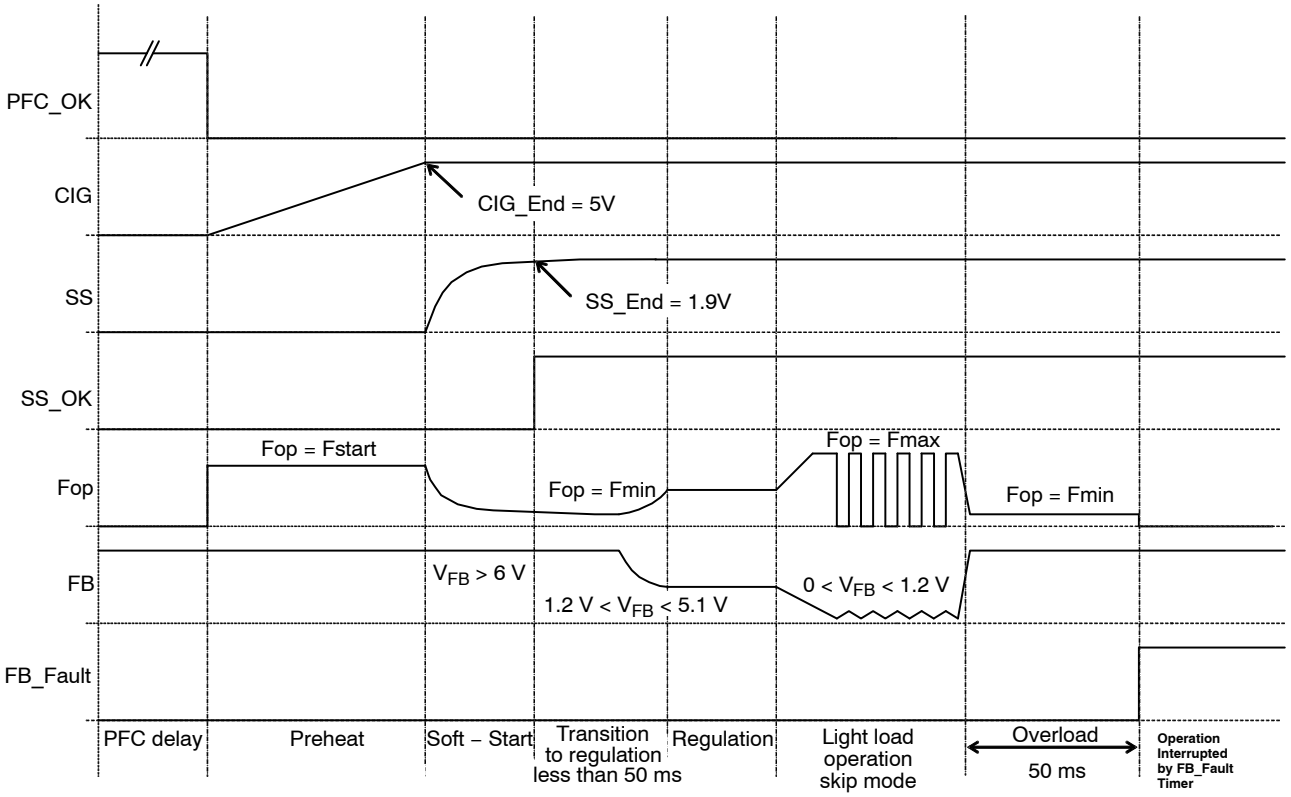


Figure 44. The IC Behavior under Various Operating Conditions

Brown−Out Protection

The Brown−Out circuitry (BO) offers a way to protect the application from low DC input voltages. The controller disables the output pulses if below a given level, if above it, it authorizes them. The internal circuitry, shown in Figure 45, offers a way to observe the high−voltage (HV) rail.

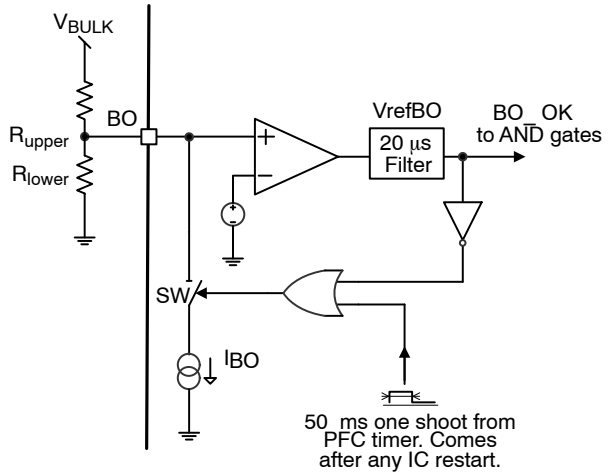


Figure 45. The Internal Brown−out Configuration with an Offset Current Sink

A resistive divider made of R_{upper} and R_{lower}, brings a portion of the HV rail on pin 1. The 20 μA current sink (IBO) is on if below the BO turn−on level. Therefore, the turn−on level is higher than the level given by the division ratio brought by the resistive divider. To the contrary, when the internal BO_OK signal is high, the IBO sink is deactivated. As a result, it becomes possible to select the turn−on and turn−off levels using the below equations:

IBO is On

$$V_{refBO} = V_{bulk1} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} - I_{BO} \cdot \left(\frac{R_{lower} \cdot R_{upper}}{R_{lower} + R_{upper}} \right) \quad \text{(eq. 2)}$$

IBO is Off

$$V_{refBO} = V_{bulk2} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} \quad \text{(eq. 3)}$$

We can extract R_{lower} from Equation 2 and plug it into Equation 1, then solve for R_{upper}:

$$R_{lower} = V_{refBO} \cdot \frac{V_{bulk1} - V_{bulk2}}{I_{BO} \cdot (V_{bulk2} - V_{refBO})} \quad \text{(eq. 4)}$$

$$R_{upper} = R_{lower} \cdot \frac{V_{bulk2} - V_{refBO}}{V_{refBO}} \quad \text{(eq. 5)}$$

If we decide to turn−on our converter for V_{bulk1} = 350 V and turn it off for V_{bulk2} = 250 V, then for I_{BO} = 20 μA and V_{refBO} = 1 V we obtain:

R_{upper} = 5 MΩ

R_{lower} = 20 kΩ

The bridge power dissipation is 400^2 / 5.02 * 1E06 = 32 mW when front−end PFC stage delivers 400 V. Figure 46 simulation result confirms our calculations.

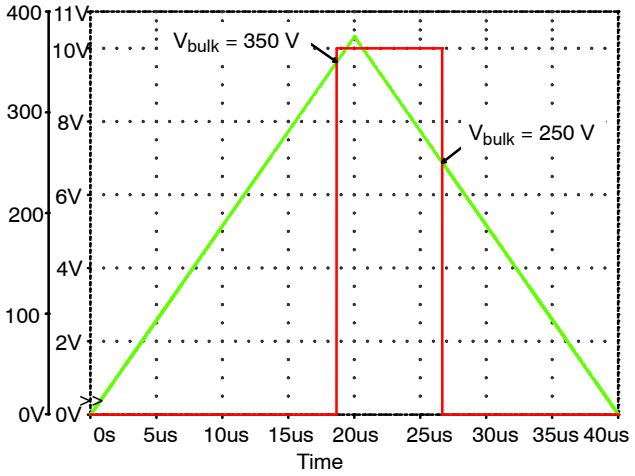


Figure 46. Simulation Results for 350/250 ON/OFF Brown Out Levels

Note that the brown−out input will disable the controller operation anytime its voltage goes below 1 V threshold. A 20 μs filter is used to improve the noise immunity of this input. The full start−up sequence (i.e. PFC delay, preheat and soft start) is provided by the controller in case the BO input is re−enabled.

The IBO current sink is turned ON for 50 ms after any controller restart to let the BO input voltage stabilize (big capacitor can be connected to the BO input and the I_{BO} is only 20 μA so it will take some time to discharge). Once the 50 ms one shoot pulse ends the BO comparator is supposed to either hold the I_{BO} sink turned ON (if the bulk voltage level is not sufficient) or turn it OFF (if the bulk voltage is higher than V_{bulk1}).

See Figures 47 − 50 for better understanding on how the BO input works.

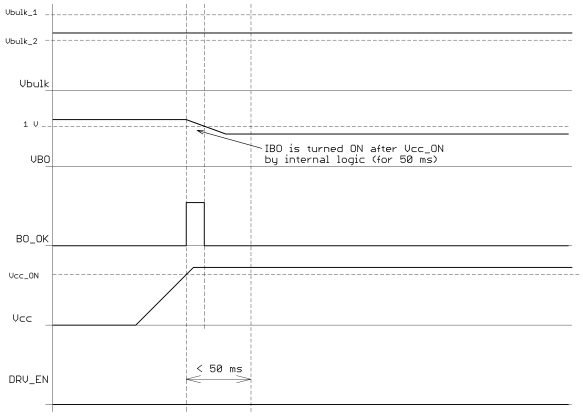


Figure 47. BO Input Functionality − $V_{bulk2} < V_{bulk} < V_{bulk1}$

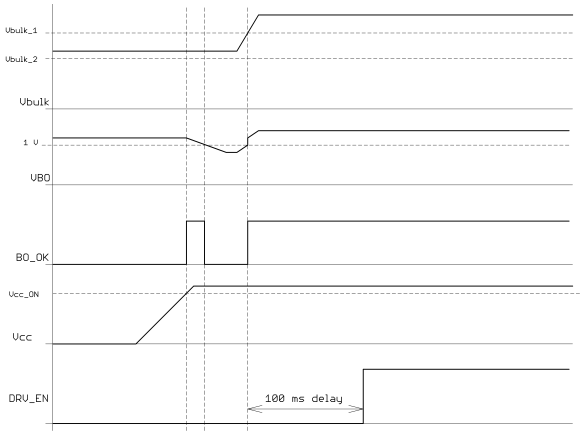


Figure 48. BO Input Functionality − $V_{bulk2} < V_{bulk} < V_{bulk1}$, PFC Start Follows

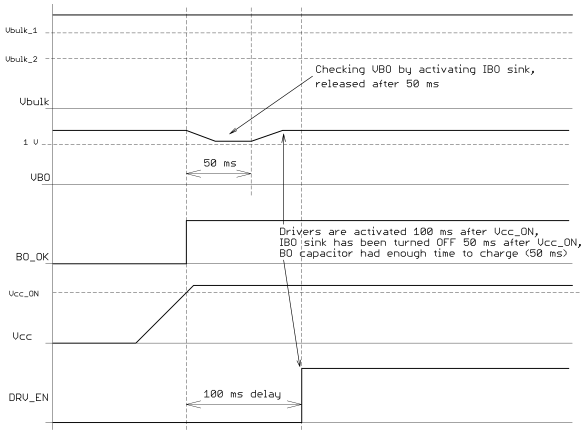


Figure 49. BO Input Functionality − $V_{bulk} > V_{bulk1}$

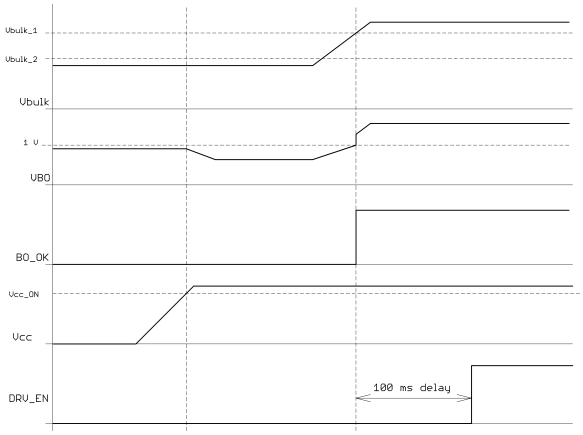


Figure 50. BO Input Functionality − $V_{bulk} < V_{bulk2}$, PFC Start Follows

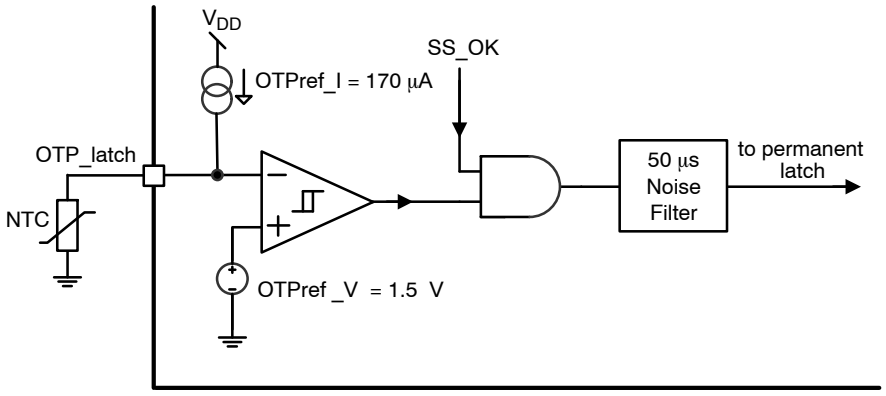


Figure 51. Internal Connection of the OTP Latch

OTP Latch

For most of the consumer electronic products there is a necessity to implement over temperature protection to comply with international standards. The DDA002C controller features special OTP Latch input that makes OTP implementation very easy and cheap since it does not require any active components. Connection of the OTP Latch can be seen in Figure 51.

The OTP_latch input permanently latches off the controller if the external NTC resistor resistance decreases below 8.8 kΩ (1.5 V). The temperature turn off threshold can be accurately adjusted using a serial or parallel resistor connected to the given NTC sensor. The OTP_latch input includes a 50 μs filter that improves noise immunity. Note that the OTP_latch input is ignored during the whole startup sequence (i.e. PFC delay, preheat and soft−start). When the latch is once asserted, the V_{CC} of the controller has to be decreased below the $V_{CC(min)}$ level or the BO comparator has to be re−triggered in order to restart the controller. Figure 54 shows typical operating waveforms of the OPT_latch input.

EN1 Input

The enable 1 input offers a way to permanently latch off the controller in case the critical operating conditions of the application are reached − such as over current or over voltage conditions. Since this is the latching input it includes 50 μs noise filter to overcome false triggering caused by the switching noise (pure grounding etc.). Internal connection of the EN1 comparator is depicted in Figure 52. Note that the enable 1 input functionality is disabled until preheat period ends.

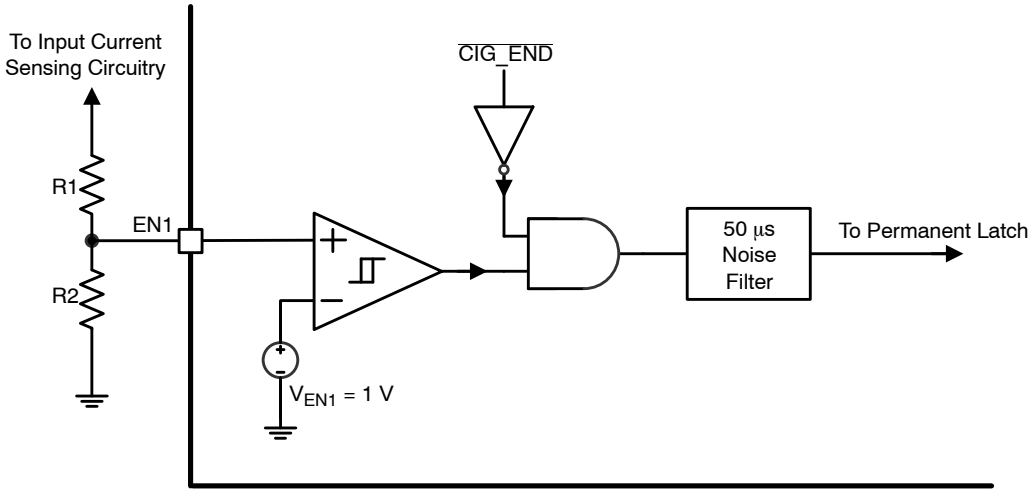


Figure 52. Internal Connection of the EN1 Comparator

The Enable 1 comparator features −50 mV hysteresis, which means that the EN1 input voltage has to go 50 mV below VEN1 reference voltage to allow the controller to restart. The controller can be restarted by two different events: 1st The V_{CC} is cycled down and up through the $V_{CC(off)}$ level, or 2nd, the BO input is re−triggered (i.e. bulk voltage is cycled down and up). Full start up sequence (PFC delay, preheat and soft−start) occurs when the controller restarts from EN1 latching event. Figure 53 shows the EN1 input related waveforms.

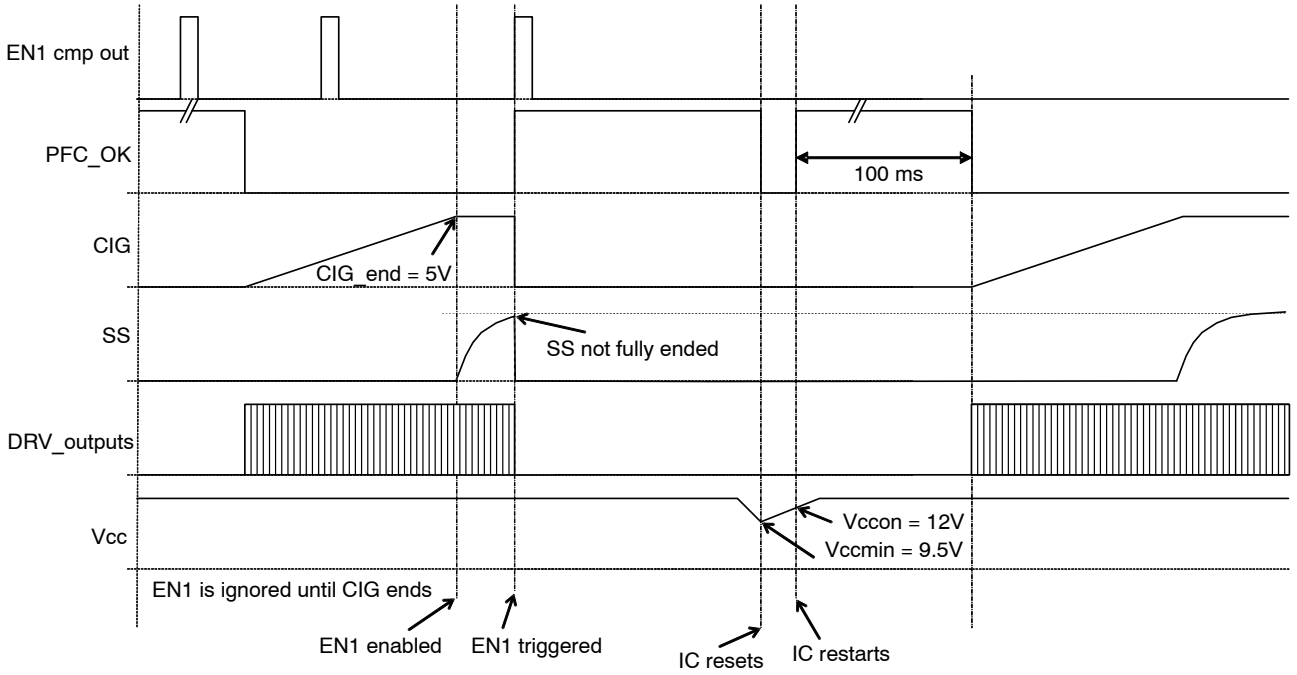


Figure 53. EN1 Input Functionality Description Waveforms − Vcc Restarted

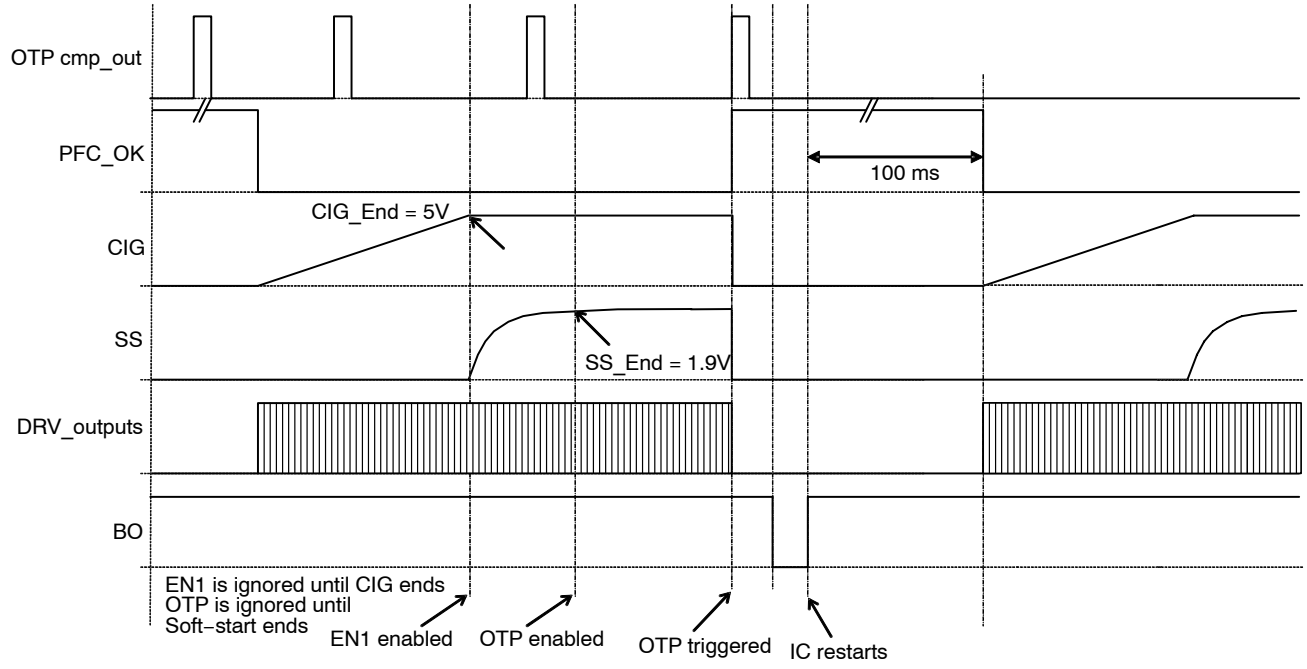


Figure 54. OTP Input Functionality Description Waveforms − BO Restarted

EN2 Input

This enable input is non−latched and thus can be used either for simple ON/OFF control or, because of its reaction time that is maximally 120 ns, as an ultra fast over current protection input. Connection of the EN 2 comparator can be seen in Figure 55. Functionality of this input is independent of any timers i.e. it works immediately when the VCC_{ON} threshold is reached.

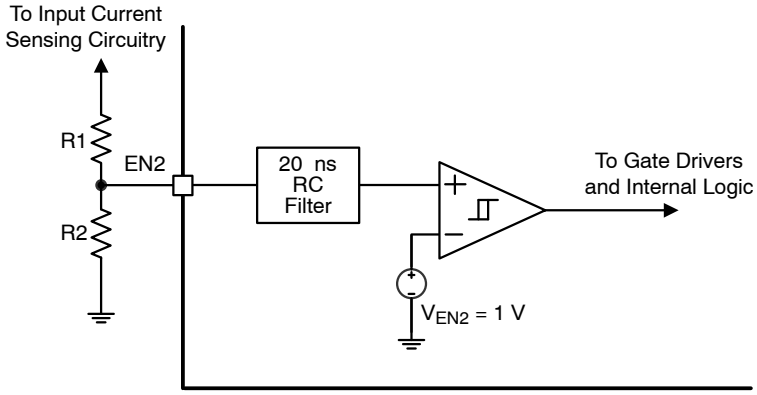


Figure 55. Internal Connection of the EN2 Comparator

The EN2 comparator incorporates −50 mV hysteresis − it means that the controller will restore operation via full start−up period (i.e. PFC delay, preheat and soft−start) when EN2 input voltage goes below VEN2−0.05 V. Figure 56 shows the EN2 input related operating waveforms.

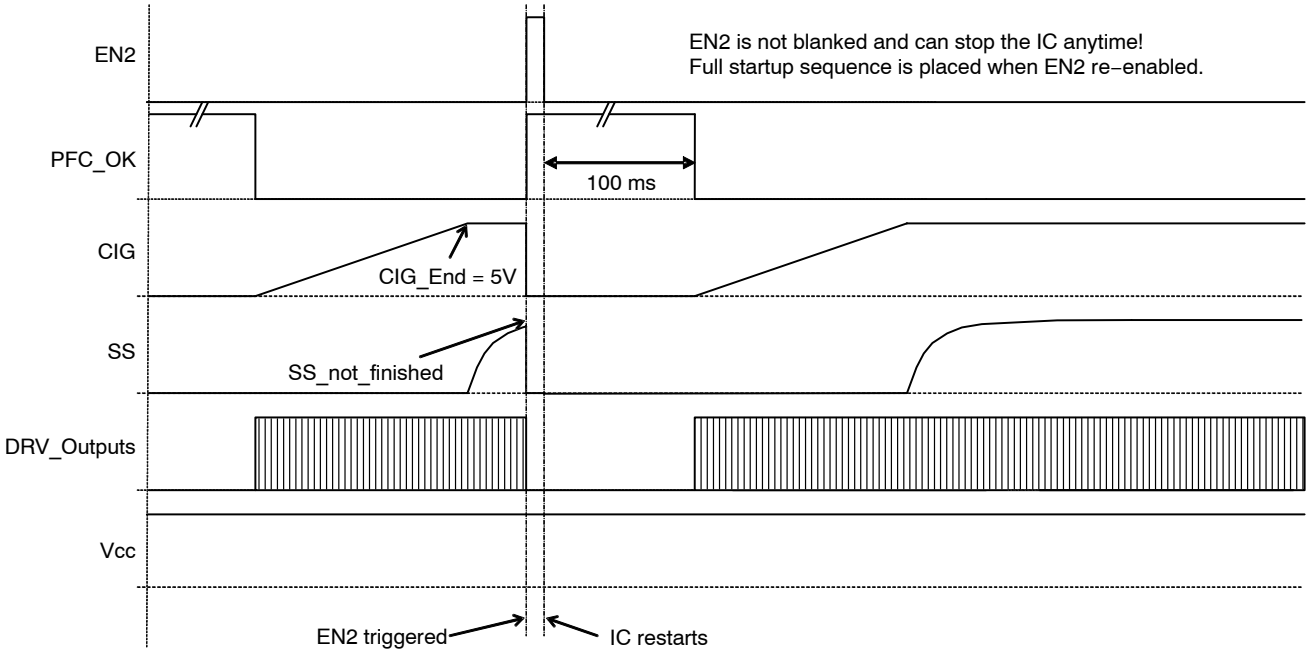


Figure 56. EN2 Input Functionality Description Waveforms

The High−voltage Driver

The controller features an internal high voltage driver that enables direct connection to the half bridge topologies. Figure 57 shows the internal architecture of the Lgd and Hgd drivers section. The device incorporates an upper UVLO circuitry that ensures adequate Vgs is available for the upper side MOSFET.

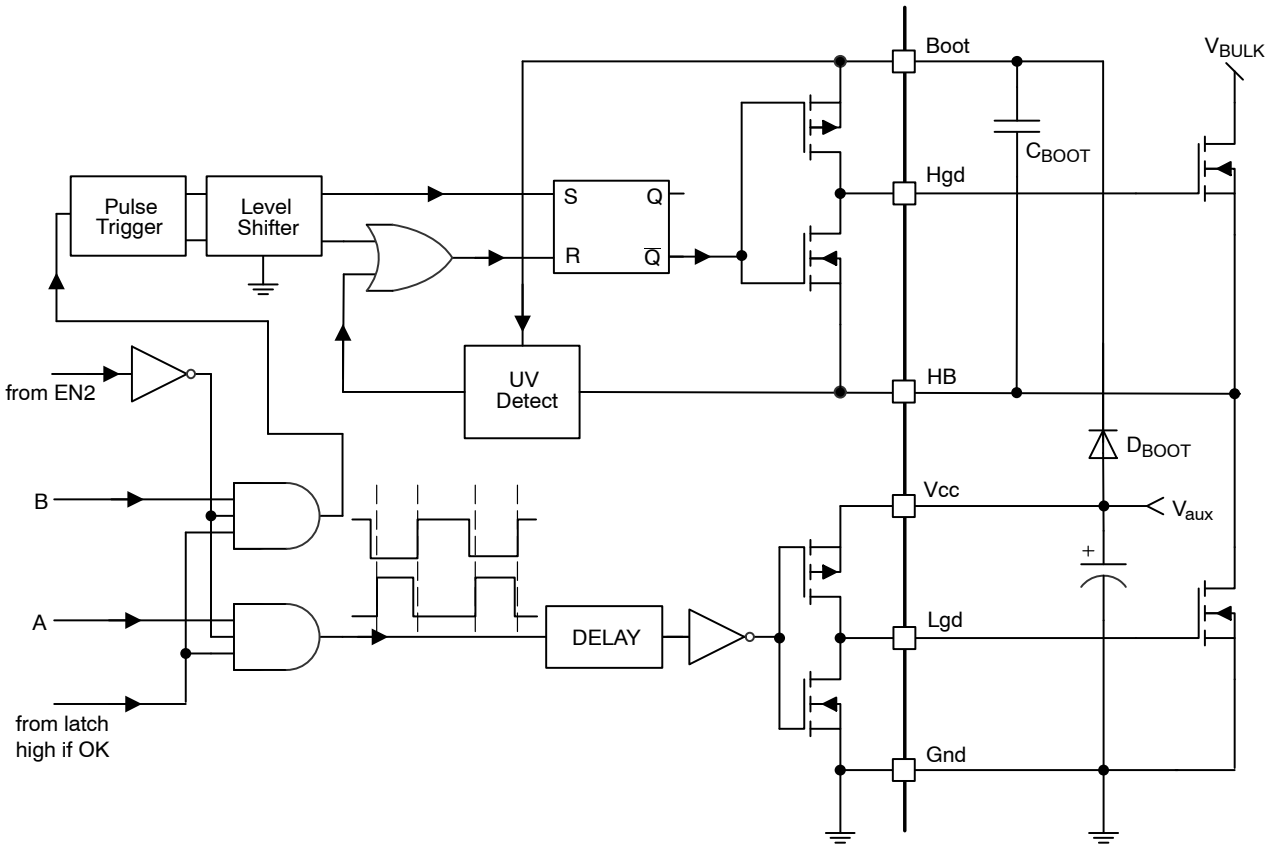


Figure 57. The Internal Lgd and Hgd Driver Section of the DDA002C

The A and B outputs are delivered by the internal logic, as depicted in VCO block diagram. This logic is constructed in such a way that the Lgd driver starts to pulse first after any controller restart. The bootstrap capacitor is thus charged during first pulse. A delay is included in the lower rail to ensure good matching between these propagating signals. As stated in the maximum rating section, the floating portion can go up to 600 VDC and makes the IC perfectly suitable for offline applications featuring a 400 V PFC front−end stage.

The Synchronization Outputs (Lgs and Hgs)

In addition to the power drivers, this IC features two ground referenced low power synchronization outputs that can be used to drive second power driver (in full bridge applications) or to trigger synchronous rectification circuitry via isolation transformer. On−time of the synchronization outputs can be easily clamped to needed value using a single resistor connected from the Dgs pin to ground. Maximum feasible on−time of the synchronization outputs is never higher than the on−time of the power outputs. Please refer to Figures 35 and 37 for more details on how the synchronization output signals are generated. The selection table for the Rdgs resistor that dictates the maximum on−time on the Lgs ang Hgs outputs can be seen in Figure 58.

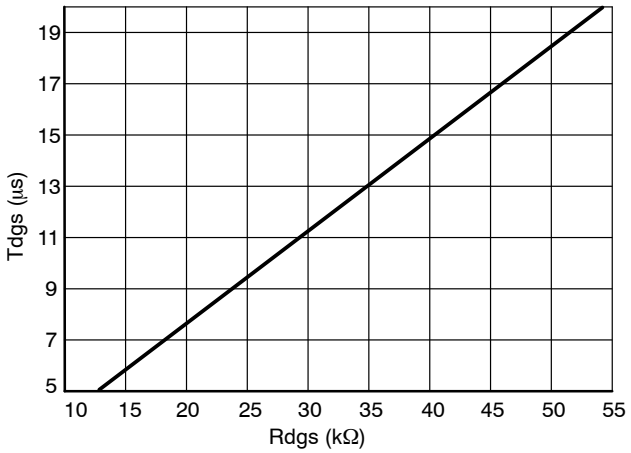


Figure 58. On Time Clamp Selection Chart

Layout Recommendations

The DDA002C contains sensitive inputs that uses high resistance resistors (depends on desired operating frequency range, deadtime and sync outputs on time clamp duration). Mentioned high impedance inputs can be sensitive to noise generated by HB and/or driver pins. Care thus has to be taken during SMPS layout design. Please refer to Figure 59 for recommended layout.

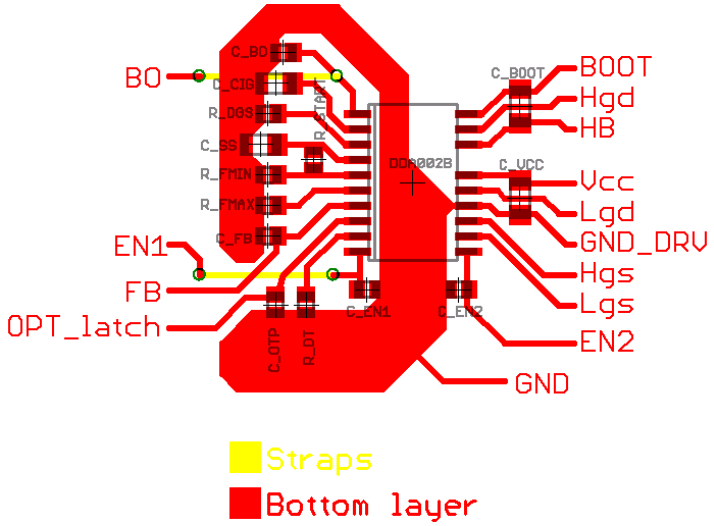


Figure 59. Recommended Layout for DDA002C Device

Maximum Substrate Charge Measurements

This chapter refers to Qmax parameter measurements. The DDA002C has been connected according to the Figure 60 during Qmax measurements. This connection allows measuring just only the substrate current that flows during the L1 demagnetization. Once the current is integrated one can get maximum charge that can flow to the substrate without causing device malfunction. Measurements didn't show that the Qmax depends on the operating frequency of the device. Measurements have been done for T_A = 125°C.

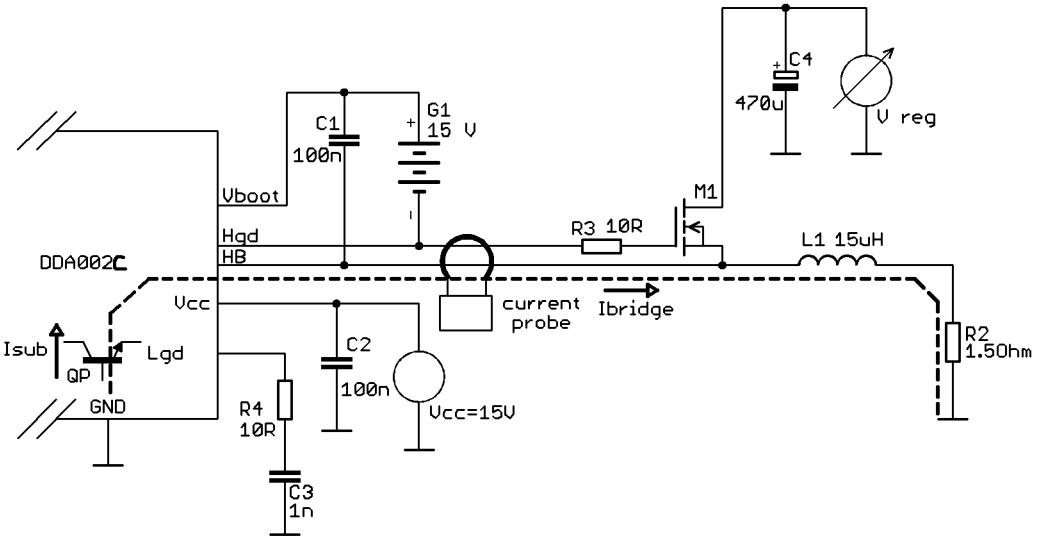


Figure 60. Substrate Injection Measurements Schematic

Ordering Information

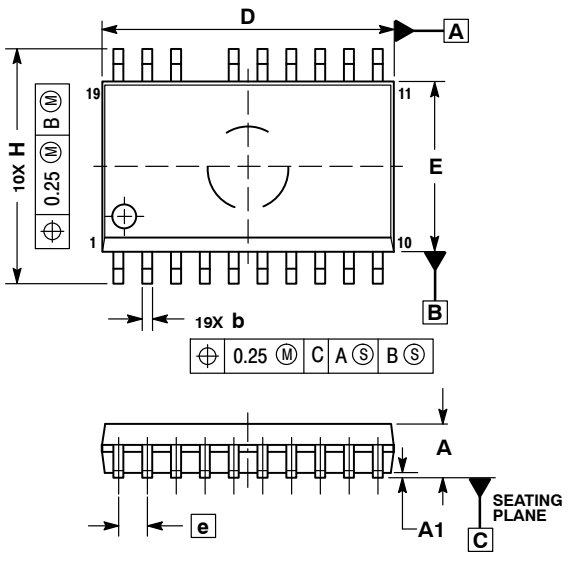
DELTA device	ON Semiconductor Device	Package	Shipping†
DDA002C	SCY99080CDWR2G	SOIC−19WB (Pb−Free)	1000 / Tape & Reel

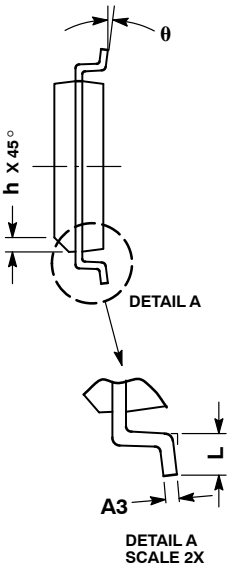
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

DDA002C

PACKAGE DIMENSIONS

SOIC20 WB LESS PIN 17 (SO−19)
CASE 752AA−01
ISSUE O

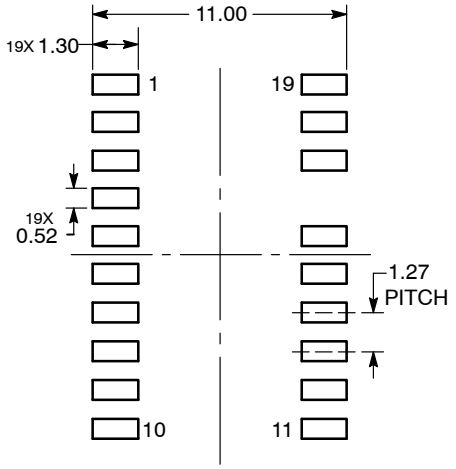




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
A3	0.23	0.32
b	0.35	0.49
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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