SONY

CXD3172AR

Signal Processor LSI for Single CCD Color Camera

Description

The CXD3172AR is a signal processor LSI for Ye, Cy, Mg and G single CCD color cameras. In addition to basic camera signal processing functions, it includes an AE/AWB detection circuit, a sync signal generation circuit and an external sync circuit, etc.

This chip also has a built-in microcontroller to realize basic camera functions such as AE/AWB without an external microcomputer.

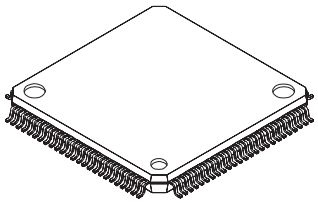
Features

- Generates timing pulses to drive the single CCD image sensor
  Built-in H/V driver for CCD image sensor
  Luminance/chroma signal processing
- Supports NTSC/PAL modes
- Supports 510H/760H system CCD image sensor
- Built-in 10-bit A/D converter
- Built-in EVR (3ch)
- Analog composite output
  — Built-in digital encoder
  — 10-bit D/A converter output
- Digital output
  — Conforms to ITU-REC656/ITU-REC601 format
- Supports external sync functions
  — Sync separation circuit
  — Phase comparator
- AE/AWB detector
- Block control functions with a built-in microcontroller
  — AE/AWB/CLAMP/Blemish detection and compensation
- Peripheral IC control function
  — EVR/EEPROM communication control
- Serial communication function (2 mode selection)
  — Microcomputer communication/start-stop synchronous system communication (RS232C)
- Auto blemish detection and compensation function
- Mirror function

Applications

- Industrial CCD cameras
  (Surveillance/FA/image input cameras)
- Multimedia CCD cameras
  (Teleconferencing/personal computer cameras)

100 pin LQFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	V_{DD}	V_{SS} – 0.5 to +4.6	V
	AVD	V_{SS} – 0.5 to +4.6	V
	VH	VL – 0.5 to VL + 26.0	V
	VM	VL – 0.5 to VL + 26.0	V
• Input voltage	V_I	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Output voltage	V_O	V_{SS} – 0.5 to V_{DD} + 0.5	V
• Operating Temperature			
	Topr	–20 to +75	°C
• Storage Temperature			
	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	V_{DD}	3.0 to 3.6	V
	AVD1, 3, 4, 5, 6		
		3.0 to 3.6	V
	AVD2	3.0 to 5.5	V
	VH	11.64 to 15.45	V
	VL	–7.5 to –4.5	V
	VM	0	V
• Operating Temperature			
	Topr	–20 to +75	°C

Applicable CCD Image Sensors*

- 510H color CCDs
  (Type 1/3, 1/4, NTSC/PAL)
- 760H color CCDs
  (Type 1/3, 1/4, NTSC/PAL)

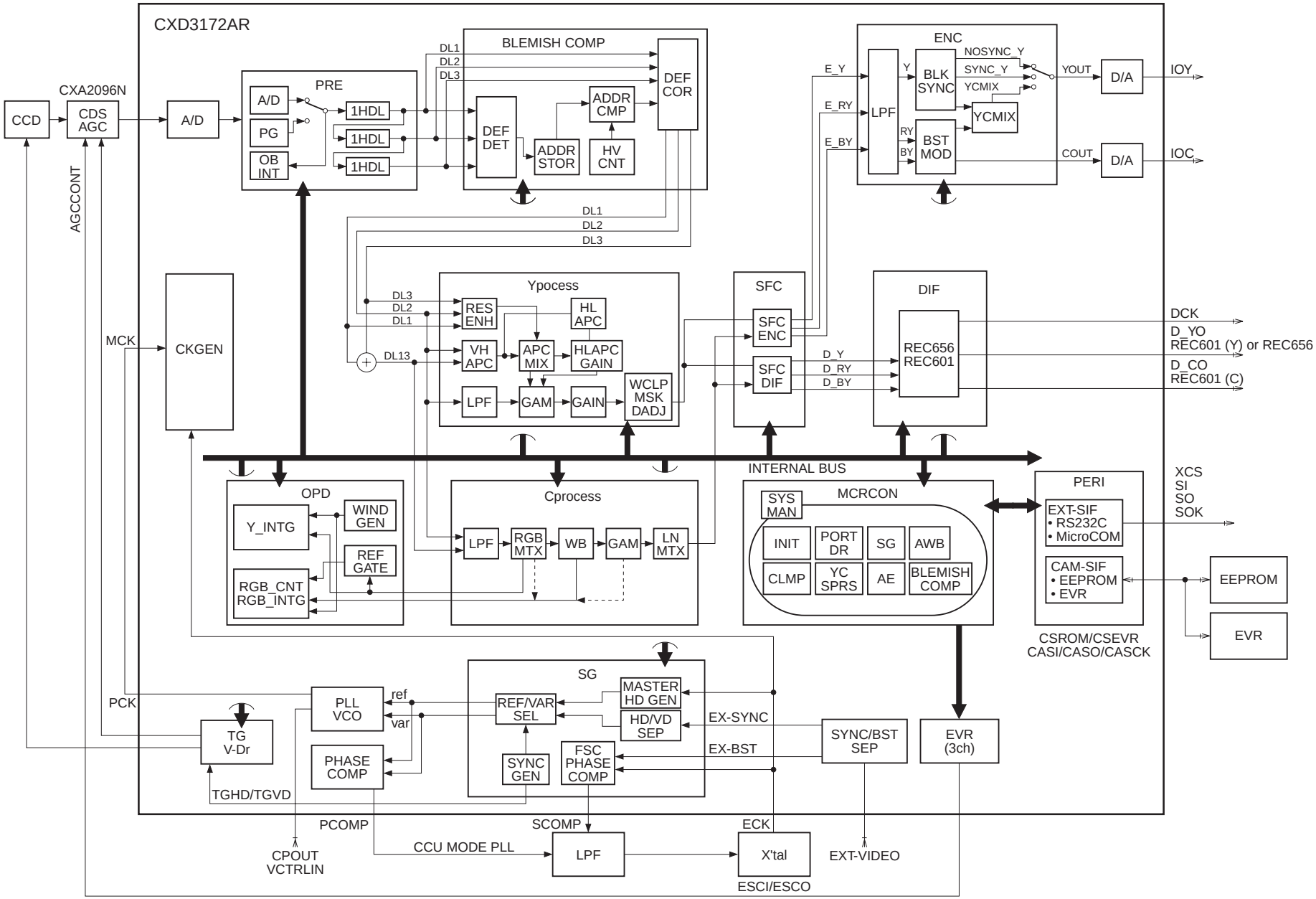
Supported Relates LSIs

AGC	CXA2096N
EVR	MB88347 (Fujitsu Limited.)
EEPROM	AK6480A (Asahi Kasei Microsystems Co.,Ltd.)
	BR9080A (ROHM)

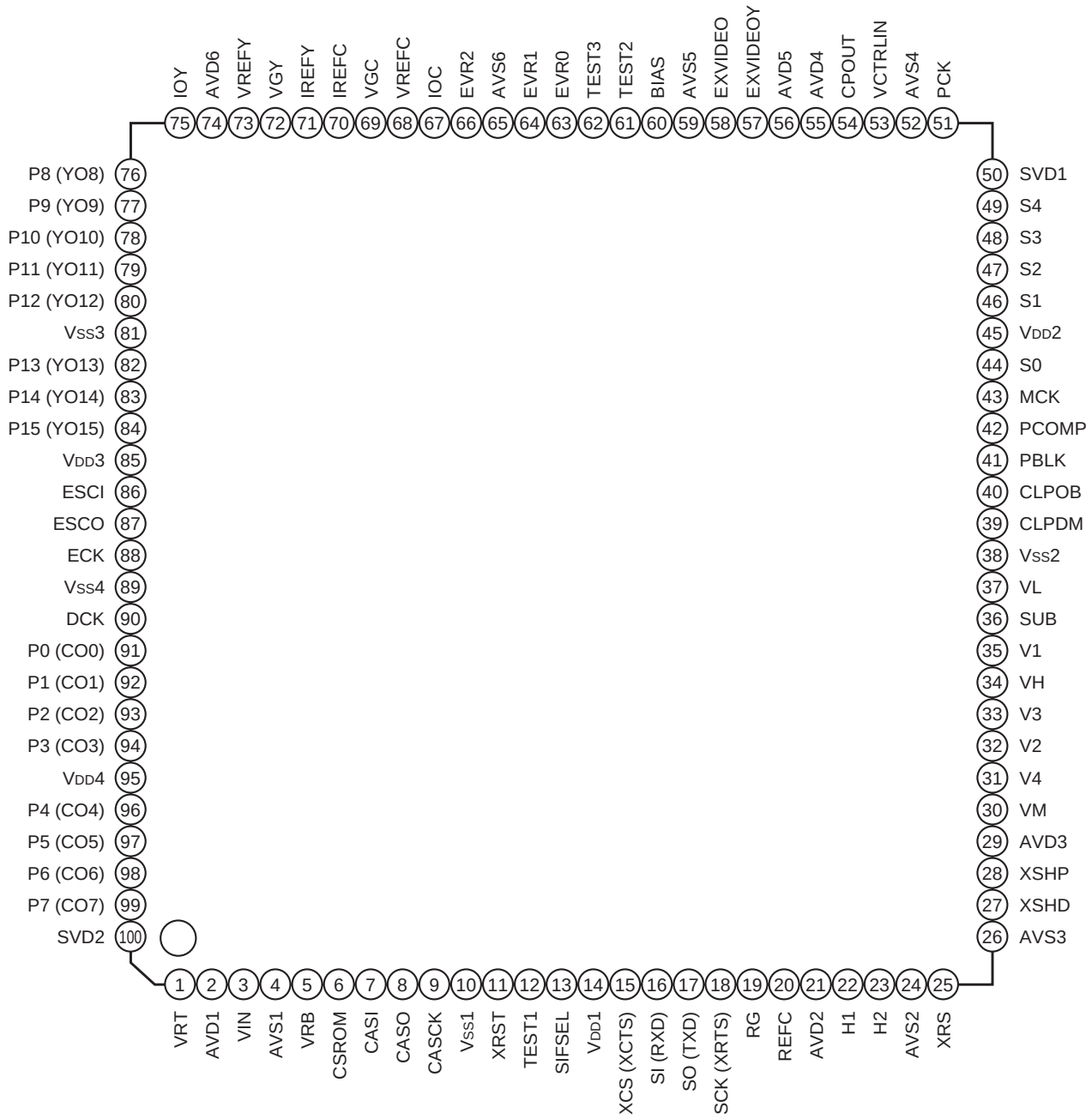
* Applicable CCD image sensors are applicable products as of preparing this data sheet. They may be changed according to the version up and production stop of CCD image sensor.

E04643-PS

Block Diagram



Pin Configuration



Note) Symbols in parentheses are the signal names when the function is switched by the communication parameter settings.

Pin Description

Pin No.	Symbol	I/O	Description	Power supply
1	VRT	I	A/D converter reference voltage (top) input.	AVD1 AVS1
2	AVD1	—	Power supply for A/D converter.	
3	VIN	I	Analog signal input. (for A/D converter)	
4	AVS1	—	GND	
5	VRB	I	A/D converter reference voltage (bottom) input.	
6	CSROM	O	Chip select output for camera peripheral ICs. (to EEPROM)	$V_{DD}1$ $V_{SS}1$
7	CASI	I	Serial data input for system communication.	
8	CASO	O	Serial data output for system communication.	
9	CASCK	O	Serial clock output for system communication.	
10	$V_{SS}1$	—	GND	
11	XRST	I	Reset input.	
12	TEST1	I	Test	
13	SIFSEL	I	Serial interface mode switching. 0: microcomputer (3 wires) 1: RS232C	
14	$V_{DD}1$	—	Power supply for logic.	
15	XCS	I	Chip select input for 3 wires serial interface. (Clear to Send)	
16	SI	I	Serial data input for 3 wires serial interface. (Received Data)	
17	SO	O	Serial data output for 3 wires serial interface. (Transmitted Data)	
18	SCK	I (O)	Serial clock input for 3 wires serial interface. (Request to Send)	
19	RG	O	Reset gate pulse output.	AVD2 AVS2
20	REFC	I	Capacitor connection.	
21	AVD2	—	Power supply for horizontal driving pulse. (3.3V/5.0V)	
22	H1	O	CCD horizontal register transfer pulse output.	
23	H2	O	CCD horizontal register transfer pulse output.	
24	AVS2	—	GND	
25	XRS	O	Resampling pulse output.	AVD3 AVS3
26	AVS3	—	GND	
27	XSHD	O	Data sample-and-hold pulse output.	
28	XSHP	O	Precharge level sample-and-hold pulse output.	
29	AVD3	—	Power supply for sample-and-hold pulse.	
30	VM	—	V-Driver Middle level power supply.	VH VL VM
31	V4	O	CCD vertical register transfer pulse output.	
32	V2	O	CCD vertical register transfer pulse output.	
33	V3	O	CCD vertical register transfer pulse output.	
34	VH	—	V-Driver High level power supply.	
35	V1	O	CCD vertical register transfer pulse output.	
36	SUB	O	CCD electronic shutter pulse output.	
37	VL	—	V-Driver Low level power supply.	

Pin No.	Symbol	I/O	Description	Power supply
38	$V_{SS}2$	—	GND	$V_{DD}2$ $V_{SS}2$
39	CLPDM	O	Dummy data clamp pulse output.	
40	CLPOB	O	Optical black clamp pulse output.	
41	PBLK	O	Preblanking pulse output.	
42	PCOMP	O	Phase comparator output.	
43	MCK	I	System drive clock input.	
44	S0	I/O	Sync signal input/output 0.	
45	$V_{DD}2$	—	Power supply for logic.	
46	S1	I/O	Sync signal input/output 1.	
47	S2	I/O	Sync signal input/output 2.	
48	S3	I/O	Sync signal input/output 3.	
49	S4	O	Sync signal output.	
50	SVD1	—	Sub power supply.	
51	PCK	O	PLL clock output.	
52	AVS4	—	GND	AVD4 AVS4
53	VCTRLIN	I	Built-in VCO input.	
54	CPOUT	O	Built-in charge pump output.	
55	AVD4	—	Analog power supply for PLL.	
56	AVD5	—	Power supply for burst separator.	AVD5 AVS5
57	EXVIDEOY	I	Y signal input for external synchronization.	
58	EXVIDEO	I	Video signal input for external synchronization.	
59	AVS5	—	GND	
60	BIAS	I	Bias current source.	AVD6 AVS6
61	TEST2	I	Test	
62	TEST3	I	Test	
63	EVR0	O	EVR0 analog output.	
64	EVR1	O	EVR1 analog output.	
65	AVS6	—	GND	
66	EVR2	O	EVR2 analog output.	
67	IOC	O	Analog chroma output.	
68	VREFC	I	Reference voltage setting. (for chroma signal D/A converter)	
69	VGC	I	Capacitor connection. (approx. 0.1µF) (for chroma signal D/A converter)	
70	IREFC	I	Reference current setting. (for chroma signal D/A converter)	
71	IREFY	I	Reference current setting. (for luminance signal D/A converter)	
72	VGY	I	Capacitor connection. (approx. 0.1µF) (for luminance signal D/A converter)	
73	VREFY	I	Reference voltage setting. (for luminance signal D/A converter)	
74	AVD6	—	Power supply for DA converter/EVR.	
75	IOY	O	Analog Y output/compostite video output.	

Pin No.	Symbol	I/O	Description	Power supply
76	P8 (YO8)	I/O	Port 8 input or Y digital signal output or YUV digital signal output.	$V_{DD}3$ $V_{SS}3$
77	P9 (YO9)	I/O	Port 9 input or Y digital signal outout or YUV digital signal output.	
78	P10 (YO10)	I/O	Port 10 input or Y digital signal outout or YUV digital signal output.	
79	P11 (YO11)	I/O	Port 11 input or Y digital signal outout or YUV digital signal output.	
80	P12 (YO12)	I/O	Port 12 input or Y digital signal outout or YUV digital signal output.	
81	$V_{SS}3$	—	GND	
82	P13 (YO13)	I/O	Port 13 input or Y digital signal outout or YUV digital signal output.	
83	P14 (YO14)	I/O	Port 14 input or Y digital signal outout or YUV digital signal output.	
84	P15 (YO15)	I/O	Port 15 input or Y digital signal outout or YUV digital signal output.	
85	$V_{DD}3$	—	Power supply.	
86	ESCI	I	Oscillation cell input.	
87	ESCO	O	Oscillaton cell output.	
88	ECK	I	Encoder clock input.	
89	$V_{SS}4$	—	GND	$V_{DD}4$ $V_{SS}4$
90	DCK	O	Clock output for digital output.	
91	P0 (CO0)	I/O	Port 0 input or C digital signal output.	
92	P1 (CO1)	I/O	Port 1 input or C digital signal output.	
93	P2 (CO2)	I/O	Port 2 input or C digital signal output.	
94	P3 (CO3)	I/O	Port 3 input or C digital siganl output	
95	$V_{DD}4$	—	Power supply.	
96	P4 (CO4)	I/O	Port 4 input or C digital signal output or EEEPROM BUSY signal input or OPD frame pulse output.	
97	P5 (CO5)	I/O	Port 5 input or C digital signal output or VD output.	
98	P6 (CO6)	I/O	Port 6 input or C digital signal output or HD output.	
99	P7 (CO7)	I/O	Port 7 input or C digital signal output.	
100	SVD2	—	Sub power supply.	

Electrical Characteristics

DC Characteristics

(Within recommended operating range)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage 1	V_{DD}1, 2, 3, 4		3.0	3.3	3.6	V
	AVD1	A/D input amplitude = 1Vp-p	3.0	3.3	3.6	V
	AVD2		3.0	—	5.5	V
	AVD3, 4, 5		3.0	3.3	3.6	V
	AVD6	D/A output amplitude = 1Vp-p	3.0	3.3	3.6	V
Supply voltage 2	SVD1, 2		—	3.3	—	V
Supply voltage 3	VH		11.64	—	15.45	V
	VL		–7.5	—	–4.5	V
	VM		—	0	—	V
Output voltage 1	V_{OH}1 *1	I_{OH} = 1.0mA	V_{DD} – 0.4			V
	V_{OL}1 *1	I_{OL} = 1.0mA			0.4	V
Output voltage 2	V_{OH}2 *2, *3	I_{OH} = 4.0mA	V_{DD} – 0.4			V
	V_{OL}2 *2, *3	I_{OL} = 4.0mA			0.4	V
Output voltage 3	V_{OH}3 *4	I_{OH} = 12.0mA	V_{DD}/2			V
	V_{OL}3 *4	I_{OL} = 12.0mA			V_{DD}/2	V
Output voltage 4	V_{OH}4 *5	I_{OH} = 4.0mA	VH – 0.25			V
	V_{OL}4 *5	I_{OL} = 5.4mA			VL + 0.25	V
Output voltage 5	V_{OH}5 *6	I_{OH} = 5.0mA	VM – 0.25			V
	V_{OL}5 *6	I_{OL} = 10.0mA			VL + 0.25	V
Output voltage 6	V_{OH}6 *7	I_{OH} = 7.2mA	VH – 0.25			V
	V_{OM}61 *7	I_{OL} = 5.0mA			VM + 0.25	V
	V_{OM}62 *7	I_{OH} = 5.0mA	VM – 0.25			V
	V_{OL}6 *7	I_{OL} = 10.0mA			VL + 0.25	V
Input voltage	V_{T}+ *1, *3, *8		0.7V_{DD}			V
	V_{T}– *1, *3, *8				0.2V_{DD}	V
Hysteresis	V_{T}+ – V_{T}– *1, *3, *8			0.5		V
Input leak current	I_{IH} *8	V_{IN} = V_{DD}	40	100	240	µA

*1 S0, S1, S2, S3, P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15

*2 CSROM, CASO, CASCK, SO, CLPDM, CLPOB, PBLK, S4, PCK, DCK

*3 SCK

*4 ESCI, ESCO

*5 SUB

*6 V2, V4

*7 V1, V3

*8 CASI, XRST, SIFSEL, XCS, SI, TEST2, TEST3

*9 TEST1

I/O Pin Capacitance (V_{DD} = V_I = 0V, f = 1MHz)

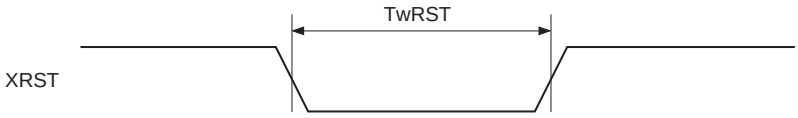
Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance	C_{IN}			9	pF
Output pin capacitance	C_{OUT}			11	pF
I/O pin capacitance	$C_{I/O}$			11	pF

AC Characteristics (Within recommended operating range)

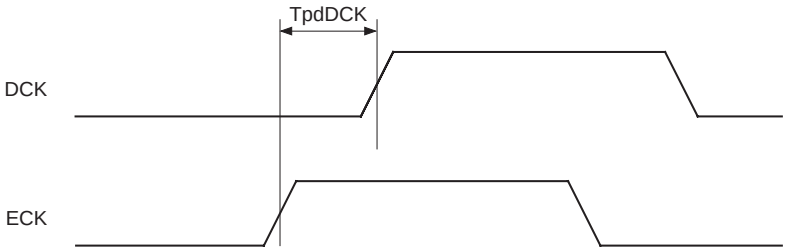
Classification	Item	Symbol	Min.	Typ.	Max.	Unit
Reset input	Min. low time of reset operation of XRST pin	TwRST	500	—	—	ns
Digital output	P0 to P15 output delay time against DCK ↑	TpdP	5	—	20	ns
	S0 output delay time against DCK ↑	TpdS0	6	—	28	ns
	S1 output delay time against DCK ↑	TpdS1	6	—	30	ns
	DCK output delay time against ECK ↑	TpdDCK	7	—	24	ns
SYNC block sync output	HD, VD, FLD and SYNC output delay time against ECK ↑	TpdSY	10	—	45	ns
Serial communication I/O	SCK input pulse width (High period)	TwHSCK	—	580	—	ns
	SCK input pulse width (Low period)	TwLSCK	—	580	—	ns
	XCE input setup time against SCK ↓	TsuXCE	580	—	—	ns
	XCE input hold time against SCK ↑	ThXCE	580	—	—	ns
	SI input setup time against SCK ↑	TsuSI	0	—	—	ns
	SI input hold time against SCK ↑	ThSI	0	—	—	ns
	SO output transit time against XCE ↓ (Hi-Z → Data active)	TzdSO	0	—	—	ns
	SO transit time against XCE ↑ (Data active → Hi-Z)	TdzSO	0	—	—	ns
	SO output delay time against SCK ↓	TpdSO	—	—	580	ns

AC Characteristics diagram

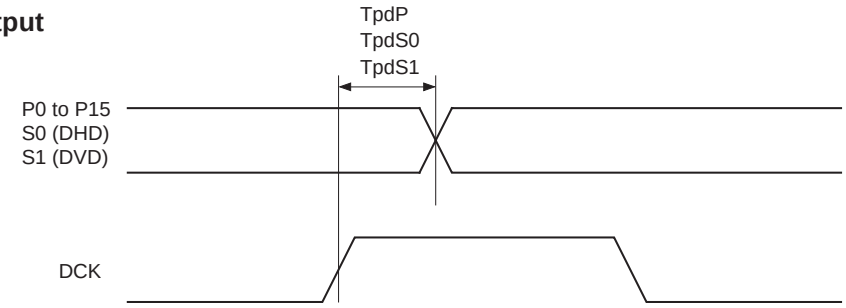
1. Reset input



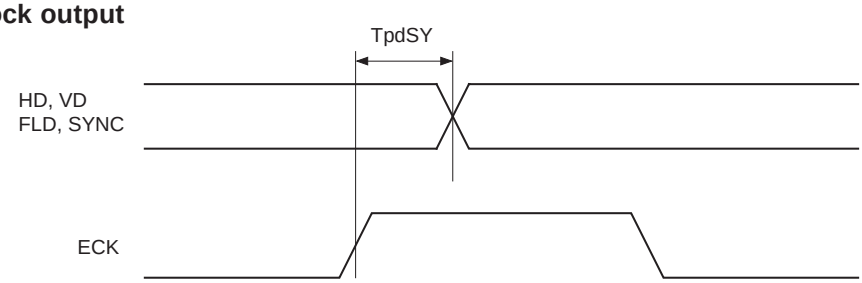
2. DCK output



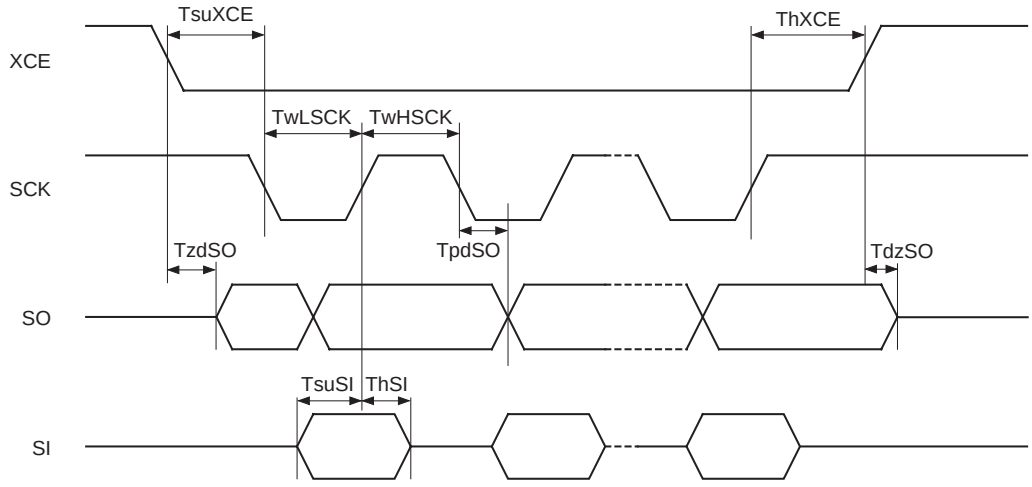
3. Digital output



4. SYNC block output



5. Serial communication I/O



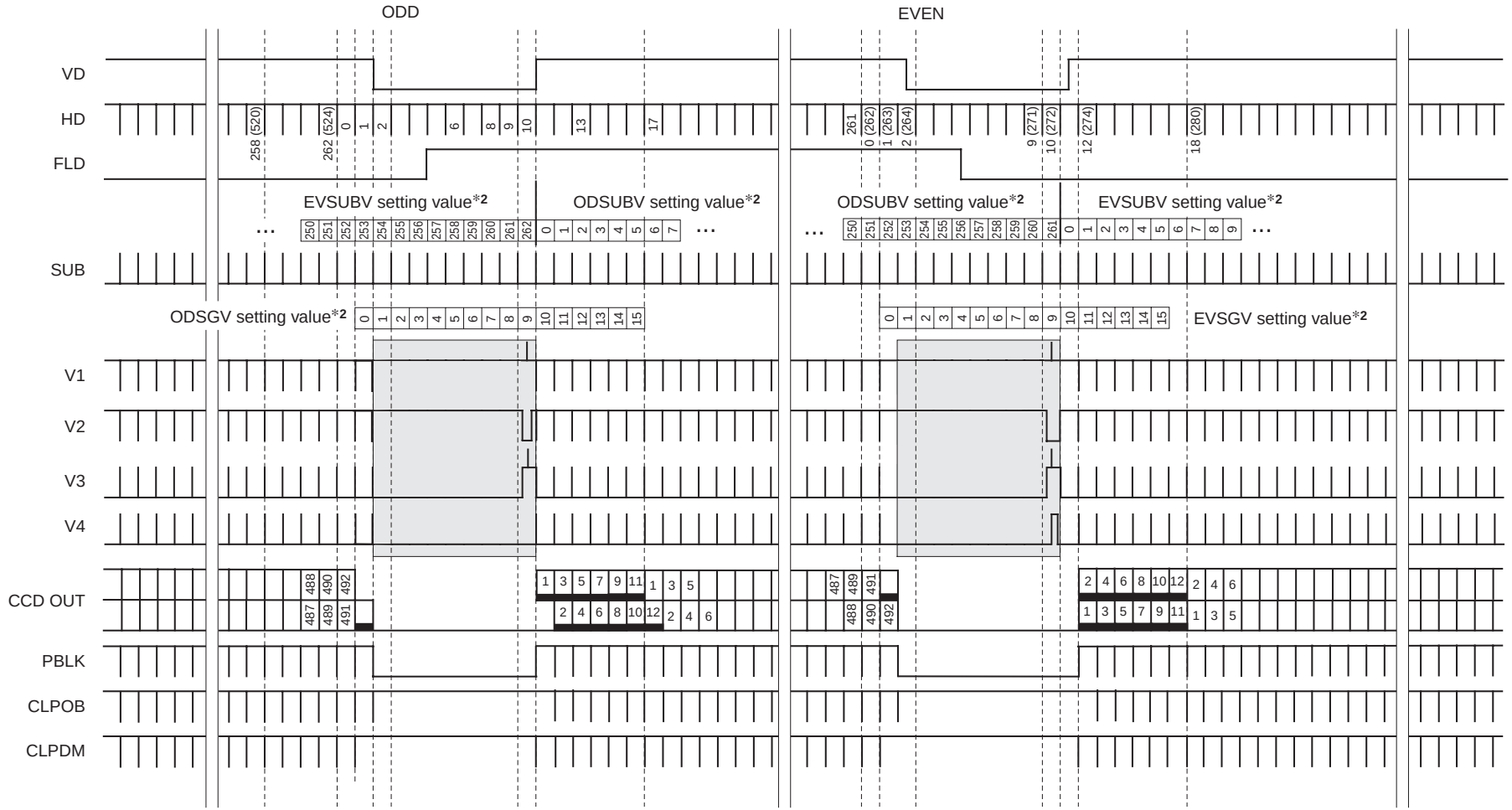
Relationship between MODESEL and Each Clock

TV system	CCD type	MODESEL	ECK	MCK	DSPCK∗1	Remarks
NTSC	510H	0	38.13986MHz	(ECK = MCK)	MCK/4	ECK and MCK are connected internally.
		1	28.63636MHz	38.13986MHz		
		2	27.00000MHz			
	760H	6	28.63636MHz	(ECK = MCK)	MCK/2	ECK and MCK are connected internally.
		8	27.00000MHz	28.63636MHz		
PAL	510H	3	37.87500MHz	(ECK = MCK)	MCK/4	ECK and MCK are connected internally.
		4	35.46895MHz	37.87500MHz		
		5	27.00000MHz			
	760H	9	28.37500MHz	(ECK = MCK)	MCK/2	ECK and MCK are connected internally.
		A	35.46895MHz	28.37500MHz		
		B	27.00000MHz			

∗1 DSPCK: clock which is not output by external pins
See the above table for the relationship between encoder clock (ECK) and system drive clock (MCK).

Vertical Timing Chart MODESEL 0, 1, 2 [510H NTSC]

Applicable CCD image sensor:
ICX206AK/226AK/254AK/404AK

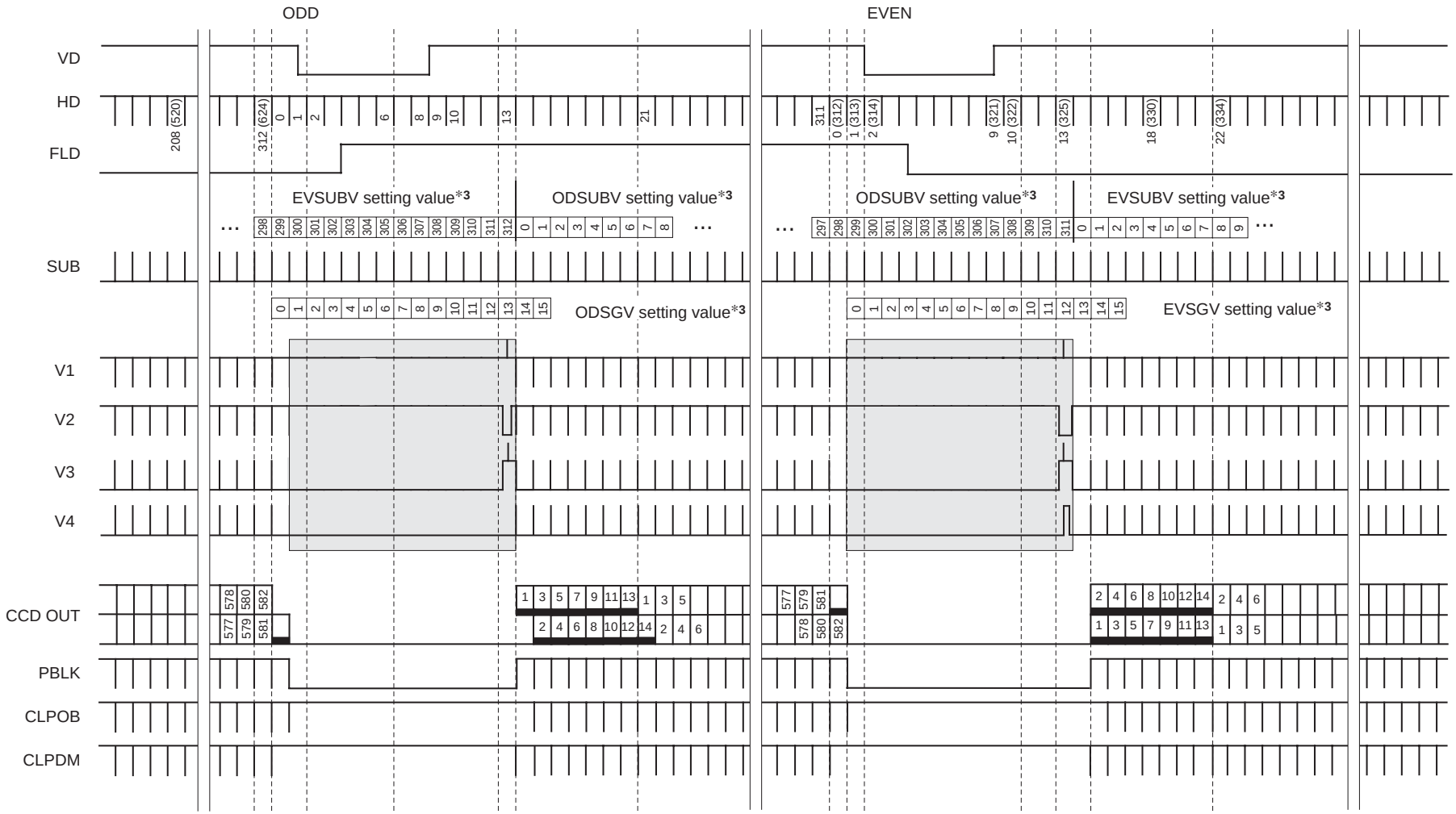


The shaded area shows the position variable range of the read SG pulse. However, note that the range may over depending on the setting.

*2 The value changes by the parameter (Category6: TG) setting.

Vertical Timing Chart MODESEL 3, 4, 5 [510H PAL]

Applicable CCD image sensor:
ICX207AK/227AK/255AK/405AK

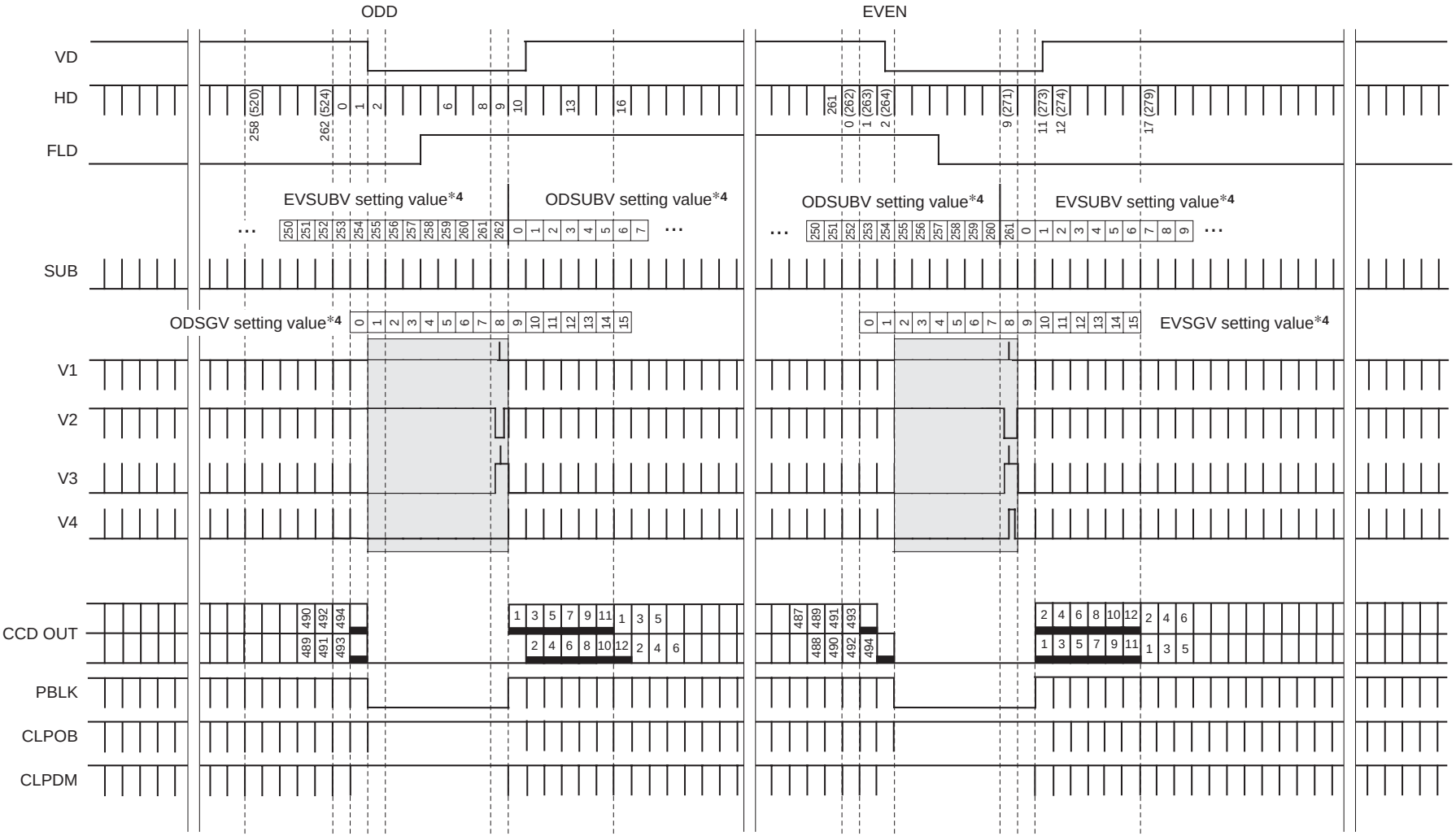


The shaded area shows the position variable range of the read SG pulse. However, note that the range may over depending on the setting.

*3 The value changes by the parameter (Category6: TG) setting.

Vertical Timing Chart **MODESEL 6, 8 [760H NTSC]**

Applicable CCD image sensor:
ICX228AK/258AK/278AK/408AK

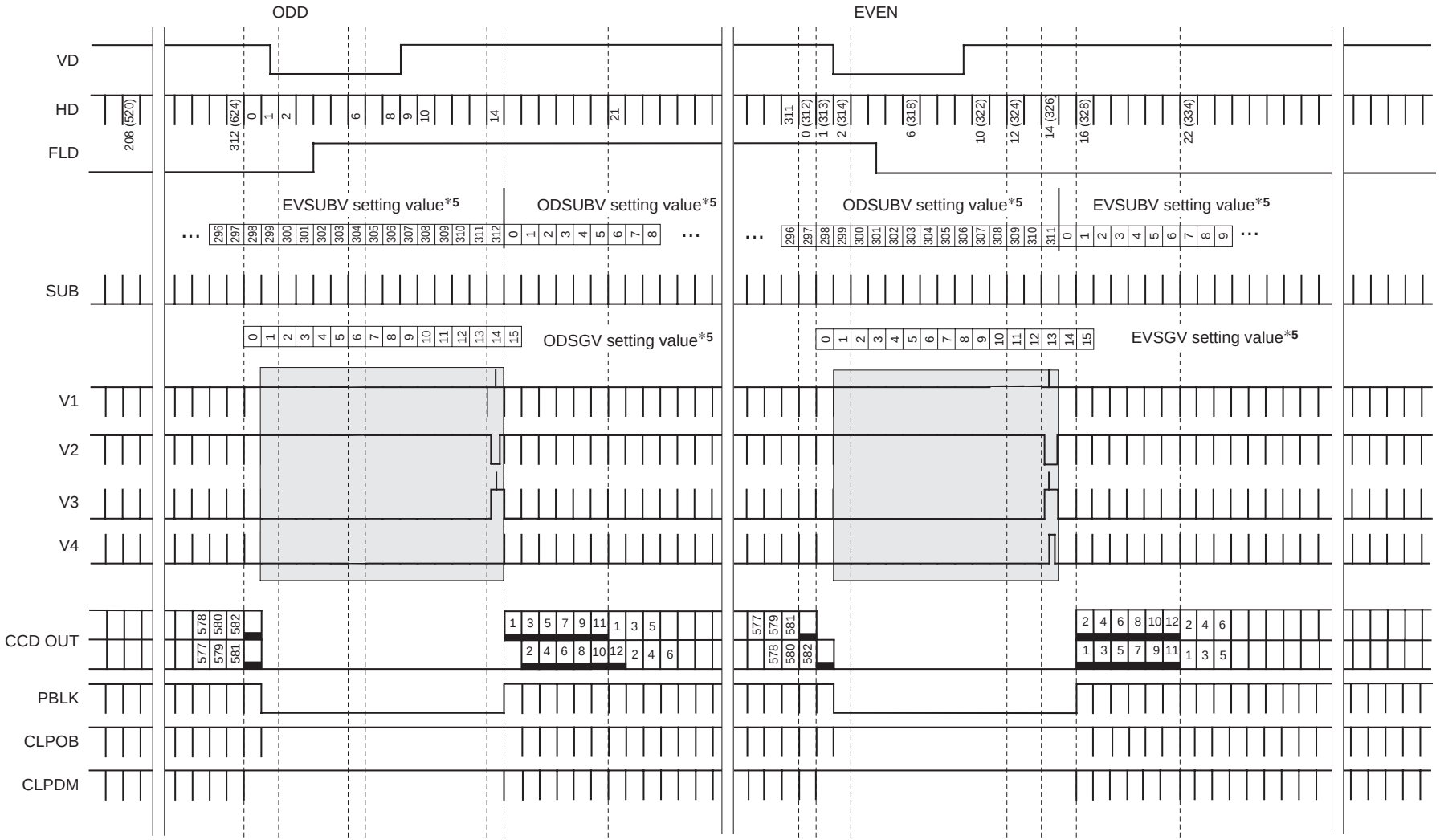


The shaded area shows the position variable range of the read SG pulse. However, note that the range may over depending on the setting.

*4 The value changes by the parameter (Category6: TG) setting.

Vertical Timing Chart MODESEL 9, A, B [760H PAL]

Applicable CCD image sensor:
ICX229AK/259AK/279AK/409AK

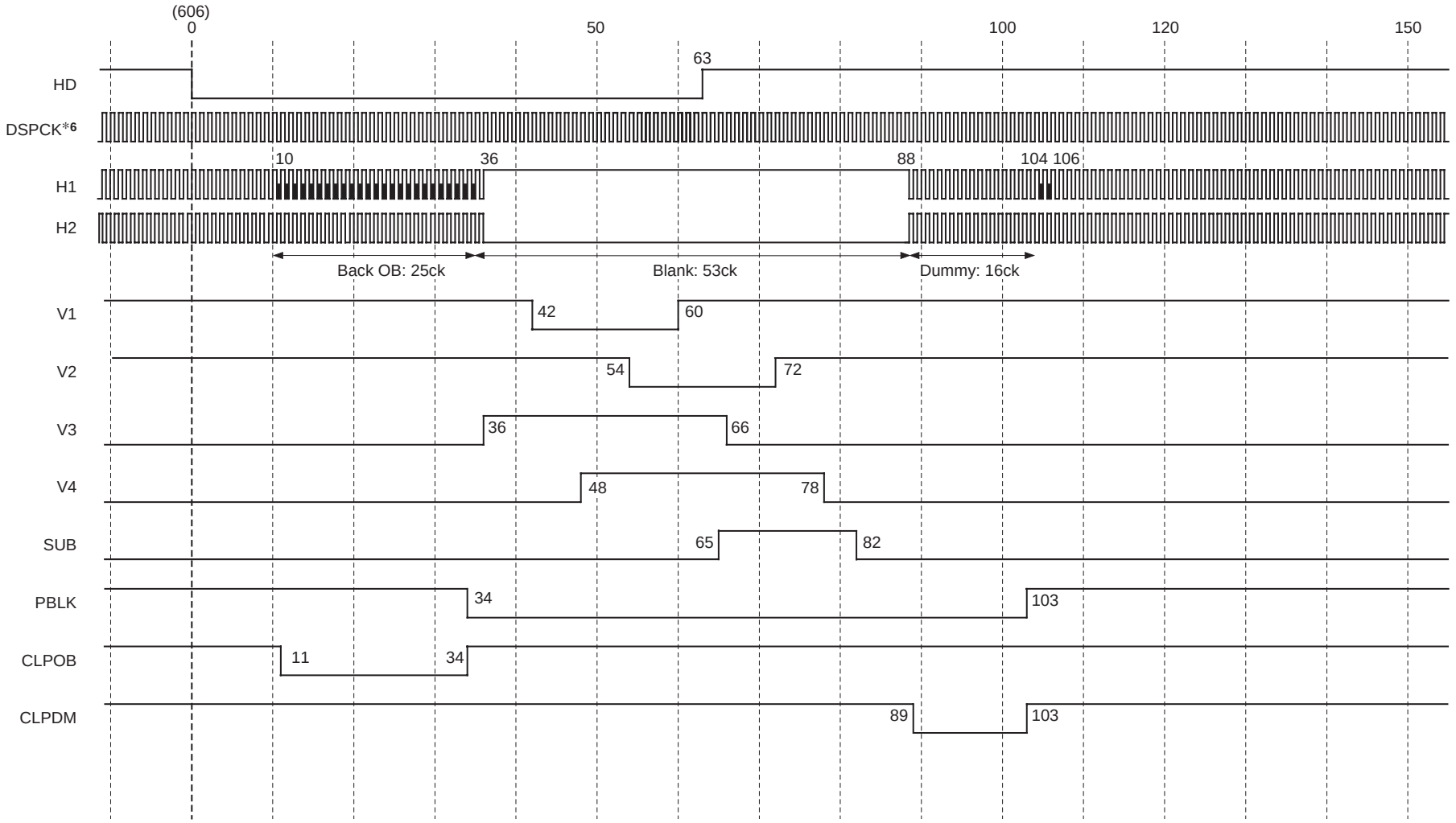


The shaded area shows the position variable range of the read SG pulse. However, note that the range may over depending on the setting.

*5 The value changes by the parameter (Category6: TG) setting.

Horizontal Timing Chart **MODESEL 0, 1, 2 [510H NTSC]** **DSPCK: 606f_H (9.534965MHz: 104.88ns)**

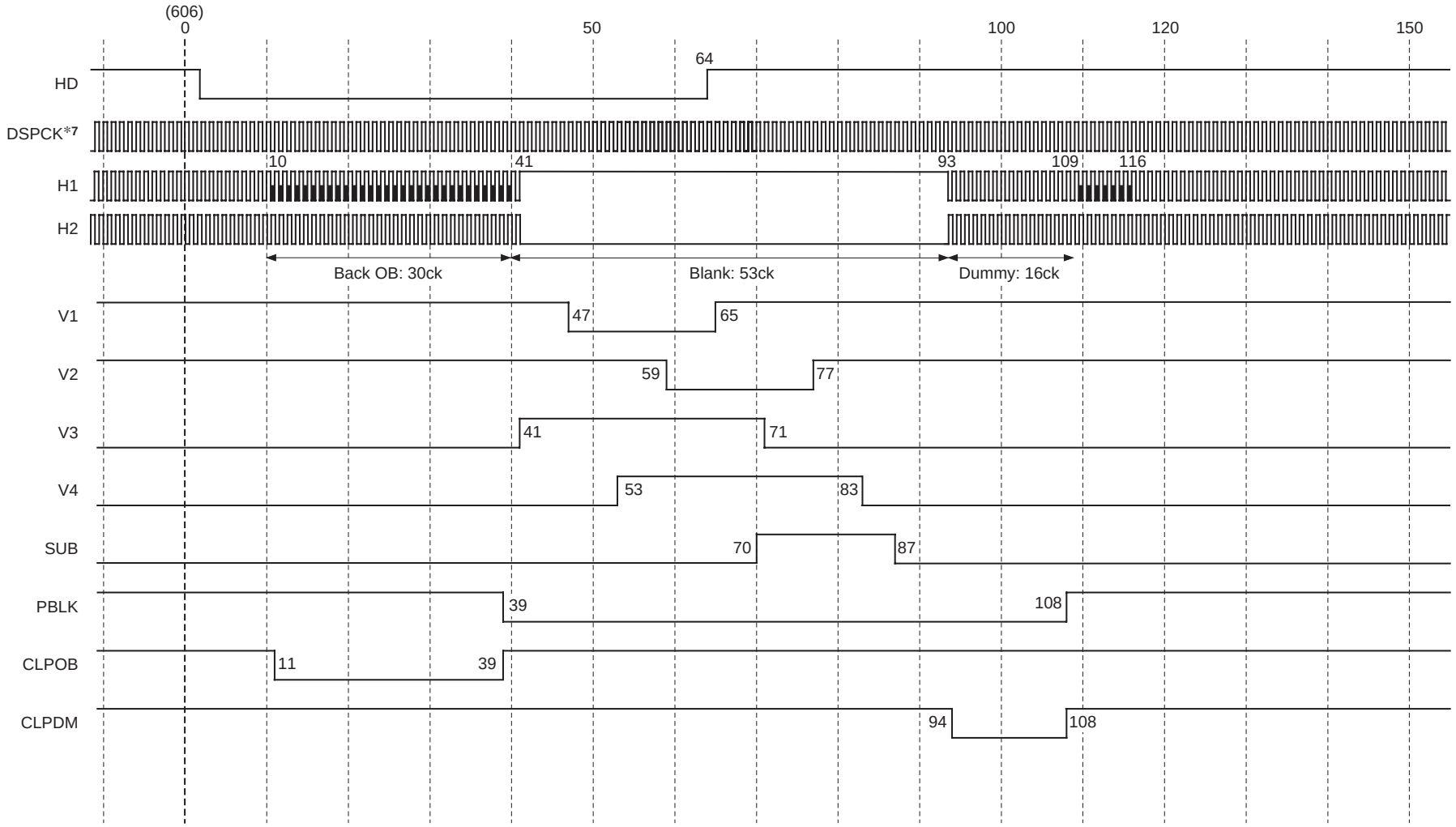
Applicable CCD image sensor:
ICX206AK/226AK/254AK/404AK



*6 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).

Horizontal Timing Chart **MODESEL 3, 4, 5 [510H PAL] DSPCK: 606f_H (9.46875MHz: 105.60ns)**

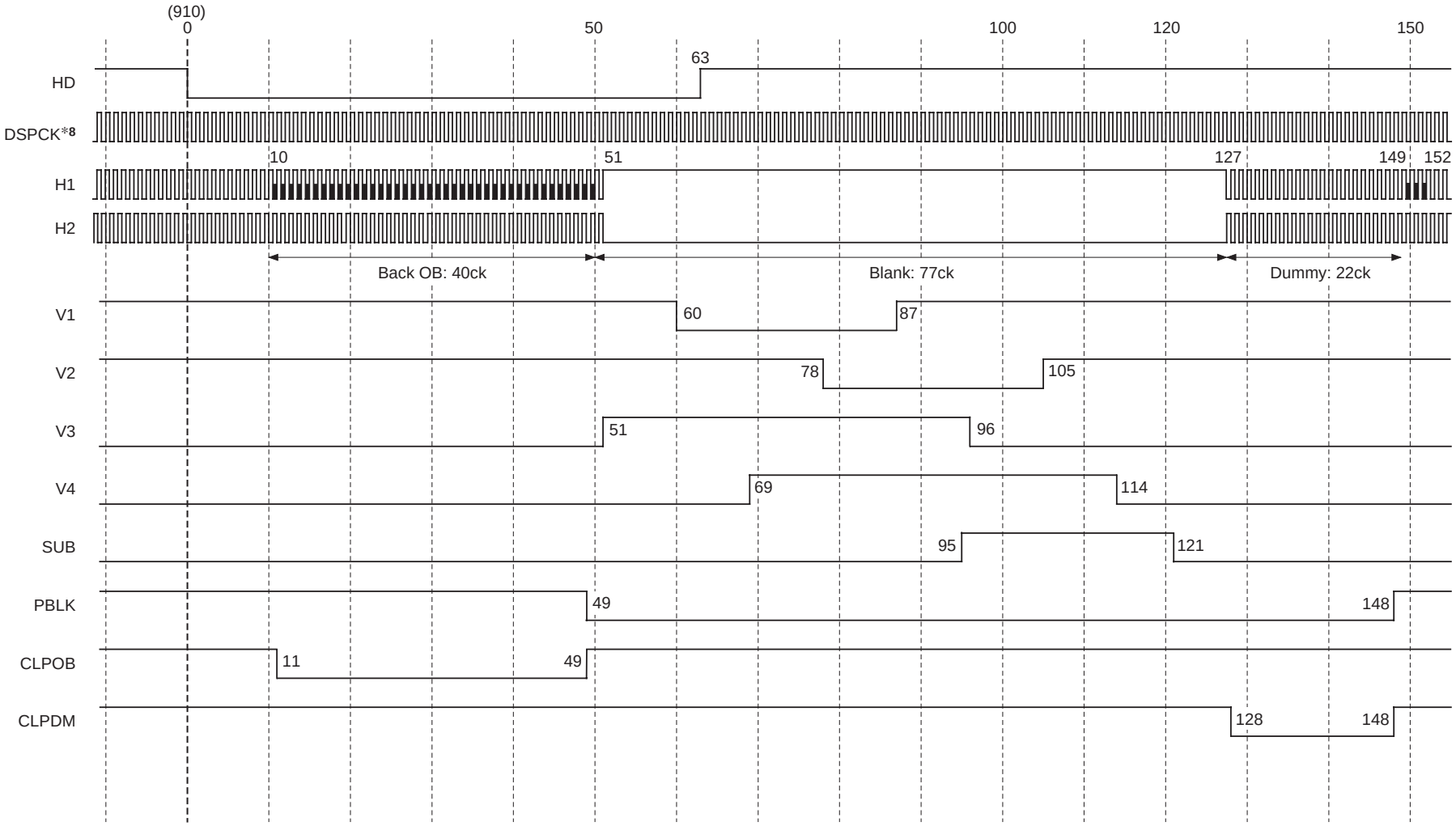
Applicable CCD image sensor:
ICX207AK/227AK/255AK/405AK



*7 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).

Horizontal Timing Chart **MODESEL 6, 8 [760H NTSC] DSPCK: 910f_H (14.31818MHz: 69.84ns)**

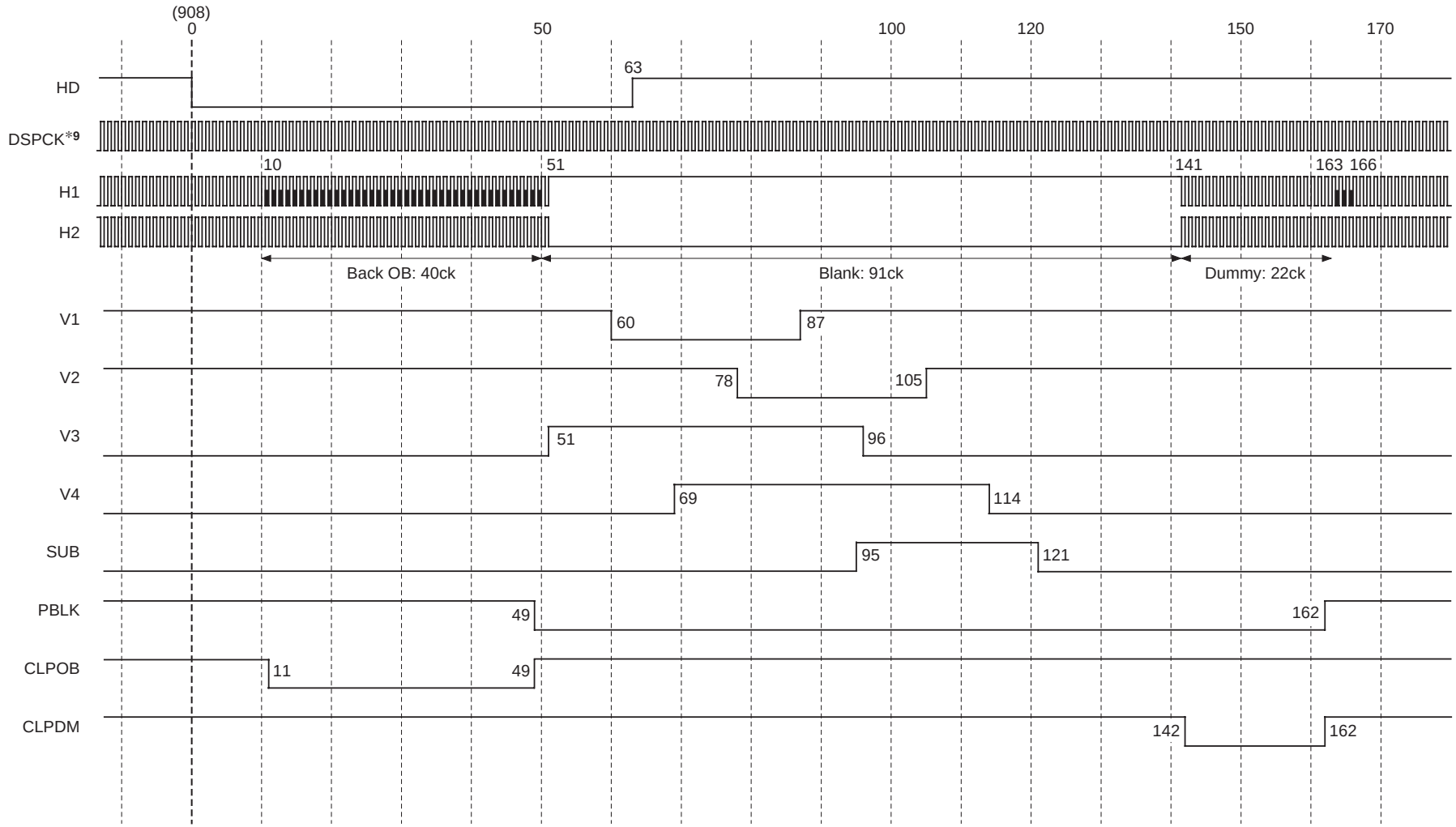
Applicable CCD image sensor:
ICX228AK/258AK/278AK/408AK



*8 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).

Horizontal Timing Chart **MODESEL 9, A, B [760H PAL] DSPCK: 908f$_H$ (14.1875MHz: 70.48ns)**

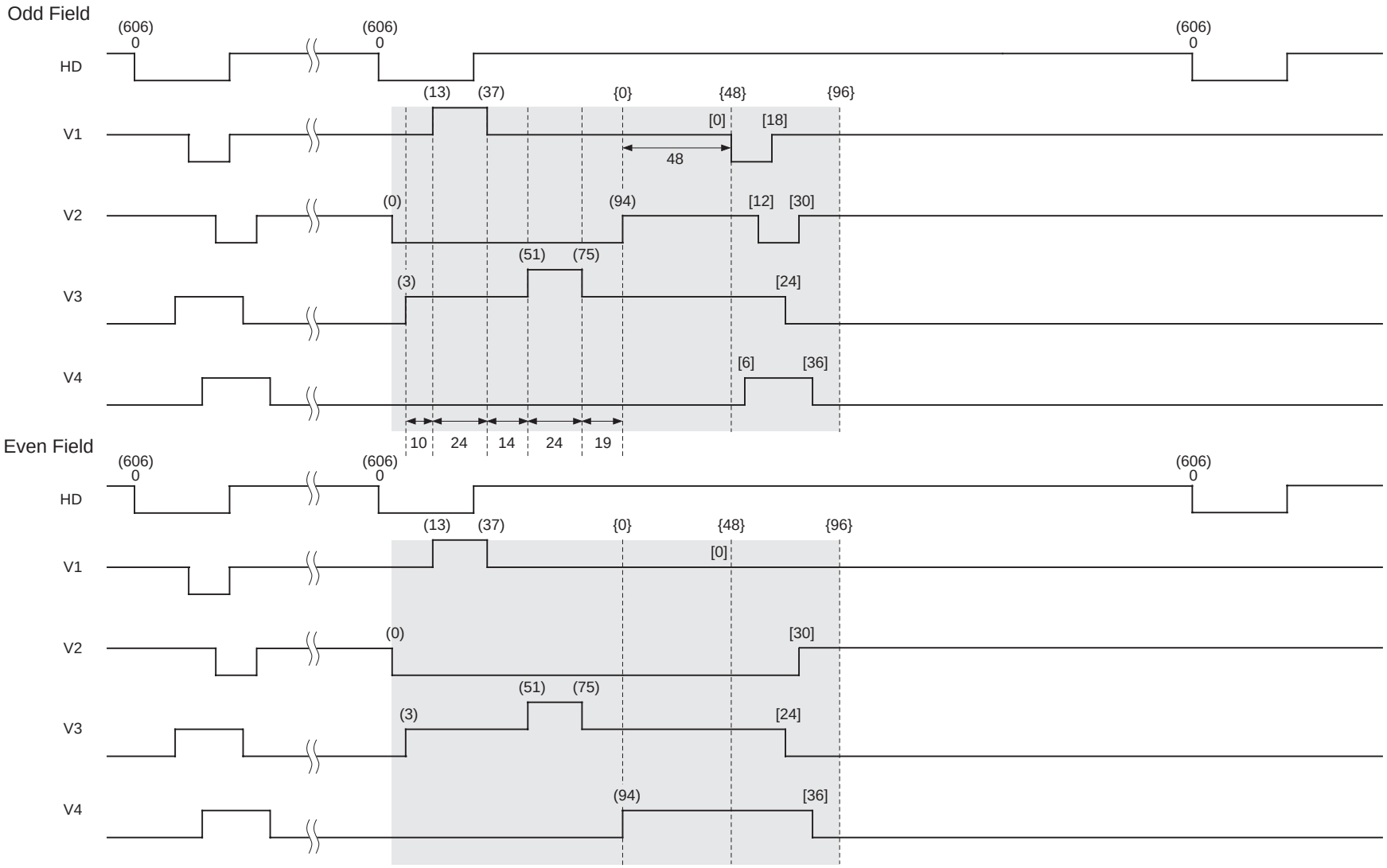
Applicable CCD image sensor:
ICX229AK/259AK/279AK/409AK



*9 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).

Horizontal Timing Chart MODESEL 0, 1, 2 [510H NTSC]

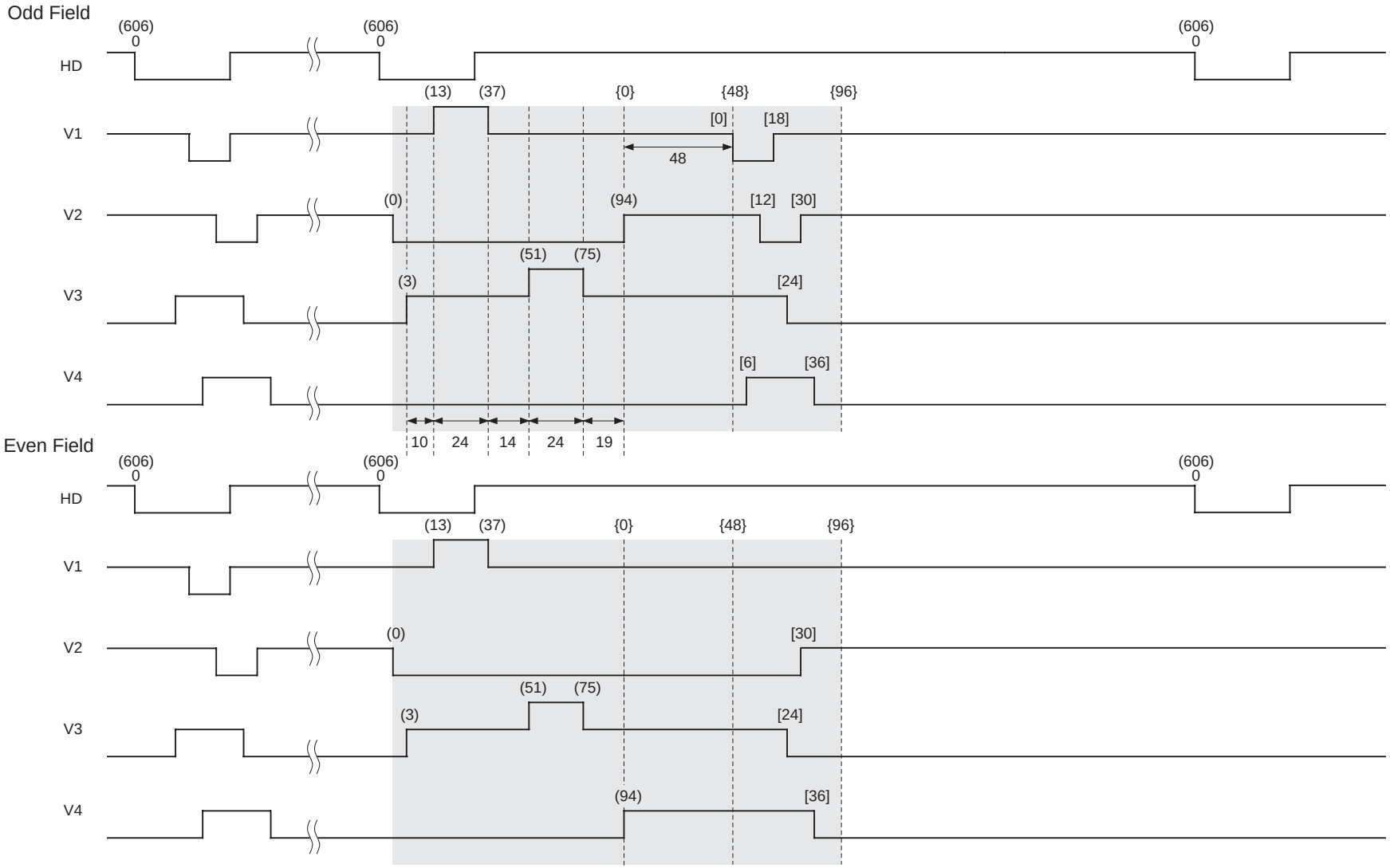
Applicable CCD image sensor:
ICX206AK/226AK/254AK/404AK



The shaded pulse area shifts while keeping the relative position relationship during shutter setting.

Horizontal Timing Chart **MODESEL 3, 4, 5 [510H PAL]**

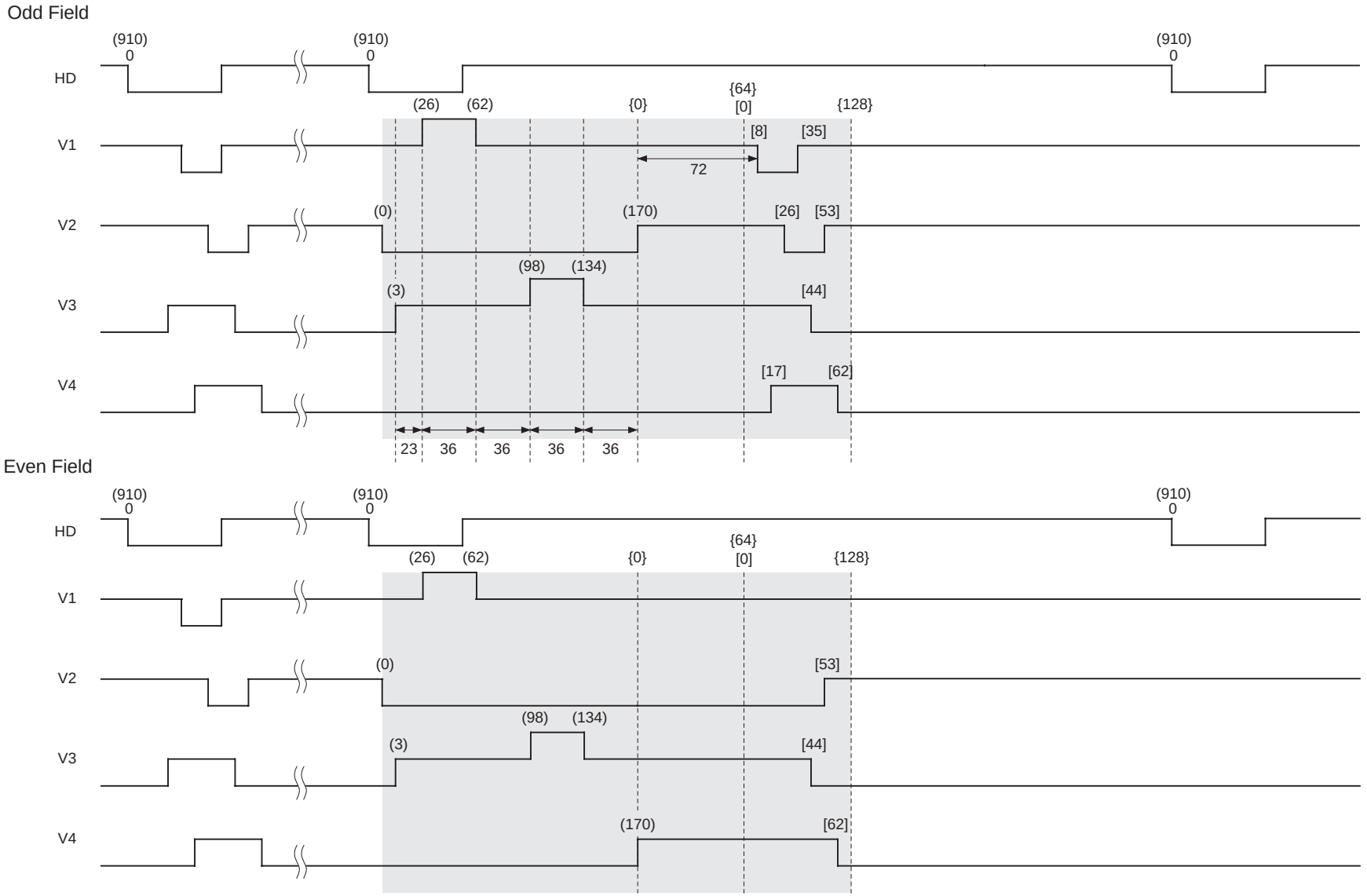
Applicable CCD image sensor:
ICX207AK/227AK/255AK/405AK



The shaded pulse area shifts while keeping the relative position relationship during shutter setting.

Horizontal Timing Chart MODESEL 6, 8 [760H NTSC]

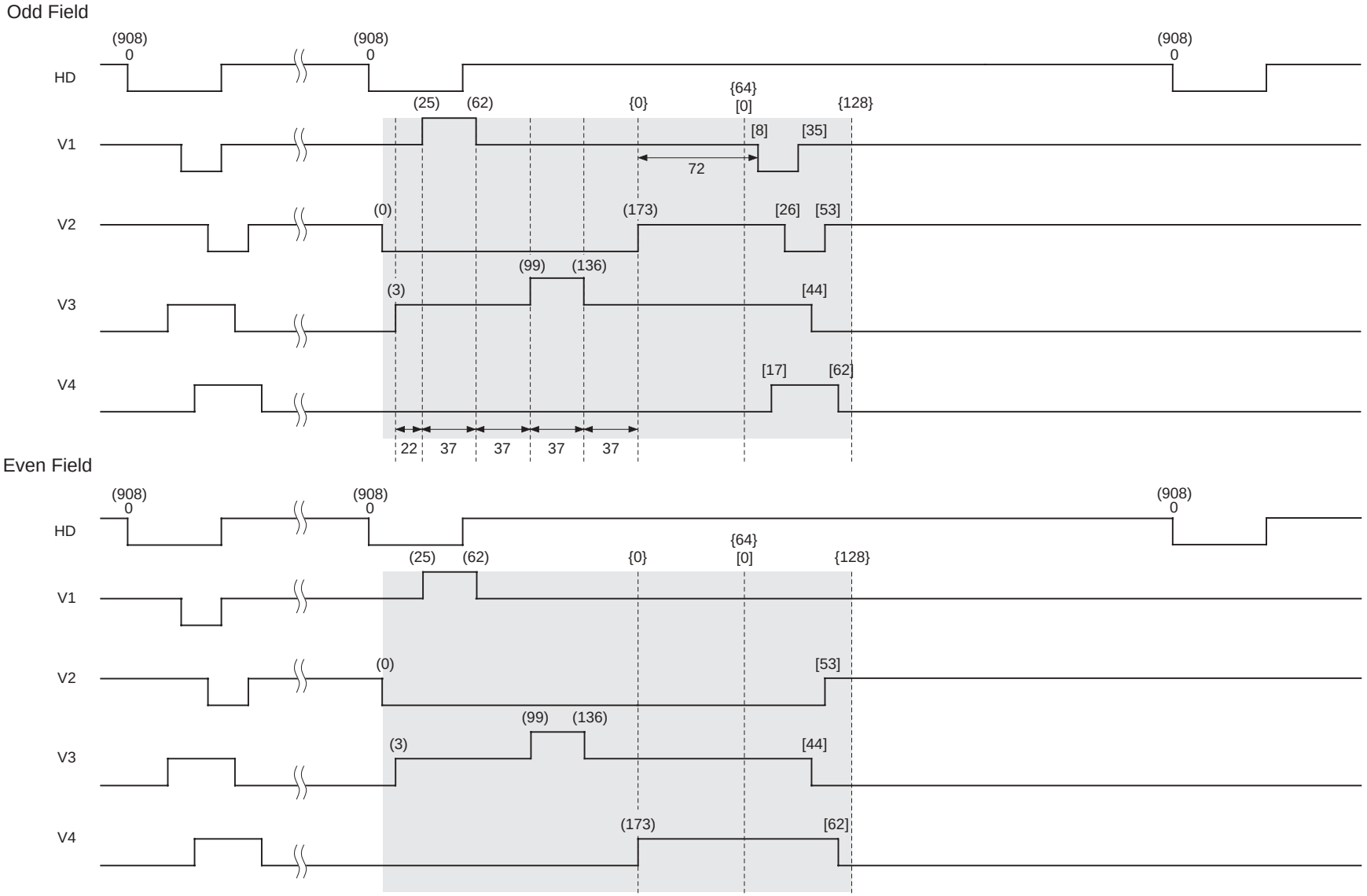
Applicable CCD image sensor:
ICX228AK/258AK/278AK/408AK



The shaded pulse area shifts while keeping the relative position relationship during shutter setting.

Horizontal Timing Chart **MODESEL 9, A, B [760H PAL]**

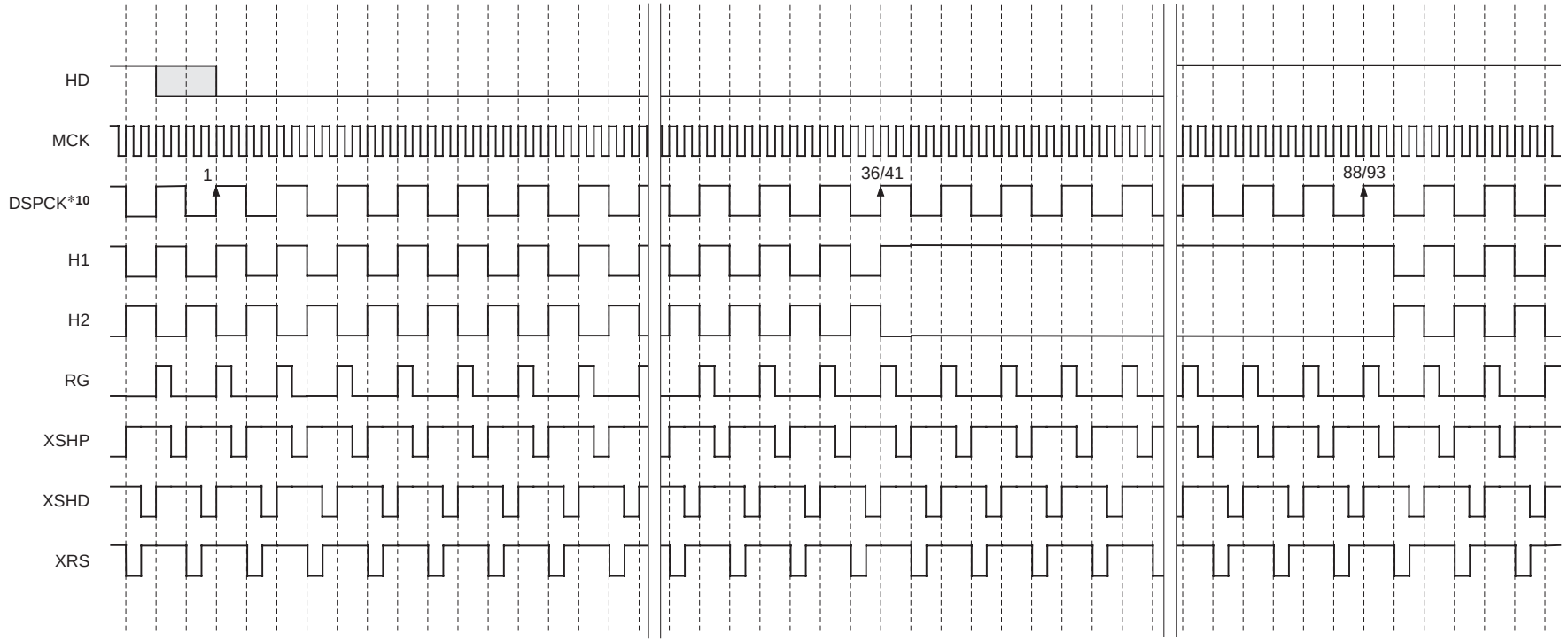
Applicable CCD image sensor:
ICX229AK/259AK/279AK/409AK



The shaded pulse area shifts while keeping the relative position relationship during shutter setting.

High-speed waveform pulse **MODESEL 0, 1, 2, 3, 4, 5 [510H NTSC/PAL]**

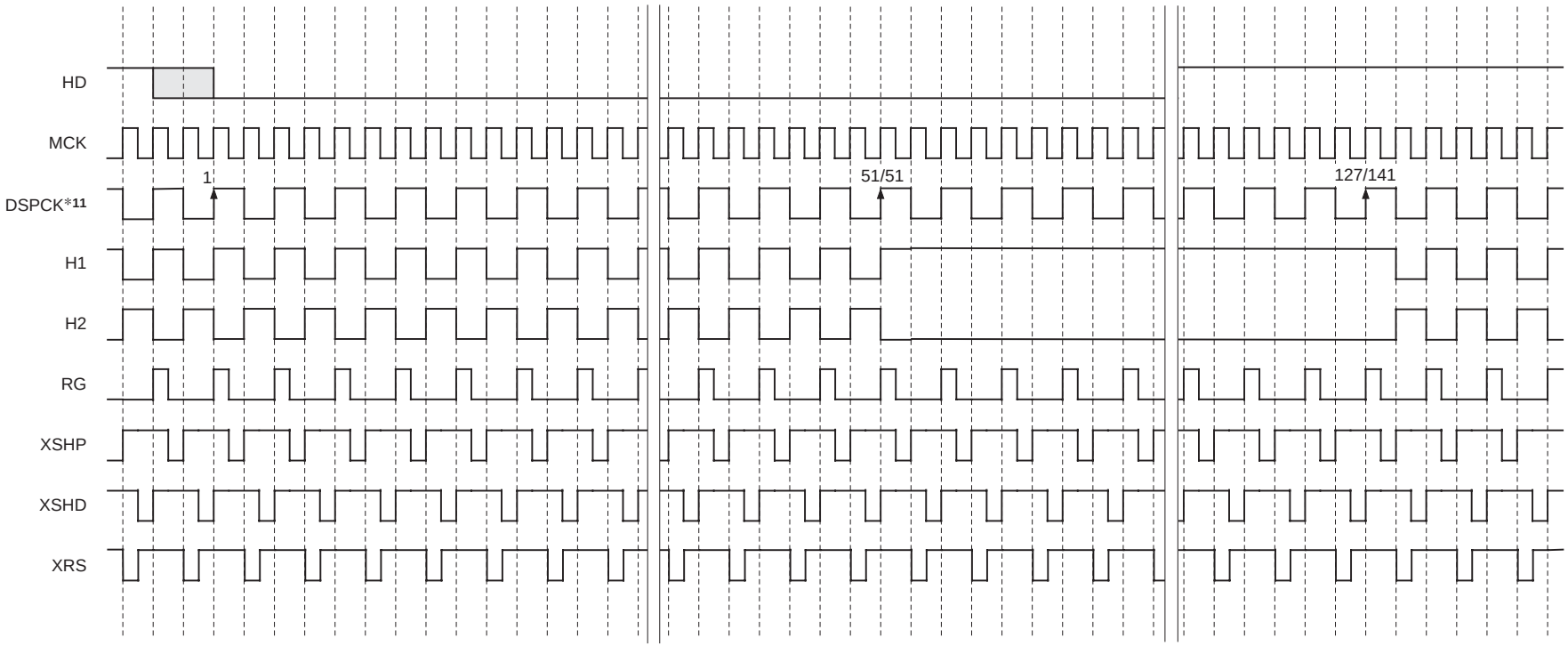
Applicable CCD image sensor:
ICX206AK/226AK/254AK/404AK
ICX207AK/227AK/255AK/405AK



*10 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).
* The phase relationship of each pulse shows the logical position relationship. For the actual output, a delay is added to each pulse.
* High-speed pulse pin setting shown above indicates the state of initial setting (delay, duty) of the parameter (Category 6: TG)

High-speed waveform pulse **MODESEL 6, 8, 9, A, B [760H NTSC/PAL]**

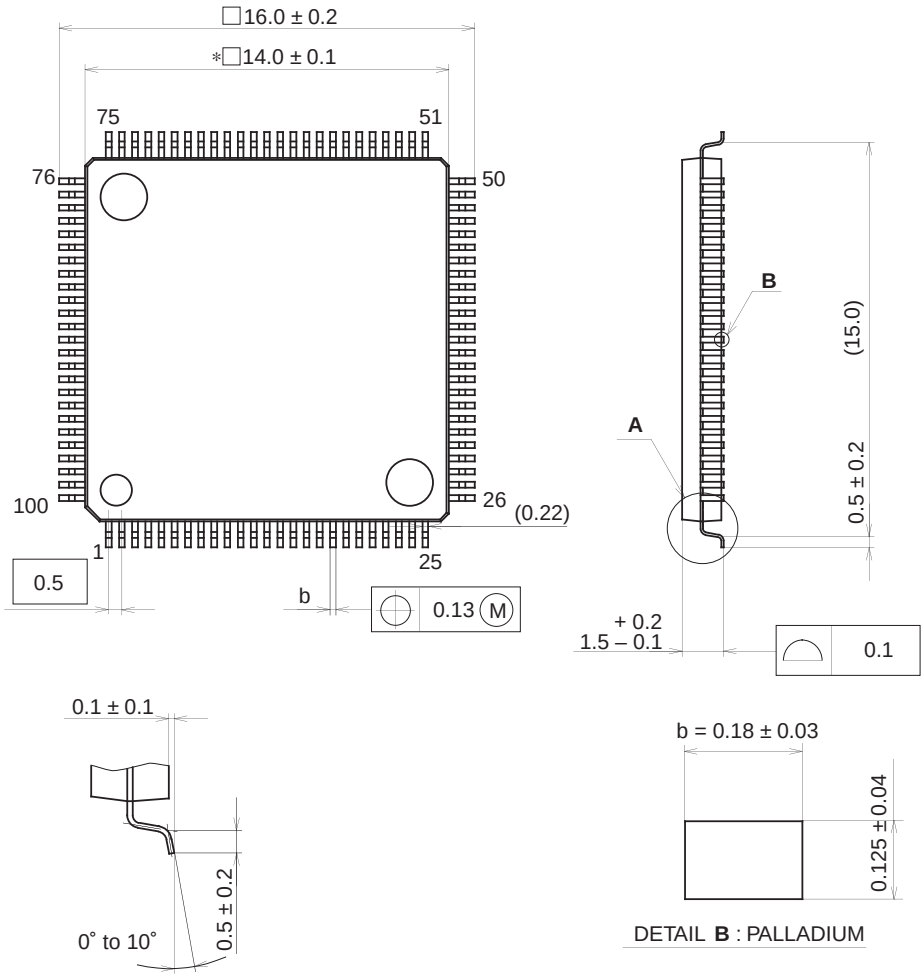
Applicable CCD image sensor:
ICX228AK/258AK/278AK/408AK
ICX229AK/259AK/279AK/409AK



*11 DSPCK is a clock which is not output by external pins. See the previously described table (Relationship between MODESEL and Each Clock).
* The phase relationship of each pulse shows the logical position relationship. For the actual output, a delay is added to each pulse.
* High-speed pulse pin setting shown above indicates the state of initial setting (delay, duty) of the parameter (Category 6: TG)

Package Outline Unit: mm

100PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B** : PALLADIUM

NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.7g