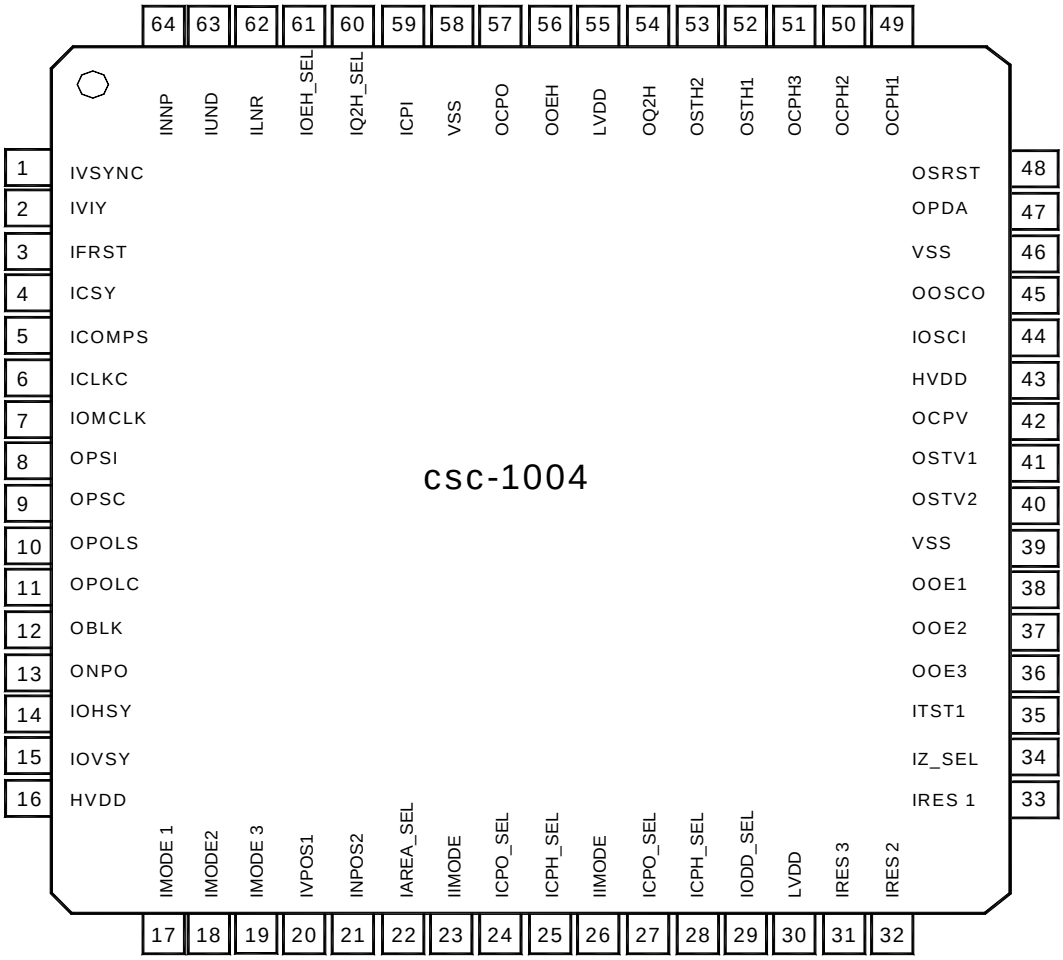
IC BLOCK DIAGRAM & DESCRIPTION

IC101 CSC-1004D



CSC-1004

Pin No.	Pin name	I/O	Remarks	Pin No.	Pin name	I/O	Remarks
1	ivsync	I	schimtt	33	ires1	I	pull_down
2	iviy	I	schimtt	34	iz_sel	I	pull_down
3	first	I	schimtt	35	itst1	I	AC/DC test
4	icsy	I	schimtt	36	ooe3	O	3mA
5	icomps	I	pull_up	37	ooe2	O	3mA
6	iclkc	I	pull_up	38	ooe1	O	3mA
7	iomclk	I/O	Bi dir.(3mA)	39	vss		
8	opsi	O	3mA	40	ostv2	O	3_state(3mA)
9	opsc	O	1mA	41	pstv1	O	3_state(3mA)
10	opols	O	3mA	42	ocpv	O	3mA
11	opolc	O	3mA	43	HVDD		5.0V
12	oblk	O	1mA	44	iosci	I	xin (25mhz)

IC BLOCK DIAGRAM & DESCRIPTION

IC101 CSC-1004

13	onpo	O	1mA	45	oosco	O	xout(25mhz)
14	iohsy	I/O	Bi dir.(3mA)	46	vss		
15	iovsy	I/O	Bi dir(3mA).	47	opda	O	3_state(3mA)
16	HVDD		5.0V	48	osrst	O	1mA
17	imode1	I	pull_down	49	ocph1	O	6mA
18	imode2	I	pull_down	50	ocph2	O	6mA
19	imode3	I	pull_down	51	pcph3	O	6mA
20	ivpos1	I	pull_down	52	osth1	O	3_state(3mA)
21	ivpos2	I	pull_down	53	osth2	O	3_state(3mA)
22	VSS			54	oq2h	O	3mA
23	ihpos1	I	pull_up	55	LVDD		3.3V
24	ihpos2	I	pull_up	56	ooeh	O	3mA
25	iarea_sel	I	pull_up	57	ocpo	O	3mA
26	iimode	I	pull_up	58	VSS		
27	icpo_sel	I	pull_up	59	icpi	I	
28	icpo_sel	I	pull_up	60	iq2h_sel	I	pull_up
29	iodd_sel	I	pull_up	61	ioeh_sel	I	pull_up
30	LVDD		3.3V	62	ilnr	I	pull_up
31	ires3	I	pull_down	63	iund	I	pull_up
32	ires2	I	pull_down	64	innp	I	pull_up

preliminary

TFT-LCD CONTROLLER LSI(PVI-1004D) SPECIFICATION

MODEL NAME. : PVI-1004D

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐PVI's Confirmation

Confirmed By _____

Prepared By _____

PRIME VIEW INTERNATIONAL CO.,LTD.
3,LI SHIN RD. 1,SCIENCE-BASED INDUSTRIAL PARK,HSINCHU,TAIWAN,R.O.C.
http://www.pvi.com.tw

Date : MAY. 15004

Contents :

Appendix

1. General Description

The PVI-1004D is a timing controller IC to control PVI AV type TFT LCD modules, which built in horizontal frequency driver and phase comparator circuit for PLL circuit.

Also this IC can support external clock mode that it doesn't need PLL circuit.

This IC generates all kind of control timing signals to the LCD source drivers and gate drivers.

This IC provides PVI's 16:9 aspect ratio TFT LCD modules and it also provides different display mode.

2. Features

- Support multiple resolution mode
- Support Standard NTSC/PAL video system
- Line Inversion Driving method.
- Provide timing scan for Left/Right and Up/Down shift control
- Support 3 shift clock
- Provide multi display mode (960*234, 1200*234, 1440*234 mode, 1920*234 mode)
- Support composite sync input mode and separate sync input mode
- Support external clock input mode (960*234,1200*234,1440*234, 1920*234 mode)
- 64 pin QFP (0.5mm pitch)
- Dual power supplies : +5.0V/+3.3V
- 0.35u CMOS process, 3.3V for core and 3.3V/5V for IO PAD

3. Pin assignment

pin No.	pin name	I/O	Remarks	pin No.	pin name	I/O	Remarks
1	ivsync	I	schimtt	33	ires1	I	pull_down
2	iviy	I	schimtt	34	iz_sel	I	Pull_down
3	ifrst	I	schimtt	35	itst1	I	AC/DC test
4	icsy	I	schimtt	36	ooe3	O	3mA
5	icomps	I	pull_up	37	ooe2	O	3mA
6	iclkc	I	pull_up	38	ooe1	O	3mA
7	iomclk	I/O	Bi dir.(3mA)	39	VSS		
8	opsi	O	3mA	40	ostv2	O	3_state(1mA)
9	opsc	O	3mA	41	ostv1	O	3_state(1mA)
10	opols	O	3mA	42	ocpv	O	3mA
11	opolc	O	3mA	43	HVDD		5.0V/3.3V
12	oblk	O	3mA	44	iosci	I	xin (25Mhz)
13	onpo	O	3mA	45	oosco	O	xout(25Mhz)
14	iohsy	I/O	Bi dir.(3mA)	46	VSS		
15	iovsy	I/O	Bi dir(3mA).	47	opda	O	3_state(3mA)
16	HVDD		5.0V/3.3V	48	osrst	O	1mA
17	imode1	I	pull_down	49	ocph1	O	6mA
18	imode2	I	pull_down	50	ocph2	O	6mA
19	imode3	I	pull_down	51	ocph3	O	6mA
20	ivpos1	I	pull_up	52	osth1	O	3_state(3mA)
21	ivpos2	I	pull_up	53	osth2	O	3_state(3mA)
22	VSS			54	oq2h	O	3mA
23	ihpos1	I	pull_up	55	LVDD		3.3V
24	ihpos2	I	pull_up	56	ooeh	O	3mA
25	iarea_sel	I	pull_up	57	ocpo	O	3mA
26	iimode	I	pull_up	58	VSS		
27	icpo_sel	I	pull_up	59	icpi	I	
28	icph_sel	I	pull_up	60	iq2h_sel	I	pull_up
29	iodd_sel	I	pull_up	61	ioeh_sel	I	pull_up
30	LVDD		3.3V	62	ilnr	I	pull_up
31	ires3	I	pull_down	63	iund	I	pull_up
32	ires2	I	pull_down	64	innp	I	pull_up

4. Pin Description

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Description</th><th>Remark</th></tr>
<tr><td>1</td><td>ivsync</td><td>I</td><td>vertical sync signal in composite sync mode (low active)</td><td></td></tr>
<tr><td>2</td><td>iviy</td><td>I</td><td>vertical sync signal in separate sync mode(low active)</td><td></td></tr>
<tr><td>3</td><td>ifrst</td><td>I</td><td>reset pin in ASIC
1) ifrst = "H" : Normal state
2) ifrst = "L" : Reset state</td><td></td></tr>
<tr><td>4</td><td>icsy</td><td>I</td><td>select composite signal/horizontal signal
1) icomps = "H" : icsy is composite sync signal (high active)
2) icomps = "L" : icsy is horizontal sync signal(low active)</td><td></td></tr>
<tr><td>5</td><td>icomps</td><td>I</td><td>select composite sync mode/separate sync mode
1) icomps = "H" : composite sync mode
2) icomps = "L" : separate sync mode</td><td>Note1)</td></tr>
<tr><td>6</td><td>iclkc</td><td>I</td><td>select PLL mode/external clock mode
1) iclkc = "H" : PLL mode
2) iclkc = "L" : external clock mode</td><td>Note1)</td></tr>
<tr><td>7</td><td>iomclk</td><td>I/O</td><td>input clock signal (external clock mode)
1) iclkc = "H" : This signal will be ground
2) iclkc = "L" : This signal will be external input ternimal</td><td></td></tr>
<tr><td>8</td><td>opsi</td><td>O</td><td>control decorder chip pin</td><td></td></tr>
<tr><td>9</td><td>opsc</td><td>O</td><td>control DC-DC chip pin</td><td></td></tr>
<tr><td>10</td><td>opols</td><td>O</td><td>polarity alternating signal for video</td><td></td></tr>
<tr><td>11</td><td>opolc</td><td>O</td><td>polarity alternating signal for Vcom</td><td></td></tr>
<tr><td>12</td><td>oblk</td><td>O</td><td>blanking control pin
1) oblk ="H" : blanking display (black)
2) oblk ="L" : normal display</td><td></td></tr>
<tr><td>13</td><td>onpo</td><td>O</td><td>auto detect pin for NTSC/PAL
1) onpo ="H" : NTSC
2) onpo ='L" : PAL</td><td>Note2)</td></tr>
<tr><td>14</td><td>iohsy</td><td>I/O</td><td>input/output horizontal sync. signal (low active)
1) iclkc = "H" : This signal outputs horizontal sync. signal
2) iclkc = "L" : This signal will be external horizontal sync. Input.</td><td></td></tr>
<tr><td>15</td><td>iovsy</td><td>I/O</td><td>input/output vertical sync. signal (low active)
1) iclkc = "H" : This signal outputs vertical sync. signal
2) iclkc = "L" : This signal will be external vertical sync. Input.</td><td></td></tr>
<tr><td>16</td><td>HVDD</td><td>-</td><td>high voltage power (5.0 V or 3.3V)</td><td>Note3)</td></tr>
<tr><td>17
18
19</td><td>imode1
imode2
imode3</td><td>I
I
I</td><td>select display mode (1440, 1200, 960 mode only)
<table>
<tr><th>imode1</th><th>imode2</th><th>imode3</th><th>Description</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Full mode</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>Normal center mode</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>Normal wide mode</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>Zoom1 mode</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Zoom2 mode</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>Normal left mode</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Normal right mode</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>Zoom3 mode</td></tr>
</table></td><td>Note4)</td></tr>
</table>

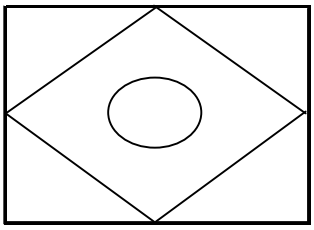
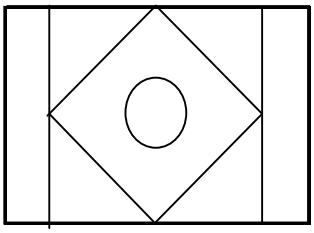
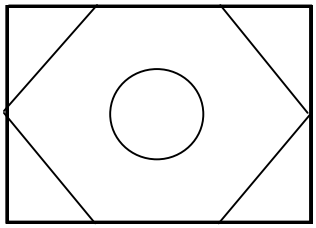
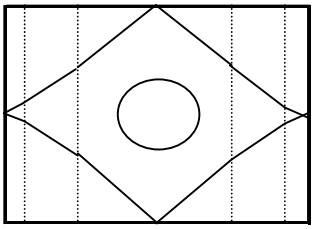
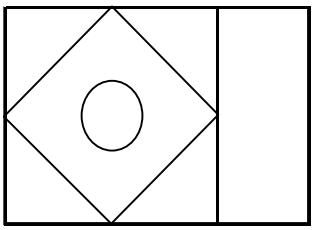
<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Description</th><th>Remark</th></tr>
<tr><td>20
21</td><td>ivpos1
ivpos2</td><td>I
I</td><td>select vertical start line
<table>
<tr><td>ivpos2</td><td>ivpos1</td><td>NTSC</td><td>PAL</td></tr>
<tr><td>L</td><td>L</td><td>20</td><td>26</td></tr>
<tr><td>L</td><td>H</td><td>21</td><td>28</td></tr>
<tr><td>H</td><td>L</td><td>22</td><td>30</td></tr>
<tr><td>H</td><td>H</td><td>23</td><td>31</td></tr>
</table></td><td>Note1)</td></tr>
<tr><td>22</td><td>VSS</td><td>-</td><td>Ground</td><td></td></tr>
<tr><td>23
24</td><td>ihpos1
ihpos2</td><td>I
I</td><td>select horizontal start point (iclkc ="L" only, ext clock mode)
<table>
<tr><td>ivpos2</td><td>ivpos1</td><td>1440</td><td>1200</td><td>960</td><td>1920</td></tr>
<tr><td>L</td><td>L</td><td>100</td><td>85</td><td>67</td><td>134</td></tr>
<tr><td>L</td><td>H</td><td>101</td><td>86</td><td>68</td><td>135</td></tr>
<tr><td>H</td><td>L</td><td>102</td><td>87</td><td>69</td><td>136</td></tr>
<tr><td>H</td><td>H</td><td>103</td><td>88</td><td>70</td><td>137</td></tr>
</table></td><td>Note1)
Note5)</td></tr>
<tr><td>25</td><td>iarea_sel</td><td>I</td><td>select display range
1) iarea_sel = "H" : The display range is 50.01us (NTSC)
2) iarea_sel = "L" : The display range is 48.00us (NTSC)</td><td>Note1)</td></tr>
<tr><td>26</td><td>iimode</td><td>I</td><td>select simultaneous mode/sequential mode
1) iimode ="H" : simultaneous mode (stripe arrangement)
2) iimode ="L" : sequential mode (delta arrangement)</td><td>Note1)</td></tr>
<tr><td>27</td><td>icpo_sel</td><td>I</td><td>select horizontal position adjust (iclkc = "H" only)
1) icpo_sel = "H" : hor. Position adjustment is normal
2) icpo_sel = "L" : hor.position adjustment is more wide</td><td>Note1)</td></tr>
<tr><td>28</td><td>icph_sel</td><td>I</td><td>select ocph1,2,3 phase (delta arrangement module only)
1) icph_sel = "H" : PVI's arrangement
2) icph_sel = "L" : another company's arrangement</td><td>Note1)
Note6)</td></tr>
<tr><td>29</td><td>iodd_sel</td><td>I</td><td>select falling edge of iovsy's position (NTSC, composite sync only
1) iodd_sel = "H" : iovsy's phase difference is 1.5H (even field)
2) iodd_sel = "L" : iovsy's phase difference is 0.5H (even field)</td><td>Note1)</td></tr>
<tr><td>30</td><td>LVDD</td><td>-</td><td>low voltage power (3.3V only)</td><td></td></tr>
<tr><td>31
32
33</td><td>ires3
ires2
ires1</td><td>I
I
I</td><td>select resolution mode
<table>
<tr><td>ires1</td><td>ires2</td><td>ires3</td><td>resolution mode</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>1200 * 234</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>-</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>1920 * 234</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>240 * 234</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>480 * 234</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>960 * 234 (S)</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>960 * 234 (D)</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>1440 * 234</td></tr>
</table></td><td>Note4)</td></tr>
<tr><td>34</td><td>iz_sel</td><td>I</td><td>select falling edge of iovsy's position (PAL mode only)
1) iz_sel = "H" : iovsy's phase difference is 0.5H (even field)
2) iz_sel = "L" : iovsy's phase difference is 1.5H (even field)</td><td>Note4)</td></tr>
</table>

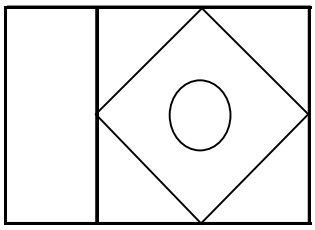
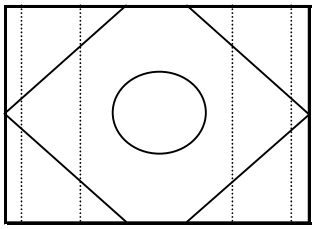
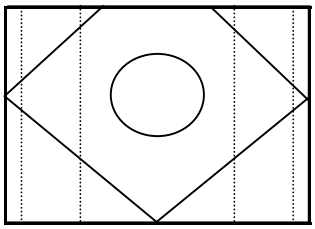
No.	Symbol	I/O	Description	Remark
35	itst1	I	select AC/DC test 1) itst1 = "H" : AC/DC test mode 2) itst1 = "L" : normal mode	
36 37 38	ooe3 ooe2 ooe1	O O O	output enable control signal for gate driver ooe1,2,3 ="H" : gate output => Vee 1) ooe1 controls 1 4 7 10 --- 238 lines 2) ooe2 controls 2 5 8 11 --- 239 lines 3) ooe3 controls 3 6 9 12 --- 240 lines	note7)
39	VSS	-	Ground	
40	ostv2	O	gate driver start pulse 1) iund = "H" : ostv2 is in high impedance state 2) iund = "L" : ostv2 is output pin of start pulse	note7)
41	ostv1	O	gate driver start pulse 1) iund = "H" : ostv1 is output pin of start pulse 2) iund = "L" : ostv1 is in high impedance state	note7)
42	ocpv	O	gate driver shift clock	
43	HVDD	-	high voltage power (5.0 V or 3.3V)	Note3)
44	iosci	I	input for clock oscillator circuit	
45	oosco	O	output for clock oscillator circuit	
46	VSS	-	Ground	
47	opda	O	output for phase comparative signal for PLL circuit	
48	osrst	O	reset source driver IC (active high)	
49	ocph1	O	source driver shift clock #1	
50	ocph2	O	source driver shift clock #2 1) iimode = "H" : ochp2 is always high signal (stripe arrangement) 2) iimode = "L" : ocph2 is shift clock (delta arrangement)	
51	ocph3	O	source driver shift clock #3 1) iimode = "H" : ochp3 is always low signal (stripe arrangement) 2) iimode = "L" : ocph3 is shift clock (delta arrangement)	
52	osth1	O	source driver start pulse 1) ilnr = "H" : osth1 is output pin of start pulse 2) ilnr = "L" : osth1 is in high impedance state	Note8)
53	osth2	O	source driver start pulse 1) ilnr = "H" : osth2 is in high impedance state 2) ilnr = "L" : osth2 is output pin of start pulse	Note8)
54	oq2h	O	pin of RGB output data order on no rotation mode 1) iimode ="H" : no use (low) 2) iimode ="L" : use (delta arrangement)	
55	LVDD	-	low voltage power (3.3V only)	
56	ooeh	O	output enable control signal for source driver 1) ioeh_sel = "H" : ooeh is active low 2) ioeh_sel = "L" : ooeh is active high	
57	ocpo	O	output for horizontal position adjustment	
58	VSS	-	Ground	
59	icpi	I	input for horizontal position adjustment	

No.	Symbol	I/O	Description	Remark
60	iq2h_sel	I	select oe's control in zoom mode 1) iq2h_sel = "H" : 3 oe (oe1,oe2,oe3) control 2) iq2h_sel = "L" : 1 oe control	Note1) note6)
61	ioeh_sel	I	select perioty of ooeh 1) ioeh_sel = "H" : ooeh is active low 2) ioeh_sel = "L" : ooeh is active high	Note1)
62	ilnr	I	select left/right direction 1) ilnr = "H" : normal scan 2) ilnr = "L" : reverse scan	Note1) Note8)
63	iund	I	select up/down direction 1) iund = "H" : normal scan 2) iund = "L" : reverse scan	Note1) Note7)
64	innp	I	select NTSC/PAL 1) ilnr = "H" : normal scan 2) ilnr = "L" : reverse scan	Note1)

Note1) Those pins are Normally pull-up
Note2) If use auto detection, this pin must connect innp
Note3) If you want to use 5V's I/O signal, It must connect 5V's Voltage,
otherwise, if you want to use 3.3V's I/O signal, it must connect 3.3V's voltage
Note4) Those pins are Normally pull-down
Note5) This count means No.of input clock from the falling edge of iohsy
Note6) If you use another company's TFT LCD module, please contact PVI.
Note7) iund controls up/down direction
1) iund = "H" : ostv1 → G1(ooe1) → G2(ooe2) → G3(ooe3) → G4(ooe1) → G5(ooe1) → --- → G238(ooe1) → G239(ooe2) → G240(ooe3) → ostv2
2) iund = "L" : ostv1 ← G1(ooe1) ← G2(ooe2) ← G3(ooe3) ← G4(ooe1) ← G5(ooe1) ← --- ← G238(ooe1) ← G239(ooe2) ← G240(ooe3) ← ostv2
Note8) ilnr controls left/right direction
1) ilnr = "H" : osth1 → ----- → osth2
2) ilnr = "L" : osth1 ← ------ ← osth2

5. Display mode (1200, 1440, 1920, 960 mode only)

Display mode	Display characteristics (4:3 aspect-ratio input)	imd 1	imd 2	imd 3	Note
Full		Lo	Lo	Lo	Input video signals are displayed in full screen (To display 4:3 signal on 16:9 screen)
Normal Center		Hi	Lo	Lo	Input video signals are displayed in the center screen (4:3 aspect ratio)
Zoom 1		Hi	Hi	Lo	Input video signal of central 176 lines are displayed in full screen (Vertically extention)
Wide		Lo	Hi	Lo	Input video signals are displayed in full screen (Horizontal modification)
Normal Left		Hi	Lo	Hi	Input video signals are displayed in the left screen (4:3 aspect ratio)

Display mode	Display characteristics (4:3 aspect-ratio input)	imd 1	imd 2	imd 3	Note
Normal Right		Lo	Hi	Hi	Input video signals are displayed in the right screen (4:3 aspect ratio)
Zoom 2		Lo	Lo	Hi	Input video signal of centeral 204 lines are displayed in full screen (Vertically extention and horizon. Modifi.)
Zoom 3		Hi	Hi	Hi	Same as Zoom 2 mode. Vertically offset centered

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Power supply voltage	HVDD	-0.3 to 7.0	V
	LVDD	-0.3 to 4.0	V
Input voltage	V_{IN}	-0.3 to HVDD+0.5	V
Output voltage	V_{OUT}	-0.3 to HVDD+0.5	V
Storage temperature	Tstg	-65 to 150	℃

6.2 Recommened Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Power supply voltage	HVDD 1	4.5	5.0	5.5	V
	HVDD 2	3.0	3.3	3.6	V
	LVDD	3.0	3.3	3.6	0
Input voltage	V_{IN}	VSS	0	HVDD	0
Operating temperature	Topr	-40	-	85	℃

6.3 General DC characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Remark
Input low current	I_{IL}	V_I = 0 V	-1	-	1	uA	
Input high current	I_{IH}	V_I = HVDD	-1	-	1	uA	
Tri state leakage current	I_{OZ}		-10	-	10	uA	
Logic input low voltage	V_{IL}	HVDD=MIN	-	-	1.0	V	
Schmitt input low voltage	V_{SIL}	HVDD=MIN	0.8	-	3.1	V	
Logic input high voltage	V_{SIL}	HVDD=MAX	3.5	-	-	V	
Schmitt input high voltage	V_{SIH}	HVDD=MAX	2.0	-	4.0	V	
Output low voltage	V_{OL}	HVDD=MIN	HVDD-0.4	-	-	V	
Output High voltage	V_{OH}	HVDD=MIN	-	-	VSS+0.4	V	
Input pull up/down resista	R_I	V_{IL} = 0V or V_{IH} = HVDD	-	60	-	kΩ	

6.4 Current consumption

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	Remark
Current consumption	I_{IN}	HVDD=5.0V	-	-	-	mA	

7. Timing conditions

7-1) 1200 * 234 mode (6.5")

a. Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
iosci period	t_{OSC}	81	83	85	ns	
icsy period	T_H	61.5	63.5	65.5	us	
icsy pulse width	t_{CSYN}	4	4.7	5.4	us	
icsy rising time	T_{cr}	-	-	700	ns	
icsy falling time	T_{cf}	-	-	300	ns	
ivsync pulse width	t_{VSY}	1	3	5	t_H	
ivsync rising time	T_{vr}	-	-	700	ns	
ivsync falling time	T_{vf}	-	-	1.5	us	
Horizontal lines per field		256	262.5	268	line	Note1

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
rising time	t_r	-	-	10	ns	
falling time	t_f	-	-	10	ns	
clock pulse width	t_{CPH}	-	1.5	-	t_{OSC}	
clock pulse duty	t_{CWH}	30	33(67)	70	%	
osth setup time	t_{SUH}	-	$t_{CPH}/2$	-	ns	
osth pulse width	t_{STH}	-	1	-	t_{CPH}	
iohsy pulse width	t_{HSY}	-	4.68	-	us	
ooeh pulse width	t_{OEH}	-	2.8	-	us	
sample & hold disable time	t_{DIS1}	-	5.56	-	us	
ooe1(2)(3) pulse width	t_{OEV}	-	16	-	us	
ocpv pulse width	t_{CPV}	-	$t_H/2$	-	us	
ocpo - ooeh time diff.	t_1	-	7.4	-	us	
ocpv - opda time diff.	t_2	-	6.1	-	us	
ooe1 - opda time diff.	t_3	-	14.28	-	us	
ocpo - opda time diff.	t_4	-	7.72	-	us	
iohsy - opsi time diff.	t_5	-	4.88	-	us	
opsi pulse width	t_{psiw}	-	4.6	-	us	
ostv1(2) setup time	t_{SUV}	-	$t_H/2$	-	us	
ostv1(2) pulse width	t_{STV}	-	1	-	t_H	
iovsy - ostv1(2) time diff.	$t_{VS1(2)}$	-	18(27)	-	t_H	Note1)

Note1) Values in brackets correspond to PAL mode

7-2) 1440 * 234 mode (6.2",7", 8.4")

a. Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
iosci period	t_{OSC}	64.5	69.5	74.5	ns	
icsy period	T_H	61.5	63.5	65.5	us	
icsy pulse width	t_{CSYN}	4	4.7	5.4	us	
icsy rising time	T_{cr}	-	-	700	ns	
icsy falling time	T_{cf}	-	-	300	ns	
ivsync pulse width	t_{VSY}	1	3	5	t_H	
ivsync rising time	T_{vr}	-	-	700	ns	
ivsync falling time	T_{vf}	-	-	1.5	us	
Horizontal lines per field		256	262.5	268	line	Note1

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
rising time	t_r	-	-	10	ns	
falling time	t_f	-	-	10	ns	
clock pulse width	t_{CPH}	-	1.5	-	t_{OSC}	
clock pulse duty	t_{CWH}	30	33(67)	70	%	
osth setup time	t_{SUH}	-	$t_{CPH}/2$	-	ns	
osth pulse width	t_{STH}	-	1	-	t_{CPH}	
iohsy pulse width	t_{HSY}	-	4.65	-	us	
ooeh pulse width	t_{OEH}	-	3.46	-	us	
sample & hold disable time	t_{DIS1}	-	5.52	-	us	
ooe1(2)(3) pulse width	t_{OEV}	-	16	-	us	
ocpv pulse width	t_{CPV}	-	$t_H/2$	-	us	
ocpo - ooeh time diff.	t_1	-	-2.8	-	us	
ocpv - opda time diff.	t_2	-	8.56	-	us	
ooe1 - opda time diff.	t_3	-	16.64	-	us	
ocpo - opda time diff.	t_4	-	-1.8	-	us	
iohsy - opsi time diff.	t_5	-	4.8	-	us	
opsi pulse width	t_{psiw}	-	4.48	-	us	
ostv1(2) setup time	t_{SUV}	-	$t_H/2$	-	us	
ostv1(2) pulse width	t_{STV}	-	1	-	t_H	
iovsy - ostv1(2) time diff.	$t_{VS1(2)}$	-	18(27)	-	t_H	Note1)

Note1) Values in brackets correspond to PAL mode

7-3) 960 * 234 mode (Stripe mode, 3.6",4.5", 5", 6.4")

a. Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
iosci period	t_{OSC}	100.2	104.2	108.2	ns	
icsy period	T_H	61.5	63.5	65.5	us	
icsy pulse width	t_{CSYN}	4	4.7	5.4	us	
icsy rising time	T_{cr}	-	-	700	ns	
icsy falling time	T_{cf}	-	-	300	ns	
ivsync pulse width	t_{VSY}	1	3	5	t_H	
ivsync rising time	T_{vr}	-	-	700	ns	
ivsync falling time	T_{vf}	-	-	1.5	us	
Horizontal lines per field		256	262.5	268	line	Note1

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
rising time	t_r	-	-	10	ns	
falling time	t_f	-	-	10	ns	
clock pulse width	t_{CPH}	-	1.5	-	t_{OSC}	
clock pulse duty	t_{CWH}	30	33(67)	70	%	
osth setup time	t_{SUH}	-	$t_{CPH}/2$	-	ns	
osth pulse width	t_{STH}	-	1	-	t_{CPH}	
iohsy pulse width	t_{HSY}	-	4.76	-	us	
ooeh pulse width	t_{OEH}	-	3.52	-	us	
sample & hold disable time	t_{DIS1}	-	5.82	-	us	
ooe1(2)(3) pulse width	t_{OEV}	-	17.2	-	us	
ocpv pulse width	t_{CPV}	-	$t_H/2$	-	us	
ocpo - ooeh time diff.	t_1	-	4.4	-	us	
ocpv - opda time diff.	t_2	-	8.56	-	us	
ooe1 - opda time diff.	t_3	-	16.6	-	us	
ocpo - opda time diff.	t_4	-	5.5	-	us	
iohsy - opsi time diff.	t_5	-	4.88	-	us	
opsi pulse width	t_{psiw}	-	4.8	-	us	
ostv1(2) setup time	t_{SUV}	-	$t_H/2$	-	us	
ostv1(2) pulse width	t_{STV}	-	1	-	t_H	
iovsy - ostv1(2) time diff.	$t_{VS1(2)}$	-	18(27)	-	t_H	Note1)

Note1) Values in brackets correspond to PAL mode

7-4) 480 * 234 mode (2.5", 3.5")

a. Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
iosci period	t_{OSC}	100.2	104.2	109.2	ns	
icsy period	T_H	61.5	63.5	65.5	us	
icsy pulse width	t_{CSYN}	4	4.7	5.4	us	
icsy rising time	T_{cr}	–	–	700	ns	
icsy falling time	T_{cf}	–	–	300	ns	
ivsync pulse width	t_{VSY}	1	3	5	t_H	
ivsync rising time	T_{vr}	–	–	700	ns	
ivsync falling time	T_{vf}	–	–	1.5	us	
Horizontal lines per field		256	262.5	268	line	Note1

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
rising time	t_r	–	–	10	ns	
falling time	t_f	–	–	10	ns	
clock pulse width	t_{CPH}	–	3	–	t_{OSC}	
clock pulse duty	t_{CWH}	30	33	40	%	
osth setup time	t_{SUH}	–	$t_{CPH}/2$	–	ns	
osth pulse width	t_{STH}	–	1	–	t_{CPH}	
iohsy pulse width	t_{HSY}	–	4.76	–	us	
ooeh pulse width	t_{OEH}	–	3.52	–	us	
sample & hold disable time	t_{DIS1}	–	5.82	–	us	
ooe1(2)(3) pulse width	t_{OEV}	–	17.2	–	us	
ocpv pulse width	t_{CPV}	–	$t_H/2$	–	us	
ocpo – ooeh time diff.	t_1	–	4.4	–	us	
ocpv – opda time diff.	t_2	–	8.56	–	us	
ooe1 – opda time diff.	t_3	–	16.6	–	us	
ocpo – opda time diff.	t_4	–	5.5	–	us	
iohsy – opsi time diff.	t_5	–	4.88	–	us	
opsi pulse width	t_{psiw}	–	4.8	–	us	
ostv1(2) setup time	t_{SUV}	–	$t_H/2$	–	us	
ostv1(2) pulse width	t_{STV}	–	1	–	t_H	
iovsy – ostv1(2) time diff.	$t_{VS1(2)}$	–	18(27)	–	t_H	Note1)

Note1) Values in brackets correspond to PAL mode

7-5) 1920 * 234 mode (9")

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
iosci period	t_{OSC}	50.1	52.1	54.1	ns	
icsy period	T_H	61.5	63.5	65.5	us	
icsy pulse width	t_{CSYN}	4	4.7	5.4	us	
icsy rising time	T_{cr}	-	-	700	ns	
icsy falling time	T_{cf}	-	-	300	ns	
ivsync pulse width	t_{VSY}	1	3	5	t_H	
ivsync rising time	T_{vr}	-	-	700	ns	
ivsync falling time	T_{vf}	-	-	1.5	us	
Horizontal lines per field		256	262.5	268	line	Note1

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
rising time	t_r	-	-	10	ns	
falling time	t_f	-	-	10	ns	
clock pulse width	t_{CPH}	-	1.5	-	t_{OSC}	
clock pulse duty	t_{CWH}	30	33(67)	70	%	
osth setup time	t_{SUH}	-	$t_{CPH}/2$	-	ns	
osth pulse width	t_{STH}	-	1	-	t_{CPH}	
iohsy pulse width	t_{HSY}	-	4.6	-	us	
ooeh pulse width	t_{OEH}	-	3.6	-	us	
sample & hold disable time	t_{DIS1}	-	5.26	-	us	
ooe1(2)(3) pulse width	t_{OEV}	-	16	-	us	
ocpv pulse width	t_{CPV}	-	$t_H/2$	-	us	
ocpo - ooeh time diff.	t_1	-	4.08	-	us	
ocpv - opda time diff.	t_2	-	8.72	-	us	
ooe1 - opda time diff.	t_3	-	16.8	-	us	
ocpo - opda time diff.	t_4	-	5	-	us	
iohsy - opsi time diff.	t_5	-	3.3	-	us	
opsi pulse width	t_{psiw}	-	4.64	-	us	
ostv1(2) setup time	t_{SUV}	-	$t_H/2$	-	us	
ostv1(2) pulse width	t_{STV}	-	1	-	t_H	
iovsy - ostv1(2) time diff.	$t_{VS1(2)}$	-	18(27)	-	t_H	Note1)

Note1) Values in brackets correspond to PAL mode

7-6) 960 * 234 mode (Delta mode, 3.5")

a. Input signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
iosci period	t_{OSC}	50.1	52.1	54.1	ns	
icsy period	T_H	61.5	63.5	65.5	us	
icsy pulse width	t_{CSYN}	4	4.7	5.4	us	
icsy rising time	T_{cr}	-	-	700	ns	
icsy falling time	T_{cf}	-	-	300	ns	
ivsync pulse width	t_{VSY}	1	3	5	t_H	
ivsync rising time	T_{vr}	-	-	700	ns	
ivsync falling time	T_{vf}	-	-	1.5	us	
Horizontal lines per field		256	262.5	268	line	Note1

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Remark
rising time	t_r	-	-	10	ns	
falling time	t_f	-	-	10	ns	
clock pulse width	t_{CPH}	-	3	-	t_{OSC}	
clock pulse duty	t_{CWH}	30	33(67)	70	%	
osth setup time	t_{SUH}	-	$t_{CPH}/2$	-	ns	
osth pulse width	t_{STH}	-	1	-	t_{CPH}	
iohsy pulse width	t_{HSY}	-	4.6	-	us	
ooeh pulse width	t_{OEH}	-	3.6	-	us	
sample & hold disable time	t_{DIS1}	-	5.26	-	us	
ooe1(2)(3) pulse width	t_{OEV}	-	16	-	us	
ocpv pulse width	t_{CPV}	-	$t_H/2$	-	us	
ocpo - ooeh time diff.	t_1	-	4.08	-	us	
ocpv - opda time diff.	t_2	-	8.72	-	us	
ooe1 - opda time diff.	t_3	-	16.8	-	us	
ocpo - opda time diff.	t_4	-	5	-	us	
iohsy - opsi time diff.	t_5	-	3.3	-	us	
opsi pulse width	t_{psiw}	-	4.64	-	us	
ostv1(2) setup time	t_{SUV}	-	$t_H/2$	-	us	
ostv1(2) pulse width	t_{STV}	-	1	-	t_H	
iovsy - ostv1(2) time diff.	$t_{VS1(2)}$	-	18(27)	-	t_H	Note1)

Note1) Values in brackets correspond to PAL mode

8. Display Position

8-1. Horizontal position

Items	Symbol	Conditions	NTSC	PAL	unit	Remark
Horizontal Start Position	HPOS	-	11.78	11.89	us	*)
Horizontal display Area	HDIS	-	50.01	50.36	us	**)

*) Sampling start based on the csy's rising edge

**) Horizontal display position is changed by delay time

8-2. Vertical position

Items	Symbol	Conditions		Display mode					unit	Remark
				Full Normal	Wide	Zoom1	Zoom2	Zoom3		
Vertical Start Position	VPOS	NTSC	Odd	25	25	55	41	56	Line	*)
			Even	288	288	318	304	318		
		PAL	Odd	31	31	65	51	68	Line	
			Even	343	343	377	363	380		
Vertical display Position	VDIS	NTSC		234	234	176	204	204	Line	
		PAL		273	273	199	234	234	Line	

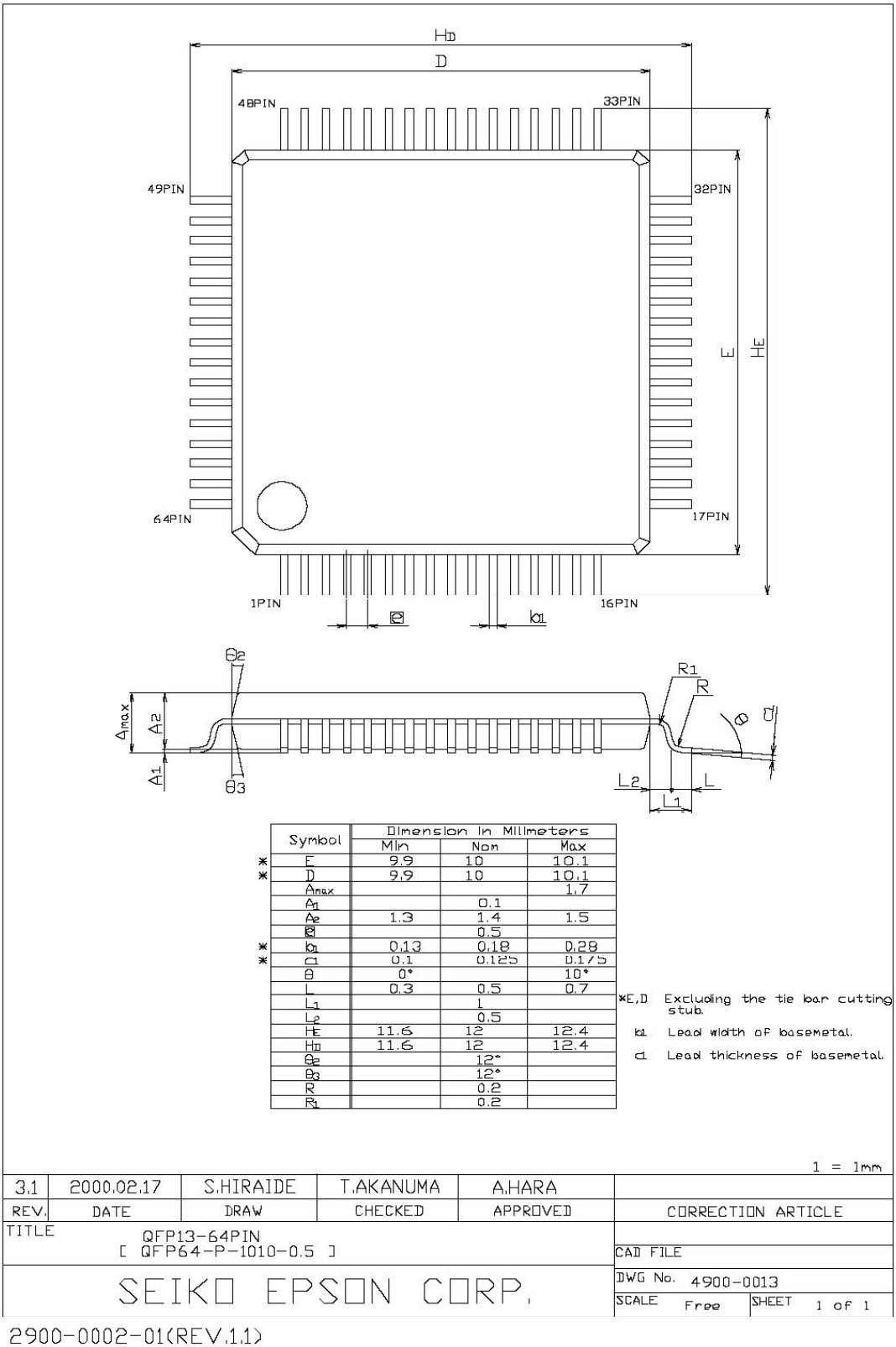
*) Sampling start line number base on Line no counter

9. Reliability test items

No.	Test items	Conditions	Remark
1	High temperature storage	Ta = 150℃ 240h	
2	Low temperature storage	Ta = -60℃ 240h	
3	High temperature operation	Ta = 85℃ 240h	
4	Low temperature operation	Ta = -40℃ 240h	
5	High temperature and High huminity	Ta = 80℃, 95%RH 240h	operation
6	Heat shock	-30℃, 25℃, 80℃ 200cycle 30min, 5mun, 30min	non- operation
7	Electrostatic discharge	±200V, 200pF(0Ω) once for each terminal	non- operation

Note : Ta = Ambient temperature

10. Package information



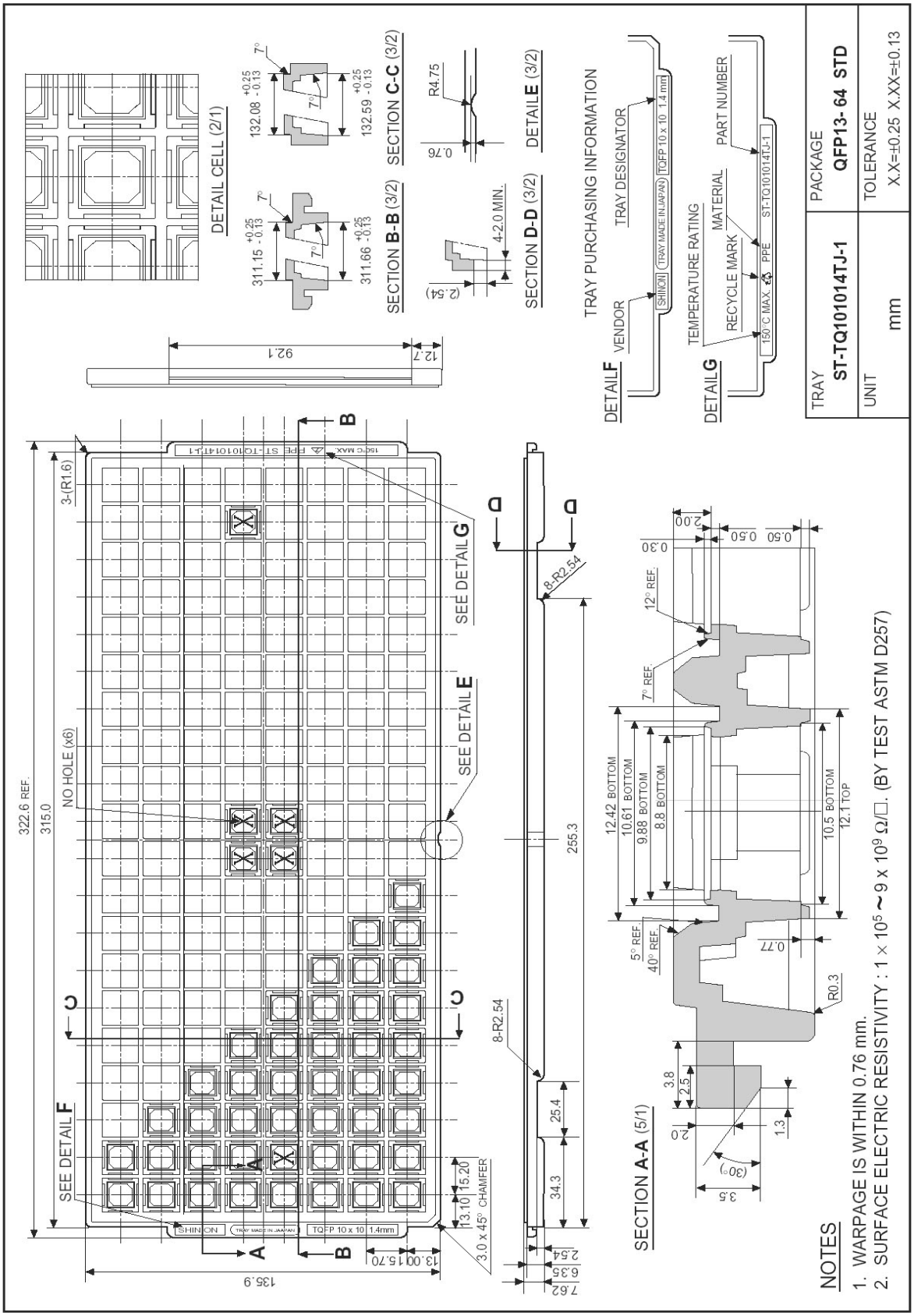
	Symbol	Dimension in Millmeters		
		Min	Nom	Max
*	E	9.9	10	10.1
*	D	9.9	10	10.1
	Amax			1.7
	A1		0.1	
	A2	1.3	1.4	1.5
	e		0.5	
*	b1	0.13	0.18	0.28
*	c1	0.1	0.125	0.175
	θ	0°		10°
	L	0.3	0.5	0.7
	L1		1	
	L2		0.5	
	HE	11.6	12	12.4
	HD	11.6	12	12.4
	θ2		12°	
	θ3		12°	
	R		0.2	
	R1		0.2	

*E,D Excluding the tie bar cutting stub.
b1 Lead width of basemetal.
c1 Lead thickness of basemetal.

1 = 1mm

3.1	2000.02.17	S.HIRAIDE	T.AKANUMA	A.HARA	
REV.	DATE	DRAW	CHECKED	APPROVED	CORRECTION ARTICLE
TITLE	QFP13-64PIN [QFP64-P-1010-0.5]				CAD FILE
SEIKO EPSON CORP.					DWG No. 4900-0013
					SCALE Free SHEET 1 of 1

2900-0002-01(REV.1.1)



11. Usage Precautions

11-1. Storage and handling before opening

Control the storage environment to prevent drastic temperature changes, which can lead to moisture condensation. Do not place any load on the package during storage.

11-2. Hygroscopic indicator monitoring

Because the appearance of normal silica gel do not change when absorbing moisture, a special blue gel manufactured by impregnating silica gel with cobalt chloride($CoCl_2$) is used as moisture absorption indicator. The molecular formula of this gel changes to $CoCl_2 \cdot 6H_2O$(pink) when it has absorbed moisture. Before mounting, you should check the silica gel condition.

11-3. Handling after opening

Do not bring any materials that can generate static electricity (plastic materials, chemical fibers, etc.) into the working area, and periodically check electrostatic conditions. Handle devices only with anti-statically treated materials or in conductive containers. Personnel should use wrist straps or other body grounding means.

11-4. Storage after opening

Due to the properties of the molding resin, plastic packages are prone to moisture absorption, also at room temperature if left for long periods of time. If the package is then inserted in the reflow oven while having absorbed moisture, cracks can develop in the resin, and joint between resin and lead frame can deteriorate. The standard storage periods for SMD packages shownbelow should therefore not be exceeded.

Table 11.1 Storage conditions after opening moisture proof packing

Storage rank	Storage condition after opening moisture proof packing	Guarantee period after opening moisture proof packing
SE 3	≤ 30℃/70% RH	Within 168 hours(1 week)

- Storage period before opening a moisture proof packing 12 months at less than ≤ 30℃/85% RH
- If reflow a package for 2 times, it should be done within storage periods for each package rank
- If the storage period is exceeded or it is undefined, perform baking again before mounting.
  Example : 125℃ for 24 hours (See section 11.5)

11-5. Baking

If the storage period is exceeded after opening, or if the opening data undefined, or if the hygroscopic indicator (blue gel) has turned pink, perform baking as indicated below.

Table 11.2 Baking conditions for surface mount devices

Baking Temperature / Package thickness	125℃
t 〈 2 mm	5 hours
t ≥ 2 mm	24 hours

Note : Baking may be performed up to maximum of two times

11-6. Soldering conditions

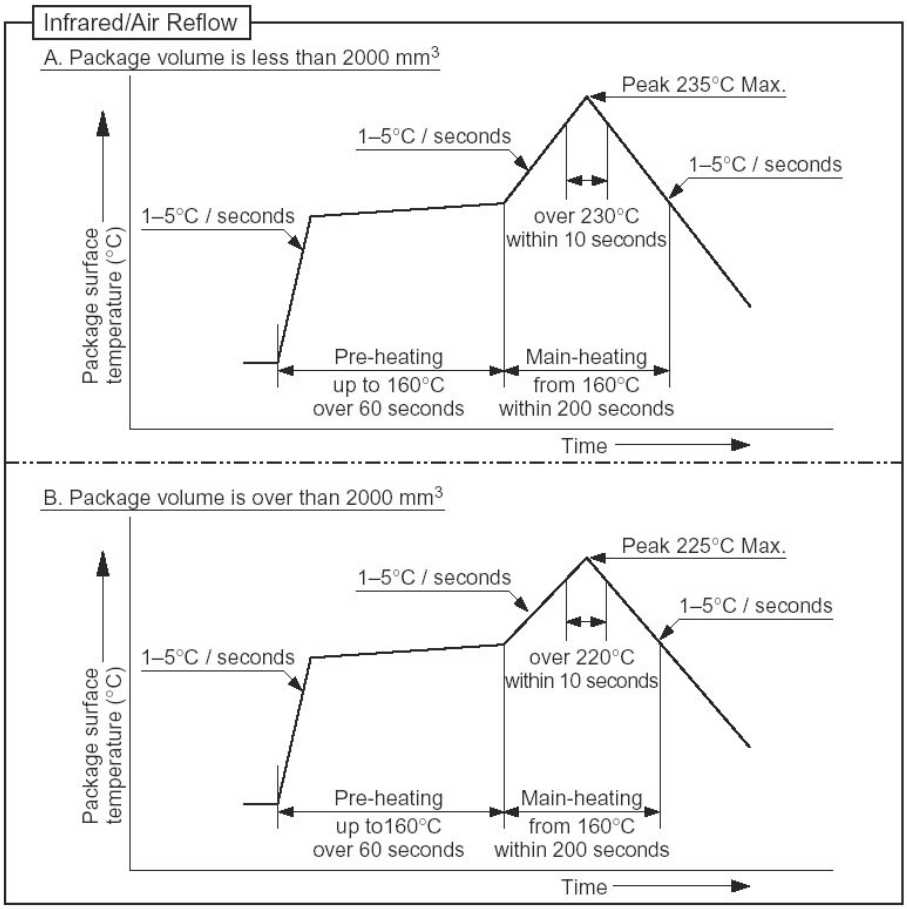
When soldering surface mount devices (QFP) using an overall soldering method such as reflow or vapor phase soldering, be sure to observe the storage conditions given in Table 11.1, This is important to prevent the possibility of crack and other damage, which increases if plastic package absorb moisture.

11-6-1 Infrared / air reflow

- Temperature profile

  The temperature profile of the reflow oven (resin surface temperature) should be controlled as shown in Fig. 11.1

Fig. 11.1 Temperature profile for standard SMD package(QFP)



- Maximum temperature

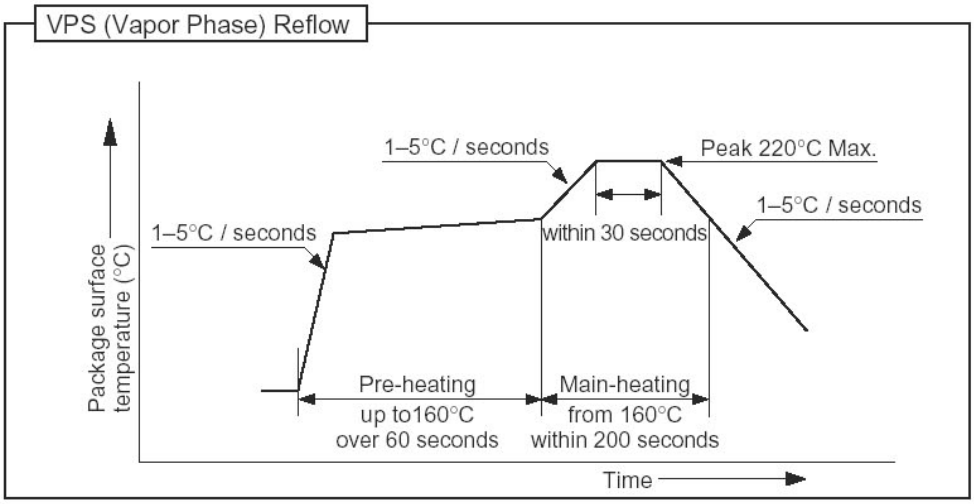
  The maximum resin surface temperature should be 235℃, for a duration of 10 seconds or less. If possible, lower temperatures and shorter times are preferable.

11-6-2 Vapor phase reflow

- Temperature profile

  The temperature profile of the vapor phase reflow oven (resin surface temperature) should be controlled as shown in Fig. 11.2

Fig. 11.2 Temperature profile for standard SMD package(QFP)



● Temperature rise ratio

The maximum rise should be kept within 1- 5℃/minute, and the curve should be as shallow as possible.

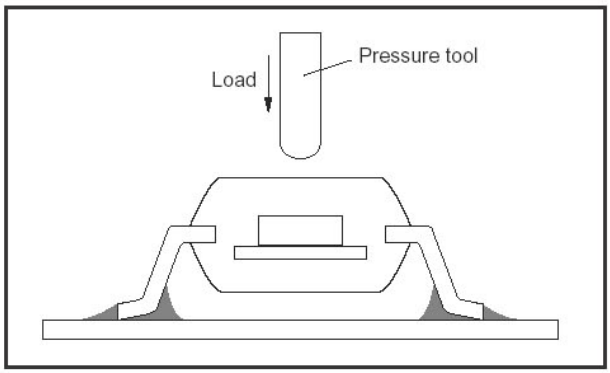
11-6-3 Solder dipping (wave soldering etc)

Because solder dipping cause a drastic change in package temperature which can damage the device, Seiko Epson normally does not approve solder dipping methods for SMD. However, certain SOP with good heat resistance may be mounted using solder dipping.

11-7 Mounting Precautions

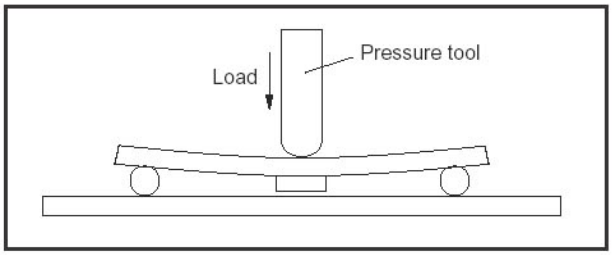
Mechanical stress during mounting should be minimized (EIAJ-ED-4702)

Fig. 11.3 Package Strength



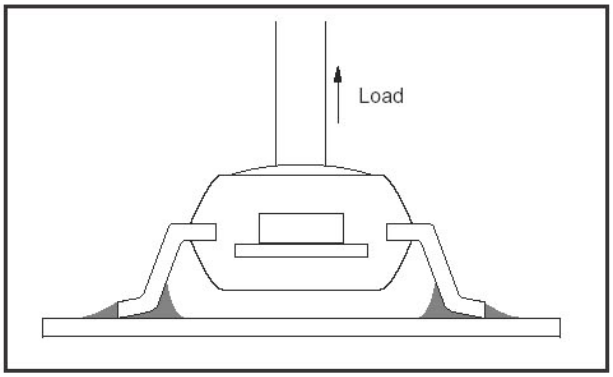
① Package load
The force exerted on the package surface during mounting should not exceed 1 kgf (10 N).

Fig. 11.4 PCB Bending Strength



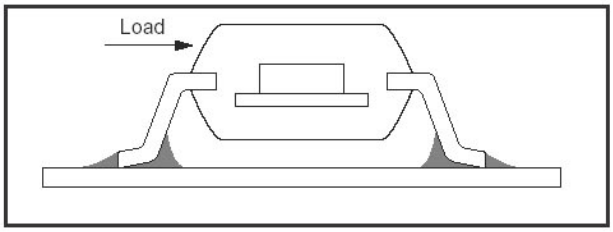
② PCB bending stress
For reasons of solder junction strength, PCB deflection after mounting should not exceed 2 mm.

Fig. 11.5 Pull Strength



③ Pull load
Pull stress (sudden force exerted on the package in vertical up direction) after mounting should not exceed 0.5 kgf (5 N).

Fig. 11.6 Sticking Strength



④ Sticking stress
Sticking stress (sudden force exerted on the package in sideways direction) after mounting should not exceed 0.5 kgf (5 N).

A. The timing Diagram

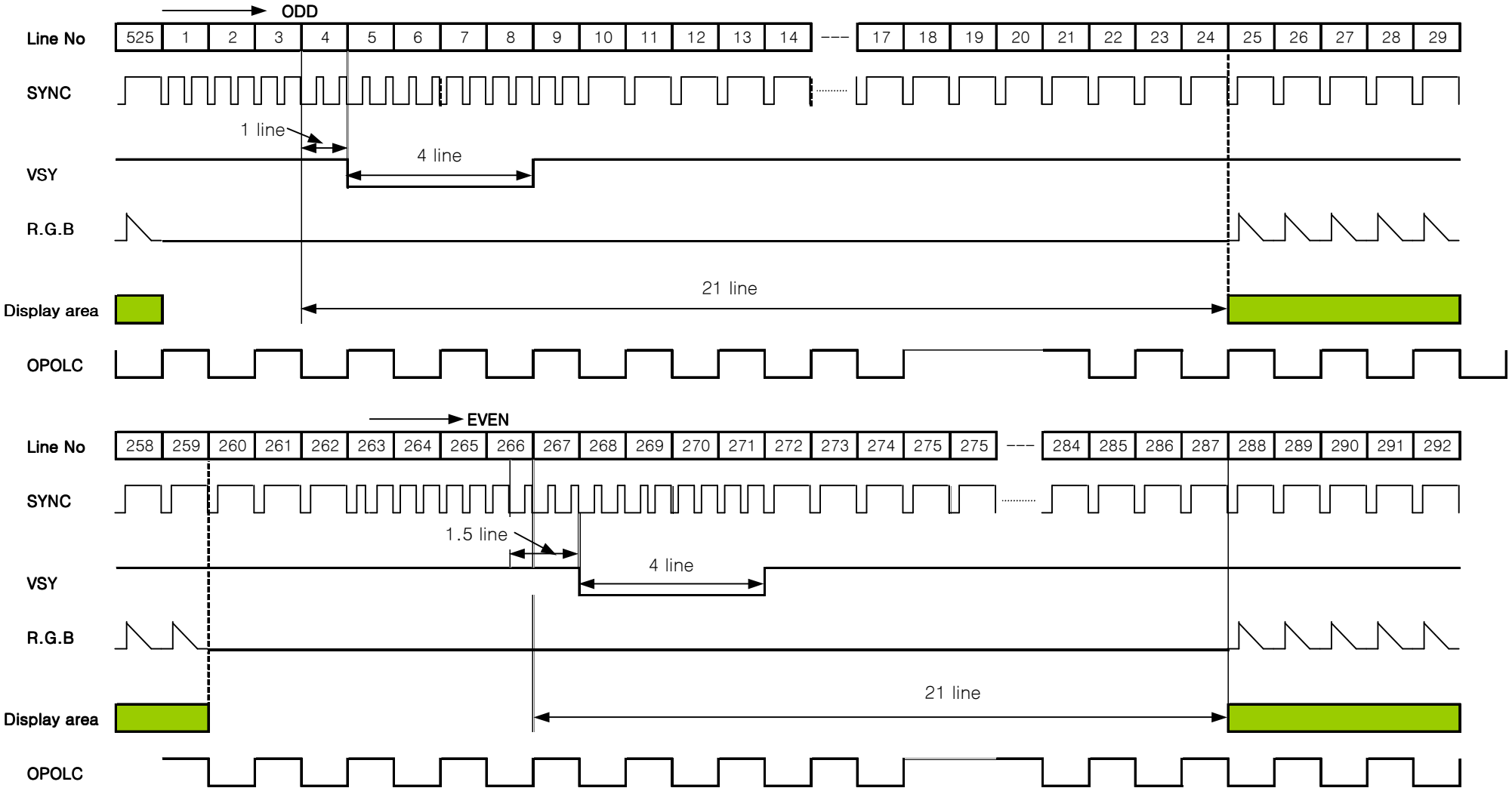


Fig.1. NTSC Vertical (iodd_sel = "High")

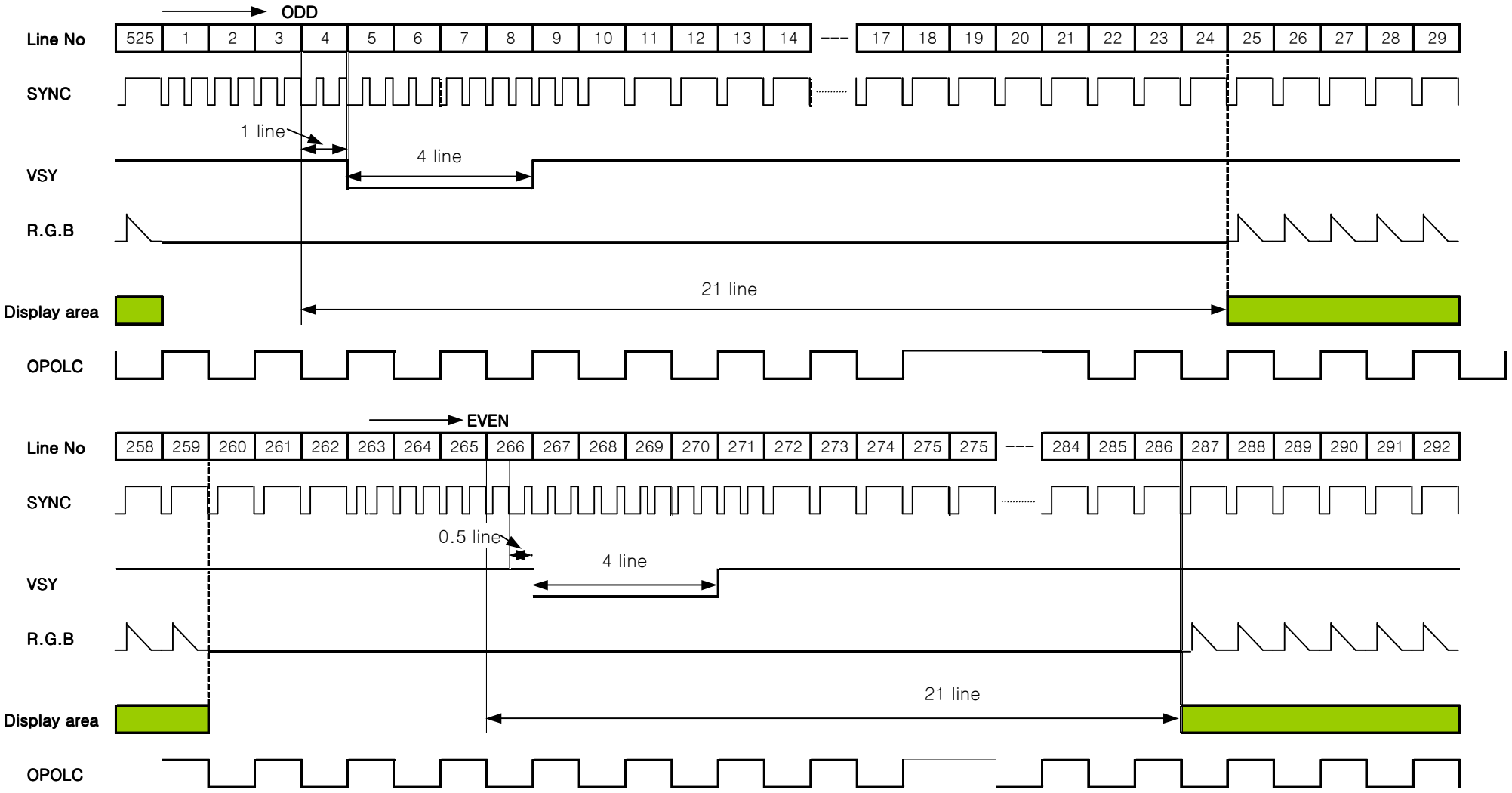


Fig.2. NTSC Vertical (iodd_sel = "Low")

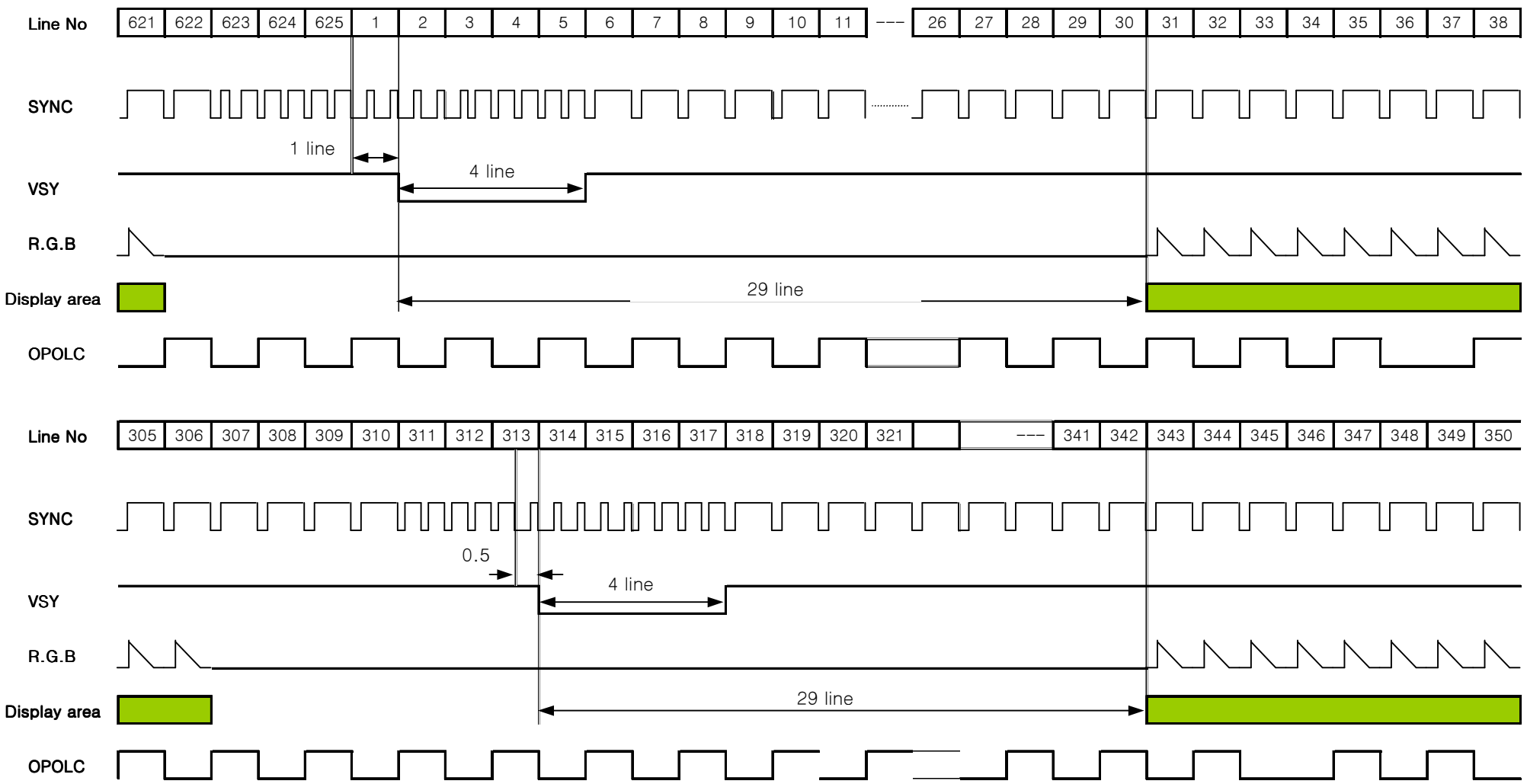


Fig.3. PAL Vertical (iz_sel = "H")

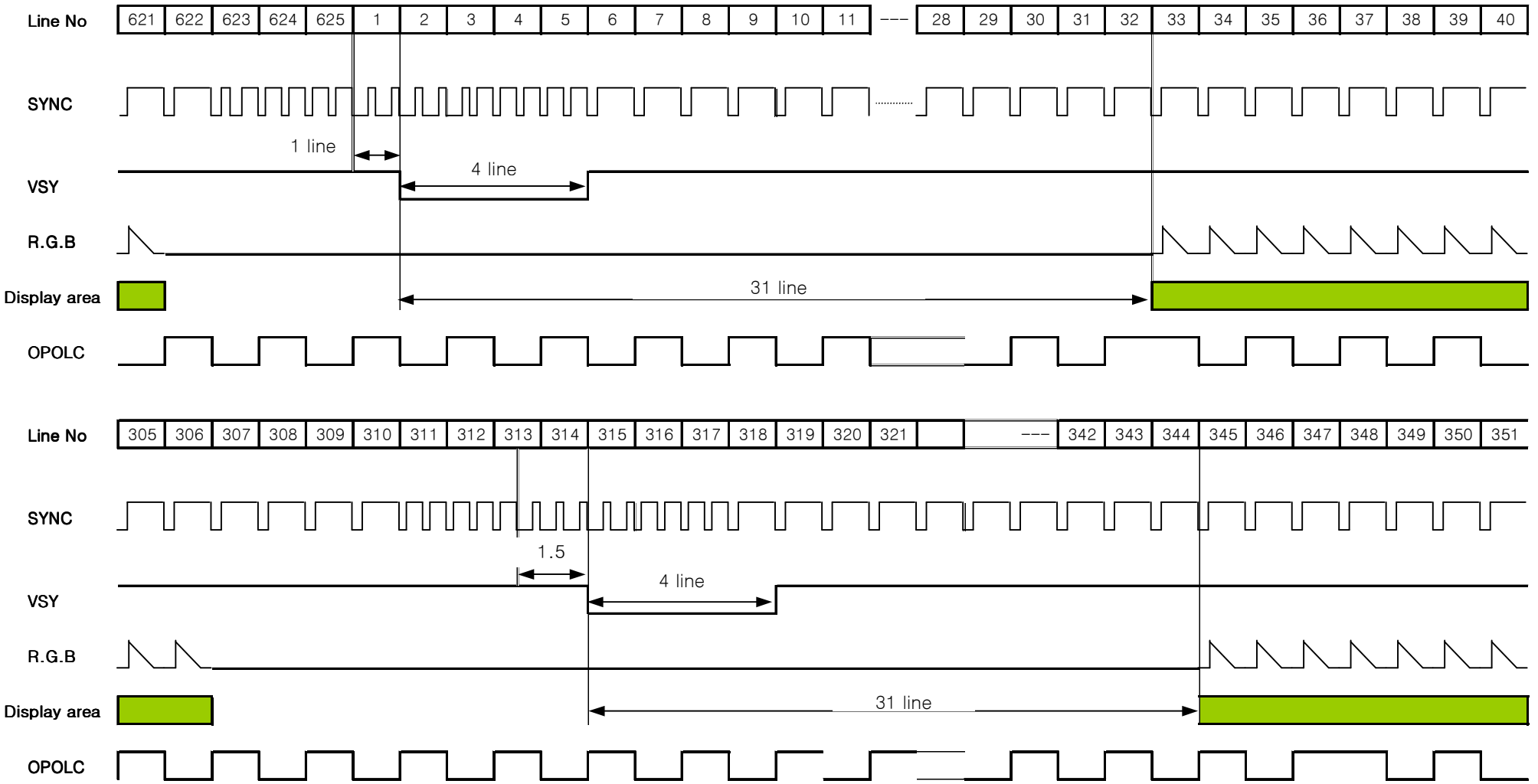
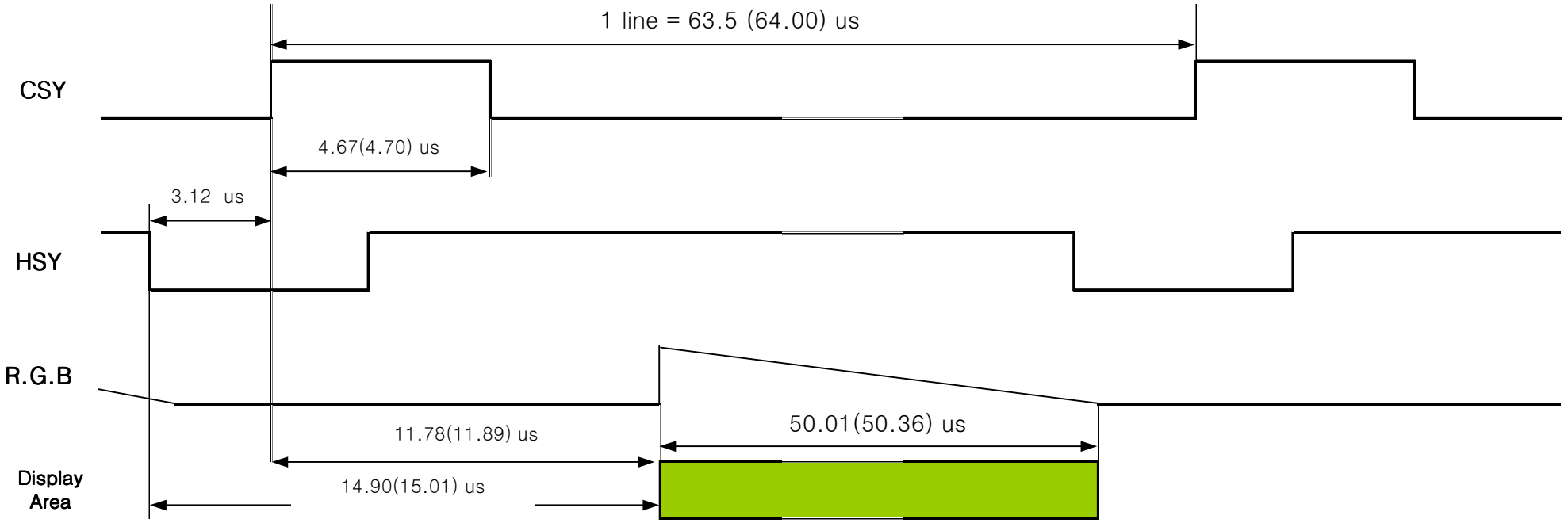


Fig.4. PAL Vertical (iz_sel = "L")



*) Values in brackets correspond to PAL mode
**) fH = 15.734(15.625) kHz
***) Horizontal display position is changed by delay time (control cpi, cpo)

Fig.5. Horizontal (NTSC/PAL)

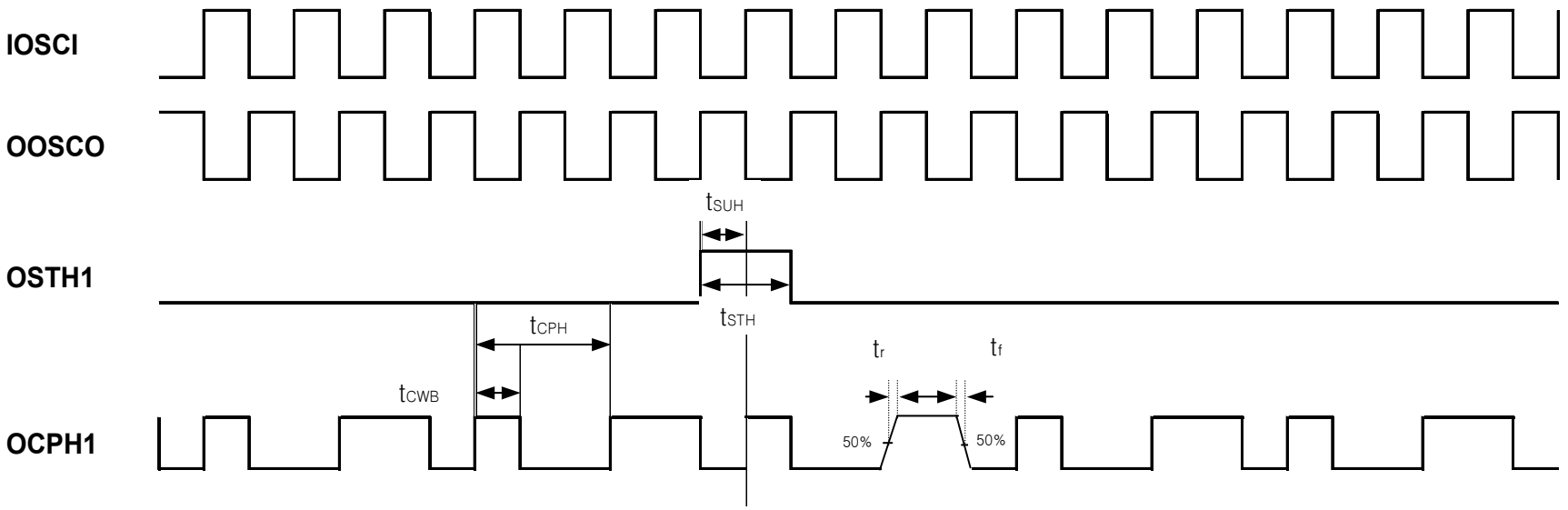


FIG.6 Sampling clock timing(1920,1440,1200,960*234mode)

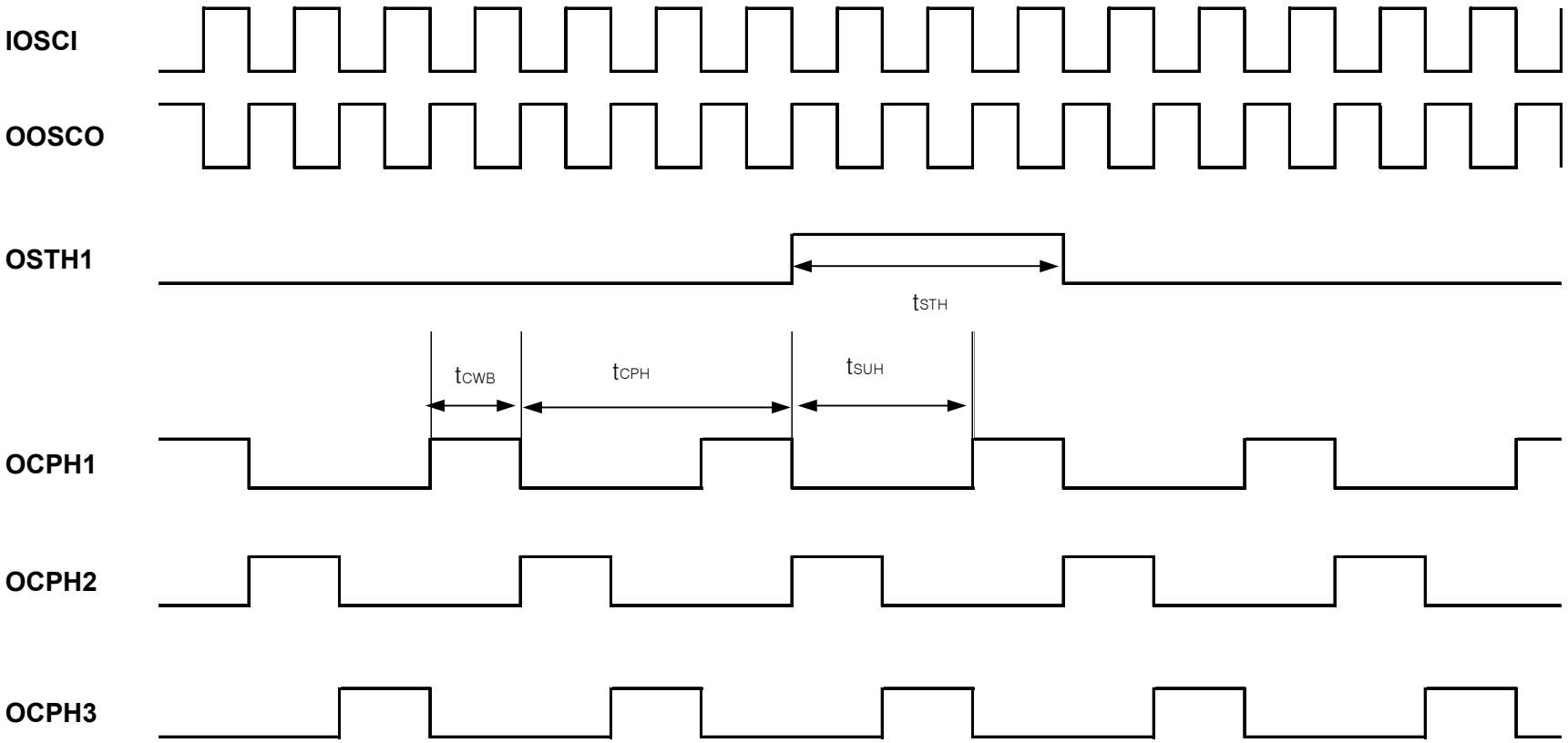


FIG.7 Sampling clock timing(960,480*234mode(Delta mode))

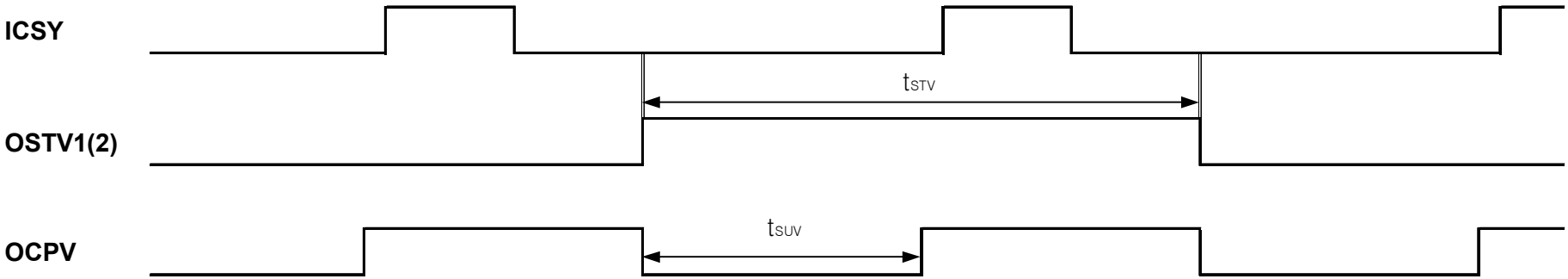


FIG.8 Vertical shift clock timing

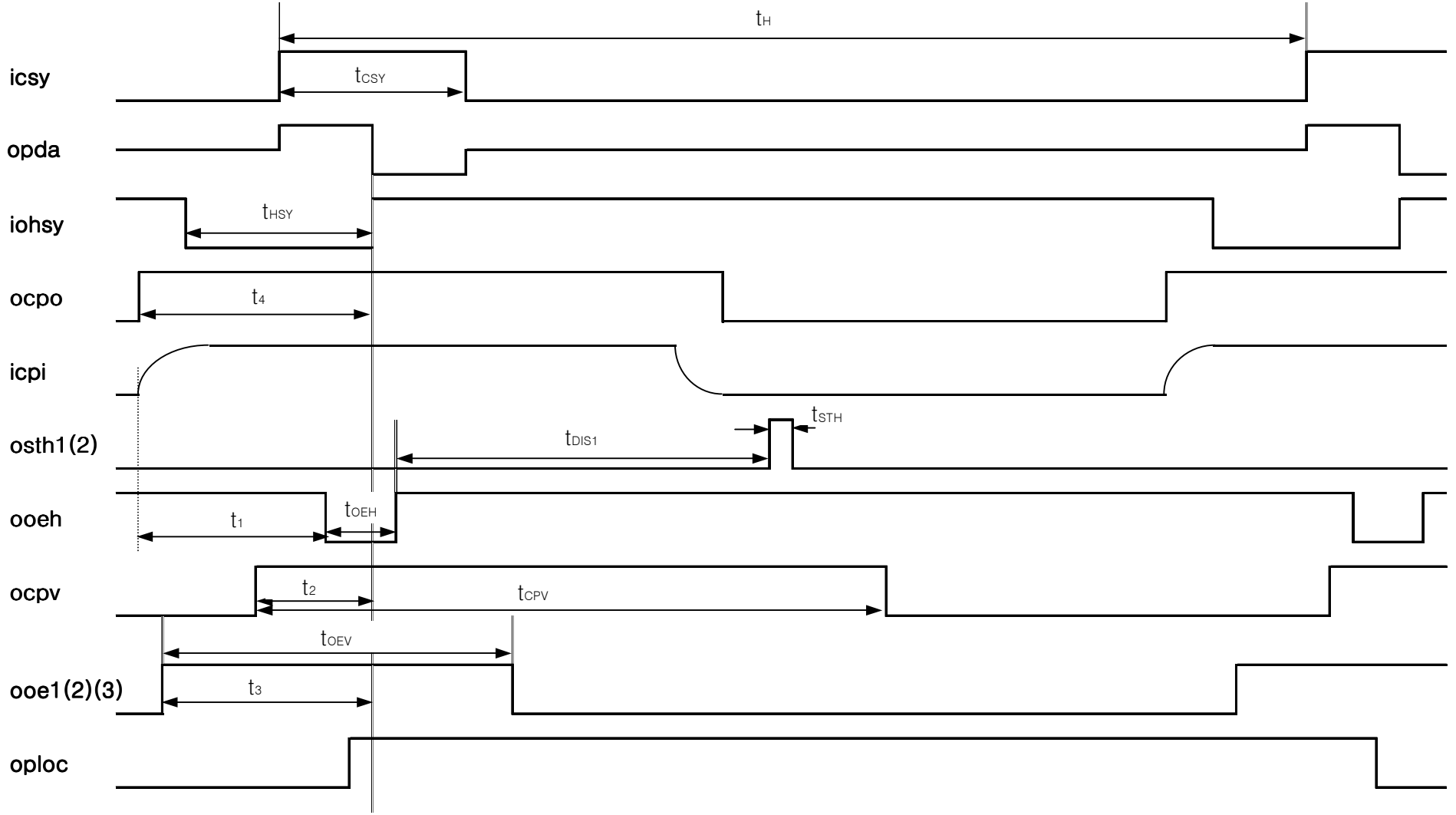


FIG.9 Horizontal Timing

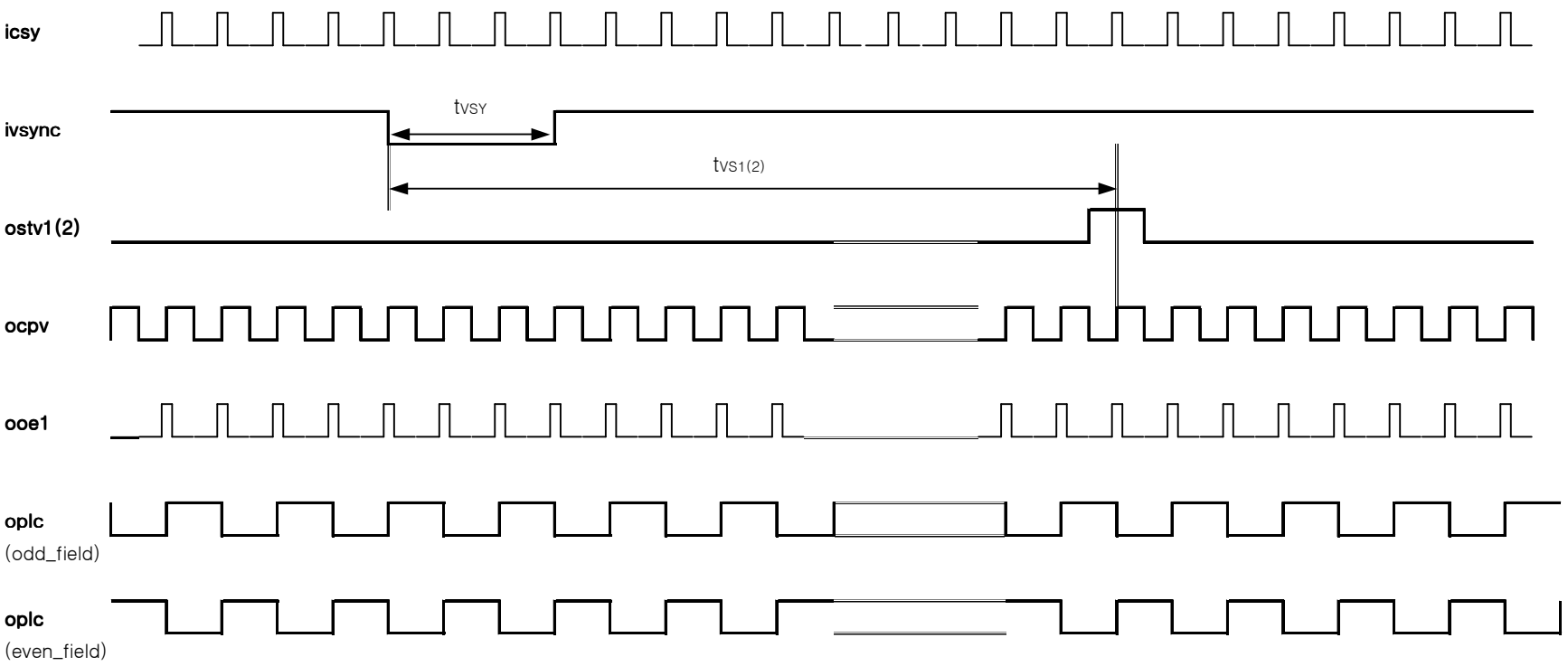
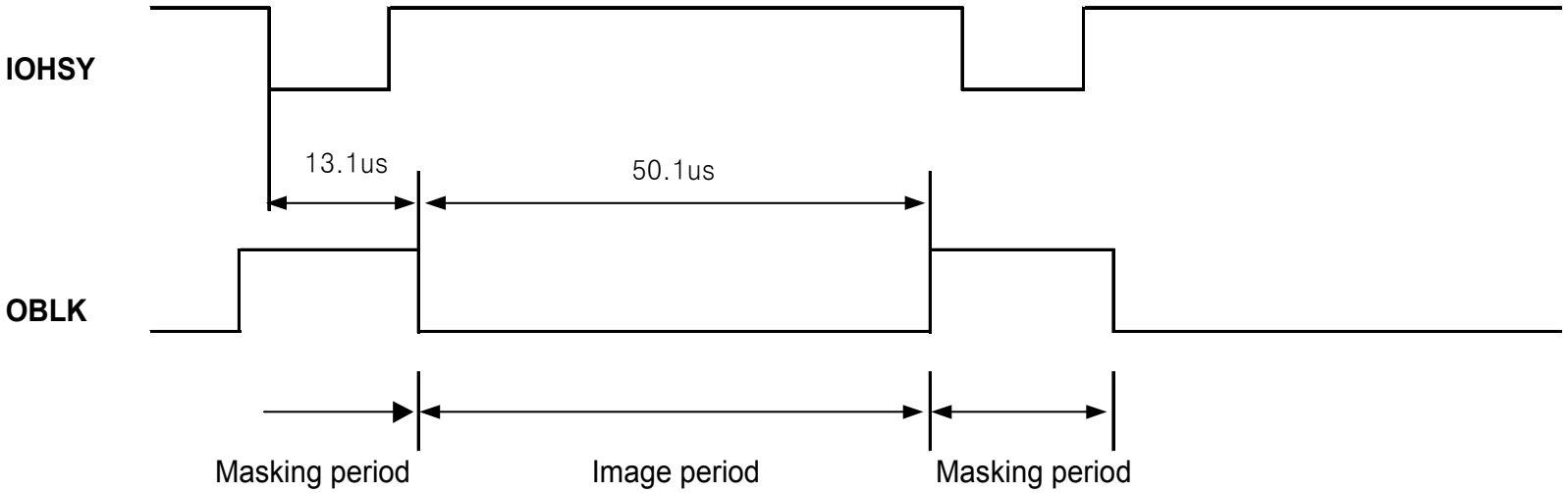


FIG.10 Vertical Timing



* Display range can adjust by H-position

FIG.11 Input/output signal waveforms(Normal center, Normal left, Normal right mode)

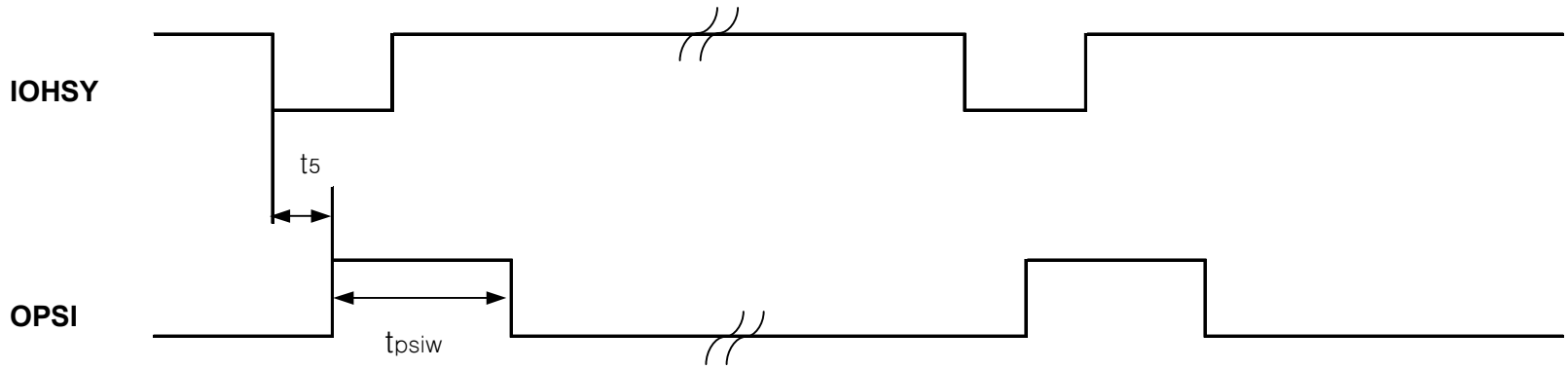
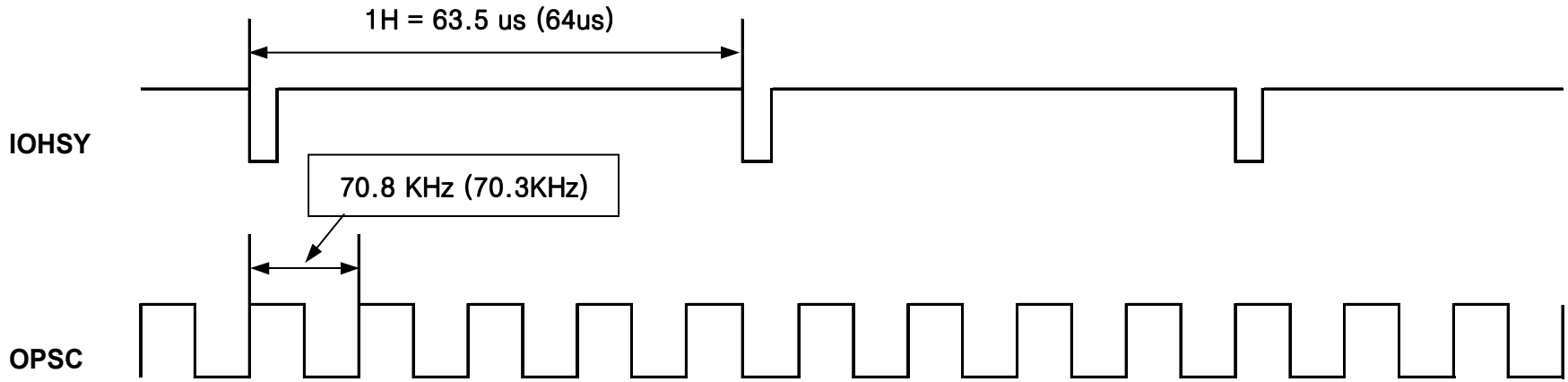


FIG.12 OPSI timing



Note1) Values in brackets correspond to PAL mode

FIG.13 OPSC dimming timing

B. Application Circuit(VCO is controlled by VL)

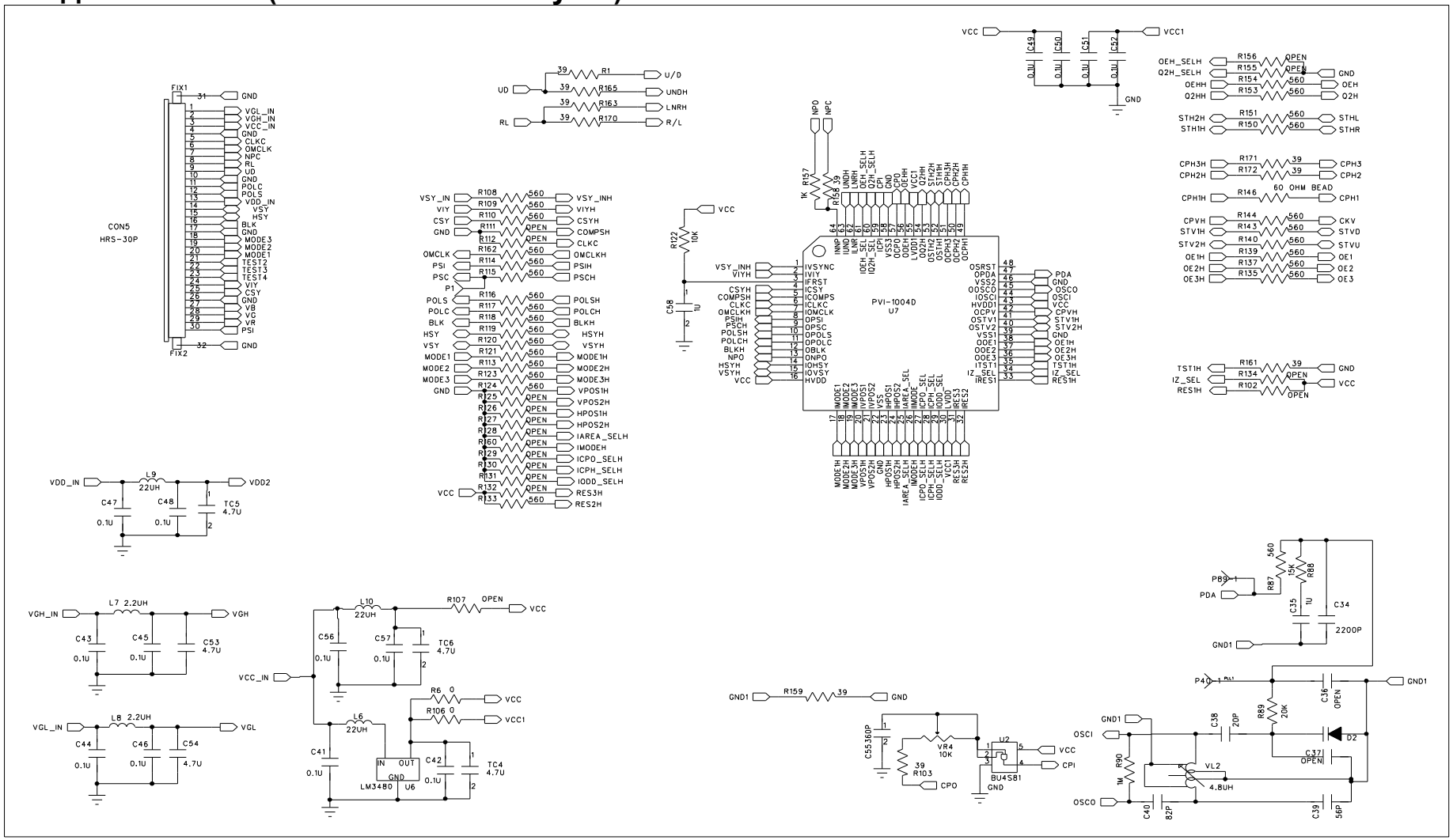


Fig.14 1920*234 mode (9 ”) (VCO is controlled by VL)

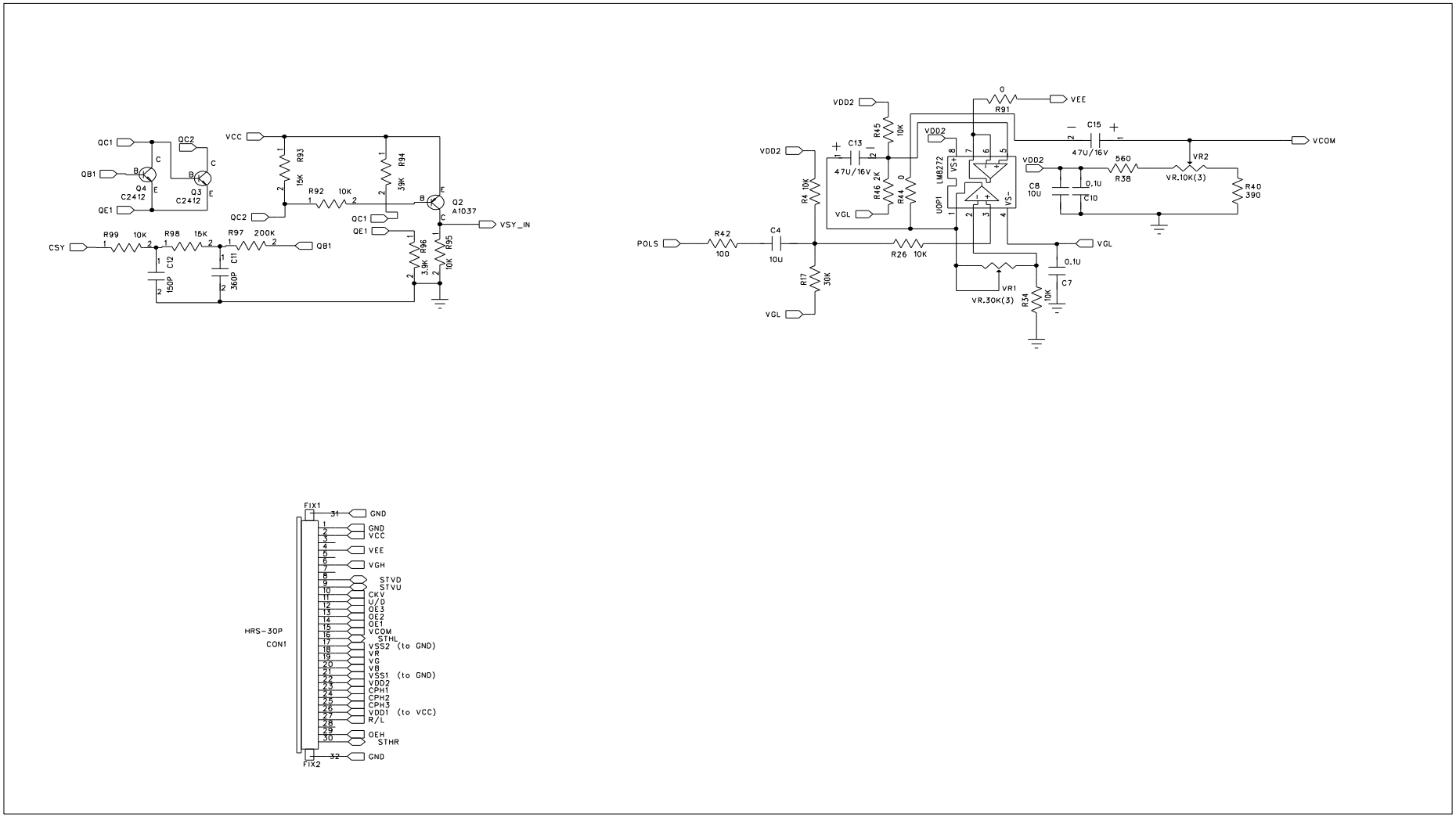


Fig.15 1920*234 mode(9”) Vcom Circuit(VCO is controlled by VL)

Table A : KEY COMPONENTS 9"(1920*234)

PART NAME	VENDER	VENDER PART NO.	SPEC	APPELLATION
VL2	SUMIDA	CP-4LB(5113-T031)	4.8U 1%	VAR.IND
U7	EPSON	PVI-1004D		TIMMING CONTROL
U6	NS	LM3480IM3-3.3		REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81		AND GATE
UOP1	NS	LM8272MM		OP
CON1,CON5	ELCO	00-6210-030-010-800		CONNECTOR(30PIN)

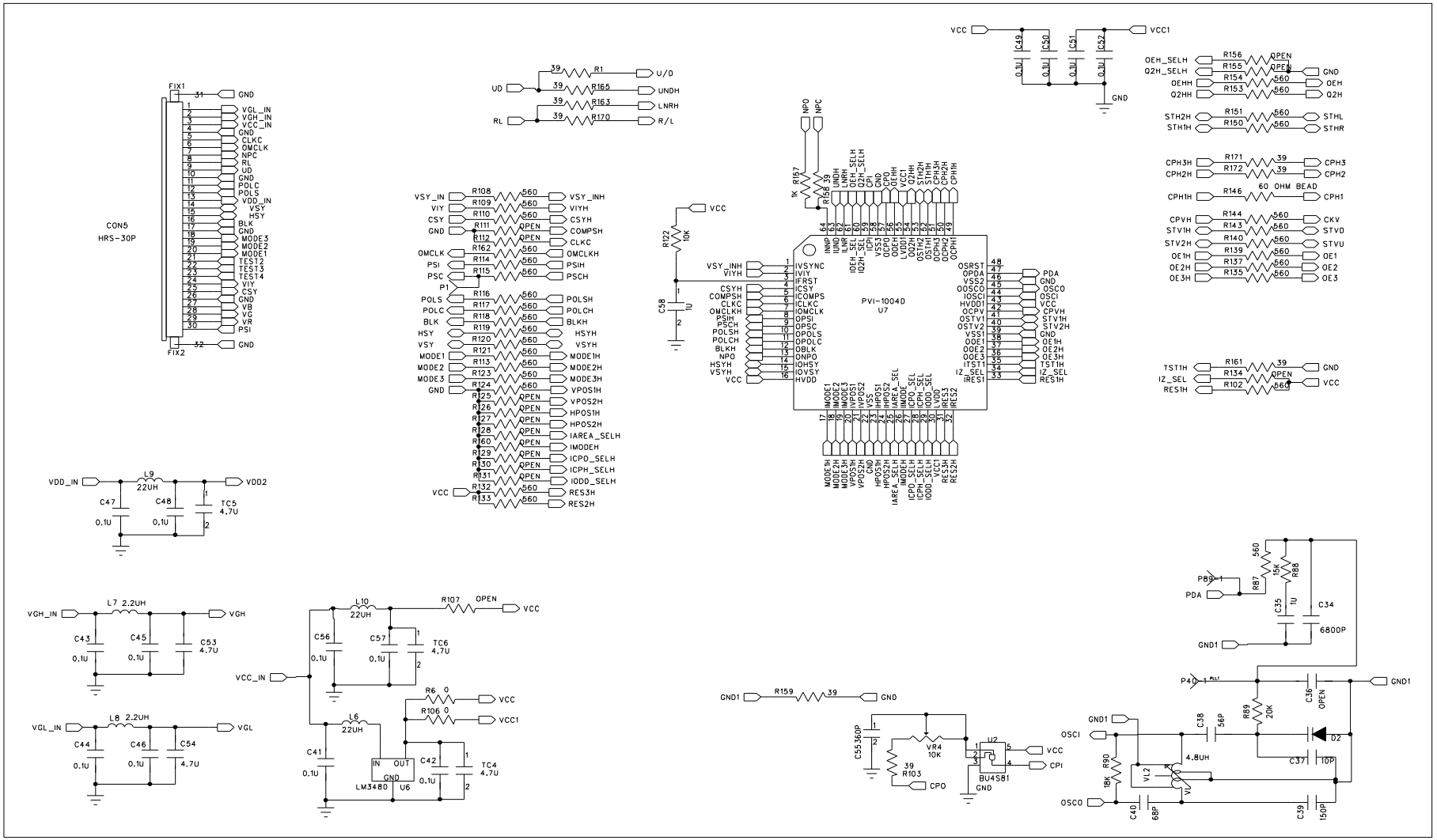


Fig.16 1440*234 mode(6.2”, 7”, 8.4”) (VCO is controlled by VL)

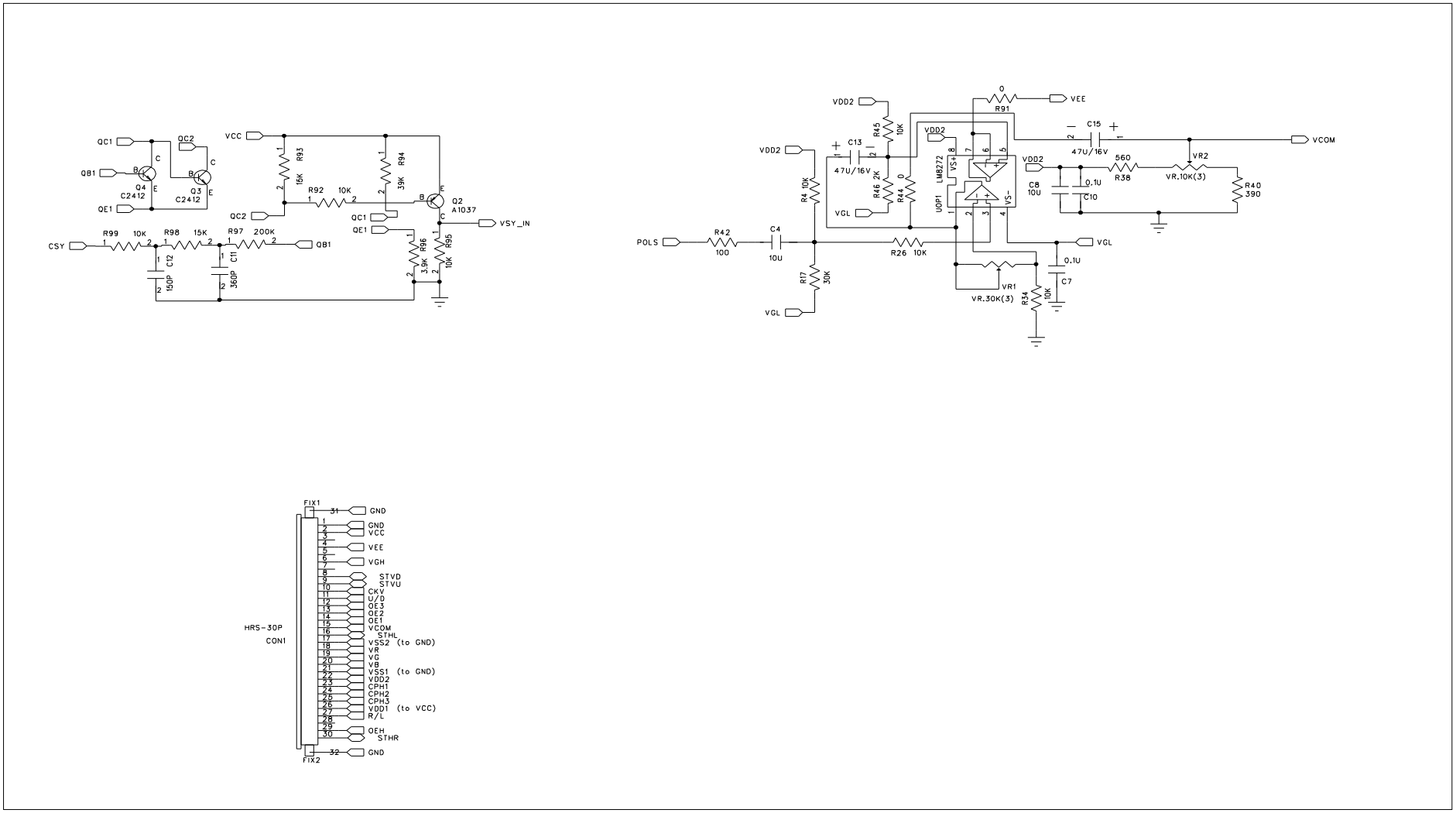


Fig.17 1440*234 mode(6.2”,7”,8.4”) Vcom Circuit(VCO is controlled by VL)

Table B : KEY COMPONENTS 6.2", 7" & 8.4"(1440*234)

PART NAME	VENDER	VENDER PART NO.	SPEC	APPELLATION
VL2	SUMIDA	CP-4LB(5113-T031)	4.8U 1%	VAR.IND
U7	EPSON	PVI-1004D		TIMMING CONTROL
U6	NS	LM3480IM3-3.3		REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81		AND GATE
UOP1	NS	LM8272MM		OP
CON1,CON5	ELCO	00-6210-030-010-800		CONNECTOR(30PIN)

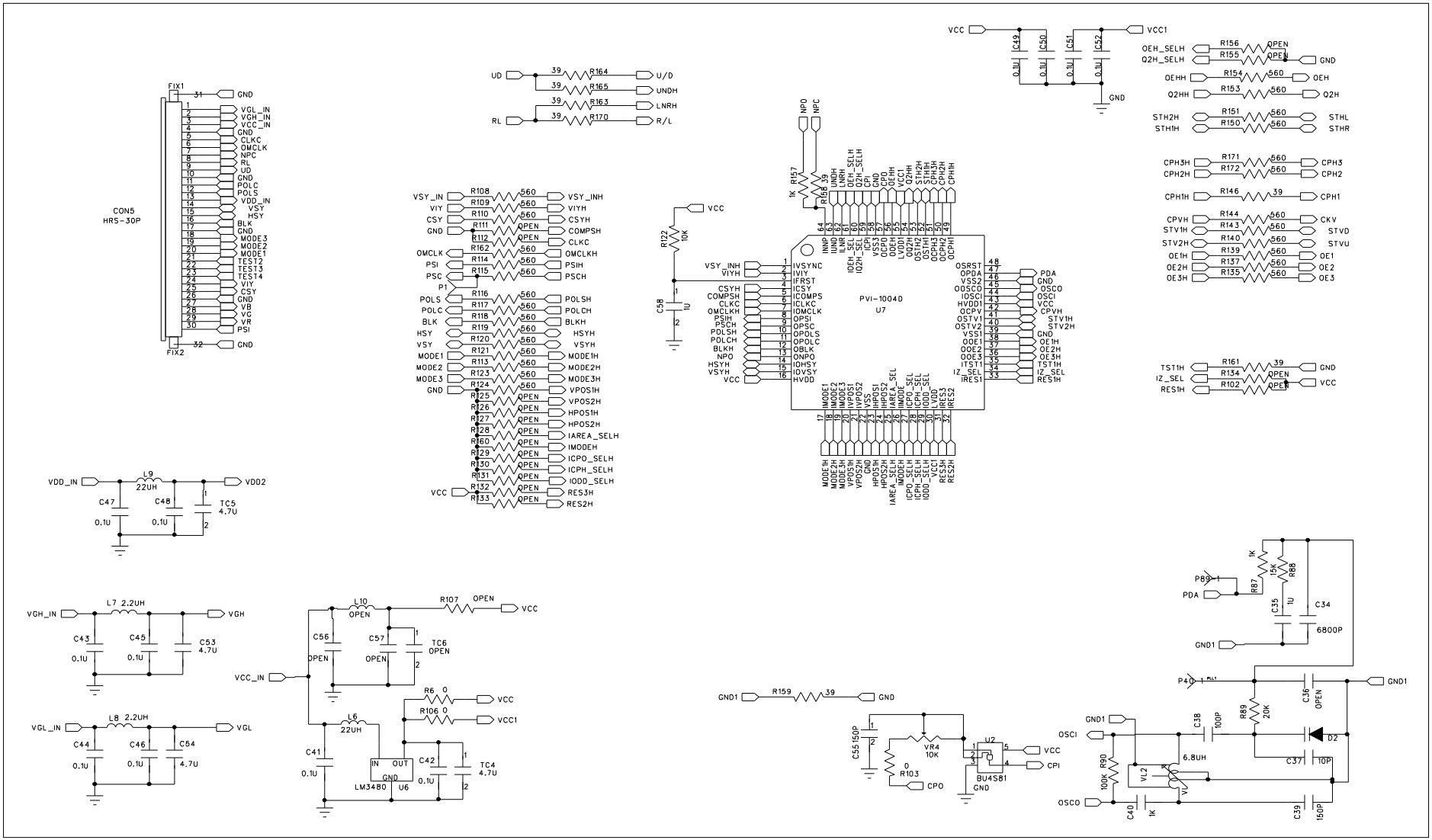
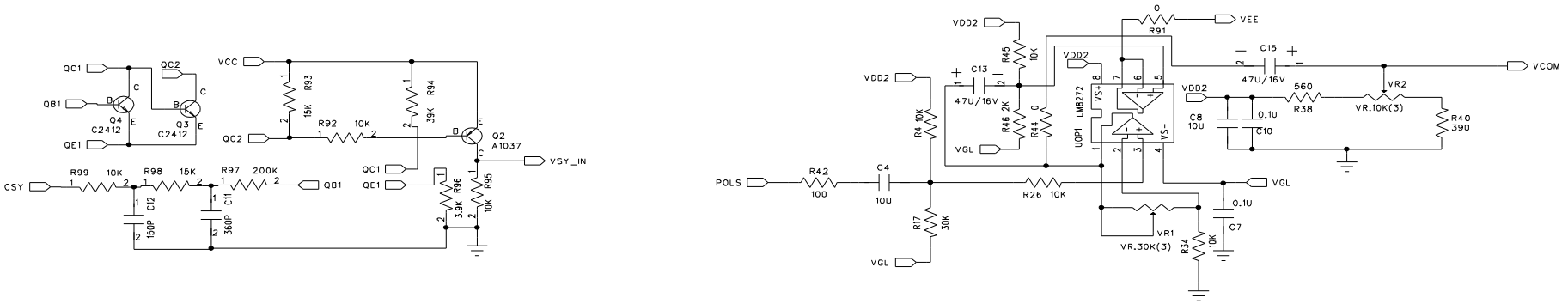


Fig.18 1200*234 mode(6.5”) (VCO is controlled by VL)



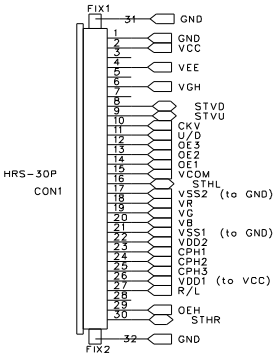


Fig.19 1200*234 mode(6.5”) Vcom Circuit(VCO is controlled by VL)

Table C : KEY COMPONENTS 6.5"(1200*234) :

PART NAME	VENDER	VENDER PART NO.	SPEC	APPELLATION
VL2	SUMIDA	CP-4LB(5113-T032)	6.8U 1%	VAR.IND
U7	EPSON	PVI-1004D		TIMMING CONTROL
U6	NS	LM3480IM3-3.3		REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81		AND GATE
UOP1	NS	LM8272MM		OP
CON1,CON5	ELCO	00-6210-030-010-800		CONNECTOR(30PIN)

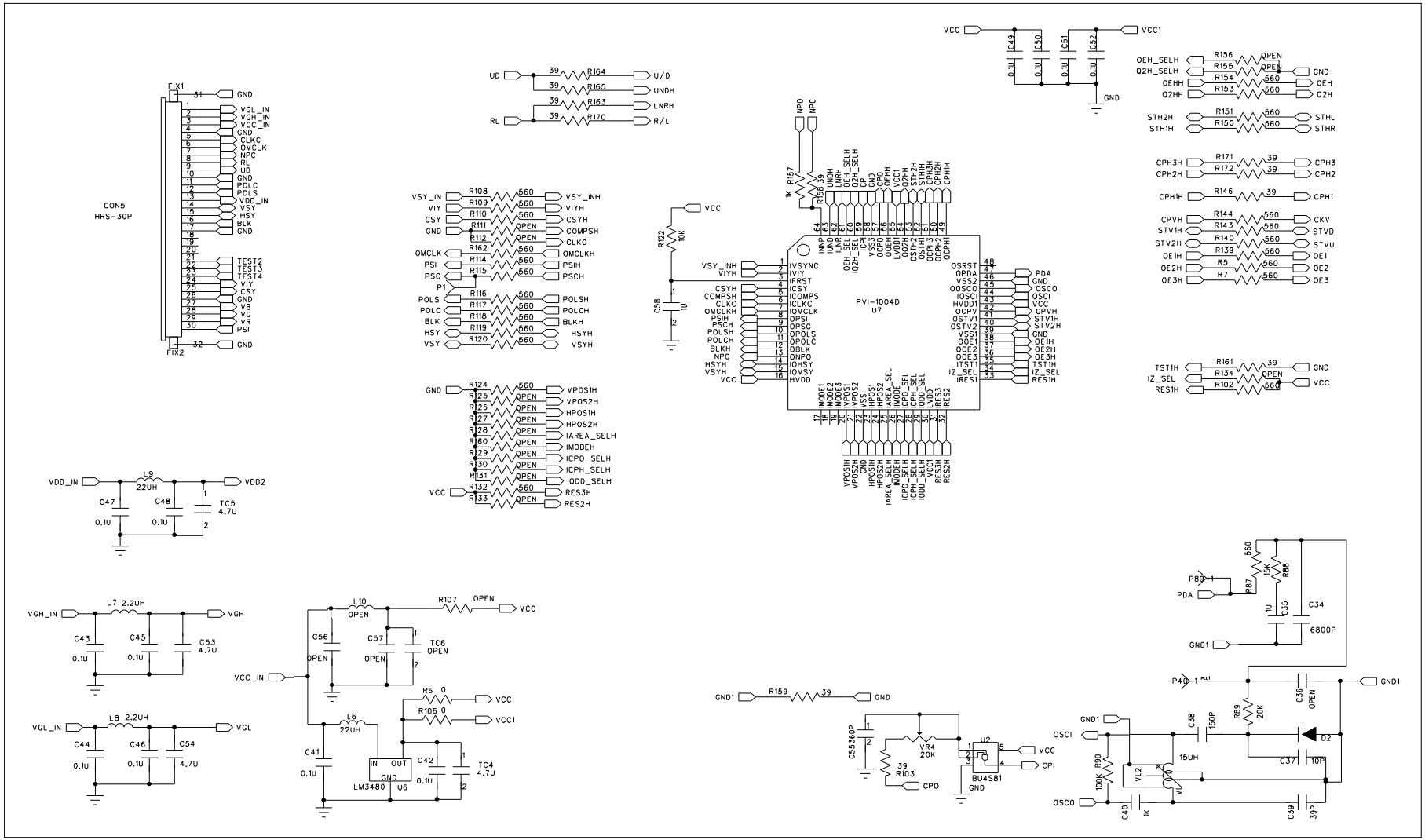


Fig.20 960*234 mode(5”,6.4”) (VCO is controlled by VL)

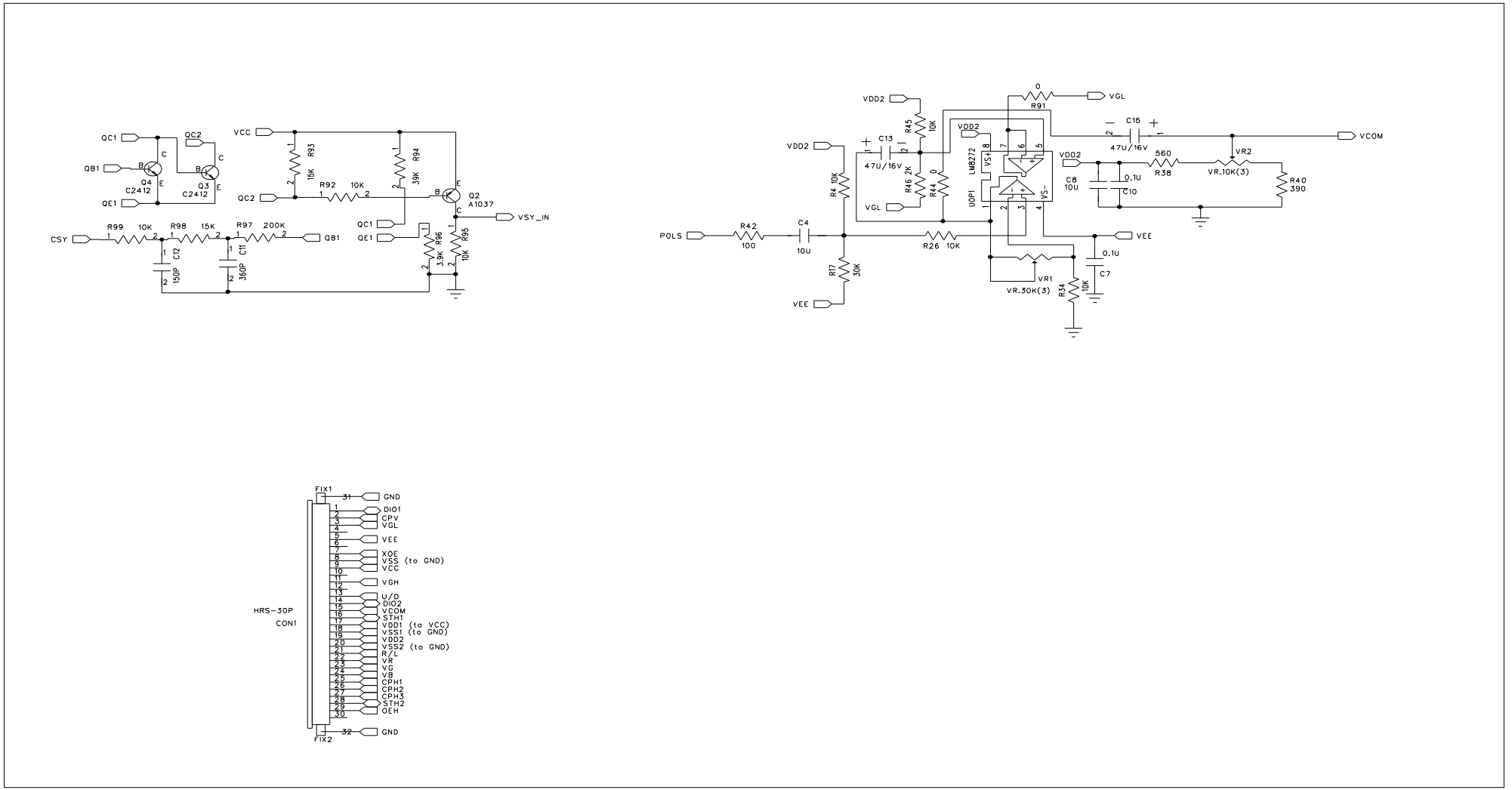


Fig.21 960*234 mode(5”,6.4”) Vcom Circuit (VCO is controlled by VL)

Table D : KEY COMPONENTS 5" & 6.4" (960*234)

PART NAME	VENDER	VENDER PART NO.	SPEC	APPELLATION
VL2	SUMIDA	CP-4LB(5113-T048)	15U 1%	VAR.IND
U7	EPSON	PVI-1004D		TIMMING CONTROL
U6	NS	LM3480IM3-3.3		REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81		AND GATE
UOP1	NS	LM8272MM		OP
CON1,CON5	ELCO	00-6210-030-010-800		CONNECTOR(30PIN)

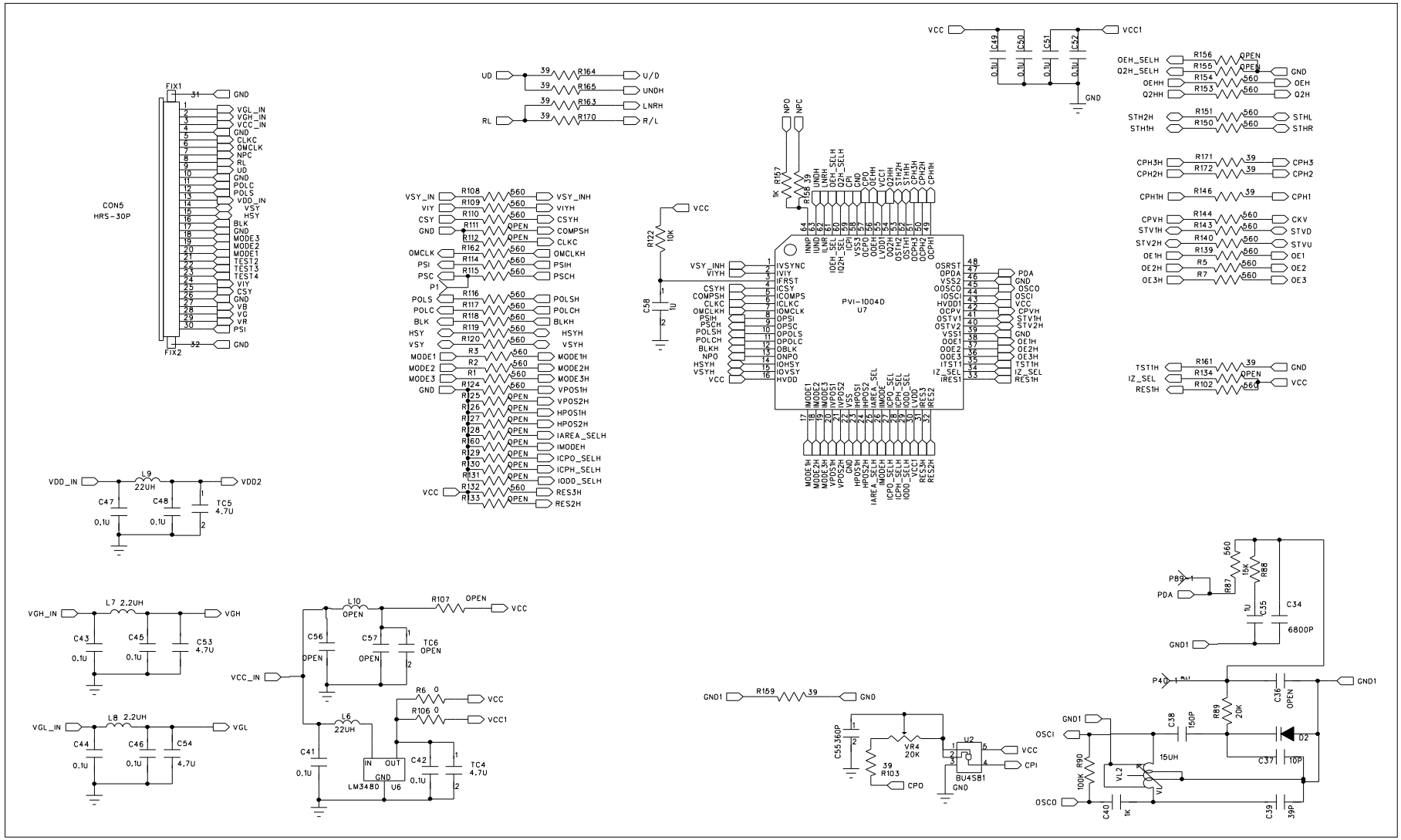


Fig.22 960*234 mode(4.5”) (VCO is controlled by VL)

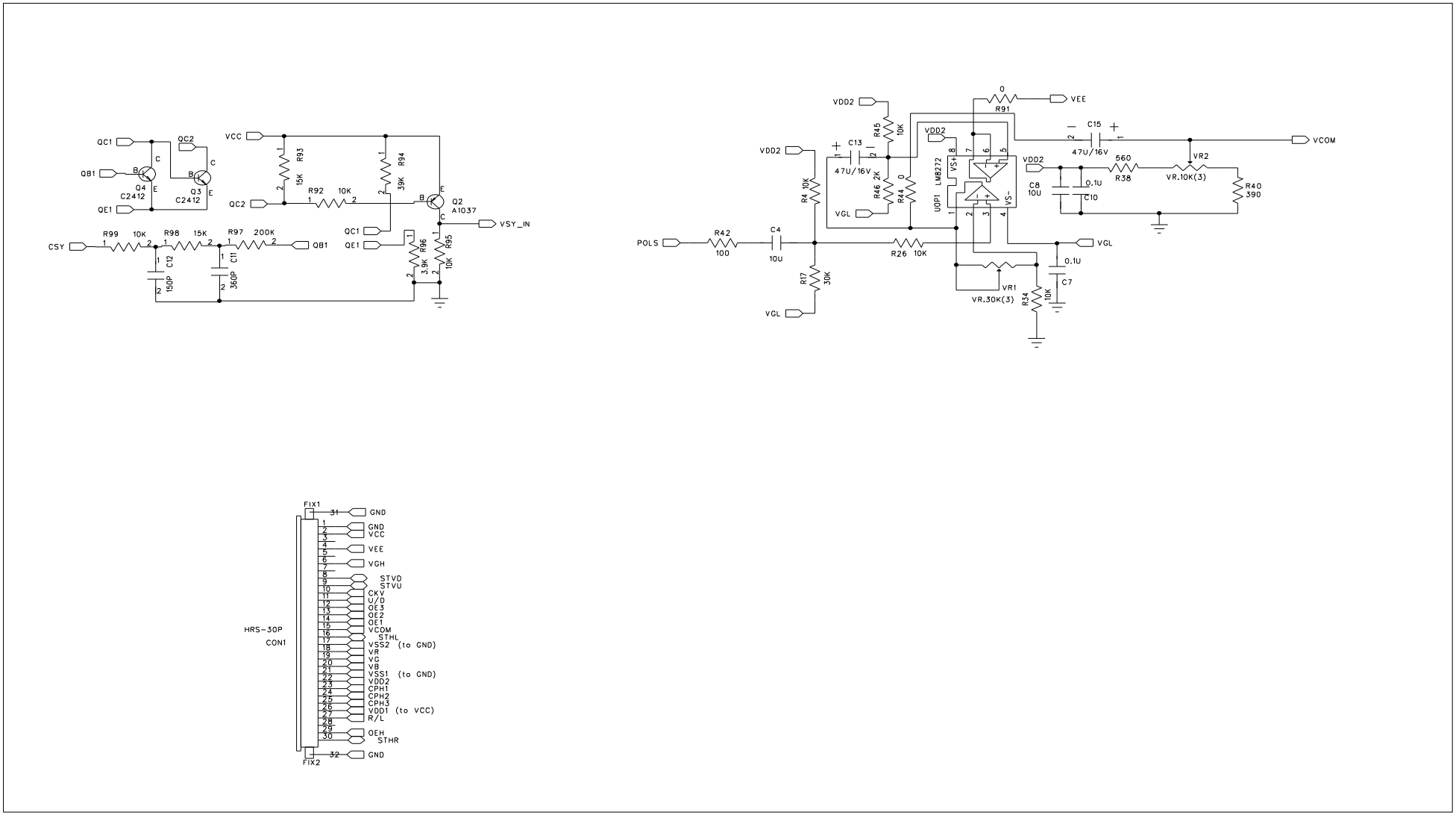


Fig.23 960*234 mode(4.5”) Vcom Circuit (VCO is controlled by VL)

Table E : KEY COMPONENTS 4.5"(960*234)

PART NAME	VENDER	VENDER PART NO.	SPEC	APPELLATION
VL2	SUMIDA	CP-4LB(5113-T048)	15U 1%	VAR.IND
U7	EPSON	PVI-1004D		TIMMING CONTROL
U6	NS	LM3480IM3-3.3		REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81		AND GATE
UOP1	NS	LM8272MM		OP
CON1, CON5	ELCO	00-6210-030-010-800		CONNECTOR(30PIN)

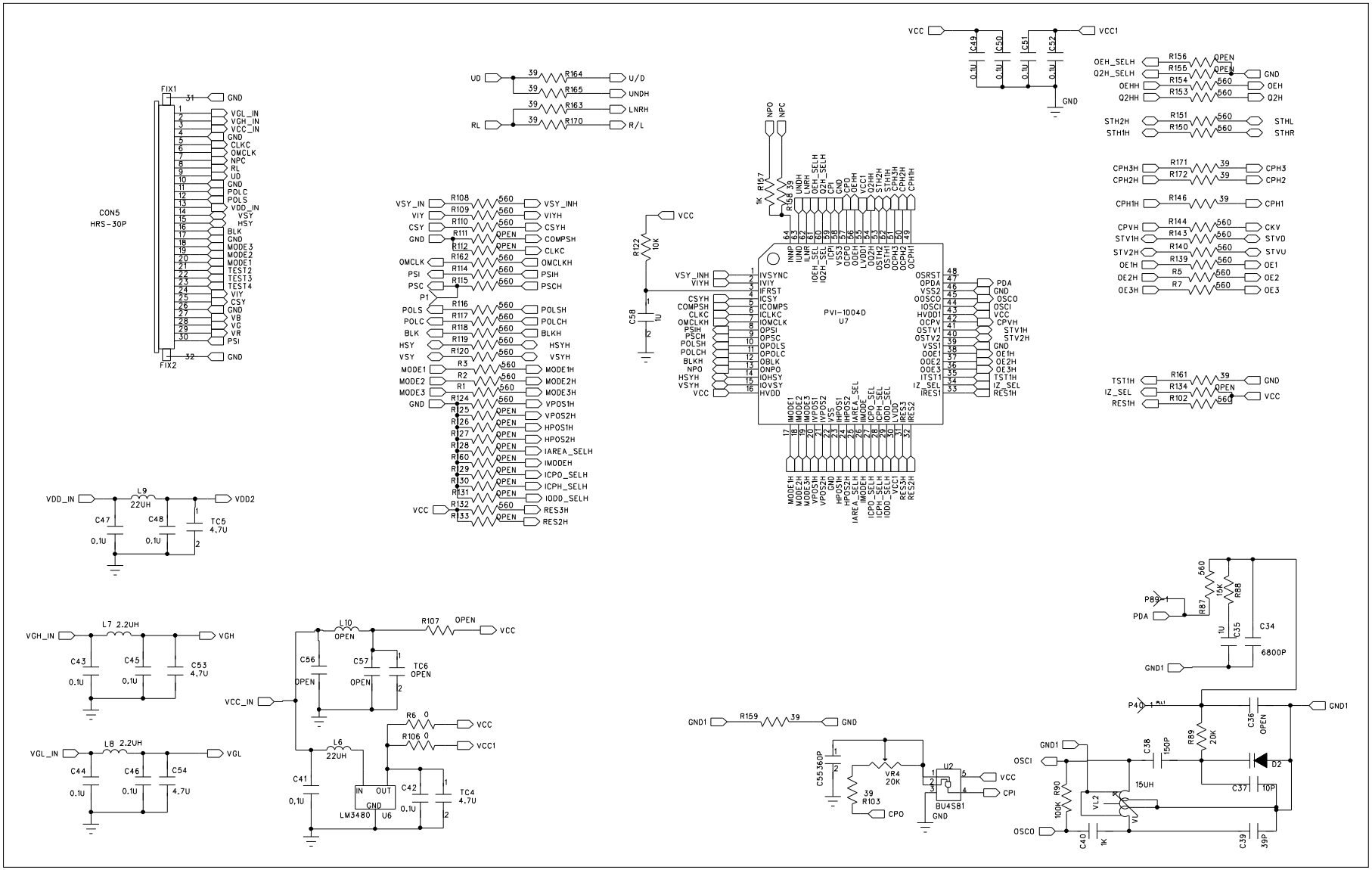


Fig.24 960*234 mode(3.6”) (VCO is controlled by VL)

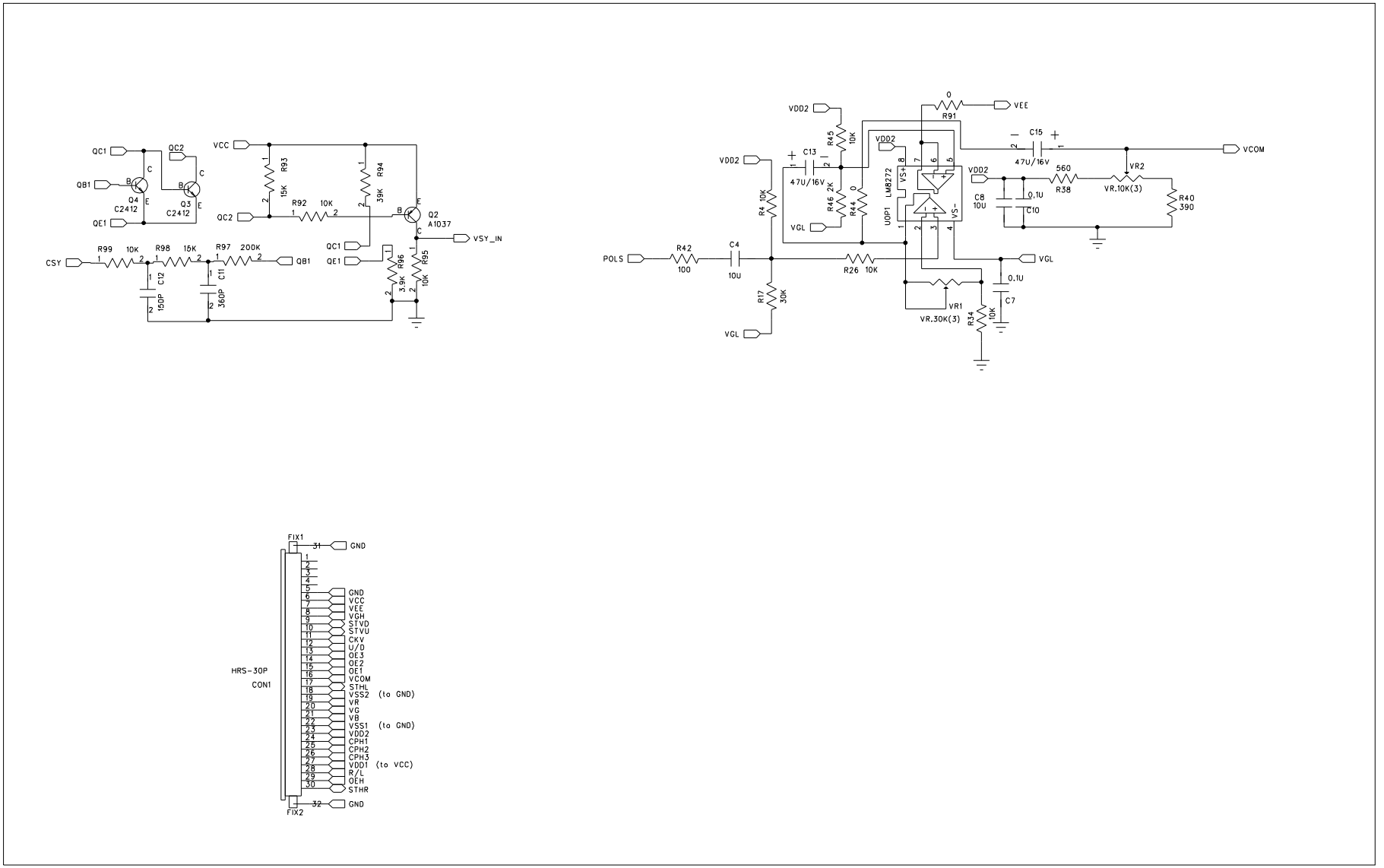


Fig.25 960*234 mode(3.6”) Vcom Circuit (VCO is controlled by VL)

Table F : KEY COMPONENTS 3.6"(960*234)

PART NAME	VENDER	VENDER PART NO.	SPEC	APPELLATION
VL2	SUMIDA	CP-4LB(5113-T048)	15U 1%	VAR.IND
U7	EPSON	PVI-1004D		TIMMING CONTROL
U6	NS	LM3480IM3-3.3		REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81		AND GATE
UOP1	NS	LM8272MM		OP
CON1, CON5	ELCO	00-6210-030-010-800		CONNECTOR(30PIN)

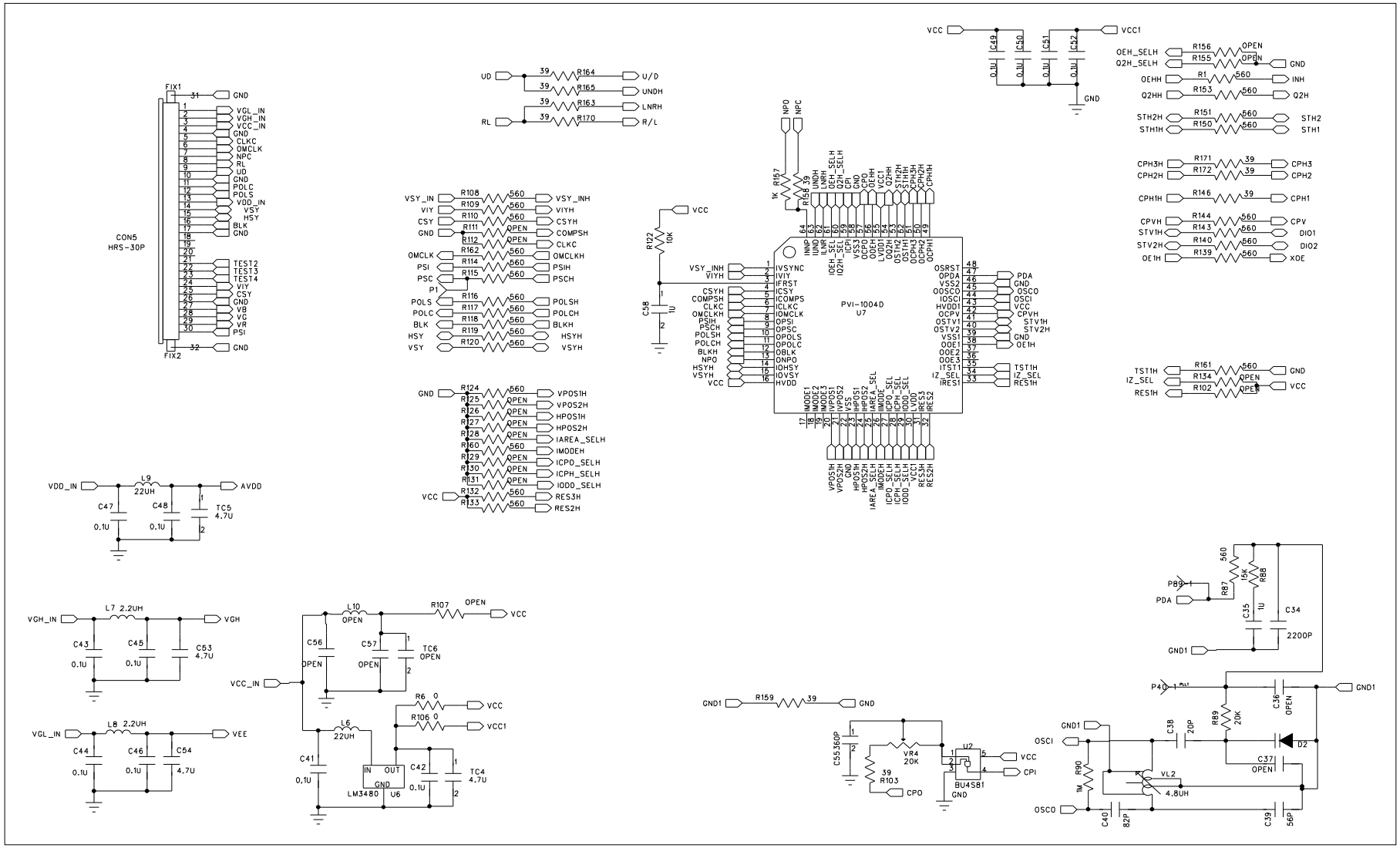


Fig.26 960*234 mode(3.5”(Delta)) (VCO is controlled by VL)

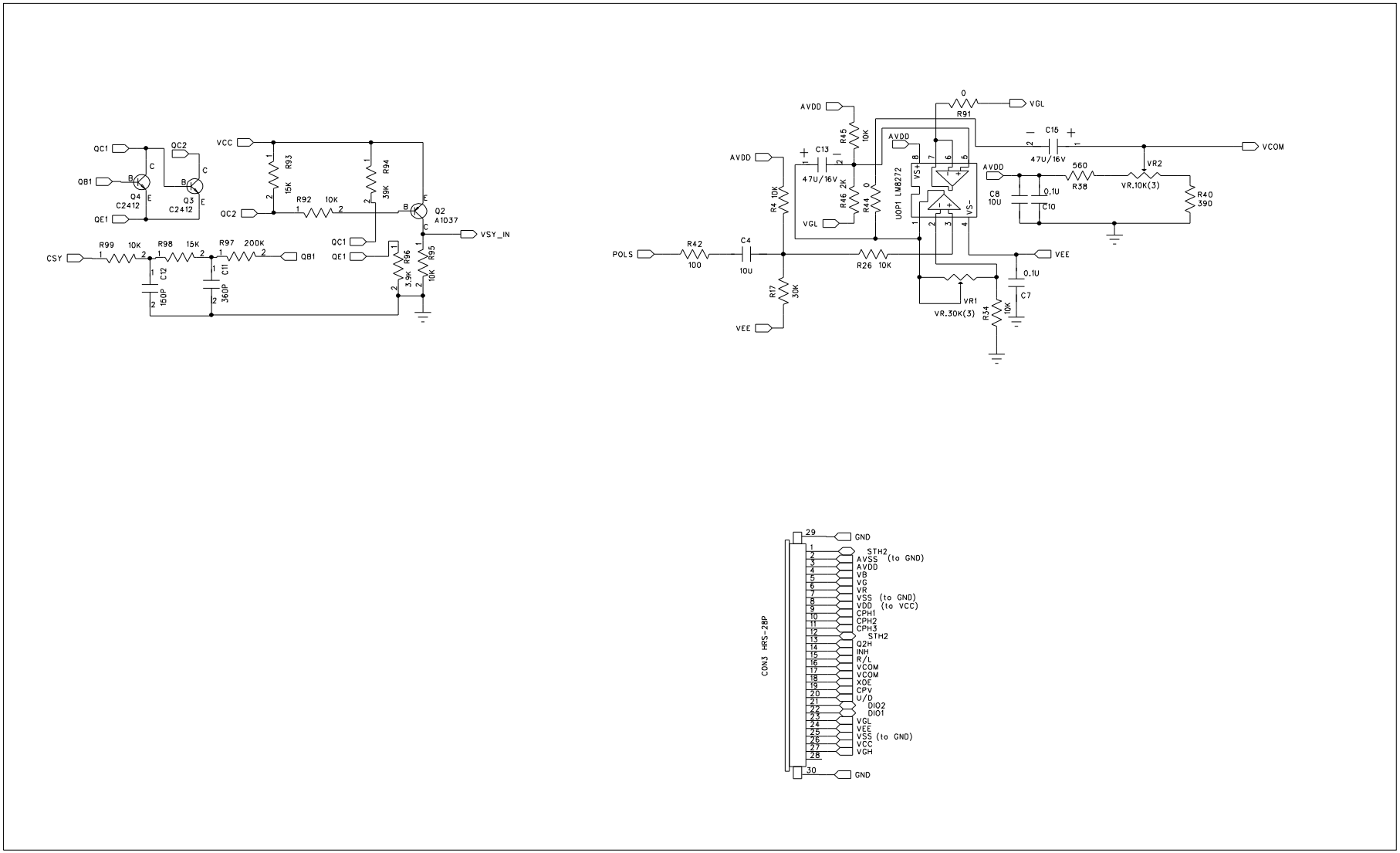


Fig.27 960*234 mode(3.5”(Delta)) Vcom Circuit (VCO is controlled by VL)

Table G : KEY COMPONENTS 3.5"(960*234(Delta mode))

PART NAME	VENDER	VENDER PART NO.	SPEC	APPELLATION
VL2	SUMIDA	CP-4LB(5113-T031)	4.8U 1%	VAR.IND
U7	EPSON	PVI-1004D		TIMMING CONTROL
U6	NS	LM3480IM3-3.3		REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81		AND GATE
UOP1	NS	LM8272MM		OP
CON1,CON5	ELCO	00-6210-030-010-800		CONNECTOR(30PIN)

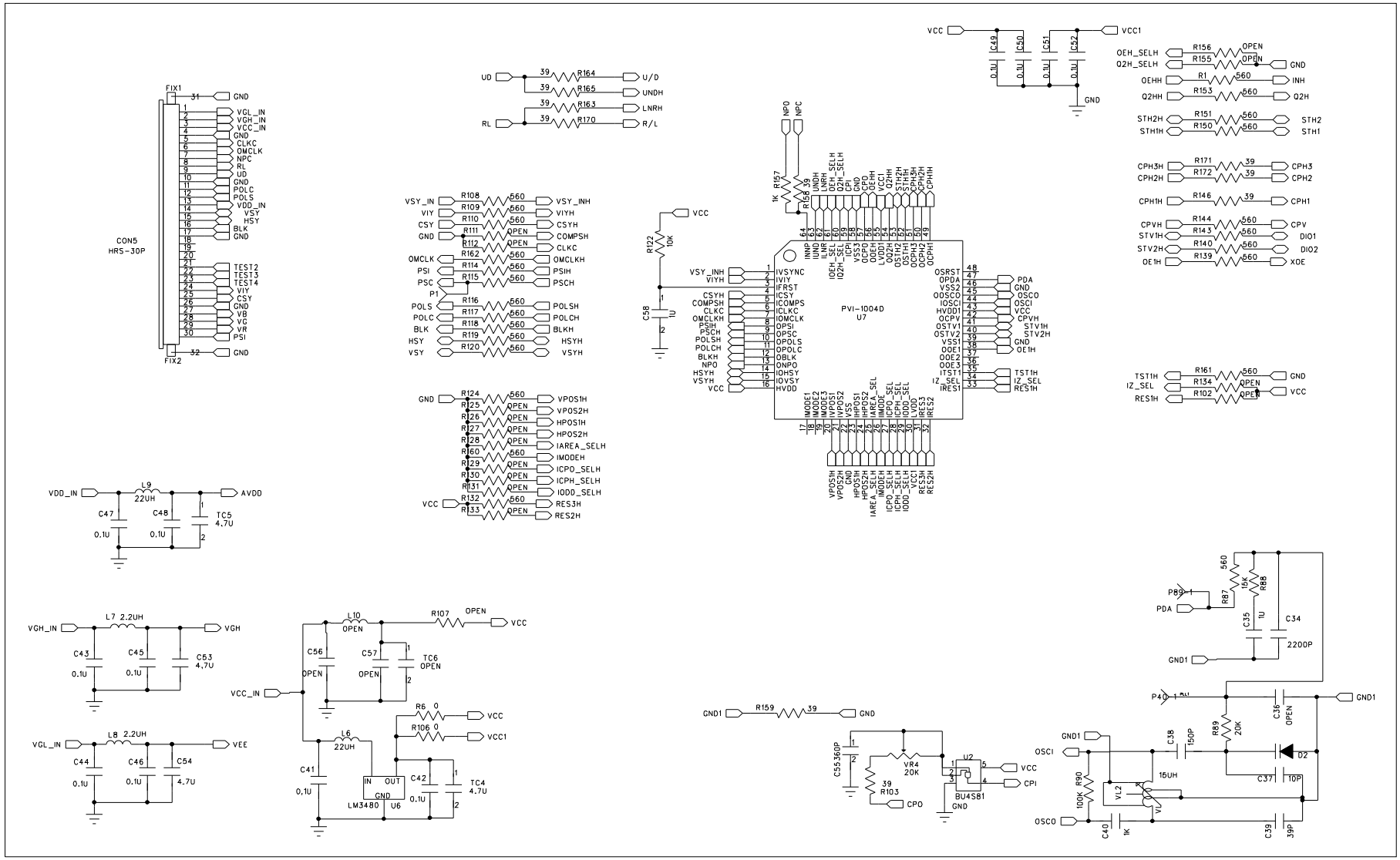


Fig.28 480*234 mode(2.5”, 3.5”(Delta)) (VCO is controlled by VL)

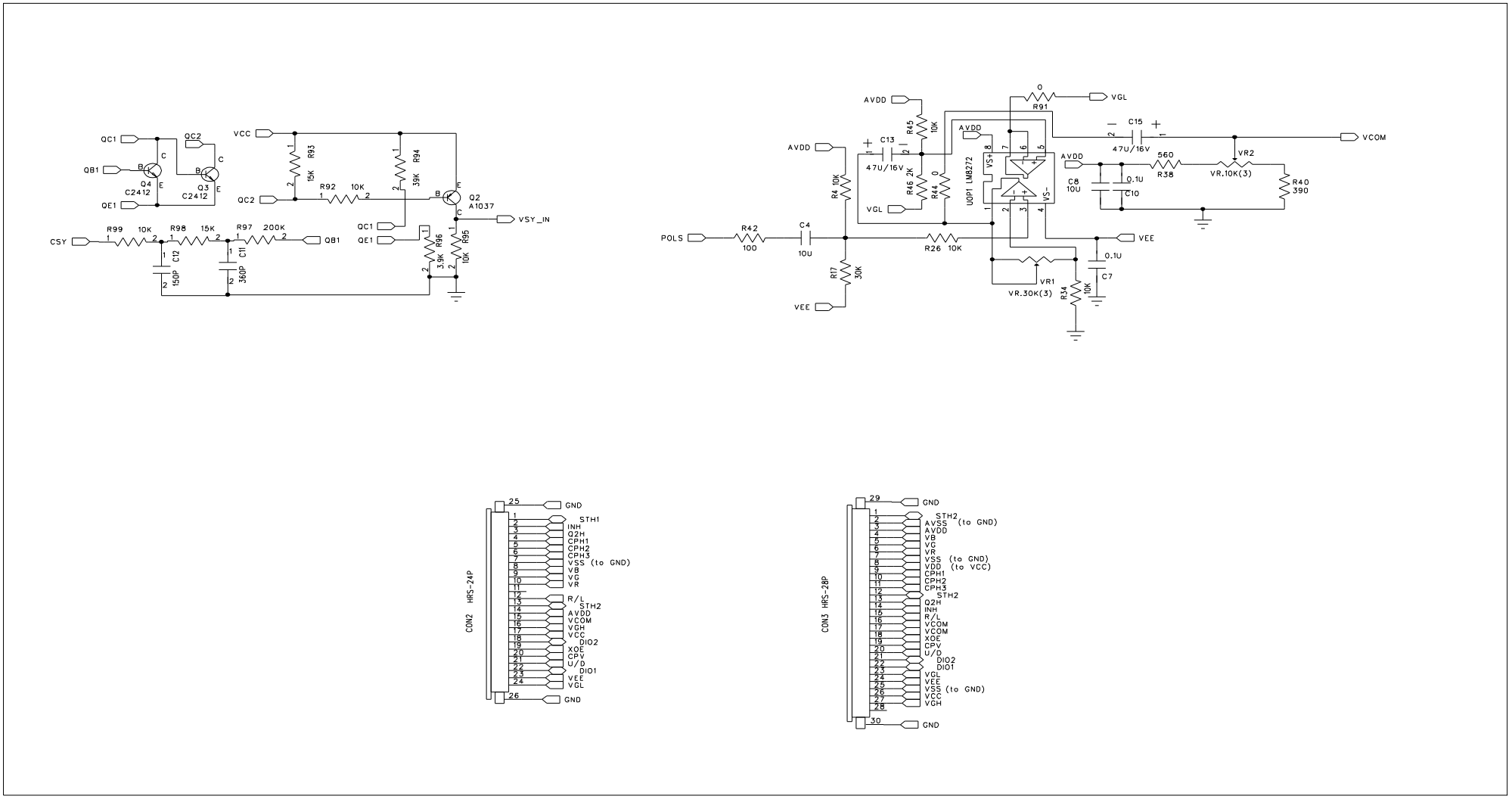


Fig.29 480*234 mode(2.5”, 3.5”(Delta)) Vcom Circuit (VCO is controlled by VL)

Table H : KEY COMPONENTS 3.5"&2.5"(480*234(Delta))

PART NAME	VENDER	VENDER PART NO.	SPEC	APPELLATION
VL2	SUMIDA	CP-4LB(5113-T048)	15U 1%	VAR.IND
U7	EPSON	PVI-1004D		TIMMING CONTROL
U6	NS	LM3480IM3-3.3		REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81		AND GATE
UOP1	NS	LM8272MM		OP
CON5	ELCO	00-6210-030-010-800		CONNECTOR(30PIN)
CON2	MOLEX	52437-2491		CONNECTOR(24PIN)
CON3	GAMON	FPC B-B-28-20R		CONNECTOR(28PIN)

C. Application Circuit(VCO is controlled by VR)

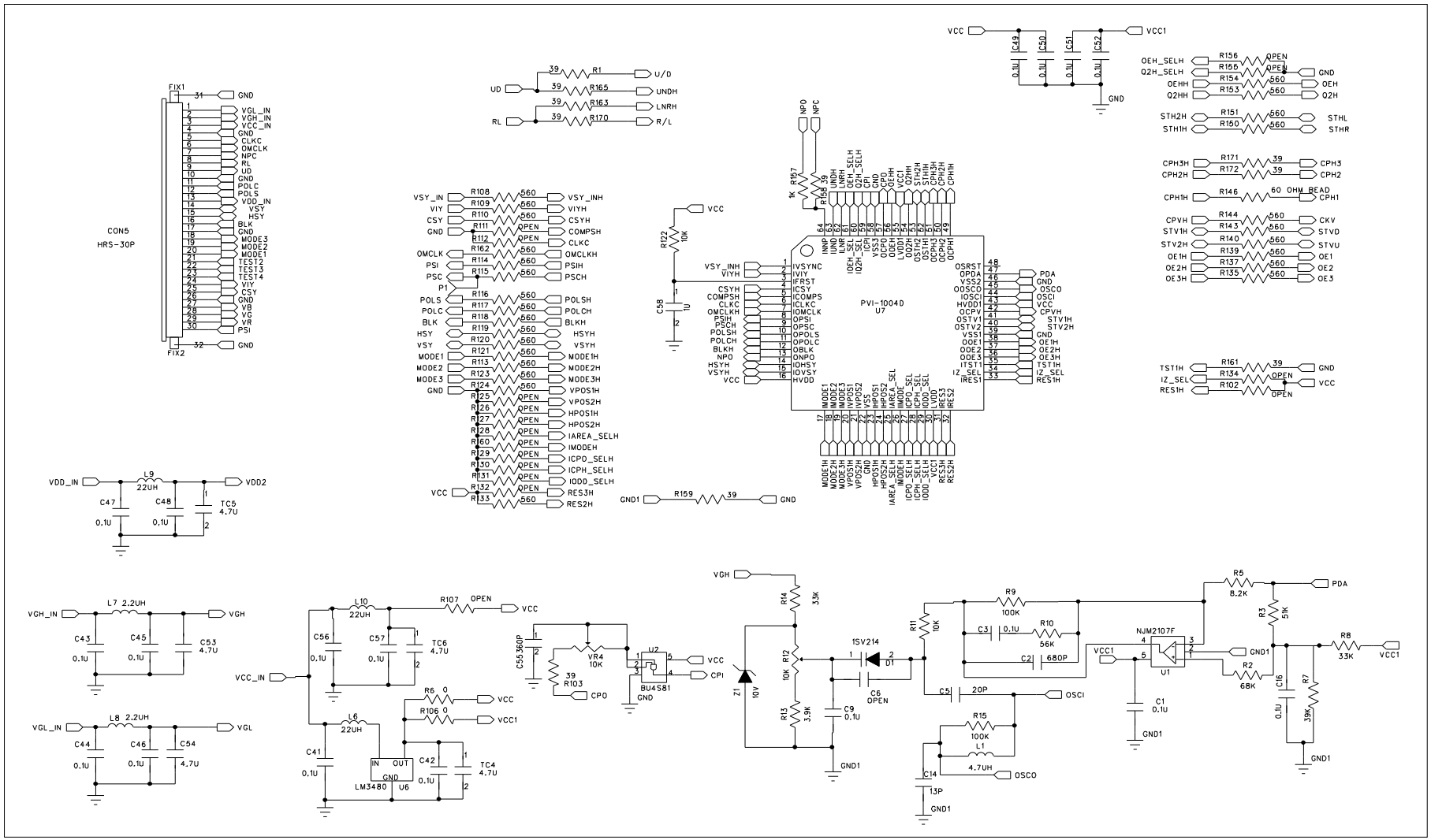


Fig.30 1920*234 mode(9”) (VCO is controlled by VR)

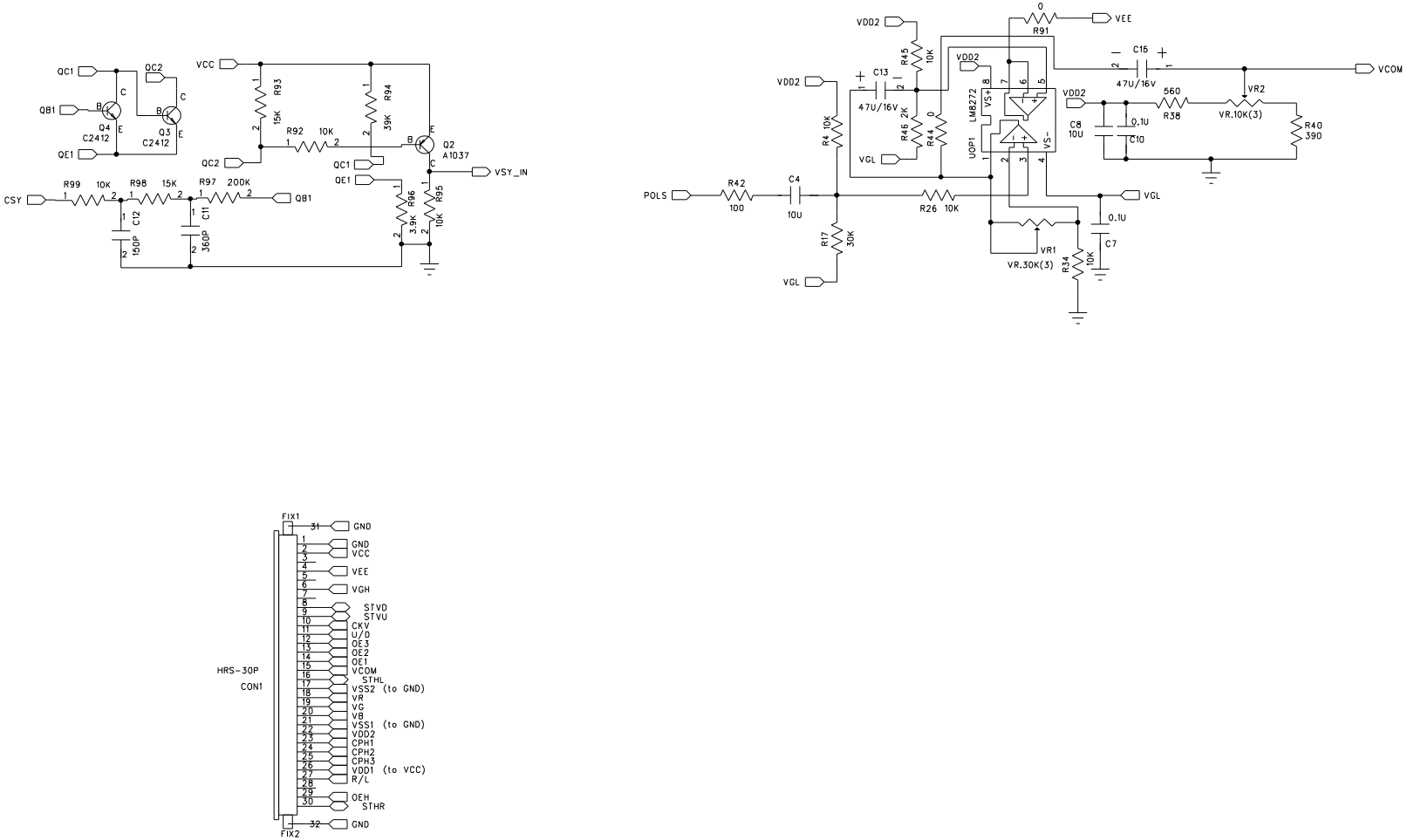


Fig.31 1920*234 mode(9”) Vcom Circuit(VCO is controlled by VR)

Table A : KEY COMPONENTS 9"(1440*234) :

PART NAME	VENDER	VENDER PART NO.	APPELLATION
U1	NJRC	NJM2107F	OP
U7	EPSON	PVI-1004D	TIMMING CONTROL
U6	NS	LM3480IM3-3.3	REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81	AND GATE
UOP1	NS	LM8272MM	OP
CON1,CON5	ELCO	00-6210-030-010-800	CONNECTOR(30PIN)

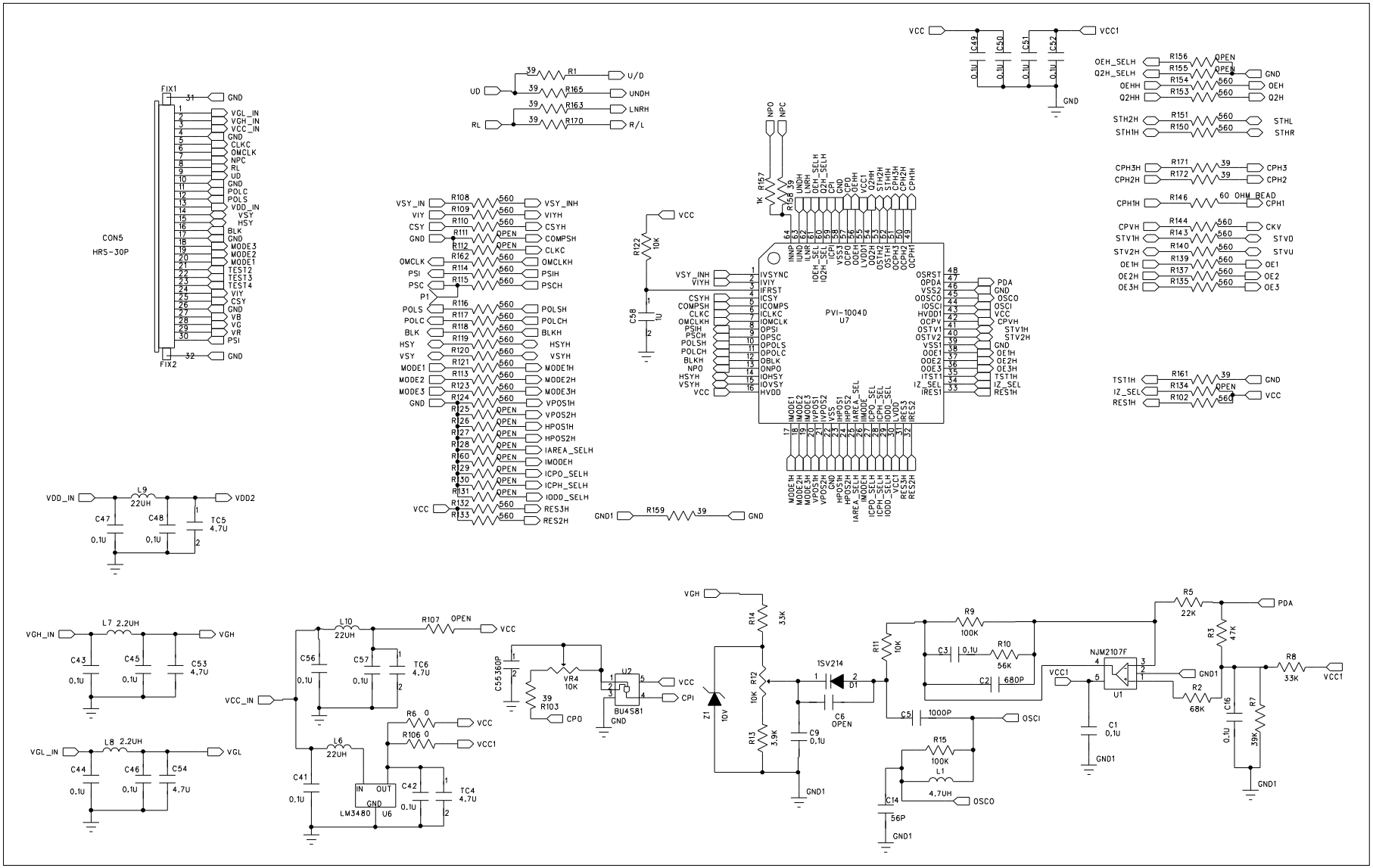


Fig.32 1440*234 mode(6.2”,7”,8.4”) (VCO is controlled by VR

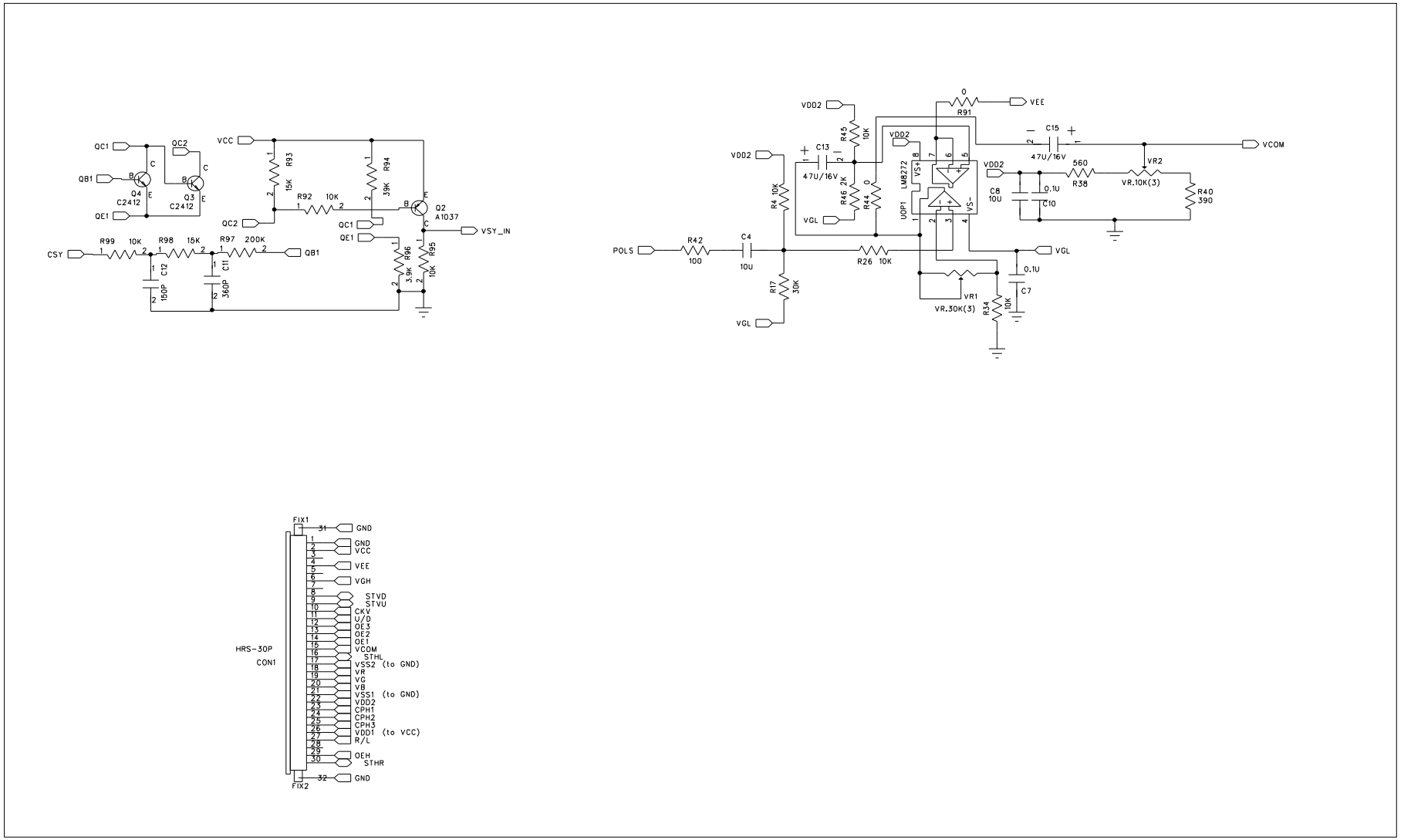


Fig.33 1440*234 mode(6.2”,7”,8.4”) Vcom Circuit(VCO is controlled by VR)

Table B : KEY COMPONENTS 6.2", 7" & 8"(1440*234) :

PART NAME	VENDER	VENDER PART NO.	APPELLATION
U1	NJRC	NJM2107F	OP
U7	EPSON	PVI-1004D	TIMMING CONTROL
U6	NS	LM3480IM3-3.3	REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81	AND GATE
UOP1	NS	LM8272MM	OP
CON1,CON5	ELCO	00-6210-030-010-800	CONNECTOR(30PIN)

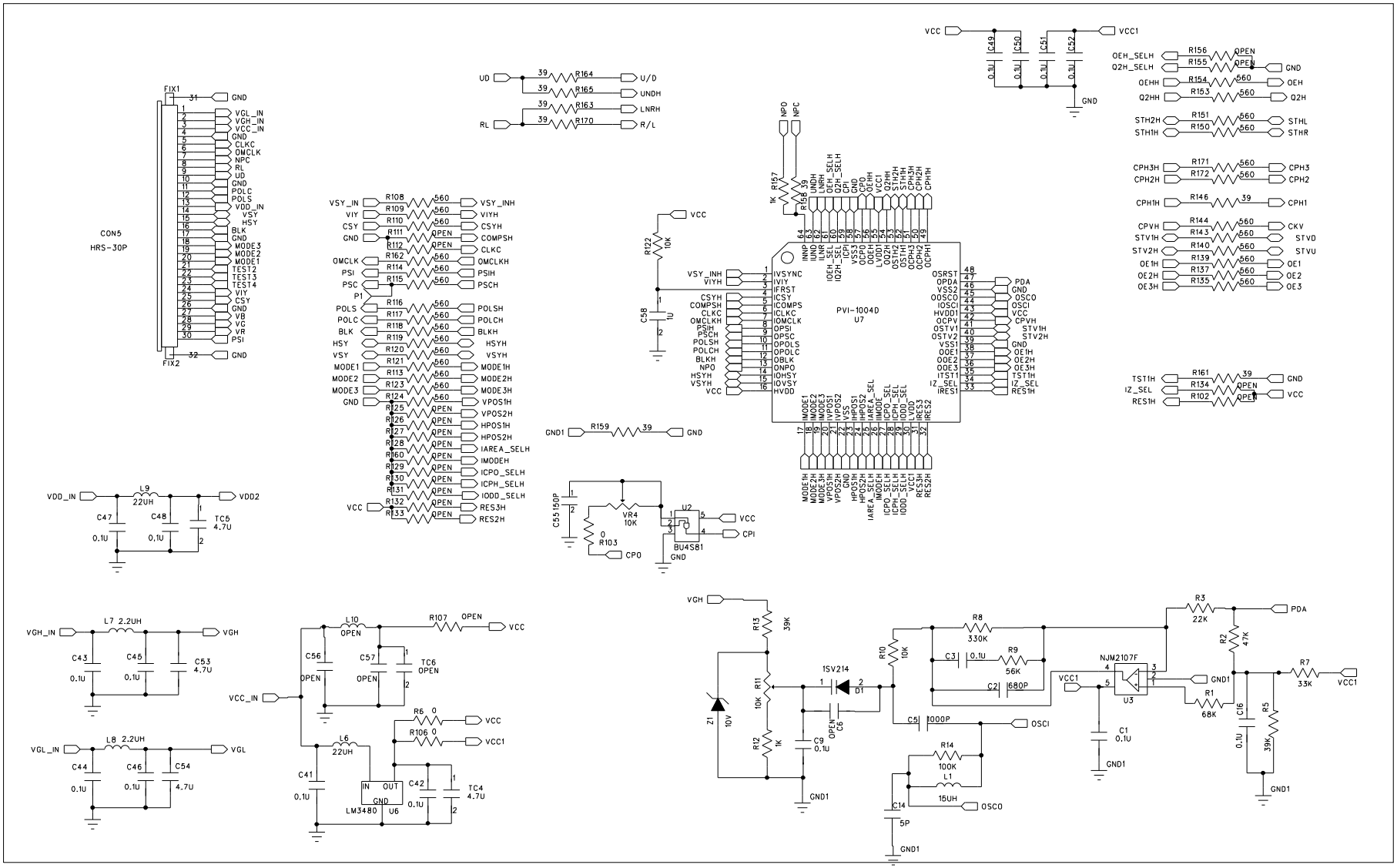


Fig.34 1200*234 mode(6.5”) (VCO is controlled by VR)

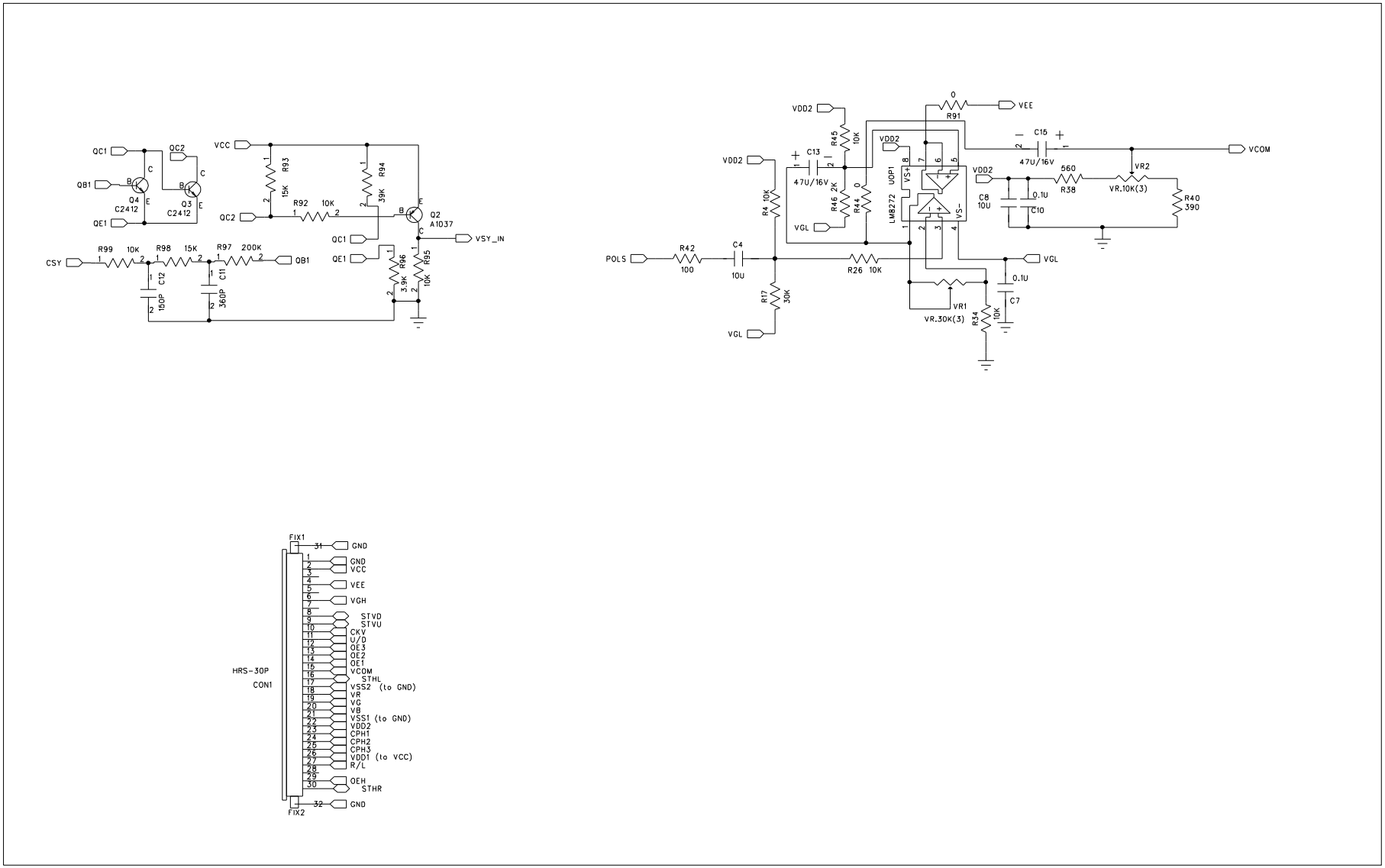


Fig.35 1200*234 mode(6.5”) Vcom Circuit(VCO is controlled by VR)

Table C : KEY COMPONENTS 6.5"(1200*234) :

PART NAME	VENDER	VENDER PART NO.	APPELLATION
U3	NJRC	NJM2107F	OP
U7	EPSON	PVI-1004D	TIMMING CONTROL
U6	NS	LM3480IM3-3.3	REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81	AND GATE
UOP1	NS	LM8272MM	OP
CON1,CON5	ELCO	00-6210-030-010-800	CONNECTOR(30PIN)

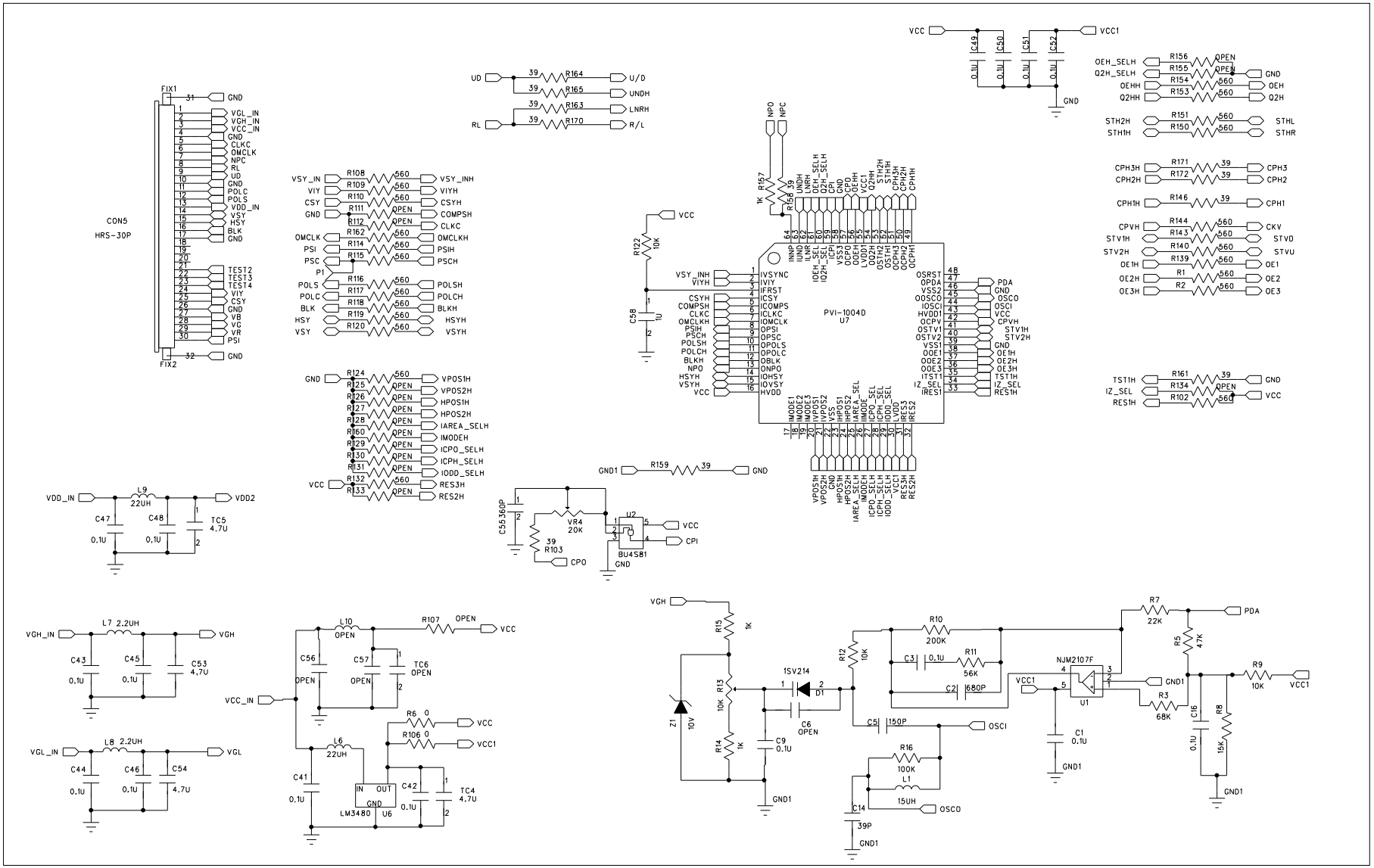


Fig.36 960*234 mode(5”,6.4”) (VCO is controlled by VR)

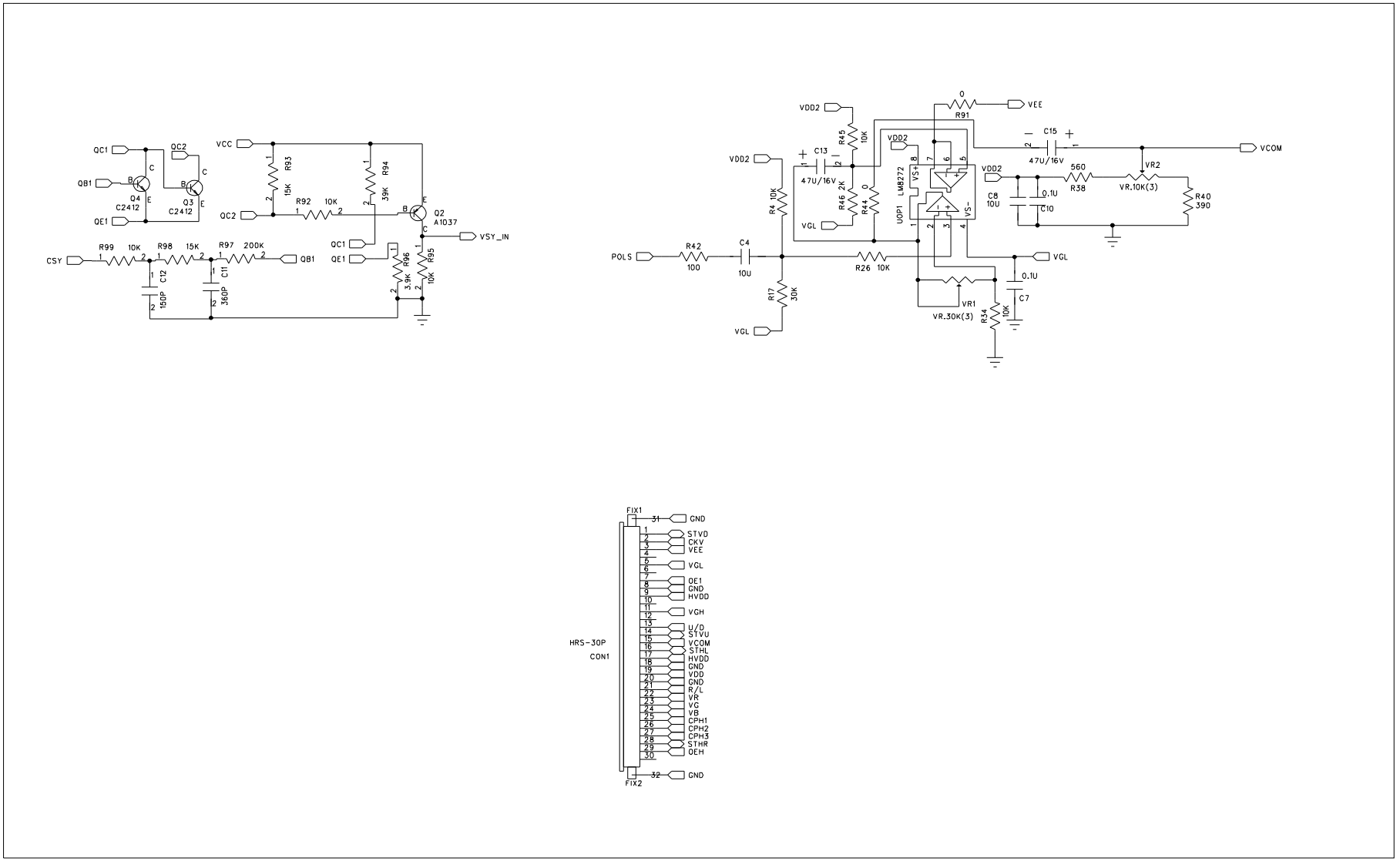


Fig.37 960*234 mode(5”,6.4”) Vcom Circuit (VCO is controlled by VR)

Table D : KEY COMPONENTS 5" & 6.4" (960*234):

PART NAME	VENDER	VENDER PART NO.	APPELLATION
U3	NJRC	NJM2107F	OP
U7	EPSON	PVI-1004D	TIMMING CONTROL
U6	NS	LM3480IM3-3.3	REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81	AND GATE
UOP1	NS	LM8272MM	OP
CON1,CON5	ELCO	00-6210-030-010-800	CONNECTOR(30PIN)

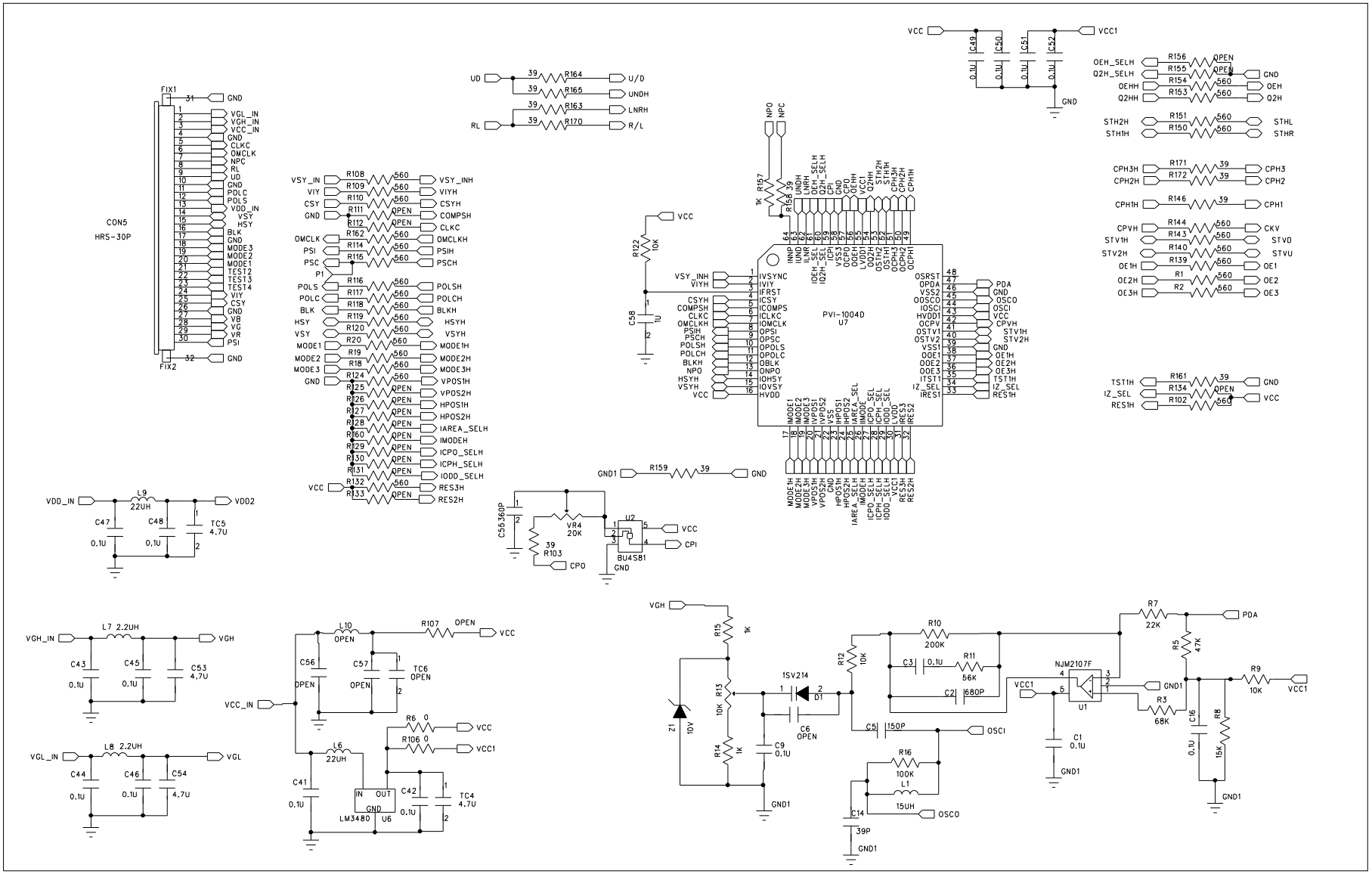


Fig.38 960*234 mode(4.5”) (VCO is controlled by VR)

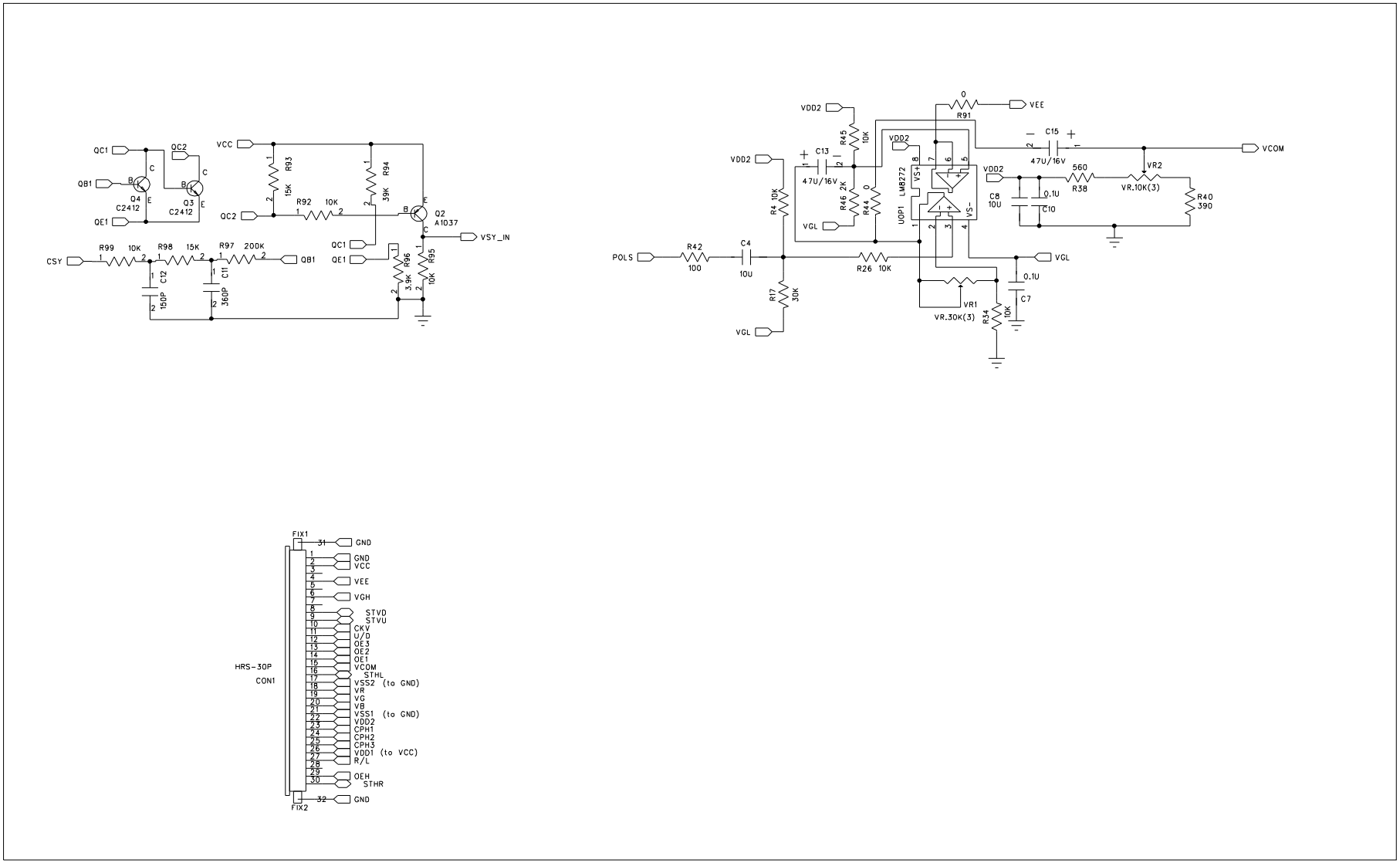


Fig.39 960*234 mode(4.5”) Vcom Circuit (VCO is controlled by VR)

Table E : KEY COMPONENTS 4.5"(960*234) :

PART NAME	VENDER	VENDER PART NO.	APPELLATION
U1	NJRC	NJM2107F	OP
U7	EPSON	PVI-1004D	TIMMING CONTROL
U6	NS	LM3480IM3-3.3	REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81	AND GATE
UOP1	NS	LM8272MM	OP
CON1, CON5	ELCO	00-6210-030-010-800	CONNECTOR(30PIN)

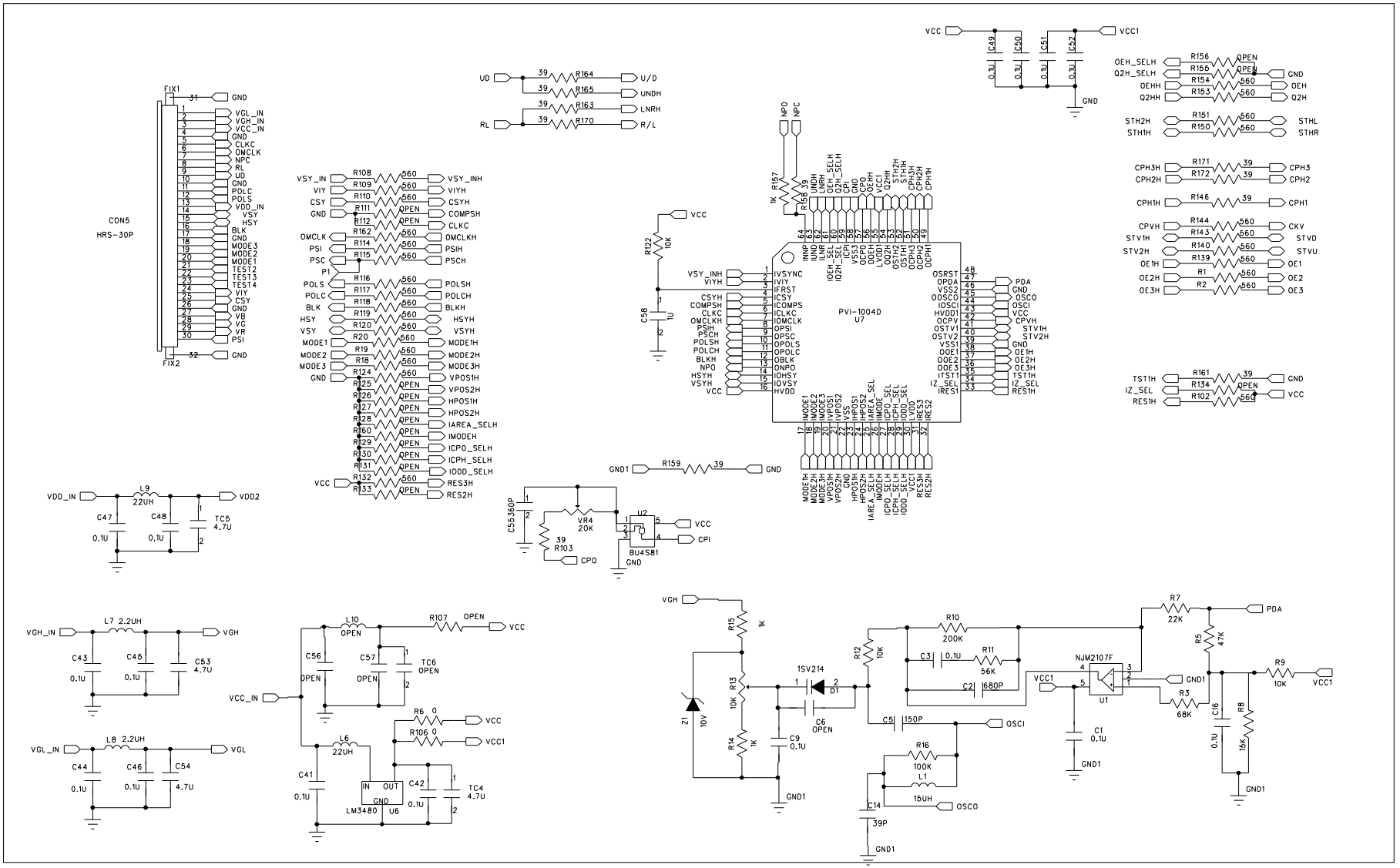


Fig.40 960*234 mode(3.6”) (VCO is controlled by VR)

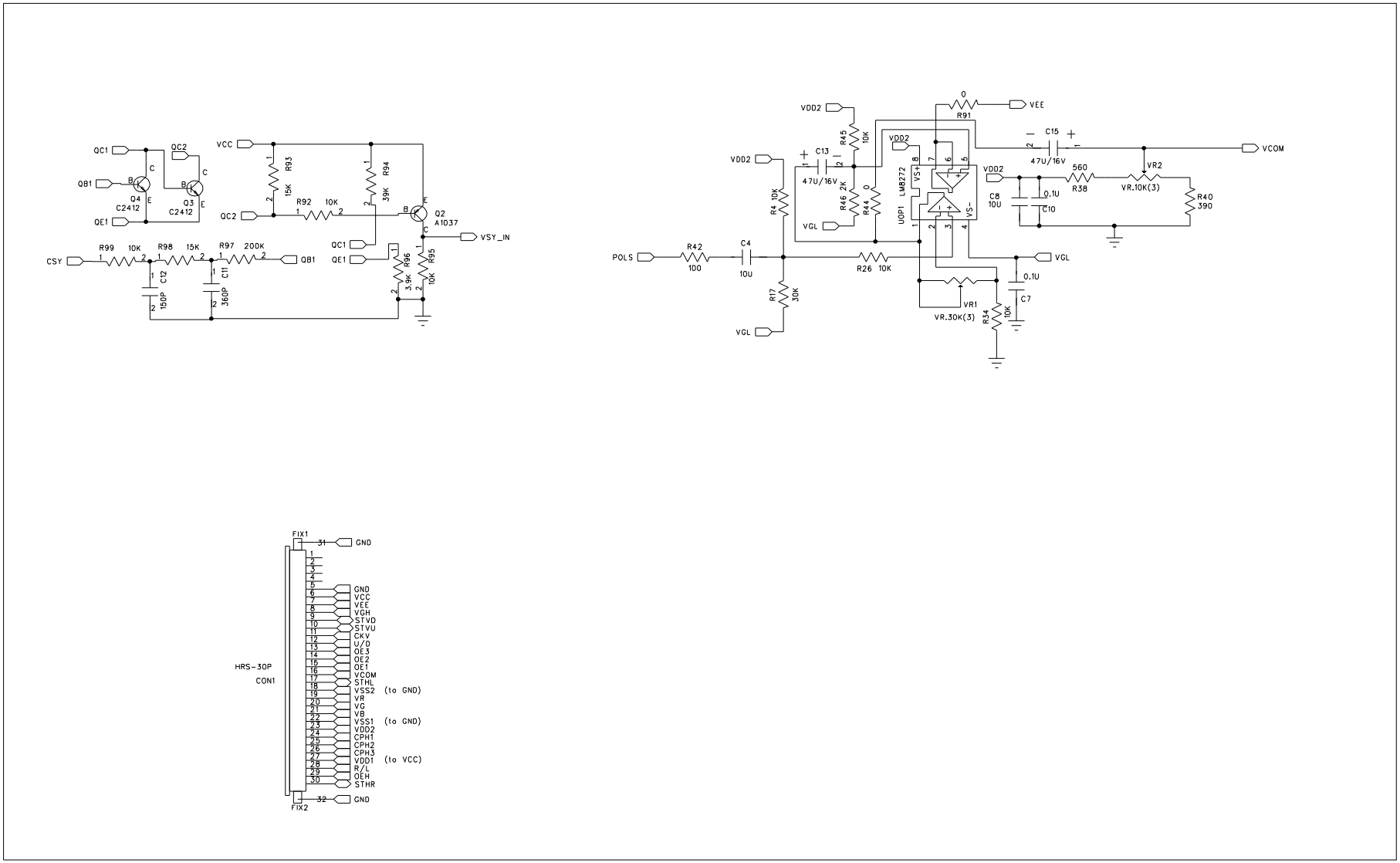


Fig.41 960*234 mode(3.6”) Vcom Circuit (VCO is controlled by VR)

Table F : KEY COMPONENTS 3.6"(960*234) :

PART NAME	VENDER	VENDER PART NO.	APPELLATION
U1	NJRC	NJM2107F	OP
U7	EPSON	PVI-1004D	TIMMING CONTROL
U6	NS	LM3480IM3-3.3	REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81	AND GATE
UOP1	NS	LM8272MM	OP
CON1, CON5	ELCO	00-6210-030-010-800	CONNECTOR(30PIN)

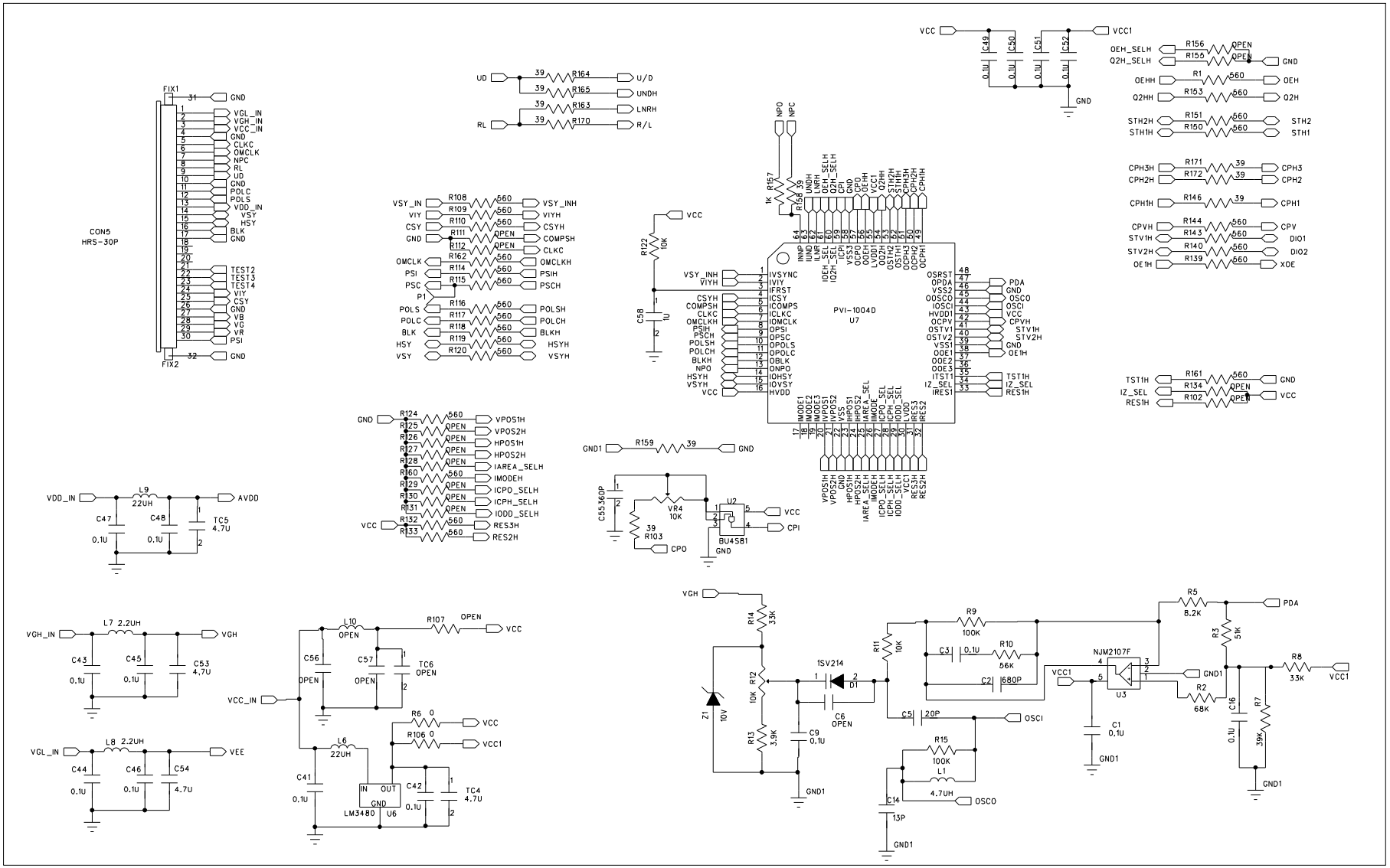


Fig.42 960*234 mode(3.5”(Delta)) (VCO is controlled by VR)

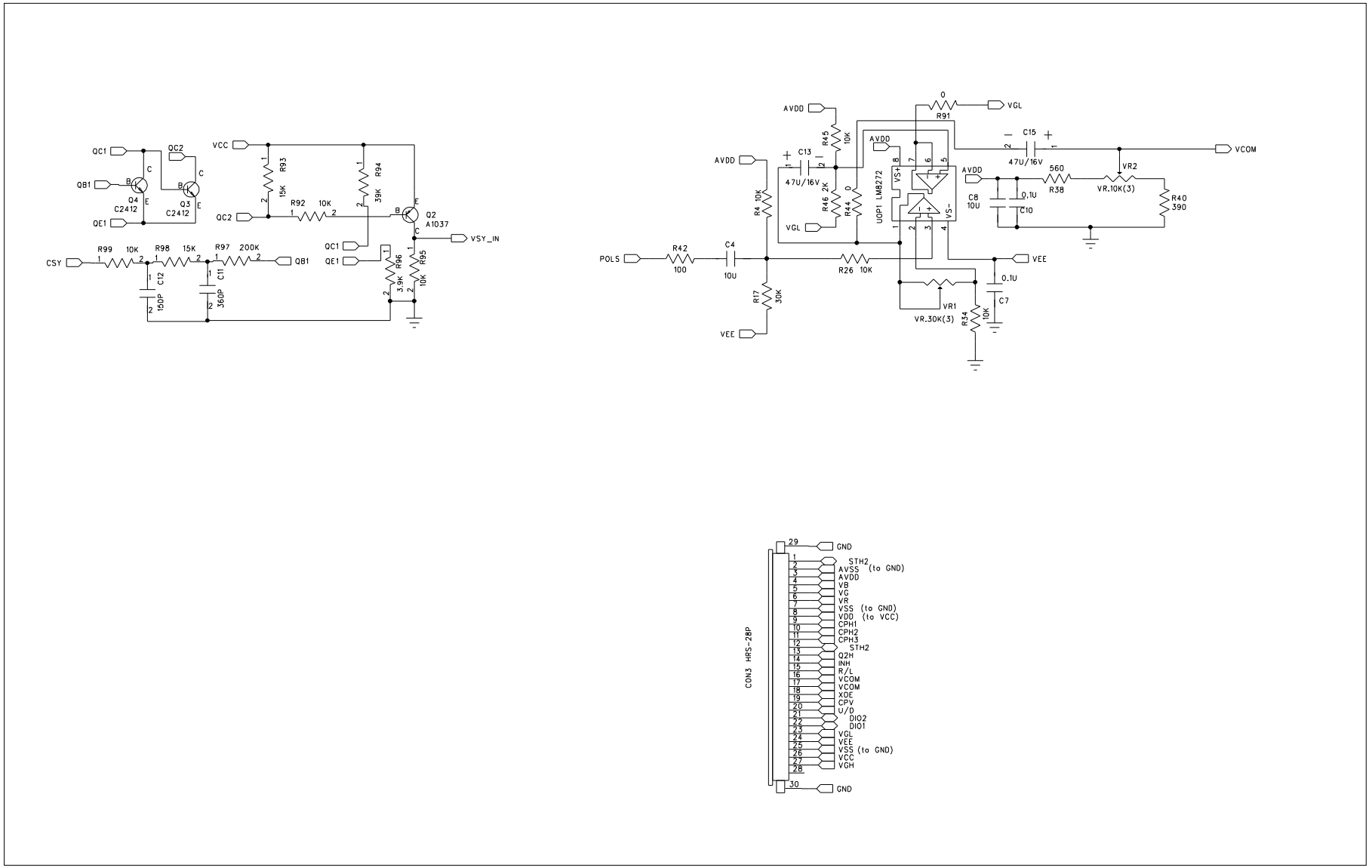


Fig.43 960*234 mode(3.5”(Delta)) Vcom Circuit (VCO is controlled by VR)

Table G : KEY COMPONENTS 3.5" (960*234(Delta)) :

PART NAME	VENDER	VENDER PART NO.	APPELLATION
U1	NJRC	NJM2107F	OP
U7	EPSON	PVI-1004D	TIMMING CONTROL
U6	NS	LM3480IM3-3.3	REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81	AND GATE
UOP1	NS	LM8272MM	OP
CON1,CON5	ELCO	00-6210-030-010-800	CONNECTOR(30PIN)

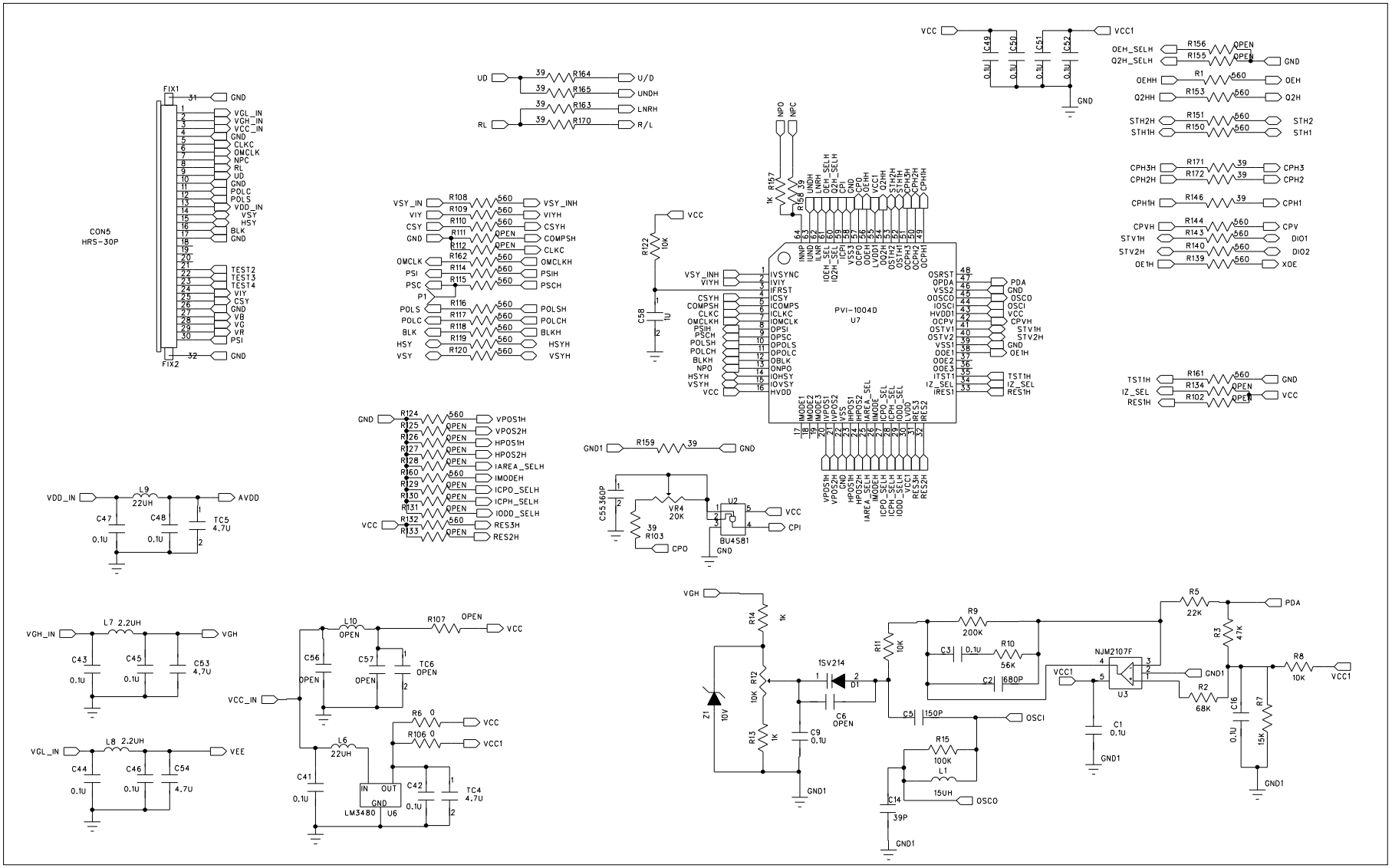


Fig.44 480*234 mode(2.5”, 3.5”(Delta)) (VCO is controlled by VR)

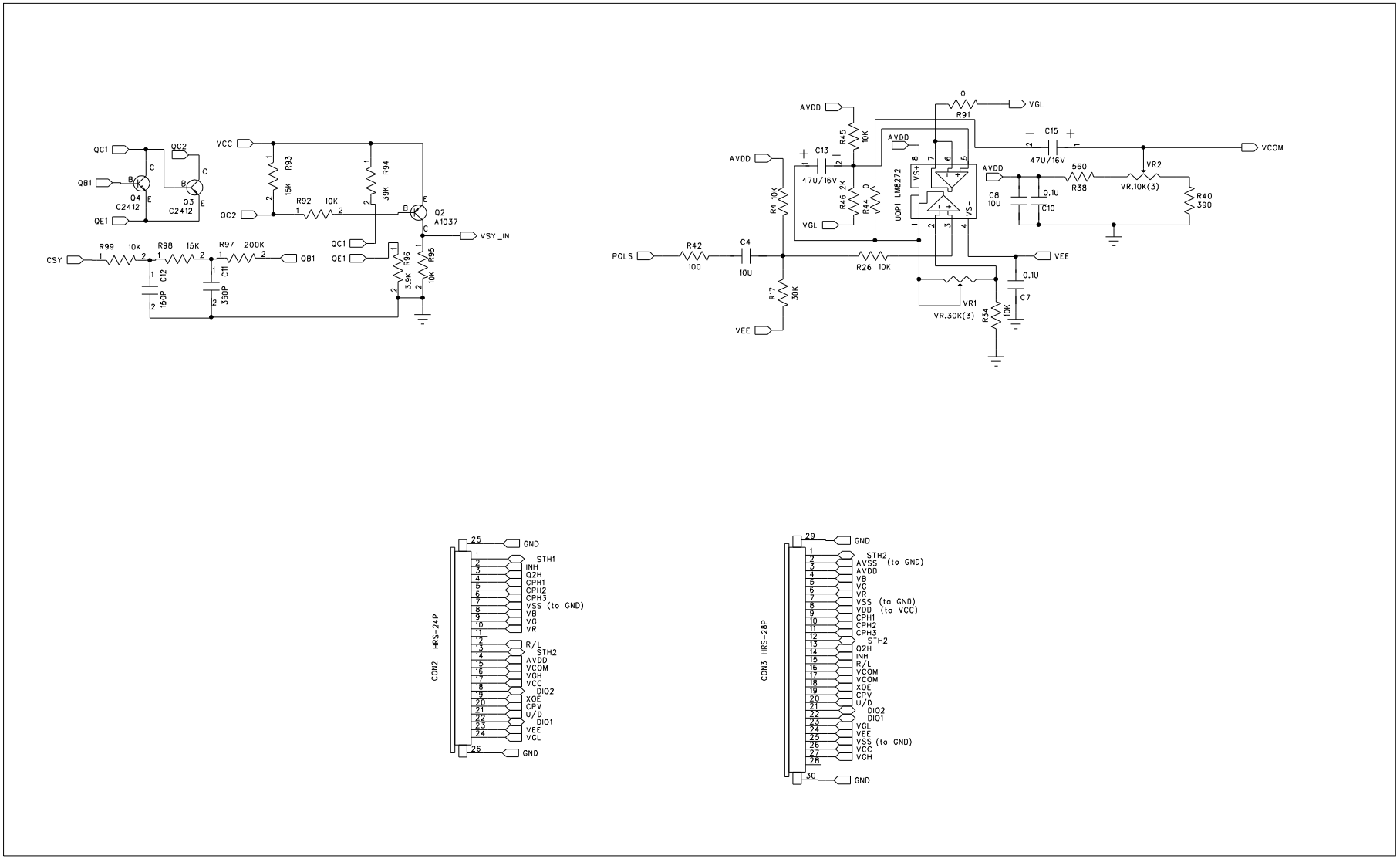


Fig.45 480*234 mode(2.5”,3.5”(Delta)) Vcom Circuit (VCO is controlled by VR)

Table H : KEY COMPONENTS 3.5"&2.5"(480*234 (Delta)) :

PART NAME	VENDER	VENDER PART NO.	APPELLATION
U3	NJRC	NJM2107F	OP
U7	EPSON	PVI-1004d	TIMMING CONTROL
U6	NS	LM3480IM3-3.3	REGULATOR(5V-->3.3V)
U2	ROHM	BU4S81	AND GATE
UOP1	NS	LM8272MM	OP
CON5	ELCO	00-6210-030-010-800	CONNECTOR(30PIN)
CON2	MOLEX	52437-2491	CONNECTOR(24PIN)
CON3	GAMON	FPC B-B-28-20R	CONNECTOR(28PIN)