

AU OPTRONICS

M190EN04

A

B

C

D

E

version	date	content
EC02	12/24/2003	R151 0, R37 3.6K, R93 0, R34 10K, R35 100K, R303 180, R311 open, C103 open, R220 820, R87 33, gamma

4

4

3

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2

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1

A

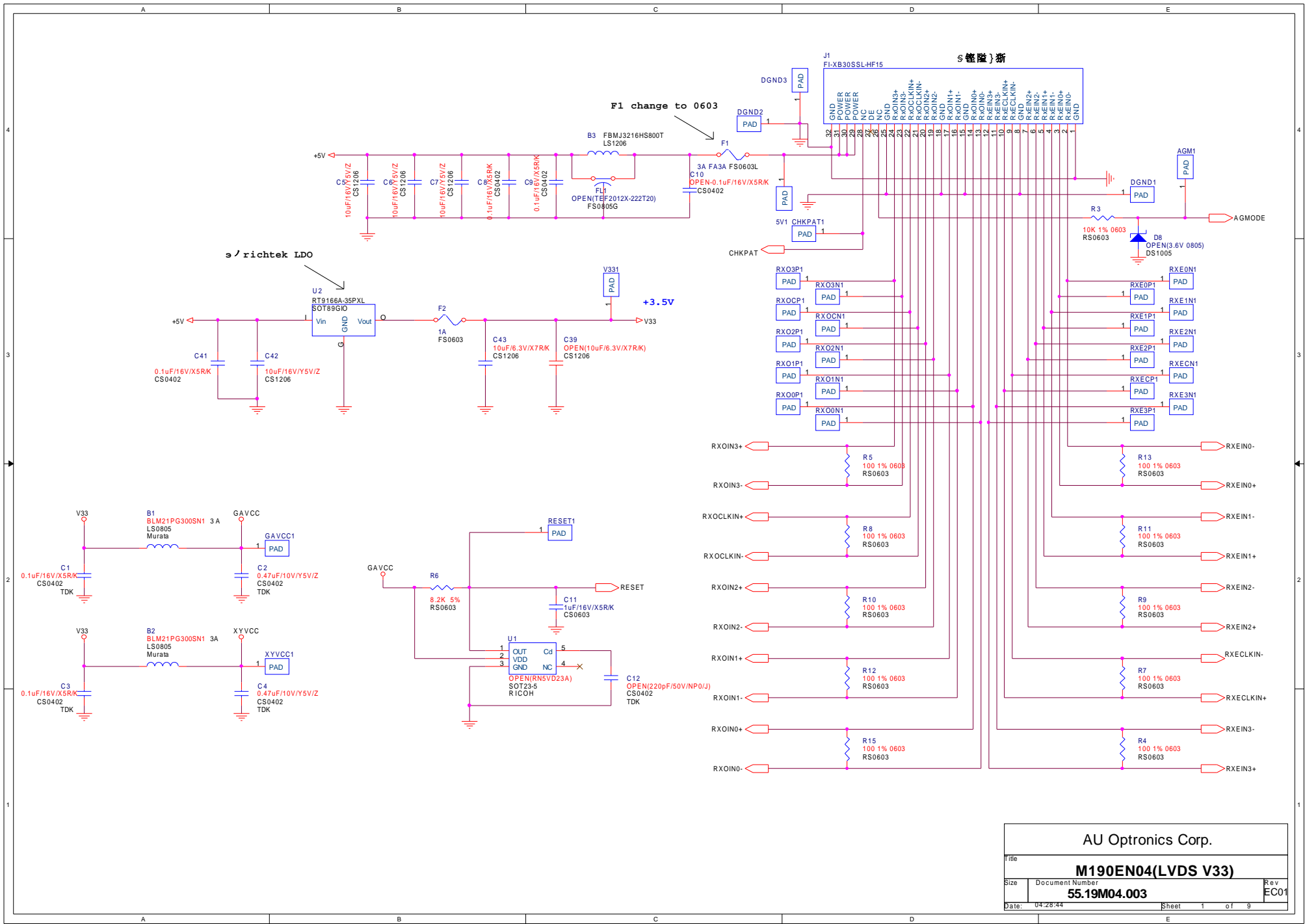
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C

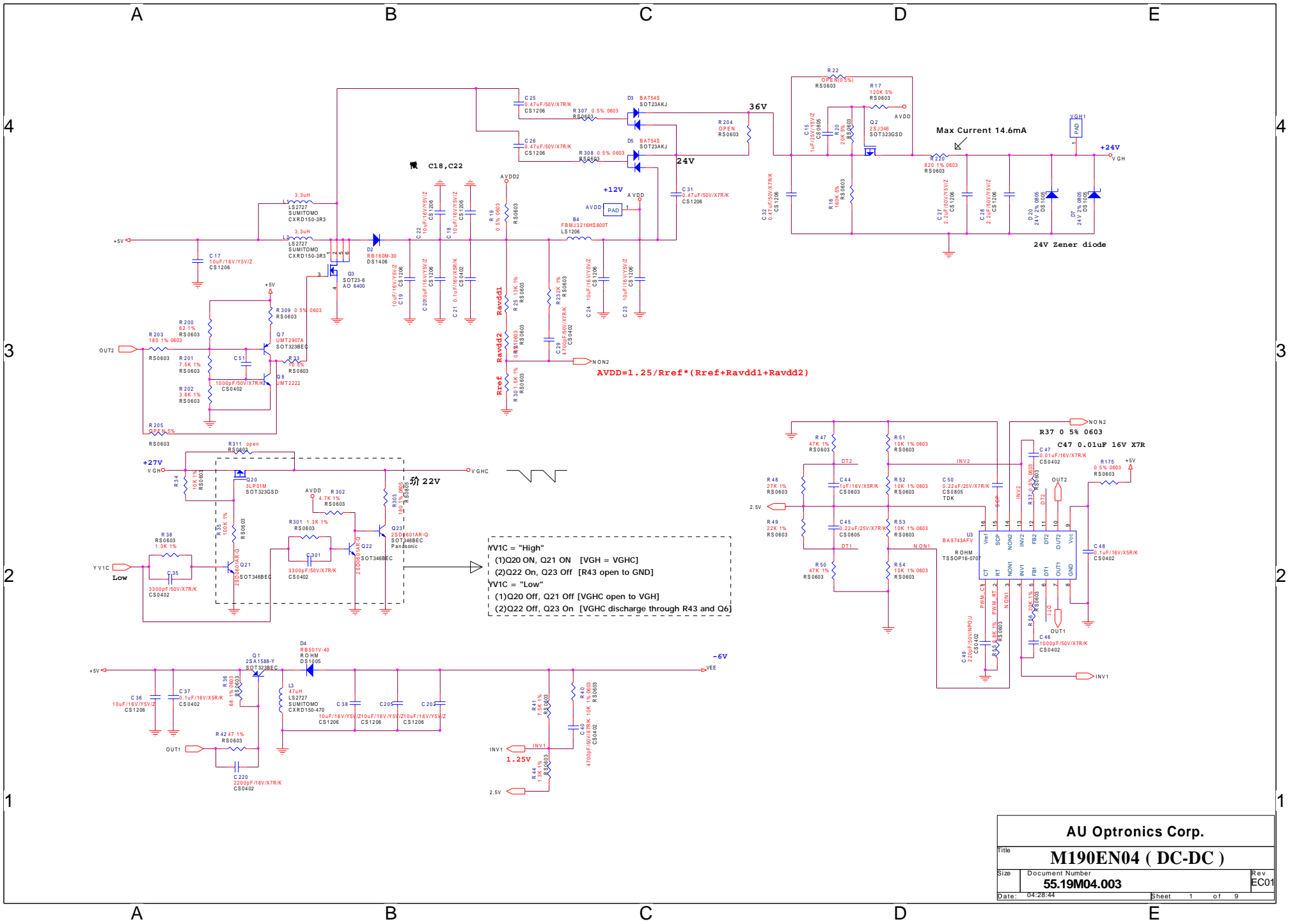
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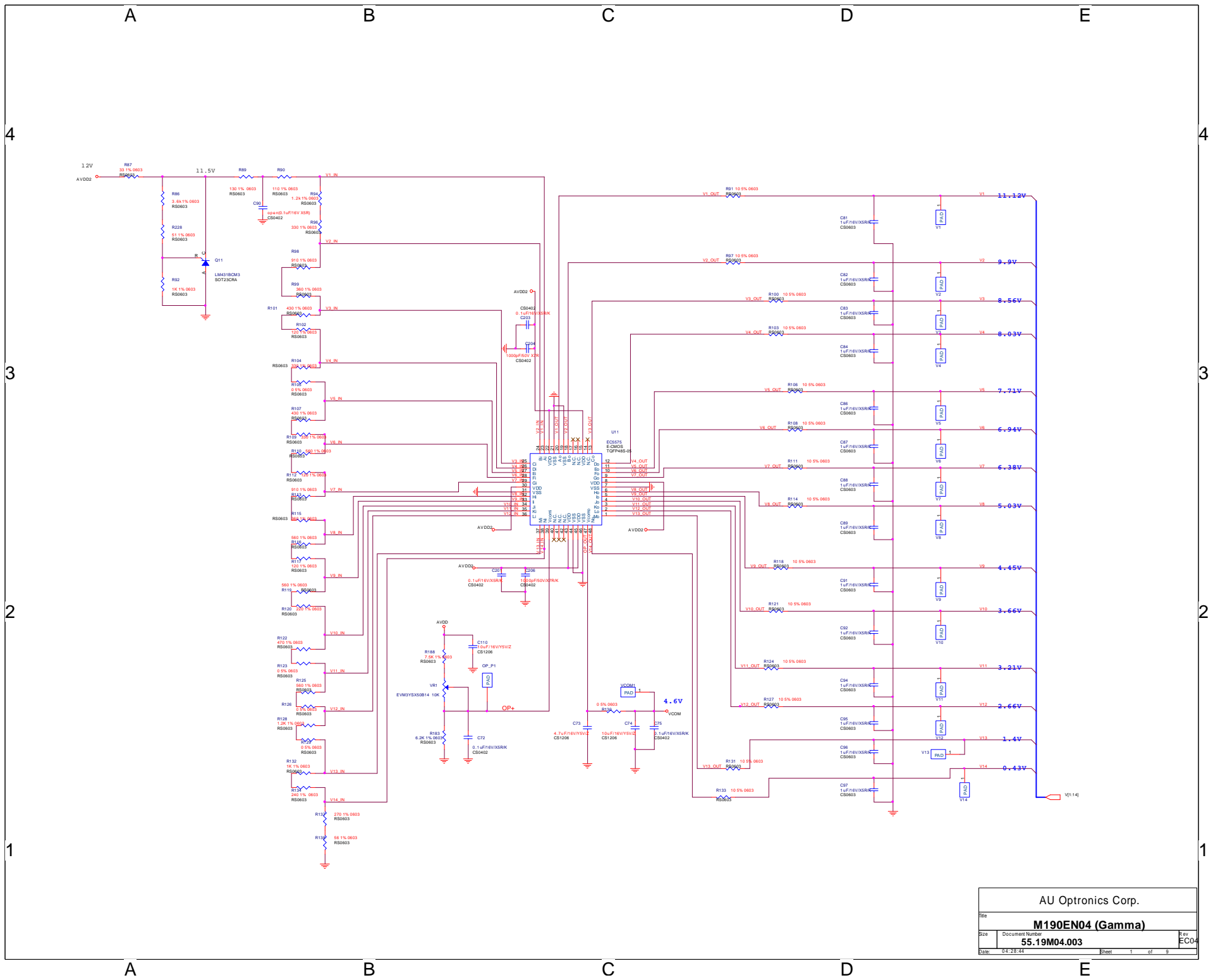
Title		
<Title>		
Size A3	Document Number <Doc>	Rev <RevCod>
Date: Thursday, June 10, 2004 Sheet 1 of 1		



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Title		
M190EN04(LVDS V33)		
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Title M190EN04 (DC-DC)		
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	55.19M04.003	EC01
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AU Optronics Corp.		
Rev	M190EN04 (Gamma)	
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	55.19M04.003	EC04
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A

B

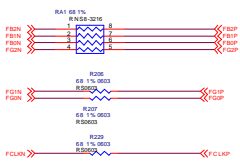
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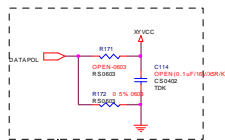
E

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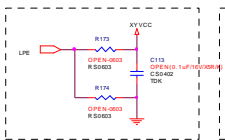
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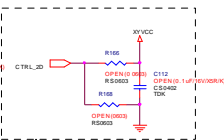
MODE	Select the output mode
1	256 CHANNELS
0	263 CHANNELS
SEL	select right or left shift
1	D101->Y1...Y264->Y2102
0	D102->Y384...Y1->Y2101



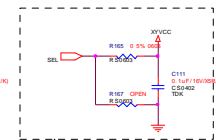
DATAPOL	DATPOL data polarity
1	Data polarity inverse
0	no inversion (normally white)



LPE	Low power control
1	Normal power, default
0	Low Power



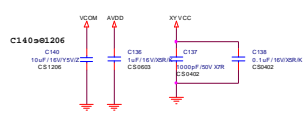
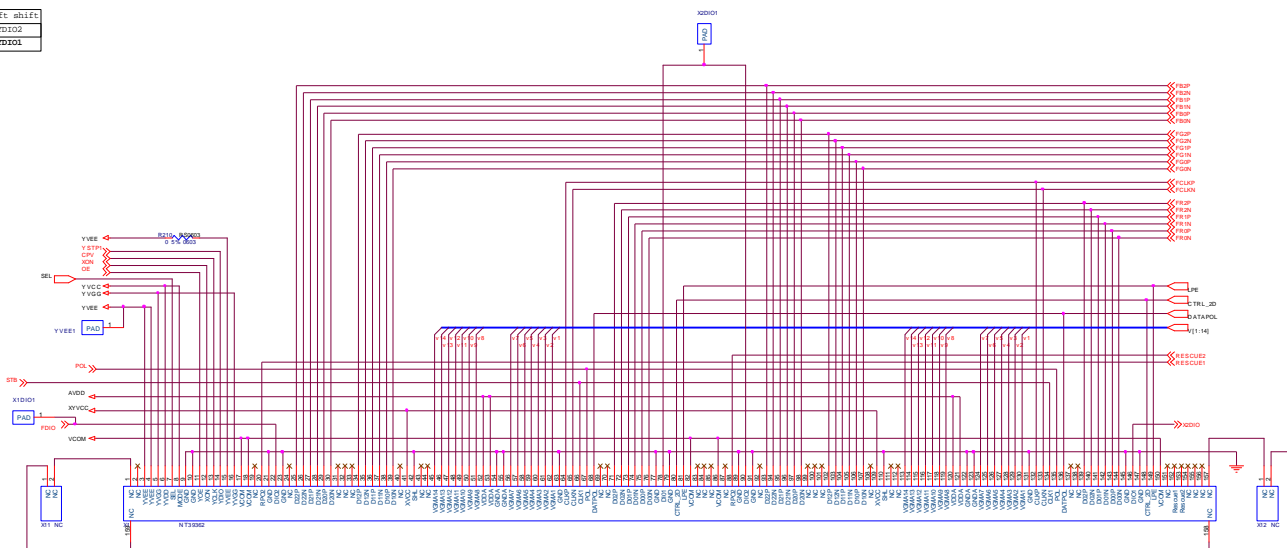
CTRL_2D	2 data inversion control
1	ONE DOT INVERSION (default)
0	TWO DOTS INVERSION



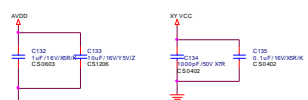
SEL	
1	NORMAL
0	ACTIVE FOR M9663549, R165 OPEN (YVBE)

3

3



Capacitors for X1



Capacitors for X2

1

1

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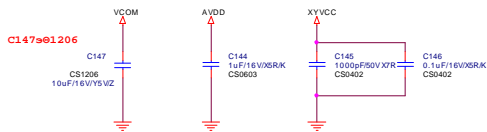
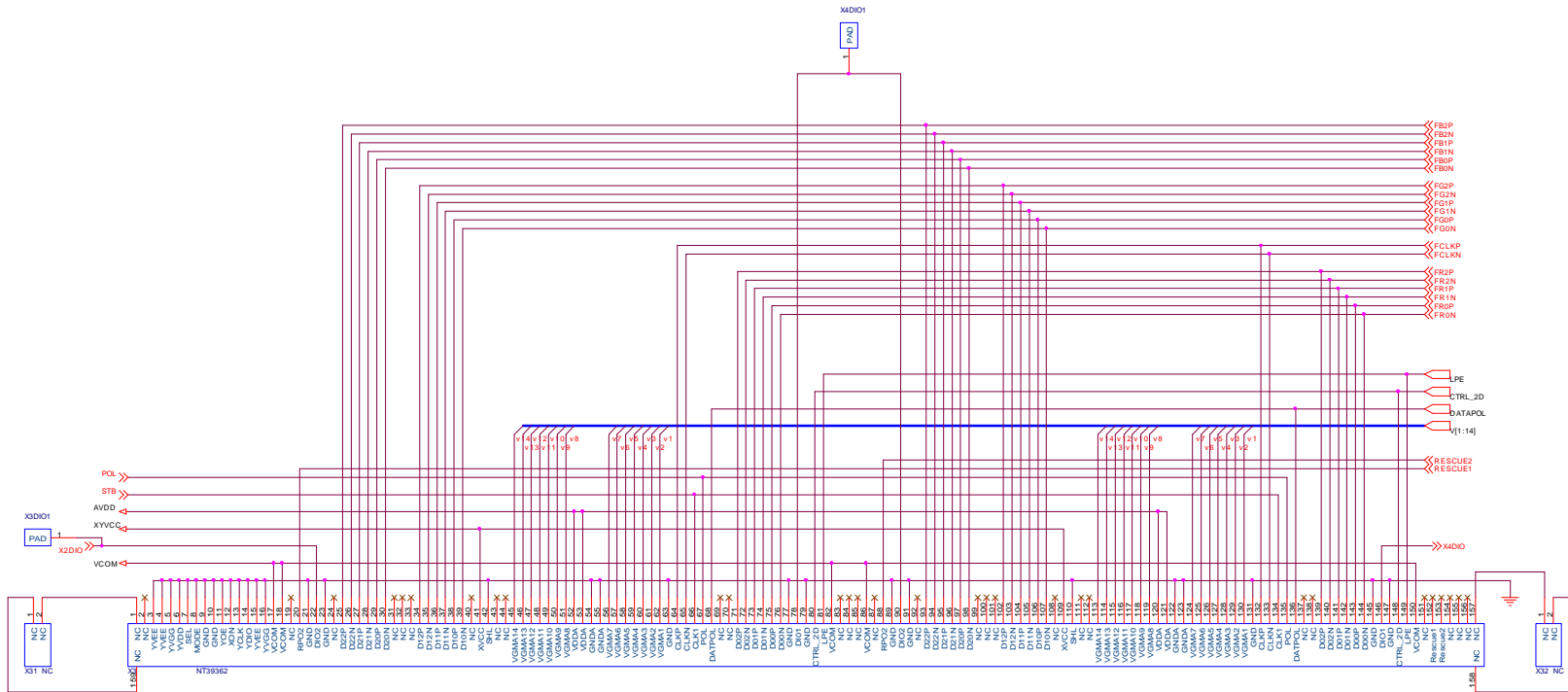
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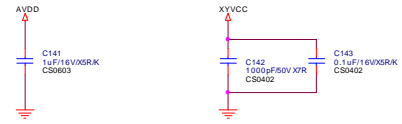
D

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M190EN04 (X-TAB X1 X2)		
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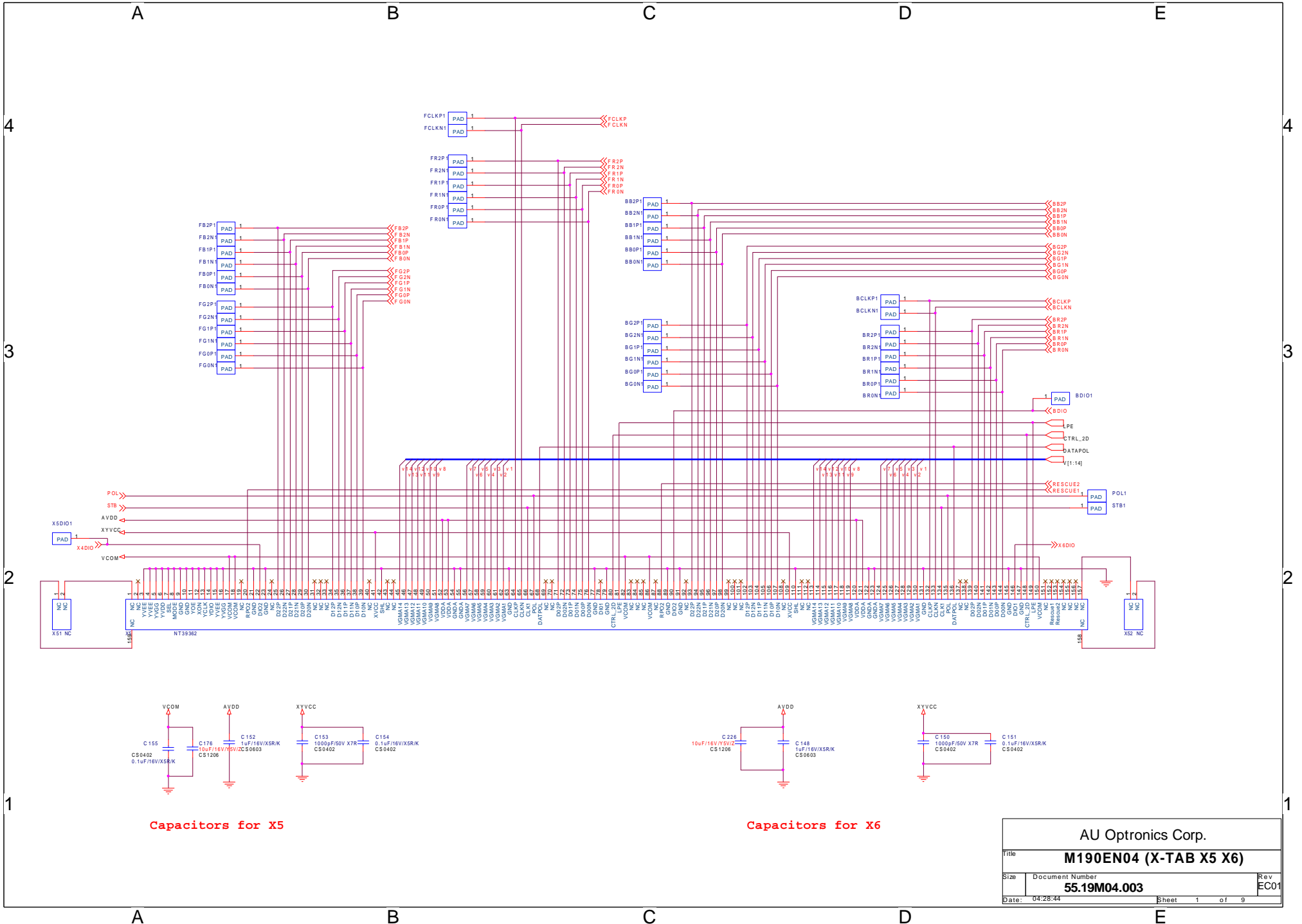


Capacitors for X3



Capacitors for X4

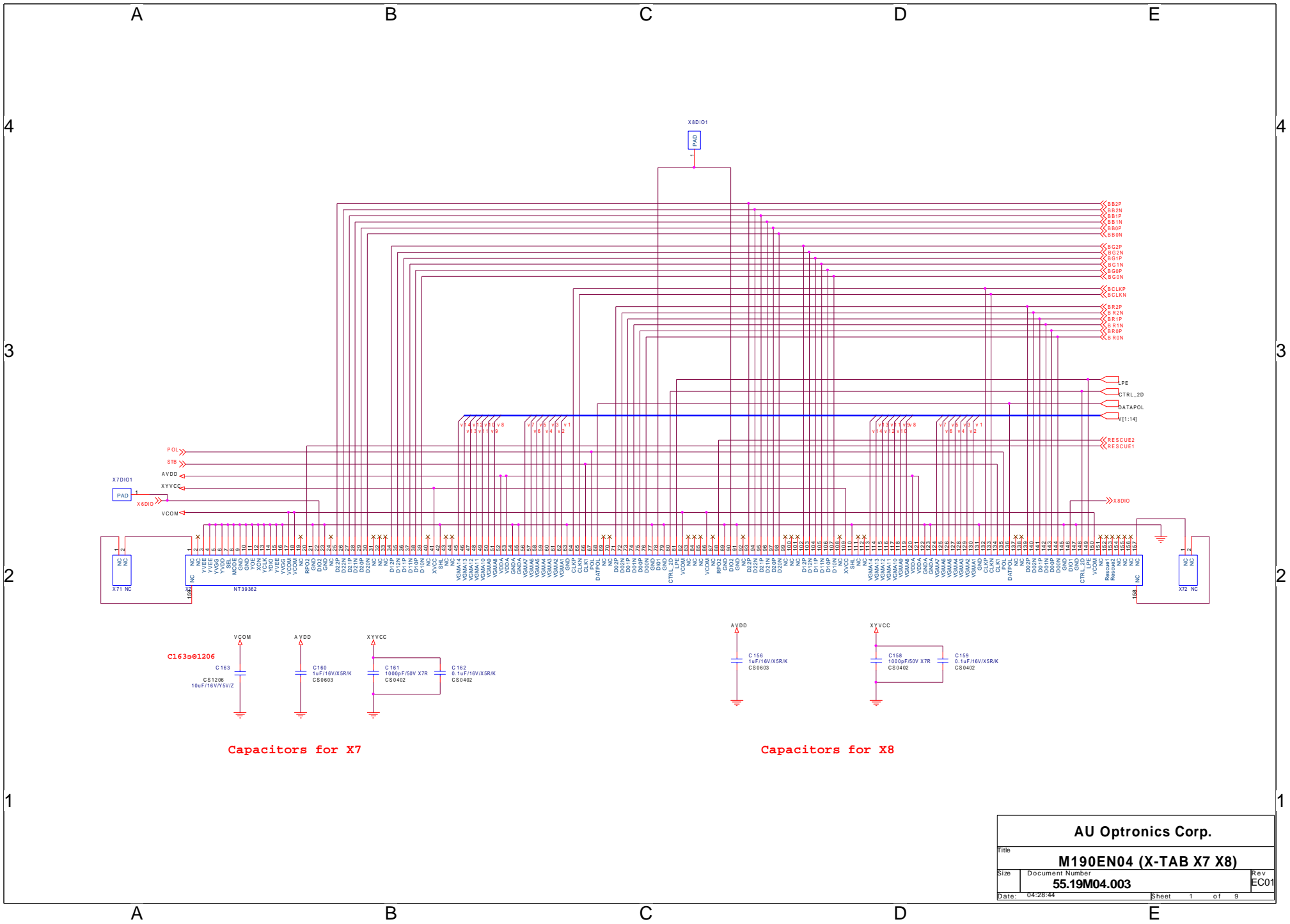
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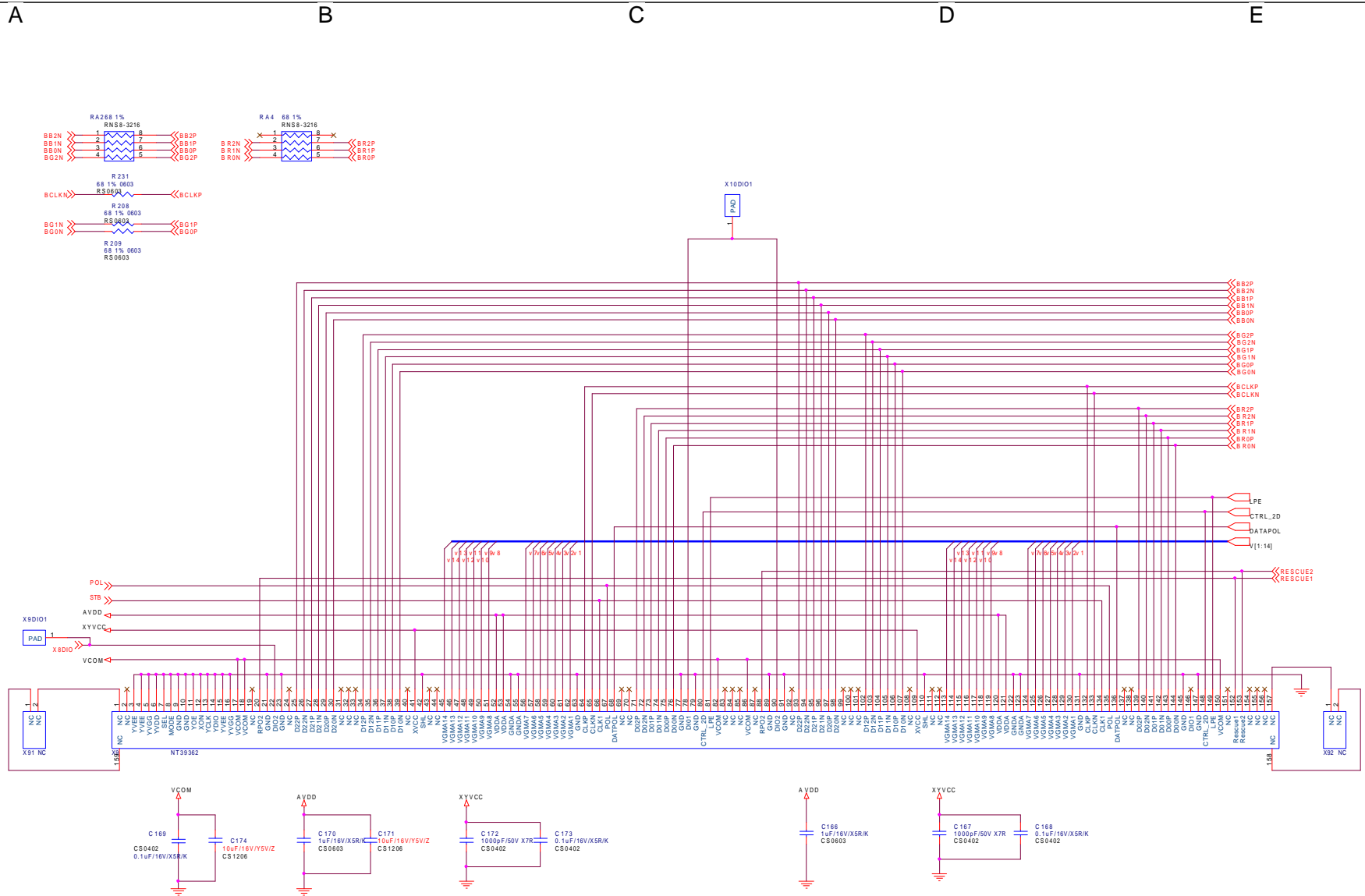
Capacitors for X5

Capacitors for X6

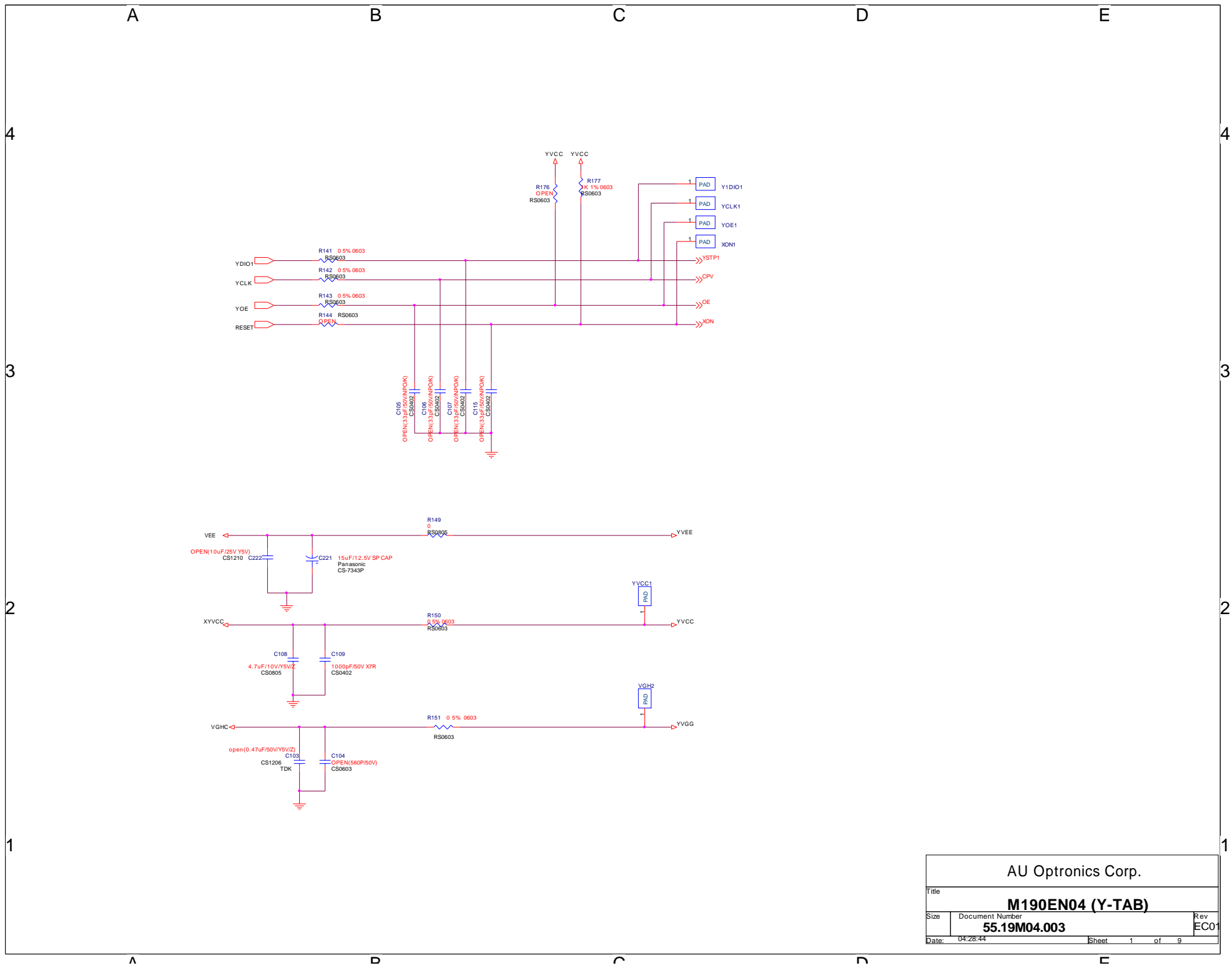
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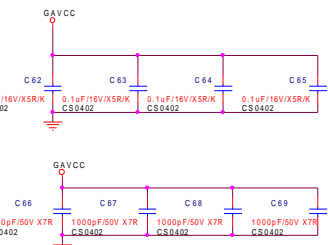
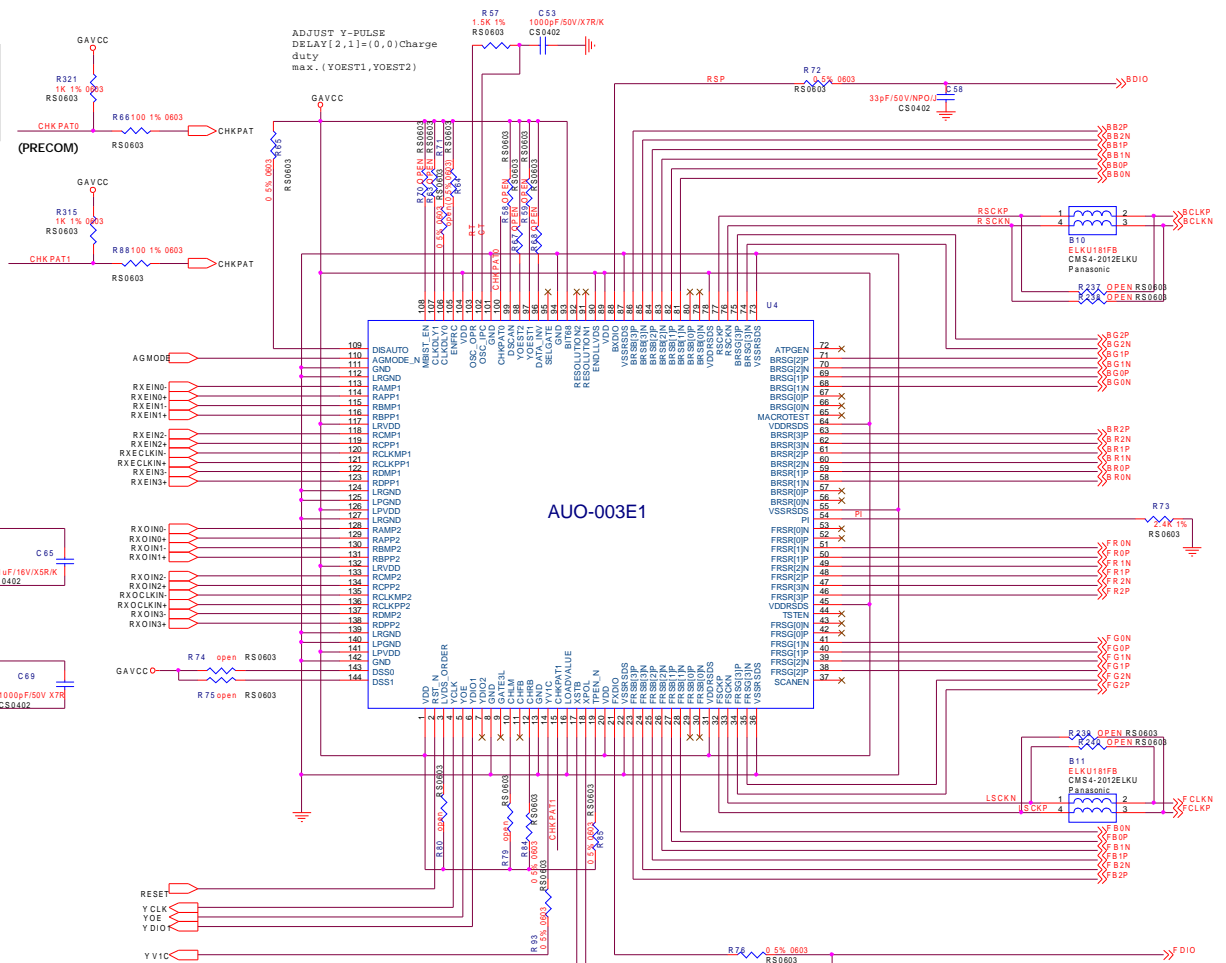
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M190EN04 (Y-TAB)		
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A B C D E

CH0	CH1	Function (For AU30702)
0	0	Dot Inversion
0	1	Chkpat1
1	0	Chkpat2
1	1	2-Line Inversion



DS0	DS1	SS Percent
1	1	+/- 3.0%
0	1	+/- 2.2%
1	0	+/- 1.6%
0	0	DISABLE

ASIC Settings

- 01. SEL68 = H, 8 Bit resolution
- 02. RESOLUTION = (L,L), SXGA
- 03. CHLR = L
- 04. CHRB = H, Change R/B
- 05. DISAUTO = H
- 06. (YOEST2,YOEST1) = (L,L), gate off period = 1.66 us
- 07. DCSCAN=L,Singal Scan
- 08. ENFRC = H, FRC ACTIVE
- 09. CLK DELAY (PIN108,107,106) = (0,0,1),-1/16 T

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