YAMAHA

PRELIMINARY

YDA179

Application Manual

D-707Di DIGITAL INPUT STEREO 20W DIGITAL AUDIO POWER AMPLIFIER

YAMAHA CORPORATION

YDA179 APPLICATION MANUAL
CATALOG No. LSI-6DA179A00
2012.12

IMPORTANT NOTICE

1. YAMAHA RESERVES THE RIGHT TO MAKE CHANGES TO ITS PRODUCTS AND TO THIS DOCUMENT WITHOUT NOTICE. THE INFORMATION CONTAINED IN THIS DOCUMENT HAS BEEN CAREFULLY CHECKED AND IS BELIEVED. HOWEVER, YAMAHA SHALL ASSUME NO RESPONSIBILITIES FOR INACCURACIES AND MAKE NO COMMITMENT TO UPDATE OR TO KEEP CURRENT THE INFORMATION CONTAINED IN THIS DOCUMENT.

2. THESE YAMAHA PRODUCTS ARE DESIGNED ONLY FOR COMMERCIAL AND NORMAL INDUSTRIAL APPLICATIONS, AND ARE NOT SUITABLE FOR OTHER USES, SUCH AS MEDICAL LIFE SUPPORT EQUIPMENT, NUCLEAR FACILITIES, CRITICAL CARE EQUIPMENT OR ANY OTHER APPLICATION THE FAILURE OF WHICH COULD LEAD TO DEATH, PERSONAL INJURY OR ENVIRONMENTAL OR PROPERTY DAMAGE. USE OF THE PRODUCTS IN ANY SUCH APPLICATION IS AT THE CUSTOMER'S OWN RISK AND EXPENSE.

3. YAMAHA SHALL ASSUME NO LIABILITY FOR INCIDENTAL, CONSEQUENTIAL OR SPECIAL DAMAGES OR INJURY THAT MAY RESULT FROM MISAPPLICATION OR IMPROPER USE OR OPERATION OF THE PRODUCT.

4. YAMAHA MAKES NO WARRANTY OR REPRESENTATION THAT THE PRODUCTS ARE SUBJECT TO INTELLECTUAL PROPERTY LICENSE FROM YAMAHA OR ANY THIRD PARTY, AND YAMAHA MAKES NO WARRANTY OR REPRESENTATION OF NON-INFRINGEMENT WITH RESPECT TO THE PRODUCTS. YAMAHA SPECIFICALLY EXCLUDES ANY LIABILITY TO THE CUSTOMER OR ANY THIRD PARTY ARISING FROM OR RELATED TO THE PRODUCTS INFRINGEMENT OF ANY THIRD PARTY'S INTELLECTUAL PROPERTY RIGHTS, INCLUDING THE PATENT, COPYRIGHT, TRADEMARK OR TRADE SECRET RIGHTS OF ANY THIRD PARTY.

5. EXAMPLES OF USE DESCRIBED HEREIN ARE MERELY TO INDICATE THE CHARACTERISTICS AND PERFORMANCE OF PRODUCTS. YAMAHA SHALL ASSUME NO RESPONSIBILITY FOR ANY INTELLECTUAL PROPERTY CLAIMES OR OTHER PROBLEMS THAT MAY RESULT FROM APPLICATIONS BASED ON THE EXAMPLES DESCRIBED HEREIN. YAMAHA MAKES NO WARRANTY WITH RESPECT TO THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR USE AND TITLE.

6. YAMAHA MAKES EVERY EFFORT TO IMPROVE THE QUALITY AND RELIABILITY OF ITS PRODUCTS. HOWEVER, ALL SEMICONDUCTOR PRODUCTS FAIL WITH SOME PROBABILITY. THEREFORE, YAMAHA REQUIRES THAT SUFFICIENT CARE BE GIVEN TO ENSURING SAFE DESIGN IN CUSTOMER PRODUCTS SUCH AS REDUNDANT DESIGN, ANTI-CONFLAGRATION DESIGN, AND DESIGN FOR PREVENTING MALFUNCTION IN ORDER TO PREVENT ACCIDENTS RESULTING IN INJURY OR DEATH, FIRE OR OTHER SOCIAL DAMAGE FROM OCCURRING AS A RESULT OF PRODUCT FAILURE.

7. INFORMATION DESCRIBED IN THIS DOCUMENT: APPLICATION CIRCUITS AND ITS CONSTANTS AND CALCULATION FORMULAS, PROGRAMS AND CONTROL PROCEDURES ARE PROVIDED FOR THE PURPOSE OF EXPLAINING TYPICAL OPERATION AND USAGE. THEREFORE, PLEASE EVALUATE THE DESIGN SUFFICIENTLY AS WHOLE SYSTEM UNDER THE CONSIDERATION OF VARIOUS EXTERNAL OR ENVIRONMENTAL CONDITIONS AND DETERMINE THEIR APPLICATION AT THE CUSTOMER'S OWN RISK. YAMAHA SHALL ASSUME NO RESPONSIBILITY FOR CLAIMS, DAMAGES, COSTS AND EXPENSES CAUSED BY THE CUSTOMER OR ANY THIRD PARTY, OWING TO THE USE OF THE ABOVE INFORMATION.

PRECAUTIONS AND INSTRUCTIONS FOR SAFETY

	WARNING
Prohibited	Do not use the device under stresses beyond those listed in Absolute Maximum Ratings.Such stresses may become causes of breakdown, damages, or deterioration, causing explosion or ignition, and this may lead to fire or personal injury.
Prohibited	Do not mount the device reversely or improperly and also do not connect a supply voltage in wrong polarity. Otherwise, this may cause current and/or power-consumption to exceed the absolute maximum ratings, causing personal injury due to explosion or ignition as well as causing breakdown, damages, or deterioration. And, do not use the device again that has been improperly mounted and powered once.
Prohibited	Do not short between pins.In particular, when different power supply pins, such as between high-voltage and low-voltage pins, are shorted, smoke, fire, or explosion may take place.
Instructions	As to devices capable of generating sound from its speaker outputs, please design with safety of your products and system in mind, such as the consequences of unusual speaker output due to a malfunction or failure. A speaker dissipates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When a DC signal (several Hz or less) is input due to device failure, heat dissipation characteristics degrade rapidly, thereby leading to voice-coil burnout, smoking or ignition of the speaker even if it is used within the rated input value.

	CAUTION
Prohibited	Do not use Yamaha products in close proximity to burning materials, combustible substances, or inflammable materials, in order to prevent the spread of the fire caused by Yamaha products, and to prevent the smoke or fire of Yamaha products due to peripheral components.
Instructions	Generally, semiconductor products may malfunction and break down due to aging, degradation, etc. It is the responsibility of the designer to take actions such as safety design of products and the entire system and also fail-safe design according to applications, so as not to cause property damage and/or bodily injury due to malfunction and/or failure of semiconductor products.
Instructions	The built-in DSP may output the maximum amplitude waveform suddenly due to malfunction from disturbances etc. and this may cause damage to headphones, external amplifiers, and human body (the ear). Please pay attention to safety measures for device malfunction and failure both in product and system design.
Instructions	As semiconductor devices are not nonflammable, overcurrent or failure may cause smoke or fire. Therefore, products should be designed with safety in mind such as using overcurrent protection circuits to control the amount of current during operation and to shut off on failure.
Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high-temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the protection circuit kicks in.
Instructions	Use a robust power supply.The use of an unrobust power supply may lead to malfunctions of the protection circuit, causing device breakdown, personal injury due to explosion, or smoke or fire.
Instructions	Product's housing should be designed with the considerations of short-circuiting between pins of the mounted device due to foreign conductive substances (such as metal pins etc.). Moreover, the housing should be designed with spatter prevention etc. due to explosion or burning. Otherwise, the spattered substance may cause bodily injury.
Instructions	The device may be heated to a high temperature due to internal heat generation during operation.Therefore, please take care not to touch an operating device directly.
Instructions	Electrostatic discharges can damage and destroy semiconductor devices.Pay close attention to static build-up when handling devices.

v03

< Table of Contents >

1. Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting)
  Loudspeaker: 97dB (PSNR), 106dB (DR) @22V
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x, 1024x Fs
  256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz/176.4kHz/192kHz
- Supply voltage
  3.3V for digital circuit
  10V~22V for loudspeaker driver
- Loudspeaker output power for Stereo@22V
  10W x 2ch into 8Ω @0.13% THD+N
  15W x 2ch into 8Ω @0.16% THD+N
  20W x 2ch into 8Ω @0.22% THD+N
- Sounds processing including:
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Power clipping
  Channel mixing
  User programmed noise gate
  DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I^2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Power saving mode
- Dynamic temperature control

2. Applications

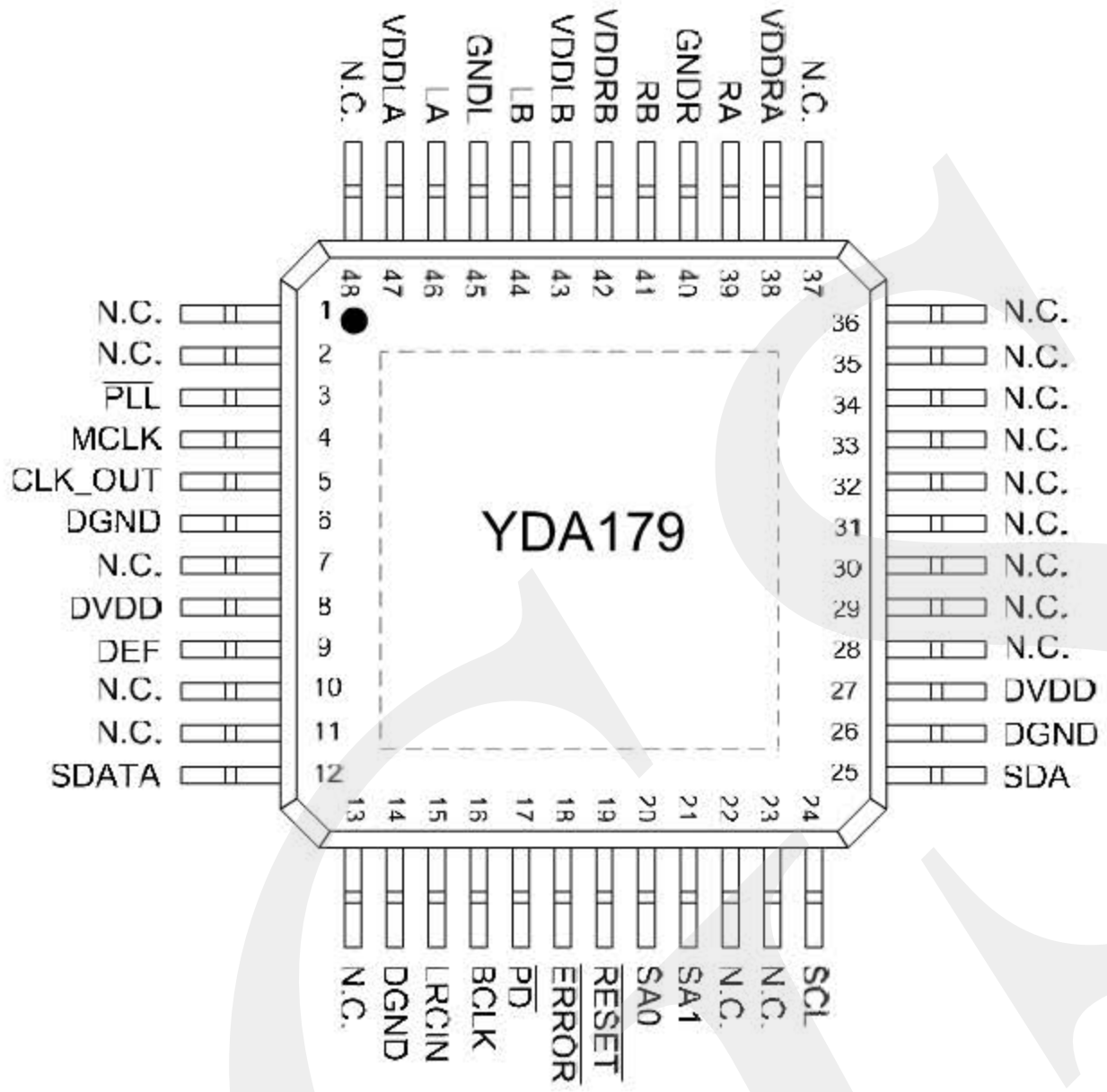
- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

3. Description

YDA179 is a digital audio amplifier capable of driving a pair of 8Ω, 20W speaker, which operate with play music at a 22V supply without external heat-sink or fan requirement.

Using I^2C digital control interface, the user can control YDA179's input format selection, mute and volume control functions. YDA179 has many built-in protection circuits to safeguard YDA179 from connection errors.

4. Pin Assignment



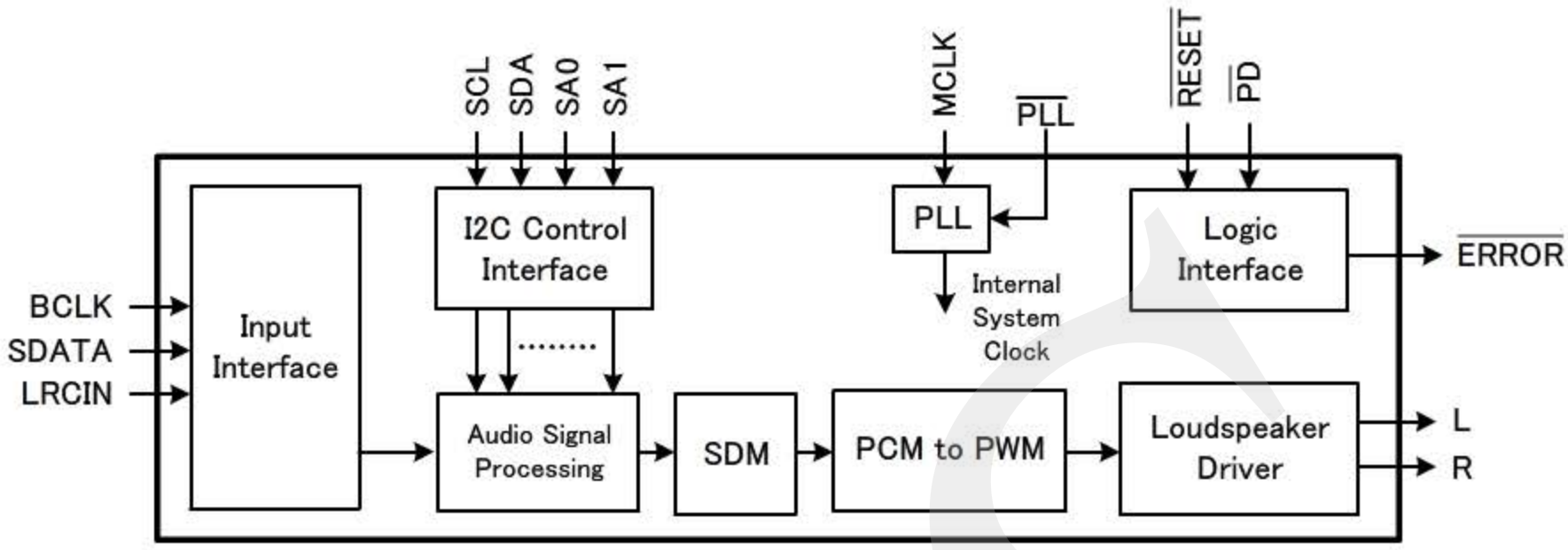
< 48 pin SQFP Top View >

5. Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	N.C.			
2	N.C.			
3	$\overline{\text{PLL}}$	I	PLL enable, low active	Schmitt trigger TTL input buffer
4	MCLK	I	Master clock input	Schmitt trigger TTL input buffer
5	CLK_OUT	O	Clock output from PLL	TTL output buffer
6	DGND	P	Digital Ground	
7	N.C.			
8	DVDD	P	Digital Power	
9	DEF	I	Default volume setting	Schmitt trigger TTL input buffer
10	N.C.			
11	N.C.			
12	SDATA	I	Serial audio data input	Schmitt trigger TTL input buffer
13	N.C			

14	DGND	P	Digital Ground	
15	LRCIN	I	Left/Right clock input (Fs)	Schmitt trigger TTL input buffer
16	BCLK	I	Bit clock input (64Fs)	Schmitt trigger TTL input buffer
17	$\overline{PD}$	I	Power down, low active	Schmitt trigger TTL input buffer
18	$\overline{ERROR}$	O	Error status	Open-drain output
19	$\overline{RESET}$	I	Reset, low active	Schmitt trigger TTL input buffer
20	SA0	I	I^2C select address 0	Schmitt trigger TTL input buffer
21	SA1	I	I^2C select address 1	Schmitt trigger TTL input buffer
22	N.C			
23	N.C			
24	SCL	I	I^2C serial clock input	Schmitt trigger TTL input buffer
25	SDA	I/O	I^2C bi-directional serial data	Schmitt trigger TTL input buffer
26	DGND	P	Digital Ground	
27	DVDD	P	Digital Power	
28	N.C			
29	N.C			
30	N.C			
31	N.C			
32	N.C			
33	N.C			
34	N.C			
35	N.C			
36	N.C.			
37	N.C.			
38	VDDRA	P	Right channel supply A	
39	RA	O	Right channel output A	
40	GNDR	P	Right channel ground	
41	RB	O	Right channel output B	
42	VDDRB	P	Right channel supply B	
43	VDDLB	P	Left channel supply B	
44	LB	O	Left channel output B	
45	GNDL	P	Left channel ground	
46	LA	O	Left channel output A	
47	VDDLA	P	Left channel supply A	
48	N.C.			

6. Functional Block Diagram



7. Thermal Resistance

Package Type	θ_{ja}(°C/W)	Ψ_{jt}(°C/W)	Exposed Thermal Pad
48SQFP	22.9	1.64	Yes (Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	24	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

8.2. Recommended Operating Conditions

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~22	V
T_A	Ambient Operating Temperature	0~70	°C

8.3. General Electrical Characteristics

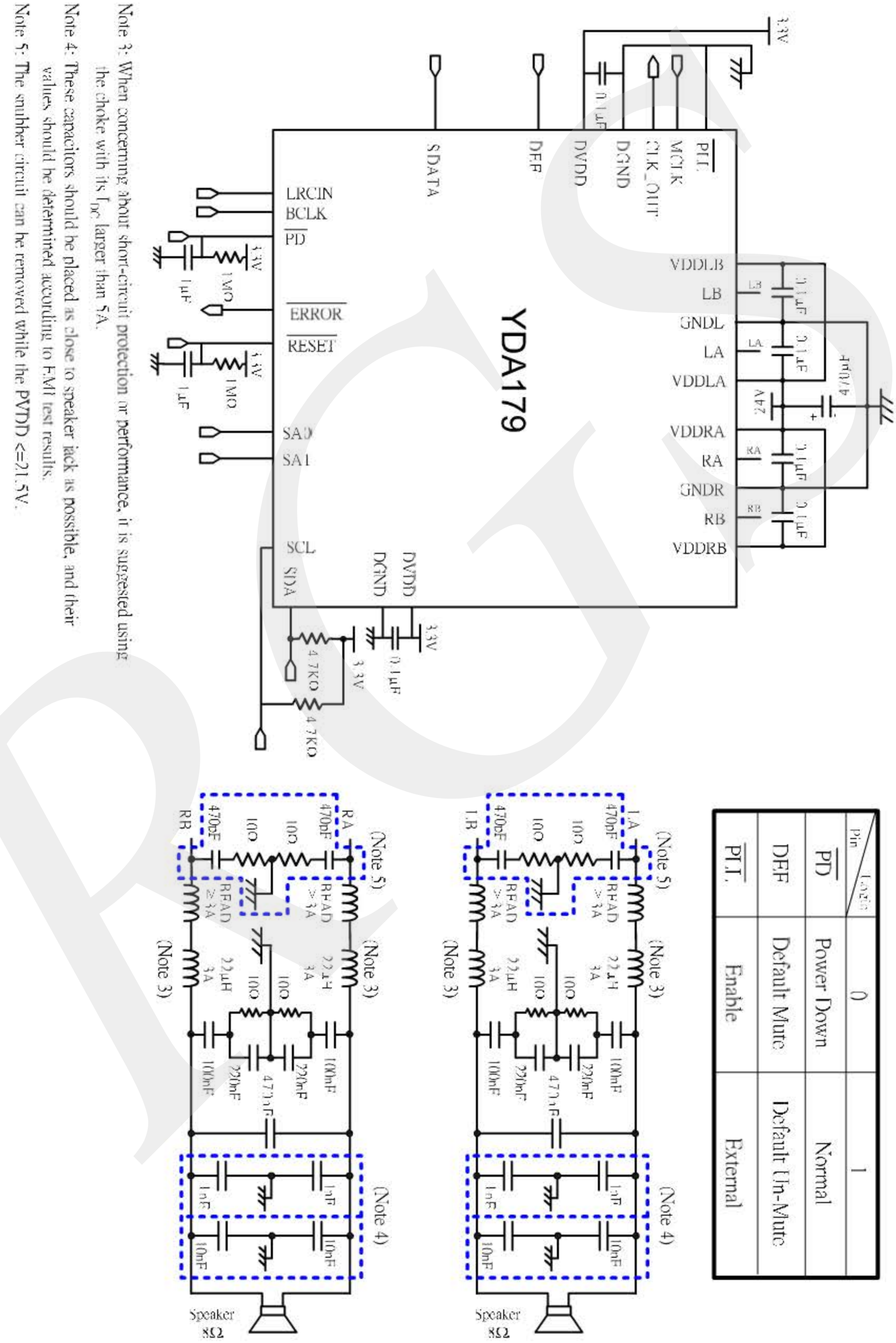
Condition: T_A=25 °C (unless otherwise specified).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{PD}(HV)	PVDD Supply Current during Power Down	PVDD=22V	—	18	200	uA
I_{PD}(LV)	DVDD Supply Current during Power Down	DVDD=3.3V	—	4	20	uA
I_Q(HV)	Quiescent current for PVDD (50%/50% PWM duty)	PVDD=22V	—	17	—	mA
I_Q(LV)	Quiescent current for DVDD	DVDD=3.3V	—	16.5	—	mA
T_{SENSOR}	Junction Temperature for Driver Shutdown		—	160	—	°C
	Temperature Hysteresis for Recovery from Shutdown		—	35	—	°C
UV_H	Under Voltage Disabled (For DVDD)		—	2.8	—	V
UV_L	Under Voltage Enabled (For DVDD)		—	2.7	—	V
Rds-on	Static Drain-to-Source On-state Resistor, PMOS	PVDD=22V, Id=500mA	—	285	—	mΩ
	Static Drain-to-Source On-state Resistor, NMOS		—	190	—	mΩ
I_{SC}	L(R) Channel Over-Current Protection (Note 2)	PVDD=22V	—	5	—	A
V_{IH}	High-Level Input Voltage	DVDD=3.3V	2.0	—	—	V
V_{IL}	Low-Level Input Voltage	DVDD=3.3V	—	—	0.8	V
V_{OH}	High-Level Output Voltage	DVDD=3.3V	2.4	—	—	V
V_{OL}	Low-Level Output Voltage	DVDD=3.3V	—	—	0.4	V
C_I	Input Capacitance		—	6.4	—	pF

Note 2: Loudspeaker over-current protection is only effective when loudspeaker drivers are properly connected with external LC filters. Please refer to the application circuit example for recommended LC filter configuration.

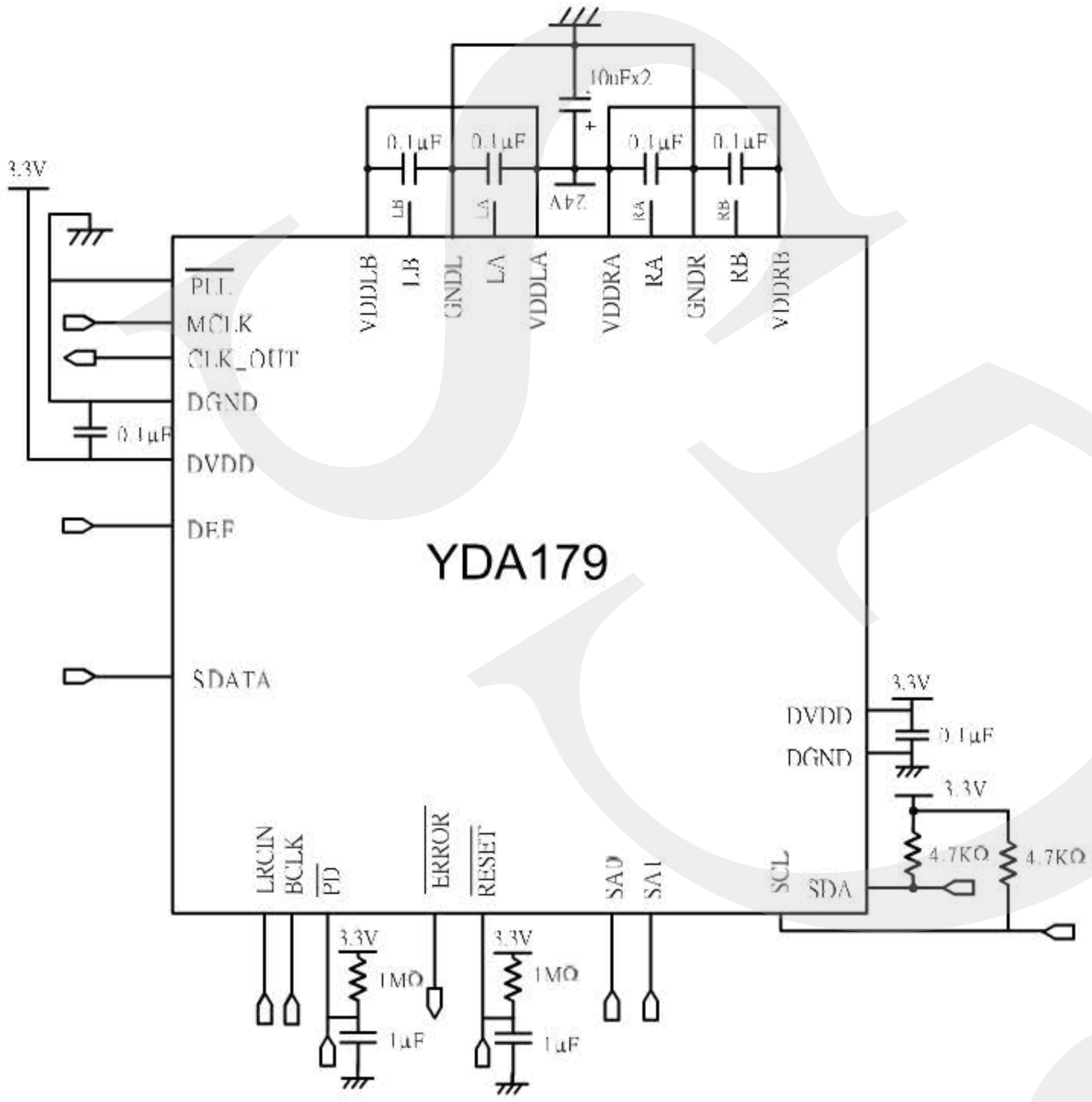
9. Application Information

9.1. Application Circuit Example for Stereo

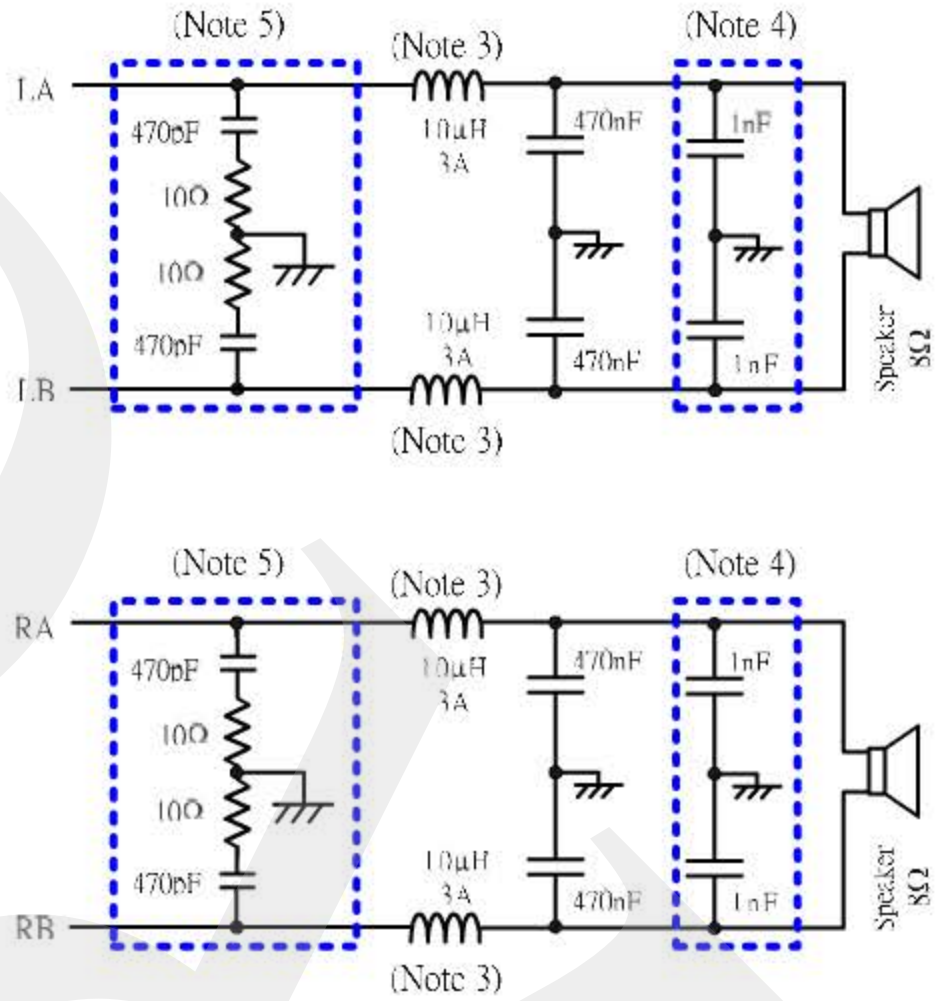


Pin / Function	0	1
$\overline{PD}$	Power Down	Normal
DFF	Default Mute	Default Un-Mute
$\overline{PLT}$	Enable	External

9.2. Application Circuit Example for Stereo (Economic type, moderate EMI suppression)



Pin \ Logic	0	1
$\overline{PD}$	Power Down	Normal
DEF	Default Mute	Default Un-Mute
$\overline{PLL}$	Enable	External



Note 3: When concerning about short-circuit protection or performance, it is suggested using the choke with its I_{DC} larger than 5A.

Note 4: These capacitors should be placed as close to speaker jack as possible, and their values should be determined according to EMI test results.

Note 5: The snubber circuit can be removed while the PVDD <=21.5V.

10. Electrical Characteristics and Specifications for Loudspeaker

- **Stereo output with 22V supply voltage**

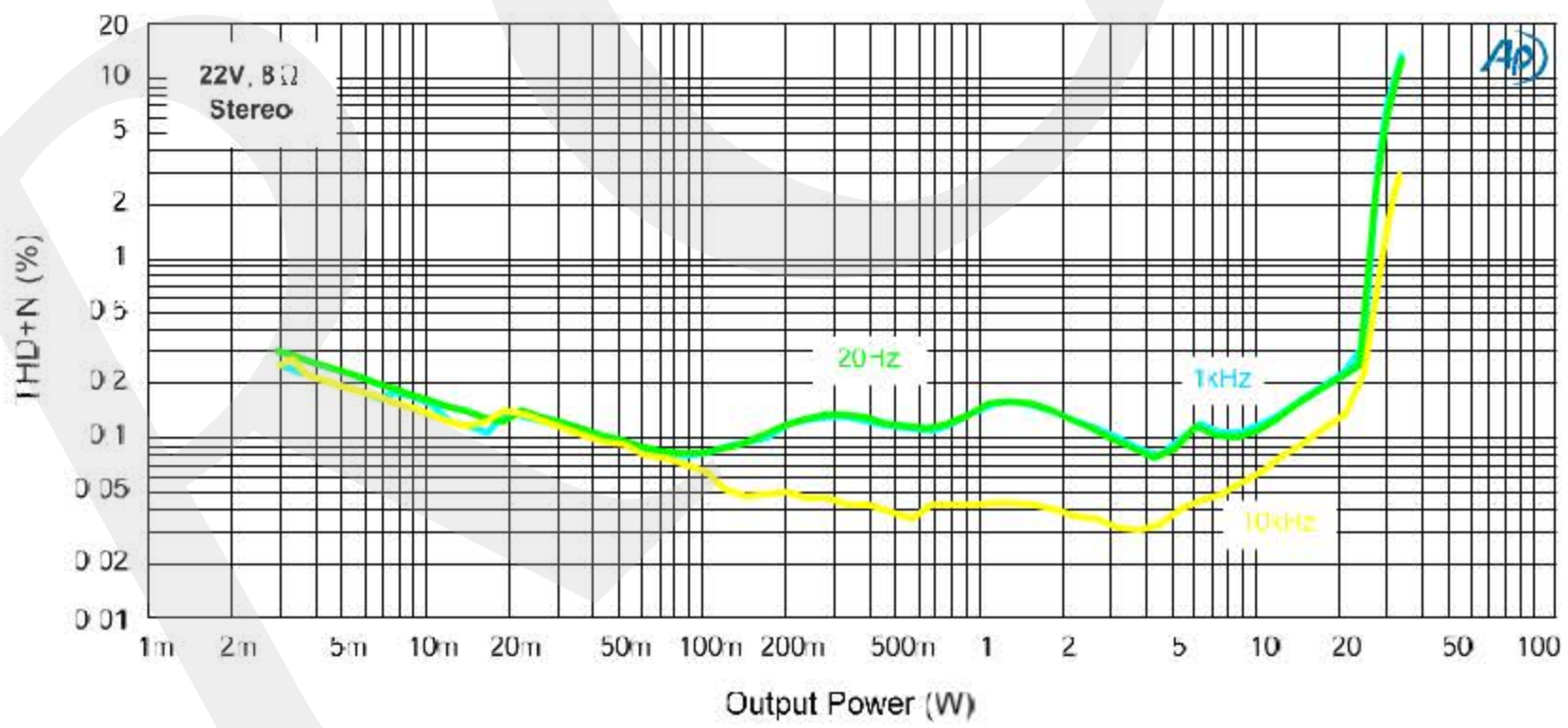
Condition: T_A=25°C, DVDD=3.3V, VDDL=VDDR=22V, F_S=48kHz, Load=8Ωwith passive LC lowpass filter (L=22μH with R_{DC}=0.12Ω, C=470nF); Input is 1kHz sinewave. Volume is 0dB unless otherwise specified.

Symbol	Parameter	Condition	Input Level	Min	Typ	Max	Units
P_O (Note 9)	RMS Output Power (THD+N=0.22%)	+8dB volume		—	20	—	W
	RMS Output Power (THD+N=0.16%)			—	15	—	W
	RMS Output Power (THD+N=0.13%)			—	10	—	W
THD+N	Total Harmonic Distortion + Noise	P_O=7.5W		—	0.1	—	%
SNR	Signal to Noise Ratio (Note 8)	+8dB volume	-9dB	—	97	—	dB
DR	Dynamic Range (Note 8)	+8dB volume	-68dB	—	106	—	dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE}=1V_{RMS} at 1kHz		—	77	—	dB
	Channel Separation (non-shield choke)	P_O=1W at 1kHz		—	70	—	dB

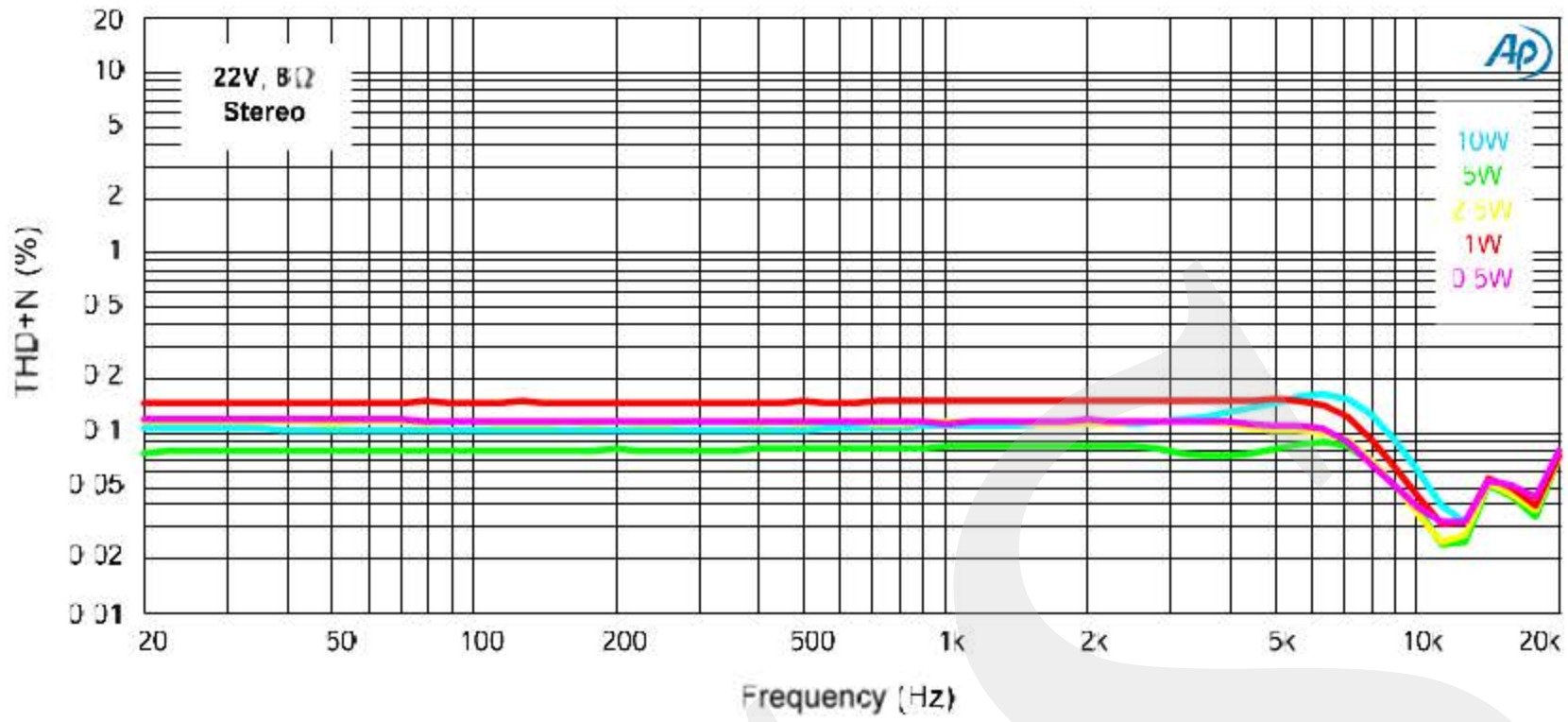
Note 8: Measured with A-weighting filter.

Note 9: Heat dissipation is limited by package type and PCB design, the external heat-sink or system cooling method should be adopted for RMS power output.

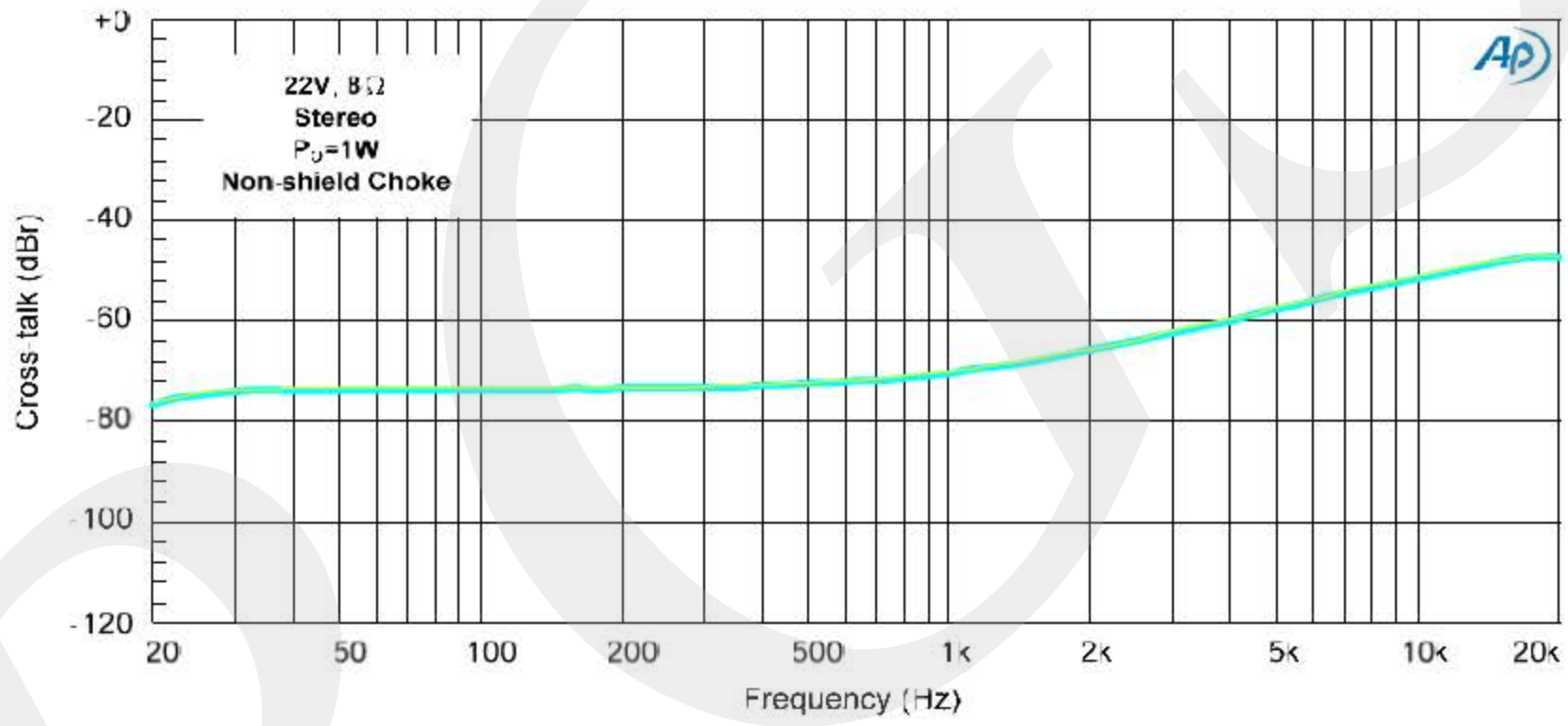
Total Harmonic Distortion + Noise vs. Output Power (Stereo)



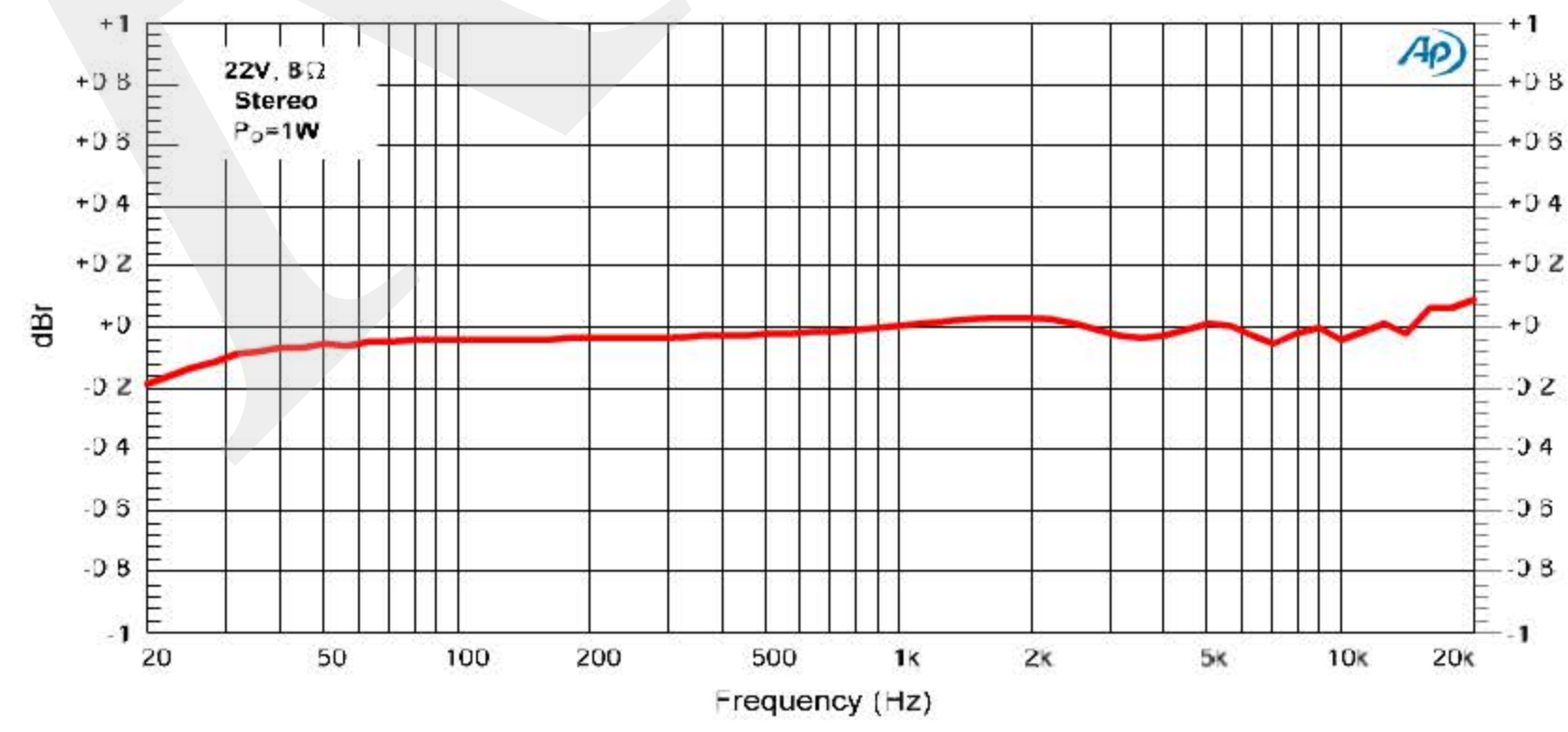
Total Harmonic Distortion + Noise vs. Frequency (Stereo)



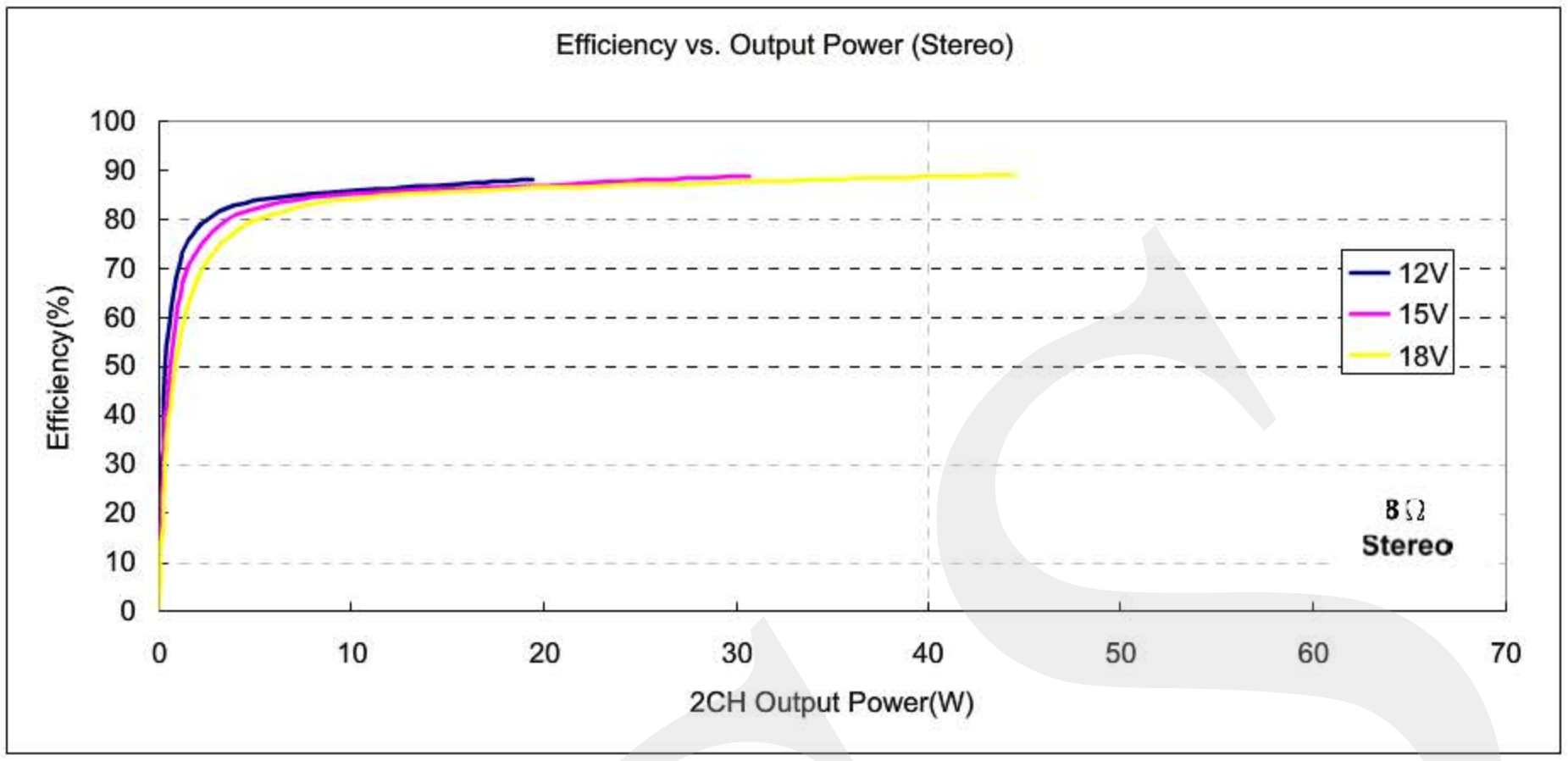
Cross-talk (Stereo)



Frequency Response (Stereo)

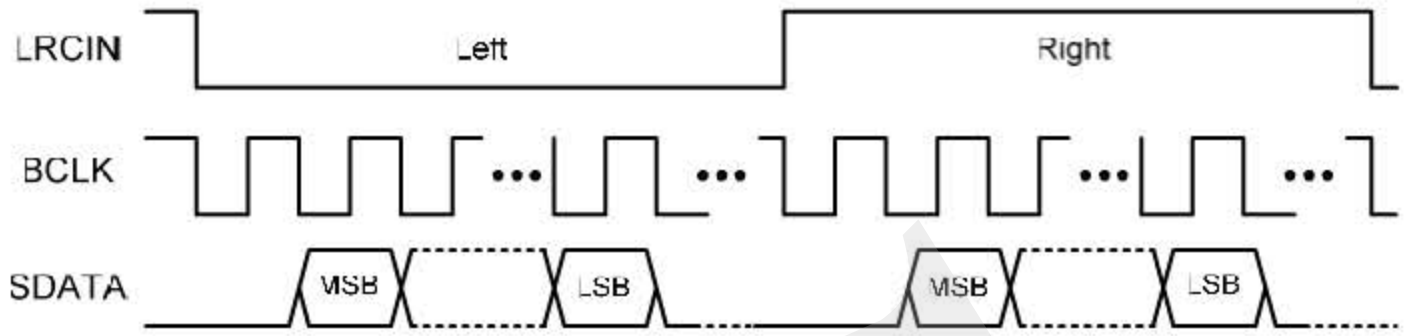


Efficiency (Stereo)

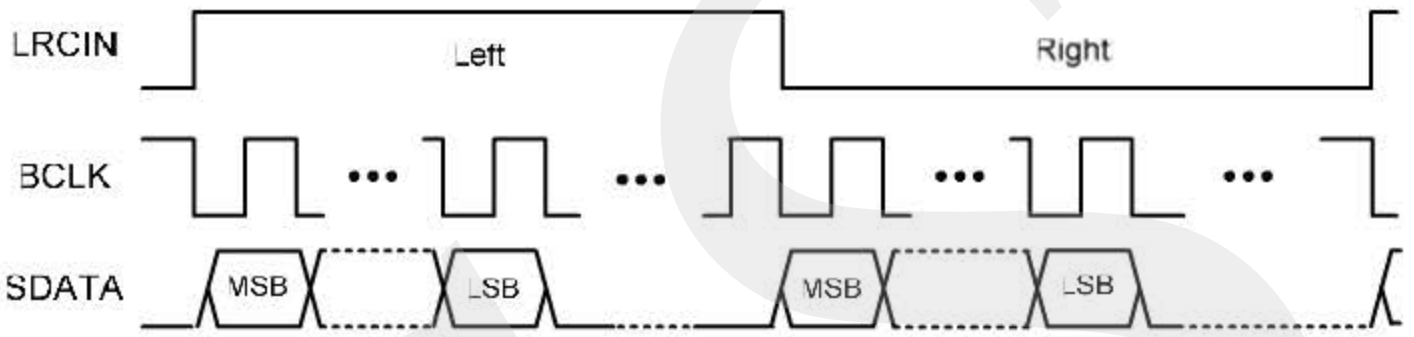


11. Interface Configuration

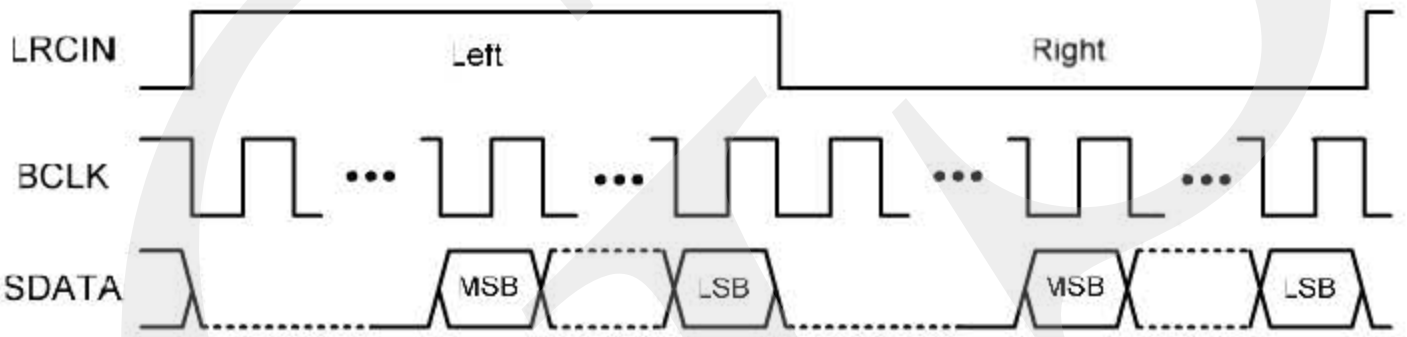
- I^2S



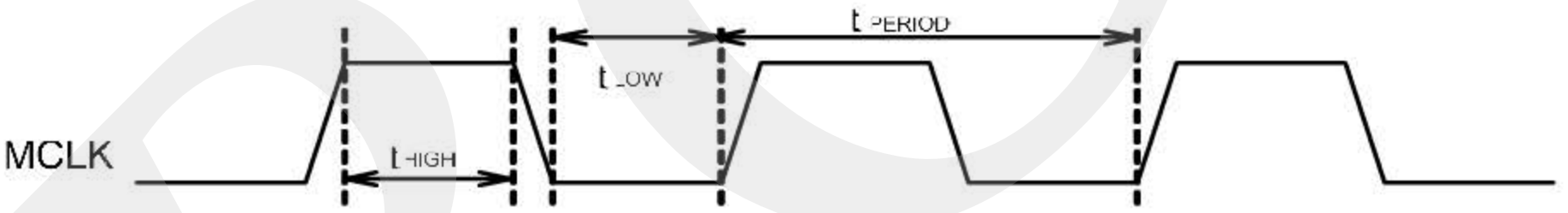
- Left-Alignment



- Right-Alignment

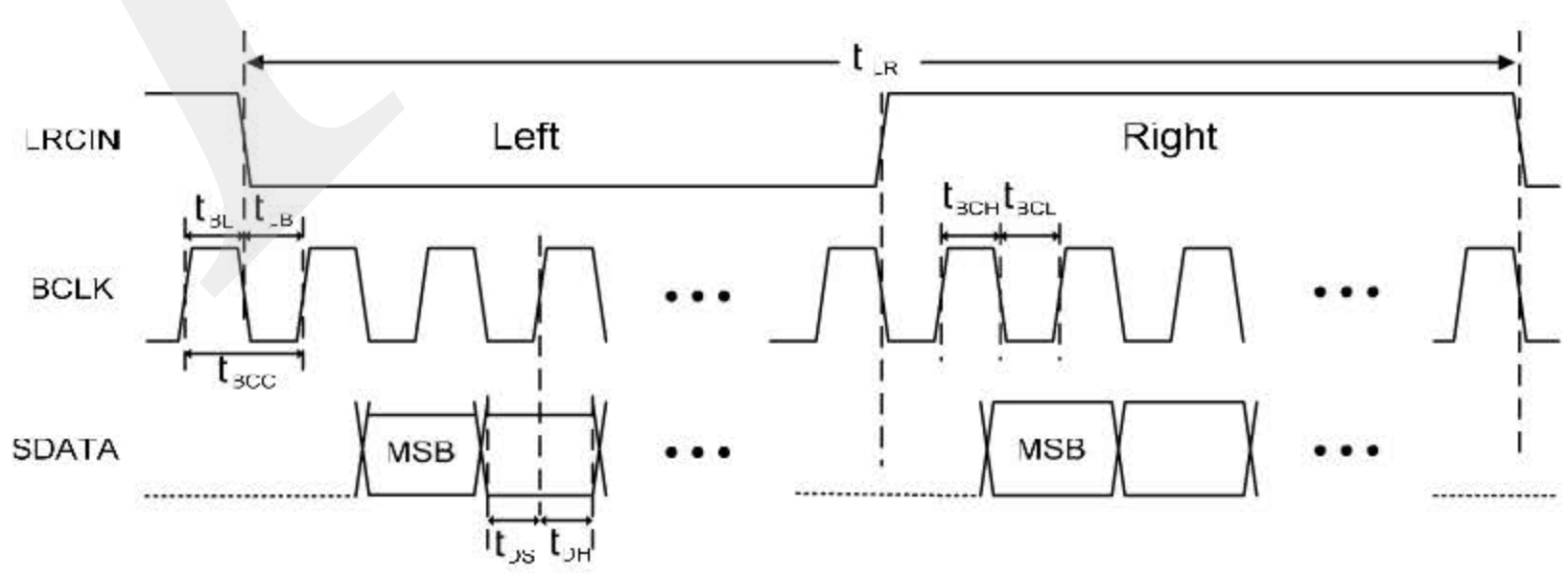


- System Clock Timing



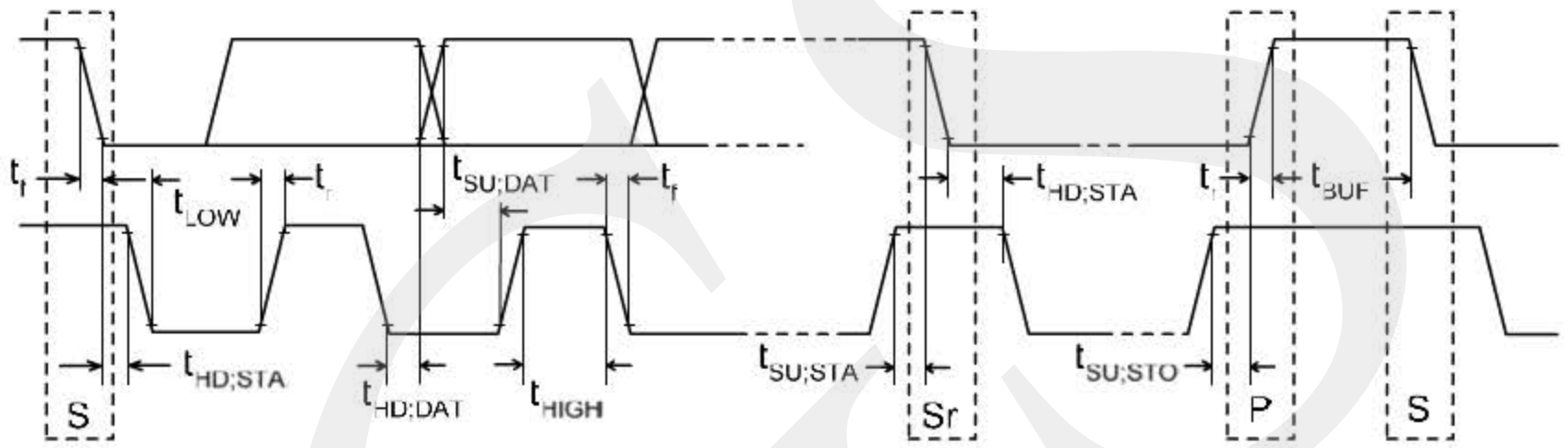
$t_{HIGH} \geqq 40.4$ ns , $t_{LOW} \geqq 40.4$ ns , $t_{PERIOD} \geqq 80.8$ ns	Default setting,when PLL is enable
$t_{HIGH} \geqq 10.1$ ns , $t_{LOW} \geqq 10.1$ ns , $t_{PERIOD} \geqq 20.2$ ns	When PLL is disable

- Timing Relationship (Using I^2S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	10.41	—	31.25	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	50	—	—	ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	50	—	—	ns
t_{BCC}	BCLK Period ($1/64F_S$)	162.76	—	488.3	ns
t_{BCH}	BCLK Pulse Width High	81.38	—	244	ns
t_{BCL}	BCLK Pulse Width Low	81.38	—	244	ns
t_{DS}	SDATA Set-Up Time	50	—	—	ns
t_{DH}	SDATA Hold Time	50	—	—	ns

- I^2C Timing



Parameter	Symbol	Standard Mode		Fast Mode		Unit
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition	$t_{HD,STA}$	4.0	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	0.6	—	μs
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	—	0.6	—	μs
Data hold time for I^2C bus devices	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Data setup time	$t_{SU;DAT}$	250	—	100	—	ns
Rise time of both SDA and SDL signals	t_r	—	1000	20+0.1Cb	300	ns
Fall time of both SDA and SDL signals	t_f	—	300	20+0.1Cb	300	ns
Setup time for STOP condition	$t_{SU;STO}$	4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	—	1.3	—	μs
Capacitive load for each bus line	C_b	—	400	—	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	—	$0.1V_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	—	$0.2V_{DD}$	—	V

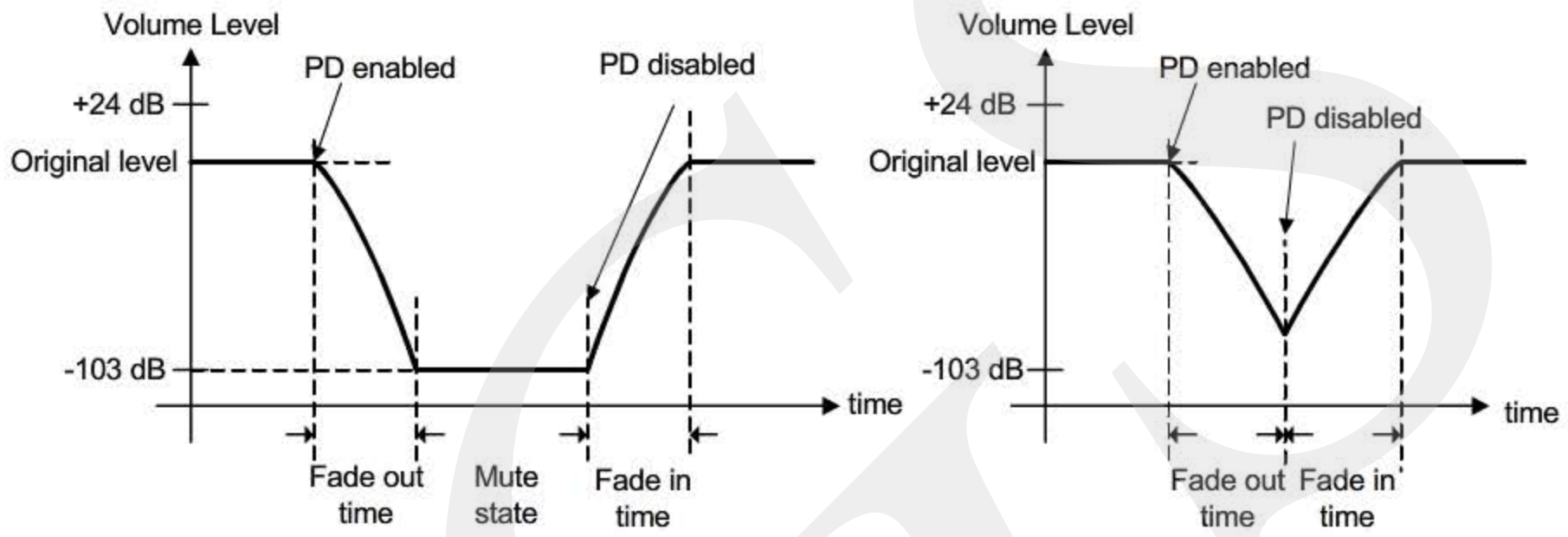
12. Operation Description

- Reset

  When the $\overline{\text{RESET}}$ pin is lowered, YDA179 will clear the stored data and reset the register table to default values. YDA179 will exit reset state at the 256th MCLK cycle after the $\overline{\text{RESET}}$ pin is raised to high.

- Power down control

YDA179 has built-in volume fade-in/fade-out design for PD/Mute function. The relative PD timing diagrams for loudspeakers are shown below.



$$T_{fade} = \left| 10^{\frac{target(dB)}{20}} - 10^{\frac{original(dB)}{20}} \right| \times 128 \times (1/96kHz)$$

The volume level will be decreased to -∞dB over several LRCIN cycles. Once the fade-out procedure is finished, YDA179 will turn off the power stages, clock signals (for digital circuits) and current (for analog circuits). After PD pin is pulled low, YDA179 requires T_{fade} time to finish the forementioned work before entering power down state. Users can not program YDA179 during power down state. Also, all settings in the registers will remain intact unless DVDD is removed.

If the PD signal goes back to high in the middle of the fade-out procedure (above, right figure), YDA179 will execute the fade-in procedure. In addition, YDA179 will establish the analog circuits' bias current and send the clock signals to digital circuits. Afterwards, YDA179 resumes normal operation.

- Internal PLL ($\overline{PLL}$)

YDA179 has a built-in PLL with multiple MCLK/FS ratio, which is selected by I^2C control interface. If $\overline{PLL}$ pin is pulled low, the built-in PLL is enabled; when $\overline{PLL}$ pin is pulled high, an external clock source for MCLK less than 50MHz must be provided. The MCLK/FS ratio will be fixed at 1024x, 512x, or 256x with a sample frequency of 48kHz, 96kHz, or 192kHz respectively.

When using YDA179 without I2C control interface, the operation is as follows.

$\overline{PLL}$ pin is set to high:

Internal PLL is bypassed(Disable). The following master clock frequncy can be inputted into a MCK pin. A carrer clock frequency is the frequency divided by 128 of the following each inputted master clock.

*When the following master clock frequency cannot be inputted,/PLL is set low suggested.

Fs	MCLK frequency
48kHz	49.152MHz
44.1kHz	45.158MHz
32kHz	32.768MHz

$\overline{PLL}$ pin is set to low:

Internal PLL is enabled. The master clock inputted into the MCK pin becomes the frequency of quad edge evaluation. A carrier clock frequency is the frequency divided by 128 of the frequency of quad edge evaluation. (Divided by 32 of the frequency of master clock inputted into the MCK.)

- Anti-pop design

YDA179 will generate appropriate control signals to suppress pop sounds during initial power on/off, power down/up, mute, and volume level changes.

- Default volume (DEF)

The volume of YDA179 is +1.625dB when DEF pin is high, and the volume is muted when DEF pin low. When using YDA179 without I^2C control interface, user should set the pin high. The user can change the values of the register table setting for volume control. For detailed information, refer to the register table section.

- Self-protection circuits

YDA179 has built-in protection circuits including thermal, short-circuit and under-voltage detection circuits.

(i) When the internal junction temperature is higher than 160 °C, power stages will be turned off and YDA179 will return to normal operation once the temperature drops to 125 °C. The temperature values may vary around 10%.

(ii) The short-circuit protection circuit protects the output stage when the wires connected to loudspeakers are shorted to each other or GND/VDD. For normal 22V operations, the current flowing through the power stage will be less than 5A for stereo configuration. Otherwise, the short-circuit detectors may pull the $\overline{\text{ERROR}}$ pin to DGND, disabling the output stages. When the over-temperature or short-circuit condition occurs, the open-drain $\overline{\text{ERROR}}$ pin will be pulled low and latched into ERROR state. Once the over-temperature or short-circuit condition is removed, YDA179 will exit ERROR state when one of the following conditions is met: (1)$\overline{\text{RESET}}$ pin is pulled low, (2)$\overline{\text{PD}}$ pin is pulled low, (3) Master mute is enabled through the I^2C interface.

(iii) Once the DVDD voltage is lower than 2.7V, YDA179 will turn off its loudspeaker power stages and cease the operation of digital processing circuits. When DVDD becomes larger than 2.8V, YDA179 will return to normal operation.

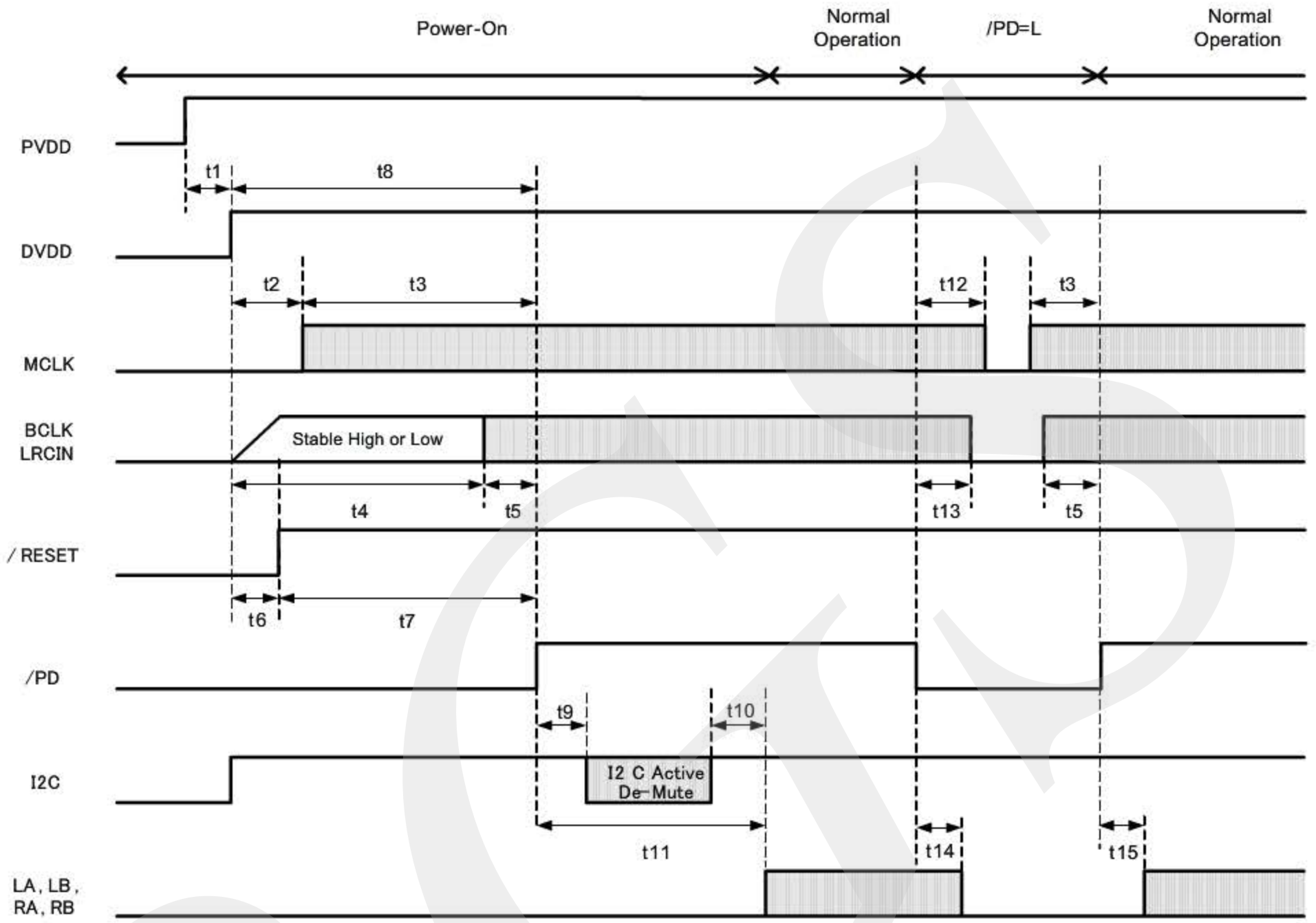
(iv) If the master clock inputted into MCLK pin stops during the period for 500 ns or more, YDA179 detect the stop of MCK. In this state, amplifier outputs are forced to Weak Low. If master clock is inputted normally again, $\overline{\text{ERROR}}$ pin is set to low. YDA179 won't leave ERROR state until one of the following conditions: (1)$\overline{\text{RESET}}$ pin is pulled low, (2)$\overline{\text{PD}}$ pin is pulled low, (3) Programming master mute via I^2C interface.

$\overline{\text{PD}}$ pin is set to low, when stop the clock inputted into MCLK, BCLK, and LRCIN during operation.

(v) If it will be in the state where PVDD power supply is OFF and DVDD power supply is ON, $\overline{\text{ERROR}}$ pin is set to Low.

● Power on sequence

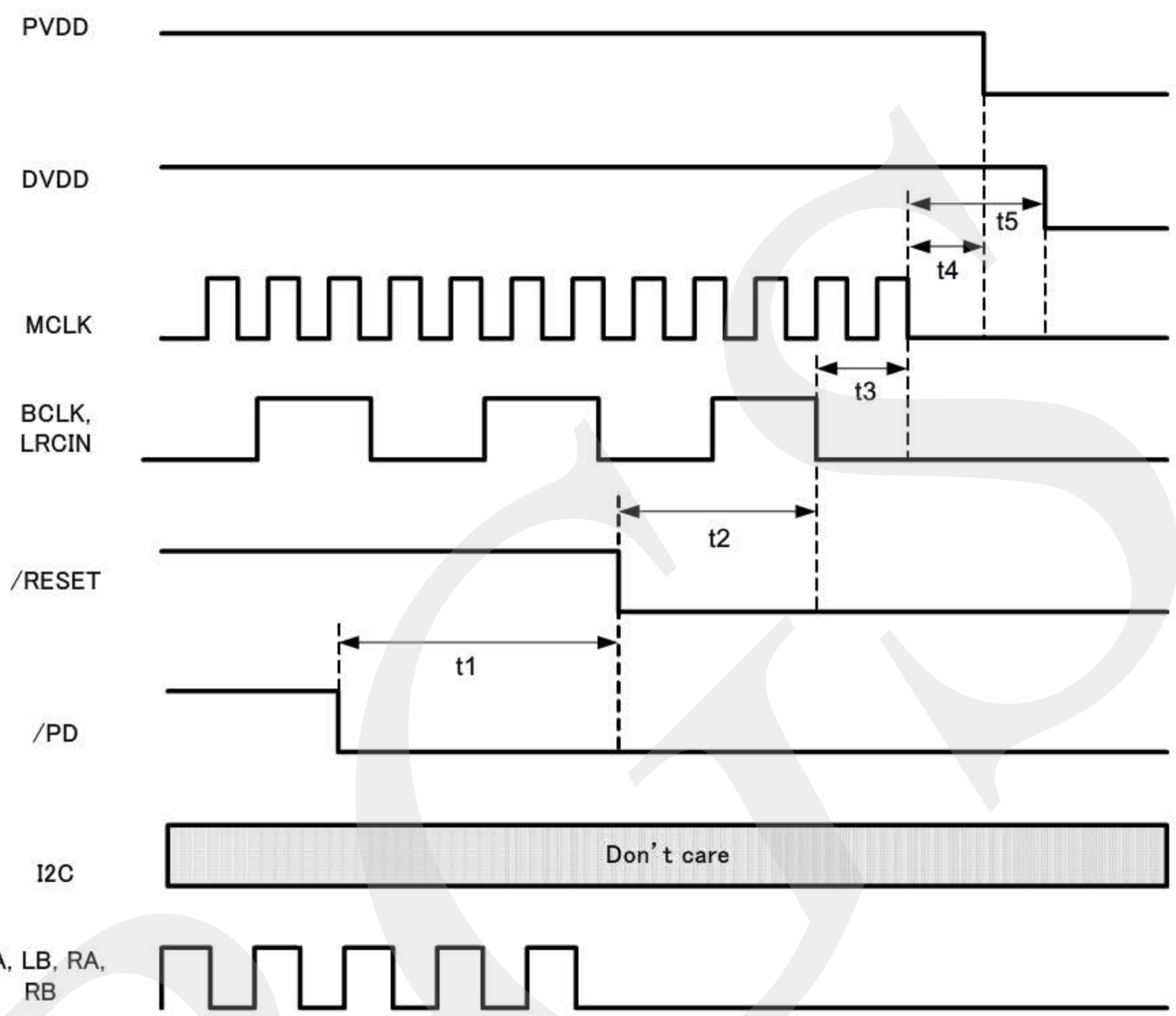
YDA179's power on sequence is shown below. Please note that we suggest users set DEF pin at low state initially, and then give a de-mute command via I^2C when the whole system is stable.



Symbol	Condition	Min	Max	Units
t1		0	-	msec
t2		0	-	msec
t3		10	-	msec
t4		0	-	msec
t5		10	-	msec
t6		3	-	msec
t7		0	-	msec
t8		200	-	msec
t9		20	-	msec
t10	DEF=L	-	0.1	msec
t11	DEF=H	-	0.1	msec
t12		25	-	msec
t13		25	-	msec
t14		-	22	msec
t15	DEF= L or H	-	0.1	msec

● Power off sequence

YDA179's power off sequence is shown below.



Symbol	Condition	Min	Max	Units
t1	With I^2C Control	35	-	msec
	Without I^2C Control	5	-	
t2		0 (*1)	-	msec
t3		0	-	msec
t4		1	-	msec
t5		1	-	msec

Note *1: When t2 is less than 0.1 msec, pop noise may occur.

13. I2C-Bus Transfer Protocol

- Introduction

  YDA179 employs I^2C-bus transfer protocol. Two wires, serial data and serial clock carry information between the devices connected to the bus. Each device is recognized by a unique 7-bit address and can operate as either a transmitter or a receiver. The master device initiates a data transfer and provides the serial clock on the bus. YDA179 is always an I^2C slave device.

- Protocol

  - START and STOP condition

    START is indicated by a high to low transition of the SDA signal. A START condition must precede any command for data transfer. A STOP is indicated by a low to high transition of the SDA signal. A STOP condition terminates communication between YDA179 and the master device on the bus. In both START and STOP, the SCL is stable in the high state.

  - Data validity

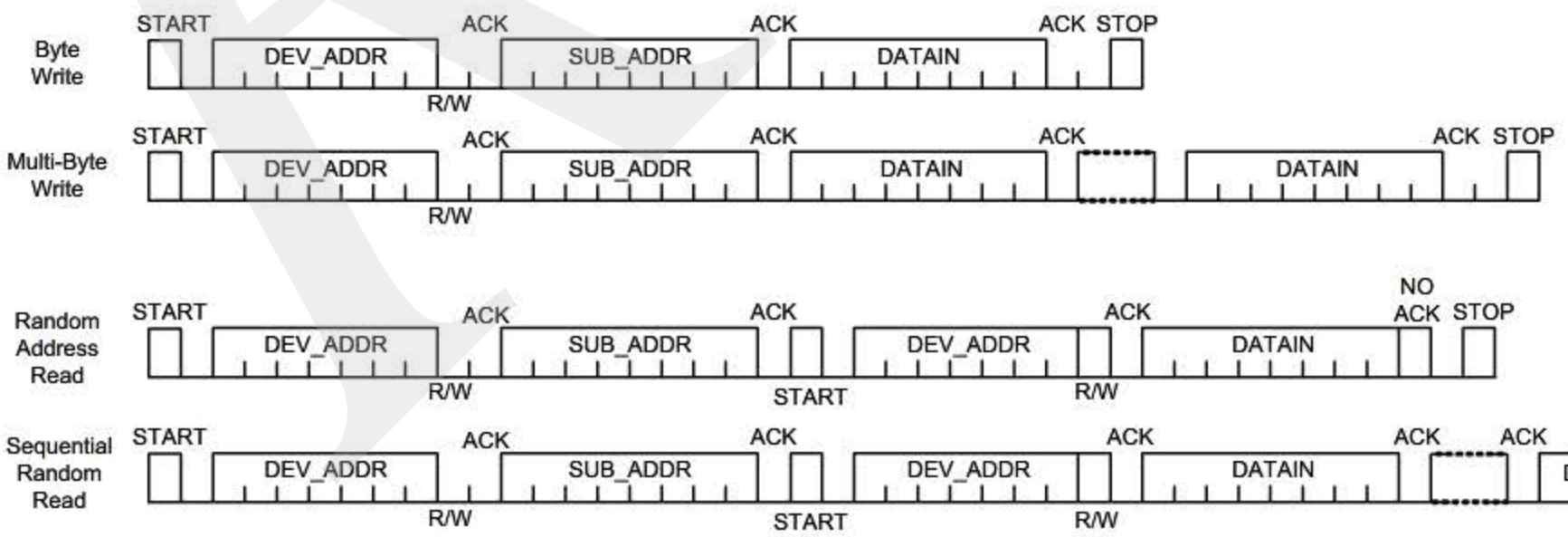
    The SDA signal must be stable during the high period of the clock. The high or low change of SDA only occurs when SCL signal is low. YDA179 samples the SDA signal at the rising edge of SCL signal.

  - Device addressing

    The master generates 7-bit address to recognize slave devices. When YDA179 receives 7-bit address matched with 0110x0y (where x and y can be selected by external SA0 and SA1 pins, respectively), YDA179 will acknowledge at the 9th bit (the 8th bit is for R/W bit). The bytes following the device identification address are for YDA179 internal sub-addresses.

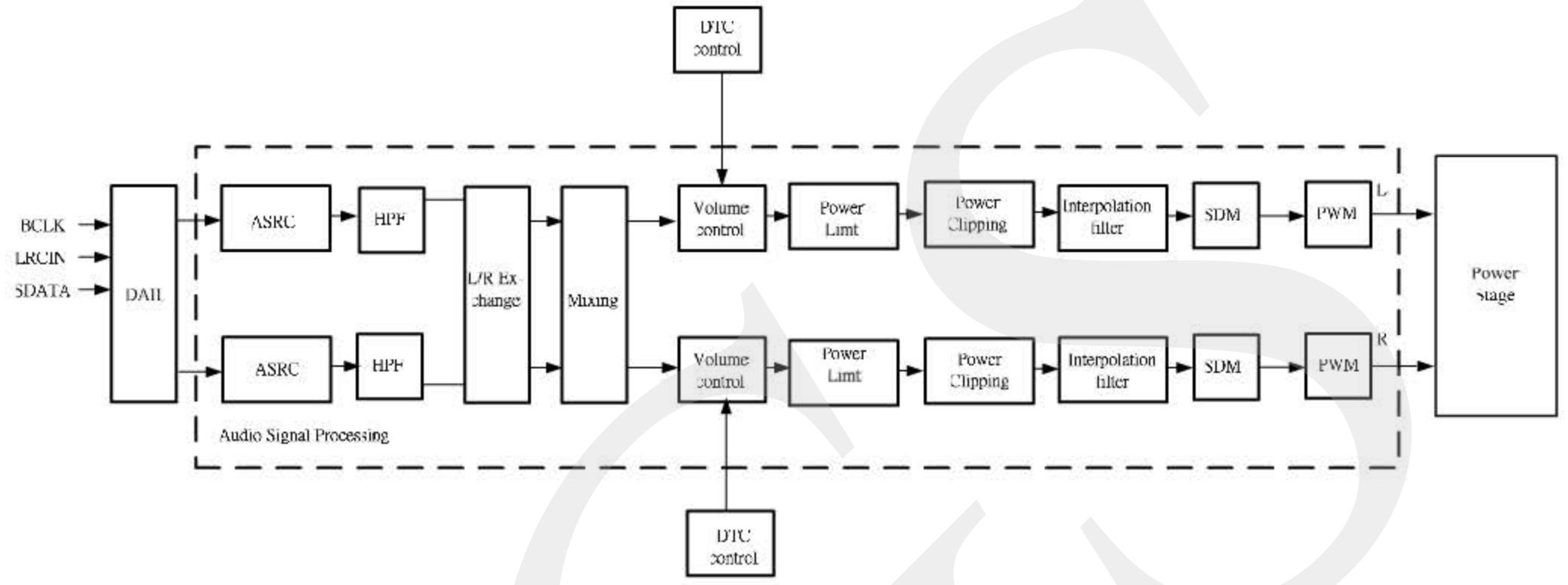
  - Data transferring

    Each byte of SDA signaling must consist of 8 consecutive bits, and the byte is followed by an acknowledge bit. Data is transferred with MSB first, as shown in the figure below. In both write and read operations, YDA179 supports both single-byte and multi-byte transfers. Refer to the figure below for detailed data-transferring protocol.



14. Register Table

The audio signal processing data flow is shown in figure below. Users can control these function by programming appropriate setting to register table. In this section, the register table is summarized first. The definition of each register follows in the next section.



Address	Register	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
0X00	SCTL1	IF[2]	IF[1]	IF[0]	LREXC	PWML_X	PWMRX	Reserved	NGE
0X01	SCTL 2	Reserved		FS[1]	FS[0]	PMF[3]	PMF[2]	PMF[1]	PMF[0]
0X02	SCTL 3	EN_CLKO	HPB	LV_UVSEL	SW_RSTB	MUTE	CM1	CM2	CompSDMEn
0X03	MVOL	MV[7]	MV[6]	MV[5]	MV[4]	MV[3]	MV[2]	MV[1]	MV[0]
0X04	C1VOL	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
0X05	C2VOL	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
0X06	HVUV	DIS_HVUV	Reserved			HVUVSEL[3]	HVUVSEL[2]	HVUVSEL[1]	HVUVSEL[0]
0X07	SCTL 4	Reserved		PC_EN	DRC_EN	Reserved			
0X08	LAR	LA[3]	LA[2]	LA[1]	LA[0]	LR[3]	LR[2]	LR[1]	LR[0]
0X09	X	Reserved							
0X0A	X	Reserved							
0X0B	OC SET	Reserved							
0X0C	STATUS	Reserved							
0X0D	ACFG	Reserved							
0X0E	TM_CTRL	Reserved							
0X0F	PWM_CTRL	Reserved							
0X10	ATT	Reserved			ATT[4]	ATT[3]	ATT[2]	ATT[1]	ATT[0]
0X11	ATM	ATM[7]	ATM[6]	ATM[5]	ATM[4]	ATM[3]	ATM[2]	ATM[1]	ATM[0]
0X12	ATB	ATB[7]	ATB[6]	ATB[5]	ATB [4]	ATB [3]	ATB [2]	ATB [1]	ATB [0]

0X13	PCT	Reserved			PCT[4]	PCT[3]	PCT[2]	PCT[1]	PCT[0]
0X14	PCM	PCM[7]	PCM[6]	PCM[5]	PCM[4]	PCM[3]	PCM[2]	PCM[1]	PCM[0]
0X15	PCB	PCB[7]	PCB[6]	PCB[5]	PCB [4]	PCB [3]	PCB [2]	PCB [1]	PCB [0]
0X16	NGG	Reserved			DIS_ZD _FADE	Reserved		NG_GAIN[1]	NG_GAIN[0]
0X17	VFT	MV_FT[1]	MV_FT[0]	C1V_FT[1]	C1V_FT[0]	C2V_FT[1]	C2V_FT[0]	Reserved	
0X18	DTC	DTC_EN	DTC_TH[1]	DTC_TH[0]	DTC_RATE[1]	DTC_RATE[0]	Reserved		
0X19		Reserved							
0X1A	NGALT	NGALT[7]	NGALT[6]	NGALT[5]	NGALT[4]	NGALT[3]	NGALT[2]	NGALT[1]	NGALT[0]
0X1B	NGALM	NGALM[7]	NGALM[6]	NGALM[5]	NGALM[4]	NGALM[3]	NGALM[2]	NGALM[1]	NGALM[0]
0X1C	NGALB	NGALB[7]	NGALB [6]	NGALB [5]	NGALB [4]	NGALB [3]	NGALB [2]	NGALB [1]	NGALB [0]
0X1D	NGRLT	NGRLT[7]	NGRLT[6]	NGRLT[5]	NGRLT[4]	NGRLT[3]	NGRLT[2]	NGRLT[1]	NGRLT[0]
0X1E	NGRLM	NGRLM[7]	NGRLM[6]	NGRLM[5]	NGRLM[4]	NGRLM[3]	NGRLM[2]	NGRLM[1]	NGRLM[0]
0X1F	NGRLB	NGRLB[7]	NGRLB [6]	NGRLB[5]	NGRLB[4]	NGRLB [3]	NGRLB [2]	NGRLB [1]	NGRLB [0]
0X20	DRC_ECT	DRC_ECT[7]	DRC_ECT[6]	DRC_ECT[5]	DRC_ECT[4]	DRC_ECT[3]	DRC_ECT[2]	DRC_ECT[1]	DRC_ECT[0]
0X21	DRC_ECB	DRC_ECB[7]	DRC_ECB[6]	DRC_ECB[5]	DRC_ECB[4]	DRC_ECB[3]	DRC_ECB[2]	DRC_ECB[1]	DRC_ECB[0]
0X22	RTT	Reserved			RTT[4]	RTT[3]	RTT[2]	RTT[1]	RTT[0]
0X23	RTM	RTM[7]	RTM[6]	RTM[5]	RTM[4]	RTM[3]	RTM[2]	RTM[1]	RTM[0]
0X24	RTB	RTB[7]	RTB[6]	RTB[5]	RTB [4]	RTB [3]	RTB [2]	RTB [1]	RTB [0]

15. Detail Description for Registers

In this section, please note that the value in the highlighted columns shows the default value for those registers. If no highlighted, it is because the default setting of this bit is determined with external pin strapping.

- Address 0X00 : State control 1

  YDA179 support multiple serial data input formats including I^2S, Left-alignment and Right-alignment. These formats is chosen by user via bit7~bit5 of address 0.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:5]	IF[2:0]	Input Format	000	I^2S 16-24 bits
			001	Left-alignment 16-24 bits
			010	Right-alignment 16 bits
			011	Right-alignment 18 bits
			100	Right-alignment 20 bits
			101	Right-alignment 24 bits
			other	Reversed
B[4]	LREXC	Left/Right (L/R) Channel exchanged	0	No exchanged
			1	L/R exchanged
B[3]	PWML_X	LA/LB exchange	0	No exchange
			1	Exchange
B[2]	PWMR_X	RA/RB exchange	0	No exchange
			1	Exchange
B[1]	X	Reserved		
B[0]	NGE	Noise gate enable	0	Disable
			1	Enable

● Address 0X01 : State control 2

YDA179 has built-in PLL which can be bypassed by pulling $\overline{PLL}$ line high. When PLL is enabled, multiple MCLK/FS ratio is supported. Table below details the setting.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:6]	X	Reserved		
B[5:4]	FS	Sampling Frequency	00	32/44.1/48kHz
			01	32/44.1/48kHz
			10	64/88.2/96kHz
			11	128/176.4/192kHz

Multiple MCLK/FS ratio setting table

BIT	NAME	DESCRIPTION	VALUE	B[5:4]=00/01	B[5:4]=10	B[5:4]=11
B[3:0]	PMF[3:0]	Multiple MCLK/FS ratio setting	0001	Reset Default (256x)	Reset Default (128x)	Reset Default (64x)
			0010	512x	256x	128x
			0011	768x	384x	192x
			0100	1024x	512x	256x

● Address 0X02 : State control 3

To prevent the DC current from damaging the speaker, a high pass filter (3dB frequency = 5Hz) is built into the YDA179. It can be enabled or disabled by bit 6 at address 2.

YDA179 has master mute as well as individual channel mute. When the master mute is enabled, both left and right processing channels are muted. Individual channels can be muted by using the channel mute. When the mute function is enabled or disabled, the fade-out or fade-in process will be initiated.

The default settings of B[3:1] are determined by DEF pin. When DEF pin is pulled low or high, the default setting is muted or unmated.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	EN_CLK_OUT	PLL Clock Output	0	Disabled
			1	Enabled
B[6]	HPB	DC blocking HPF bypass	0	Enable
			1	Disabled
B[5]	LV_UVSEL	LV under voltage selection	0	2.7V
			1	3.0V
B[4]	SW_RSTB	Software reset	0	Reset
			1	Normal operating
B[3]	MUTE	Master Mute	0	Un-Mute (DEF=1)
			1	Mute (DEF=0)
B[2]	CM1	Channel 1 Mute	0	Un-Mute (DEF=1)
			1	Mute (DEF=0)
B[1]	CM2	Channel 2 Mute	0	Un-Mute (DEF=1)
			1	Mute (DEF=0)
B[0]	CompSDMEn	Compensate SDM frequency response	0	Disable
			1	Enable

● Address 0X03 : Master volume

YDA179 supports both master-volume and channel-volume control for the stereo processing channels. Both master volume control (Address 0X03) and channel volume (Address 0X04 and 0X05) settings range from +12dB ~ -102dB. Given master volume level, say, Level A (in dB unit) and channel volume level, say Level B (in dB unit), the total volume equals to Level A plus with Level B and its range is from +24dB ~ -102dB, i.e., -103dB ≦ Total Volume (Level A + Level B) ≦ +24dB.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	MV[7:0]	Master Volume	00000000	+12dB
			00000001	+11.5dB
			00000010	+11dB
			:	:
			00010111	0.5dB
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			1111111	-∞dB

● Address 0X04 : Channel1 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C1V[7:0]	Channel 1 Volume	00000000	+12dB
			00000001	+11.5dB
			:	:
			00010100	2dB
			:	:
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			1111111	-∞dB

● Address 0X05 : Channel2 volume

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7:0]	C2V[7:0]	Channel 2 Volume	00000000	+12dB
			00000001	+11.5dB
			:	:
			00010100	2dB
			:	:
			00011000	0dB
			00011001	-0.5dB
			:	:
			11100110	-103dB
			11100101	-∞dB
			:	:
			1111111	-∞dB

● Address 0X06 : Under voltage threshold for high voltage supply

YDA179 provides HV under voltage detection which can be enable or disable via bit 7. The under-voltage detection level is programmable via bit3~ bit0. Once the output stage voltage drops below the preset value (see table), YDA179 will fade out audio signals to turn off the speaker.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	Dis_HVUV	Disable HV under voltage circuit	0	Enable
			1	Disable
B[6:4]	X	Reserved		
B[3:0]	HVUVSEL[3:0]	HV Under Voltage selection (Active)	Other	9.7V
			1100	19.5V
			0100	15.5V
			0011	13.2V
			0001	9.7V
			0000	8.2V

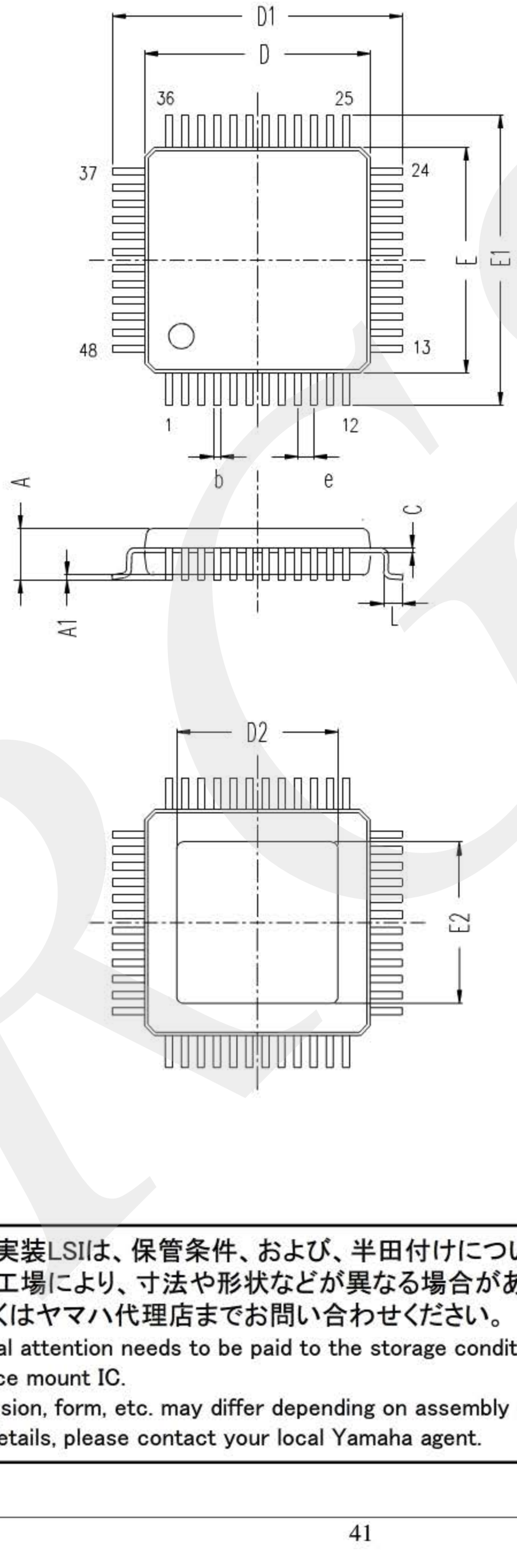
● Address 0X07 : State control 4

YDA179 provides channel mix, power clipping, and dynamic range control (DRC) function. These functions can be enable or not as the following table.

BIT	NAME	DESCRIPTION	VALUE	FUNCTION
B[7]	X	Reserved		
B[6]	X	Reserved		
B[5]	PC_EN	Power Clipping enable	0	Disable
			1	Enable
B[4]	DRC_EN	DRC enable	0	Disable
			1	Enable
B[3:0]	X	Reserved		

16. Package Dimensions

U-PK48SP2-S9-1



Symbol	Dimension in mm	
	Min	Max
A	--	1.60
A1	0.05	0.15
b	0.17	0.27
c	0.09	0.20
D	6.90	7.10
D1	8.90	9.10
E	6.90	7.10
E1	8.90	9.10
e	0.50BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	4.31	5.21
E2	4.31	5.21

注）　1. 表面実装LSIは、保管条件、および、半田付けについての特別な配慮が必要です。
　　2. 組立工場により、寸法や形状などが異なる場合があります。
　　詳しくはヤマハ代理店までお問い合わせください。

Note:　1. Special attention needs to be paid to the storage conditions and soldering method of the surface mount IC.
　　2. Dimension, form, etc. may differ depending on assembly plants.
　　For details, please contact your local Yamaha agent.

YAMAHA

CREATING 'KANDO' TOGETHER

NOTICE

The information provided is preliminary, and subject to change without notice.
Please check for the latest information when using this product in your design.

AGENT

YAMAHA CORPORATION

Address Inquiries to :
Semiconductor Sales & Marketing Department

■Head Office 203, Matsunokijima, Iwata,
Shizuoka, 438-0192, Japan
Tel. +81-539-62-4918 Fax.+81-539-62-5054

■Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8586, Japan
Tel. +81-3-5488-5431 Fax.+81-3-5488-5088

■Osaka Office Universal City Wako Bldg.
6-2-82, Shimaya, Konohana-ku,
Osaka, 554-0024, Japan
Tel. +81-6-6465-0325 Fax.+81-6-6465-0391

Printed in Japan
eM02