# WT8871S-C/8871S-E

## Video Display Controller for Analog Small Size LCD Display System

## Data Sheet

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# 1. General Description

The WT8871S-C/WT8871S-E is a highly integrated video display controller for small size LCD display application, such as portable DVD player and car TV application. It has built-in video decoder, scaler, de-interlacer, TCON, 8-bit MCU, OSD, PWM and DC-to-DC converter functions. WT8871S-C/WT8871S-E has triple DAC and VCOM output for analog LCD panel application.

## 1.1. Features

- Video input port
  - 6 analog inputs
  - Support CVBS and S-video input
  - Support RGB input for GPS module and component input
  - Digital input: 8-bit 4:2:2 ITU-BT.656 or BT.601 interface
  - Support 720x480i and 720x516i input resolution
- LCD panel interface
  - Triple 8-bit DACs output RGB signals for analog panel
  - Programmable timing controller for different type of panels
  - Programmable gamma table for panel compensation
- 2D video decoder
  - 10-bit ADC
  - Supports CVBS, S-video and RGB input
  - Decodes NTSC (M, Japan, 4.43), PAL (B ,G ,D ,H ,I ,Nc), and SECAM
  - Multi-standard adaptive 2D comb filter
  - Safe Hsync, Vsync and field signal outputs when VCR trick mode
  - Auto detection and decodes Macrovision copy protection
  - Chroma Transient Improvement (CTI)
  - Luma Transient Improvement (LTI), edge/sharpness improvement
  - Luma Coring noise reduction
- Display format conversion
  - Programmable horizontal and vertical zoom ratio
  - Support non-linear scaling for 4:3 to 16:9
  - Convert interlaced input to progressive
- Luminance and chrominance adjustment
  - Contrast adjustment with black/white level stretch
  - Brightness adjustment
  - Sharpness adjustment
  - Hue adjustment
  - Saturation adjustment
- OSD
  - Character based OSD
  - Font size: 12x18 dots
  - Font ROM: 512 single color fonts
  - Display RAM : display up to 512 characters
  - User-font RAM : up to 142 single color fonts
  - Support 2-bit multi-color font
  - Shadow and border effect of character
  - Two display windows
  - Programmable background window
  - Support alpha blending

  - Support blinking effect
  - Support fade in/out effect

- Support external OSD interface
- MCU
  - Built-in 8051 CPU
  - Data memory: 512 bytes RAM
  - Support external program memory with serial flash memory via 4-wire interface
  - Internal MCU can be disable by pin mode0 and mode1
- 8-bit ADC for keypad scanning and others
- Two slave mode $I^2C$ interfaces, up to 400KHz
  - Interface for ISP, ICE and other $I^2C$ master
- 2 Standard UART ports support.
- Support Infra-Red remote control
- Four PWM outputs including one low frequency PWM and one 10-bit PWM
- Built-in self test pattern generator
- Two DC-DC boost circuits for VGH/VGL and LED backlight
- General purpose I/Os
- Spread spectrum PLL for panel clock, lower EMI
- Crystal oscillator
  - 24MHz
- Package type:
  - 128-pin LQFP, 14mm(L) x 14mm(W) x 1.4mm(H)
  - Green package available

## 1.2. Application

- Portable DVD Player
- Car information, entertainment system
- Portable DTV
- Digital photo frame

## 1.3.Selection Guide

| | |
|---|---|
| WT8871S-C (0℃~70℃) | Commercial Use |
| WT8871S-E (-20℃~80℃) | Extending temp. range |

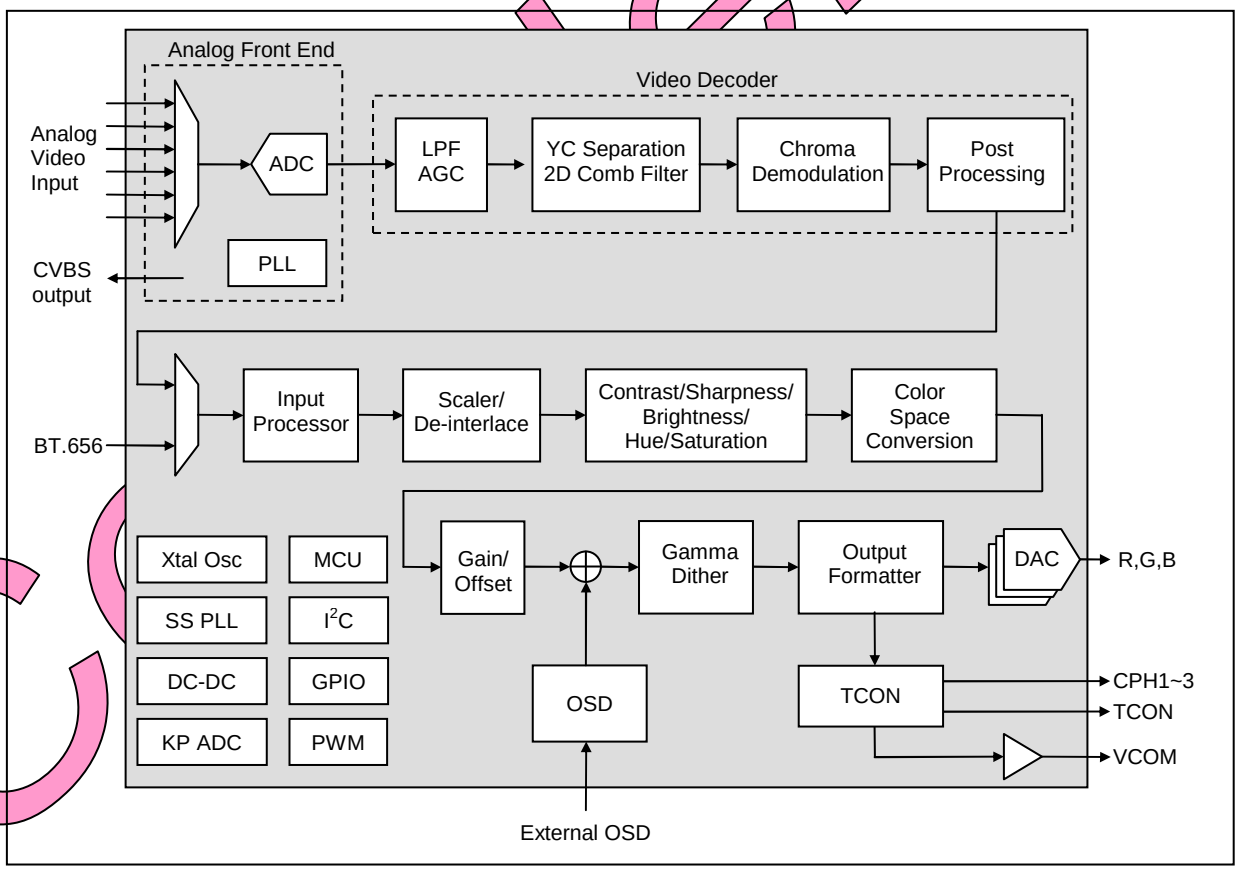
WT8871S-C 印碼:

Weltrend
WT8871S□□□01X
XXXXX C●

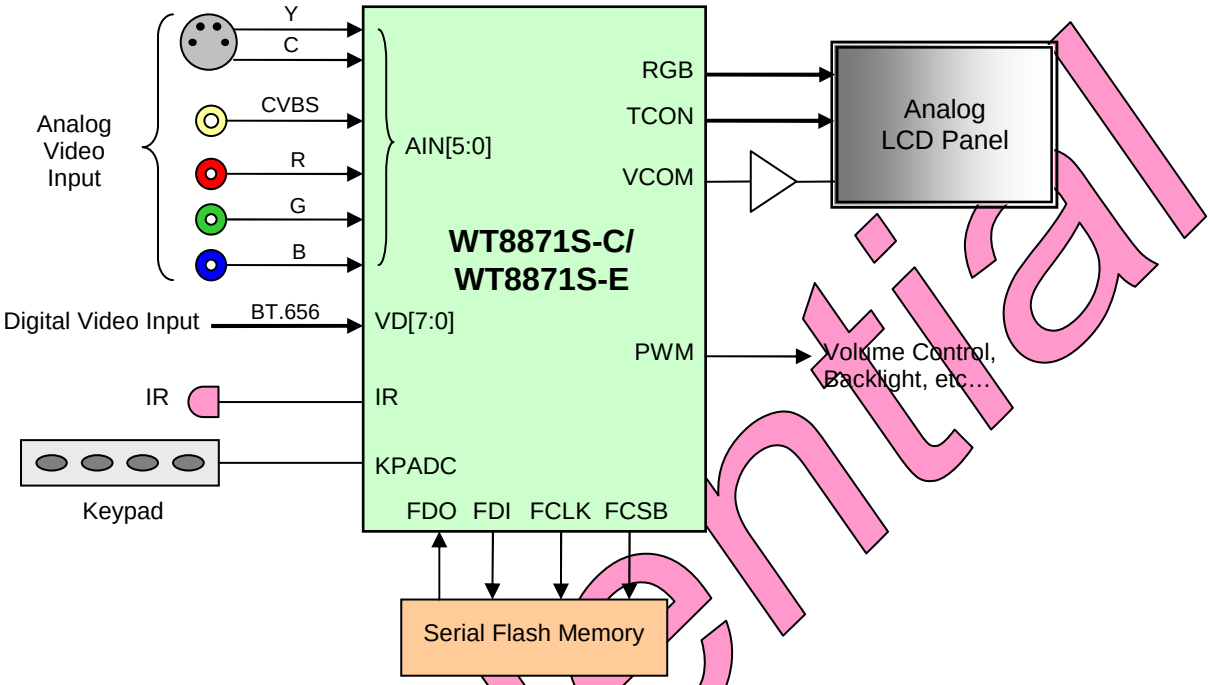
WT8871S-E 印碼:

Weltrend
WT8871S□□□01X
XXXXX ●

## 1.4. Block Diagram



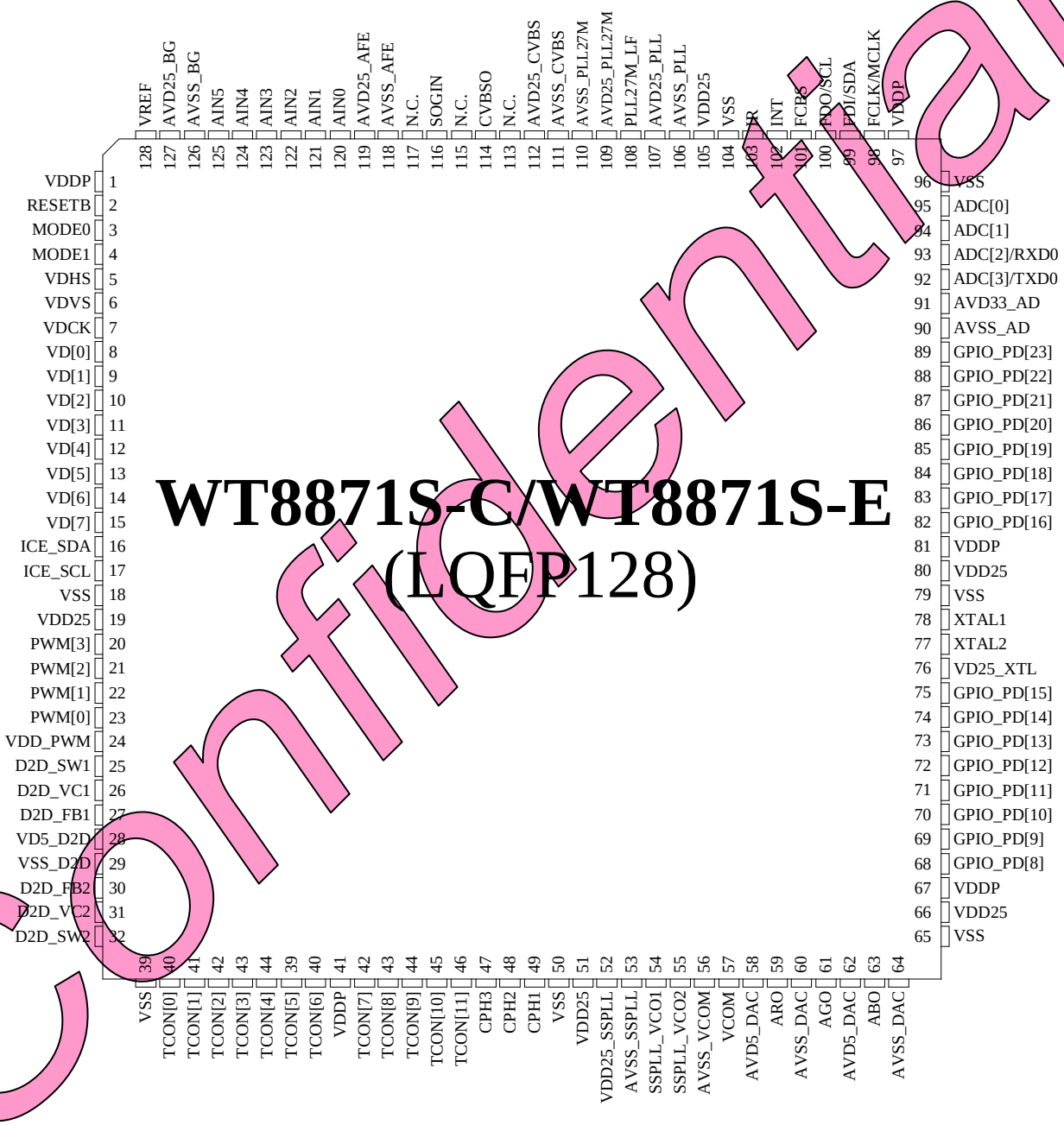
## 1.5. Application Example



# 2. Package Type and Pin Description

## 2.1. Pin Configuration

LQFP 128-pin (body size : 14mm x 14mm x 1.4mm)



## 2.2 Pin Description

| WT8871S-C/ WT8871S-E | Pad Name | I/O | Pull up/down | Description |
|---|---|---|---|---|
| 1 | VDDP | | | 3.3V Power. |
| 2 | RESETB | I | pull-up | Reset pin. Active low. |
| 3 | MODE0 | I | pull-down | Operating mode selection. |
| 4 | MODE1 | I | pull-down | 00 : Internal MCU mode using external flash<br>01 : Reserved<br>10 : External MCU mode<br>11 : Reserved |
| 5 | VDHS/OSDHS | I/O | pull-down | BT.601 Hsync I/O or Hsync output for external OSD. Shared with GPIO. |
| 6 | VDVS/OSDVS | I/O | pull-down | BT.601 Vsync I/O or Vsync output for external OSD. Shared with GPIO. |
| 7 | VDCK/OSDCK | I/O | pull-down | BT.656/601 clock I/O or clock output for external OSD. Shared with GPIO. |
| 8 | VD[0]/OSDBIN | I/O | pull-down | BT.656 /601video data I/O or external OSD blue input. Shared with GPIO. |
| 9 | VD[1]/OSDGIN | I/O | pull-down | BT.656/601 video data I/O or external OSD green input. Shared with GPIO. |
| 10 | VD[2]/OSDRIN | I/O | pull-down | BT.656/601 video data I/O or external OSD red input. Shared with GPIO. |
| 11 | VD[3]/OSDINT | I/O | pull-down | BT.656/601 video data I/O or external OSD intensity input. Shared with GPIO. |
| 12 | VD[4]/OSDFB | I/O | pull-down | BT.656 /601video data I/O or external OSD fast blanking input. Shared with GPIO. |
| 13 | VD[5] | I/O | pull-down | BT.656/601 video data I/O. Shared with GPIO. |
| 14 | VD[6] | I/O | pull-down | BT.656/601 video data I/O. Shared with GPIO. |
| 15 | VD[7] | I/O | pull-down | BT.656/601 video data I/O. Shared with GPIO. |
| 16 | ICE_SDA | I/O | pull-up | $I^2C$ data pin. |
| 17 | ICE_SCL | I/O | pull-up | $I^2C$ clock pin. |
| 18 | VSS | | | Ground. |
| 19 | VDDC | | | 2.5V Power. |
| 20 | PWM[3] | I/O | pull-up | PWM output or 8051 P1[3]. Shared with GPIO. |
| 21 | PWM[2] | I/O | pull-up | PWM output or 8051 P1[2]. Shared with GPIO. |
| 22 | PWM[1] | I/O | pull-up | PWM output. Shared with GPIO. |
| 23 | PWM[0] | I/O | pull-up | PWM output. Shared with GPIO. |
| 24 | VDDP_PWM | | | 3.3V or 5V Power. |
| 25 | D2D_SW1 | O | | DC-DC1 switching pulse. |
| 26 | D2D_VC1 | I/O | | DC-DC1 voltage control pin. Shared with GPIO. |
| 27 | D2D_FB1 | I/O | | DC-DC1 feedback pin. Shared with GPIO. |
| 28 | VD5_D2D | | | 3.3 or 5V Power for DC-to-DC. |
| 29 | VSS_D2D | | | Ground for DC-to-DC. |
| 30 | D2D_FB2 | I/O | | DC-DC2 feedback pin. Shared with GPIO. |
| 31 | D2D_VC2 | I/O | | DC-DC2 voltage control pin. Shared with GPIO. |
| 32 | D2D_SW2 | O | | DC-DC2 switching pulse. |
| 33 | VSSP | | | Ground. |
| 34 | TCON[0] | I/O | pull-down | TCON output or external OSD blue input or UART RXD1. Shared with GPIO. |
| 35 | TCON[1] | I/O | pull-down | TCON output or external OSD green input or UART TXD1. Shared with GPIO. |
| 36 | TCON[2] | I/O | pull-down | TCON output or external OSD red input. Shared with GPIO. |
| 37 | TCON[3] | I/O | pull-down | TCON output or external OSD intensity input. Shared with GPIO. |

| | | | | |
|---|---|---|---|---|
| 38 | TCON[4] | I/O | pull-down | TCON output or external OSD fast blanking input.<br>Shared with GPIO. |
| 39 | TCON[5] | I/O | pull-down | TCON output or Vsync output for external OSD.<br>Shared with GPIO. |
| 40 | TCON[6] | I/O | pull-down | TCON output or Hsync output for external OSD.<br>Shared with GPIO. |
| 41 | VDDP | | | 3.3V power for PAD |
| 42 | TCON[7] | I/O | pull-down | TCON output or clock output for external OSD.<br>Shared with GPIO. |
| 43 | TCON[8] | I/O | pull-down | TCON output. Shared with GPIO. |
| 44 | TCON[9] | I/O | pull-down | TCON output. Shared with GPIO. |
| 45 | TCON[10] | I/O | pull-down | TCON output. Shared with GPIO. |
| 46 | TCON[11] | I/O | pull-down | TCON output or panel data enable. Shared with GPIO. |
| 47 | CPH3 | I/O | pull-down | TCON clock 1 or panel hsync. Shared with GPIO. |
| 48 | CPH2 | I/O | pull-down | TCON clock 2 or panel vsync. Shared with GPIO. |
| 49 | CPH1 | I/O | pull-down | TCON clock 3 or panel clock. Shared with GPIO. |
| 50 | VSSP | | | Ground. |
| 51 | VDD25 | | | 2.5V Power. |
| 52 | AVD25_SSPLL | | | 2.5V Power. |
| 53 | AVSS_SSPLL | | | Ground. |
| 54 | SSPLL_VCO1 | | | Loop filter 1 of spectrum PLL. |
| 55 | SSPLL_VCO2 | | | Loop filter 2 of spectrum PLL. |
| 56 | AVSS_VOCM | | | Ground. |
| 57 | VCOM | AO | | VCOM Output. |
| 58 | AVD5_DAC | | | 5V power. |
| 59 | ARO | AO | | Analog Red signal output |
| 60 | AVSS_DAC | | | Ground for DAC |
| 61 | AGO | AO | | Analog Green Output |
| 62 | AVD5_DAC | | | 5V power for DAC |
| 63 | ABO | AO | | Analog Output |
| 64 | AVSS_DAC | | | Ground. |
| 65 | VSS | | | Ground. |
| 66 | VDDC | | | 2.5V Power. |
| 67 | VDDP | | | 3.3V Power. |
| 68 | GPIO_PD[8] | I/O | pull-down | GPIO. |
| 69 | GPIO_PD[9] | I/O | pull-down | GPIO. |
| 70 | GPIO_PD[10] | I/O | pull-down | GPIO. |
| 71 | GPIO_PD[11] | I/O | pull-down | GPIO. |
| 72 | GPIO_PD[12] | I/O | pull-down | GPIO. |
| 73 | GPIO_PD[13] | I/O | pull-down | GPIO. |
| 74 | GPIO_PD[14] | I/O | pull-down | GPIO. |
| 75 | GPIO_PD[15] | I/O | pull-down | GPIO. |
| 76 | VD25_XTL | | | 2.5V Power. |
| 77 | XTAL2 | O | | Crystal oscillator output. |
| 78 | XTAL1 | I | | Crystal oscillator input. |
| 79 | VSS | | | Ground |
| 80 | VDDC | | | 2.5V Power. |
| 81 | VDDP | | | 3.3V Power. |
| 82 | GPIO_PD[16] | I/O | pull-down | GPIO. |
| 83 | GPIO_PD[17] | I/O | pull-down | GPIO. |
| 84 | GPIO_PD[18] | I/O | pull-down | GPIO. |
| 85 | GPIO_PD[19] | I/O | pull-down | GPIO. |
| 86 | GPIO_PD[20] | I/O | pull-down | GPIO. |
| 87 | GPIO_PD[21] | I/O | pull-down | GPIO. |

| | | | | |
|---|---|---|---|---|
| 88 | GPIO_PD[22] | I/O | pull-down | GPIO. |
| 89 | GPIO_PD[23] | I/O | pull-down | GPIO. |
| 90 | AVSS_KP | | | Ground. |
| 91 | AVDD_KP | | | 3.3V power. |
| 92 | KPADC[3]/TXD | I/O | pull-up | Keypad ADC input or UART TXD0. Shared with GPIO. |
| 93 | KPADC[2]/RXD | I/O | pull-up | Keypad ADC input or UART RXD0. Shared with GPIO. |
| 94 | KPADC[1] | I/O | pull-up | Keypad ADC input or 8051 P1[1]. Shared with GPIO. |
| 95 | KPADC[0] | I/O | pull-up | Keypad ADC input or 8051 P1[0]. Shared with GPIO. |
| 96 | VSS | | | Ground. |
| 97 | VDDP | | | 3.3V Power. |
| 98 | FCLK | I/O | pull-up | Connects to serial flash clock. Shared with GPIO. |
| 99 | FDI | I/O | pull-up | Connects to serial flash data output. Shared with GPIO. |
| 100 | FDO | I/O | pull-up | Connects to serial flash data input. Shared with GPIO. |
| 101 | FCSB | I/O | pull-up | Connects to serial flash chip select. Shared with GPIO. |
| 102 | INTB | I/O | pull-up | Interrupt input. Shared with GPIO. |
| 103 | IR | I/O | pull-up | IR input. Shared with GPIO. |
| 104 | VSS | | | Ground |
| 105 | VDDC | | | 2.5V Power. |
| 106 | AVSS_PLL | | | Analog power for analog front end PLL. |
| 107 | AVD25_PLL | | | Analog power for analog front end PLL, |
| 108 | PLL27M_LF | | | Loop filter for 27MHz PLL. |
| 109 | AVD25_27M | | | 2.5V power.. |
| 110 | AVSS_27M | | | Ground. |
| 111 | AVSS_CVBS | | | Ground. |
| 112 | AVD25_CVBS | | | 2.5V power. |
| 113 | NC | | | No connect. |
| 114 | CVBSBO | AO | | CVBS buffer output |
| 115 | NC | | | No connect. |
| 116 | SOGI | | | SOG input. Composite sync input. |
| 117 | NC | | | No connect. |
| 118 | AVSS_AFE | | | Ground. |
| 119 | AVDD_AFE | | | 2.5V power. |
| 120 | AIN[0] | AI | | analog video input. |
| 121 | AIN[1] | AI | | analog video input. |
| 122 | AIN[2] | AI | | analog video input. |
| 123 | AIN[3] | AI | | analog video input. |
| 124 | AIN[4] | AI | | analog video input. |
| 125 | AIN[5] | AI | | analog video input. |
| 126 | AVSS_BG | | | Ground. |
| 127 | AVDD_BG | | | 2.5V power. |
| 128 | AVREF | AO | | Reference voltage of analog front end. |

# 3. Function Description

## 3.1. MCU

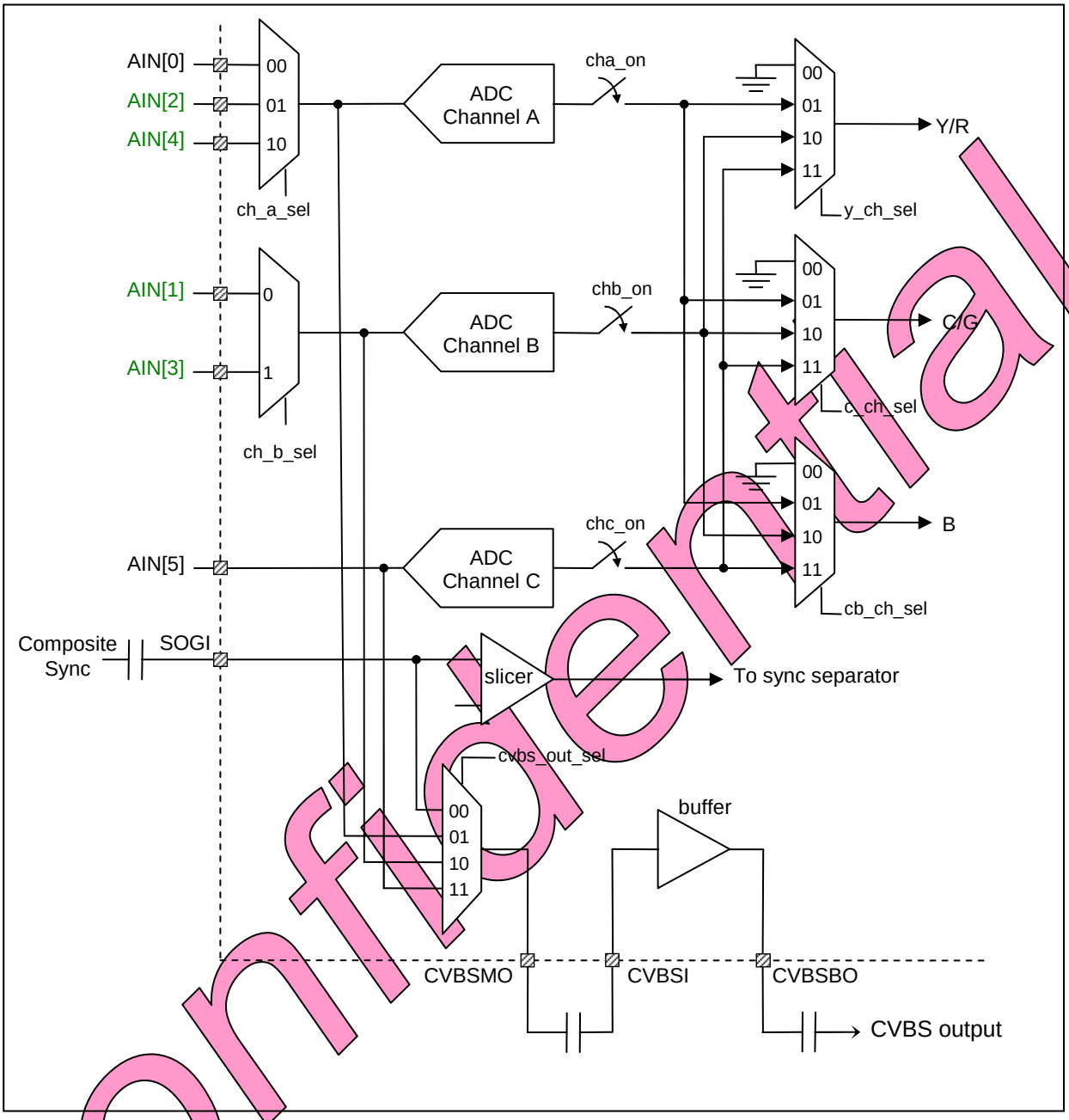
MCU is an 8-bit micro-controller compatible with 8051. It has 512 bytes data memory, 256 bytes internal RAM and 256 bytes external RAM(0x7600h~0x76FFh). Clock of MCU is from crystal oscillator. MCU controls the chip and execute program stored in external flash memory. ICE and ISP functions can be activated through $I^2C$ interface (pin 16 and 17)

## 3.2. Video Decoder

WT8871S-C/WT8871S-E has built in a high quality digital 2D video decoder with the capability of decoding NTSC/PAL/SECAM video signal and converts to YUV 4:2:2 digital video. Employing adaptive digital comb filter technology, this video decoder is able to provide the highest quality Y/C separation while maintaining excellent frequency response. Color transient enhancement provides for fast transition on color boundaries. The result is sharp, highly detailed video that dot crawl and false color effect are eliminated.

### 3.2.1. Video Input Crossbar

There are 3 ADC channels inside WT8871S-C/WT8871S-E, they sample CVBS, S-video or R/G/B analog input signals for application flexibility. Total 6 analog inputs are provided. Each one could be assigned as CVBS input, S-video or can be assigned as combination of both or RGB input.






### 3.2.2. CVBS output

It outputs CVBS signal through an uni-gain buffer. An external buffer is required if it drives 75 Ω load.

### 3.2.3. SOG Input

Composite sync (H+V) can be input from SOGI pin when interface with GPS module. Sync separator in video decoder will extract H and V timing. An AC coupling capacitor is needed when using this input.

### 3.2.4. Adaptive Comb Filter

The Y/C Separation method can be chosen form luma-bandpass, different comb filter. It is set by the adaptive mode register. The shortage of luma-bandpass filter method is dots be seen in the vertical transition pattern, comb filter in the horizontal direction. The full adaptive comb (2D adaptive comb) option can overcome the two shortages

### 3.2.5. Chroma Peaking

Peaking is an action in frequency domain which enhances the selective frequency band with certain amount of gain (> 0 dB), reflects in time domain it improves the edge transient performance.

Chroma peaking sometimes is called “Chroma Transient Improvement (CTI)” by some TV manufacturers, it enhances chroma transient performance.

The register “chroma_peak_en”, can enable the chroma edge enhancement circuit. If the register bit “chroma_coring_en” is set which will enable the “coring circuit” to function, “coring circuit” set certain threshold level (1 LSB or higher), if peaked chroma signal is below that threshold, the output is stretched to zero. “Coring” function basically does some noise reduction for the unwanted high frequency part which was introduced during “Chroma Peaking” phase.

The register, chroma_peak value determines the peak gain for this circuit, the larger the value, the sharper the chroma edge.

### 3.2.6. Luma peaking

Luma Peaking is sometimes called “Luma Transient Improvement (LTI)”, or “sharpness enhancement” in some technical textbook. Luma peaking is set by the “peak_gain” and “peak_range” registers. The method is to enlarge the high frequency part of the Y signal, thus the sharpness of picture details can be enhanced.

### 3.2.7. Luma enhancement

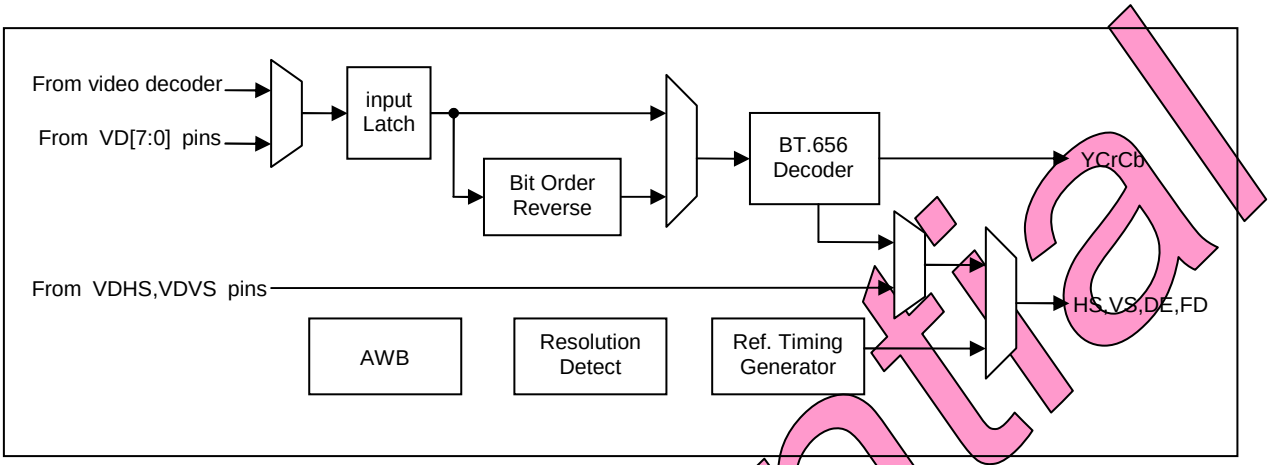
The Luma edge enhancement is set by the edge_enhance_gain and edge_enhance_range registers. The method is to enlarge the high frequency part of the Y signal at 13.5MHz data rate domain.

### 3.2.8. Auto Mode Detection

WT8871S-C/WT8871S-E can detect and set all the default settings for different TV standard such as NTSC-M/Japan, NTSC-443, PAL-B/D/G/H/I, PAL-NC, PAL-60 and SECAM. This mechanism could be enable/disabled by the register, auto_detection_en.

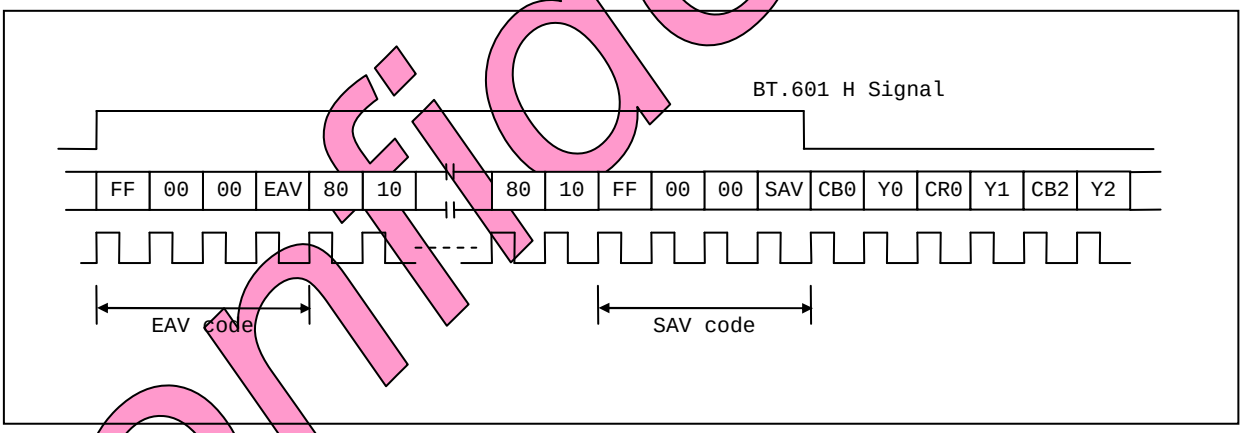
## 3.3. Input Processor

Input processor contains ITU-BT.656 interface, input timing/resolution detection, active video region detection, reference timing generation and auto white balance functions.




### 3.3.1. ITU-BT.656 Interface

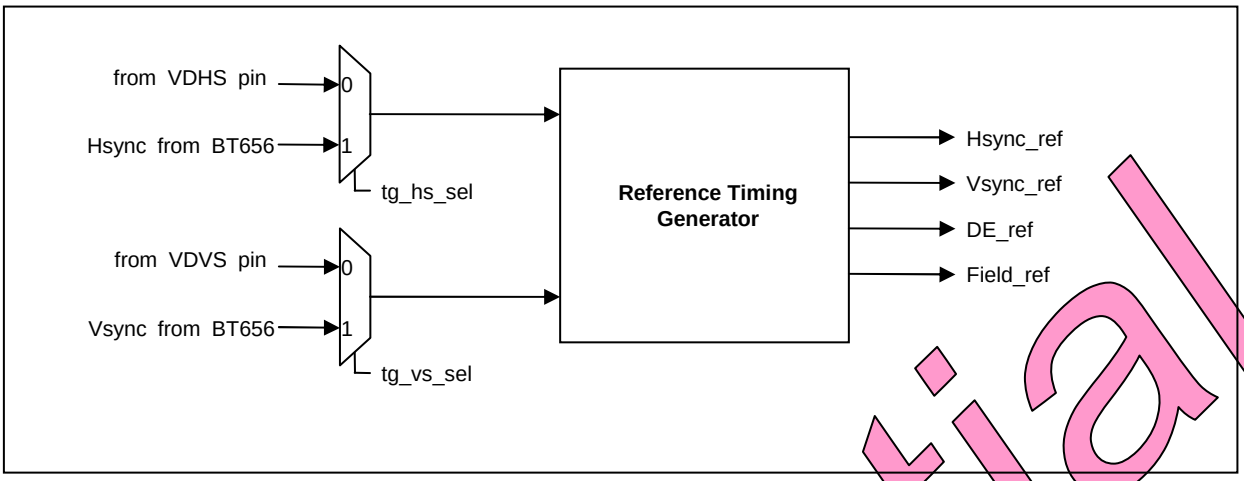
Standard 8-bit BT.656 or BT.601 signal is input from this interface. Hsync and Vsync are decoded from EVA and SAV code or from input pins.




This interface can be programmed to output video decoder data when it is not used for input.

### 3.3.2. Reference Timing Generation

It generates Hsync, Vsync, DE and field signals for video processing. In free running mode, it generates timing for test pattern generation.

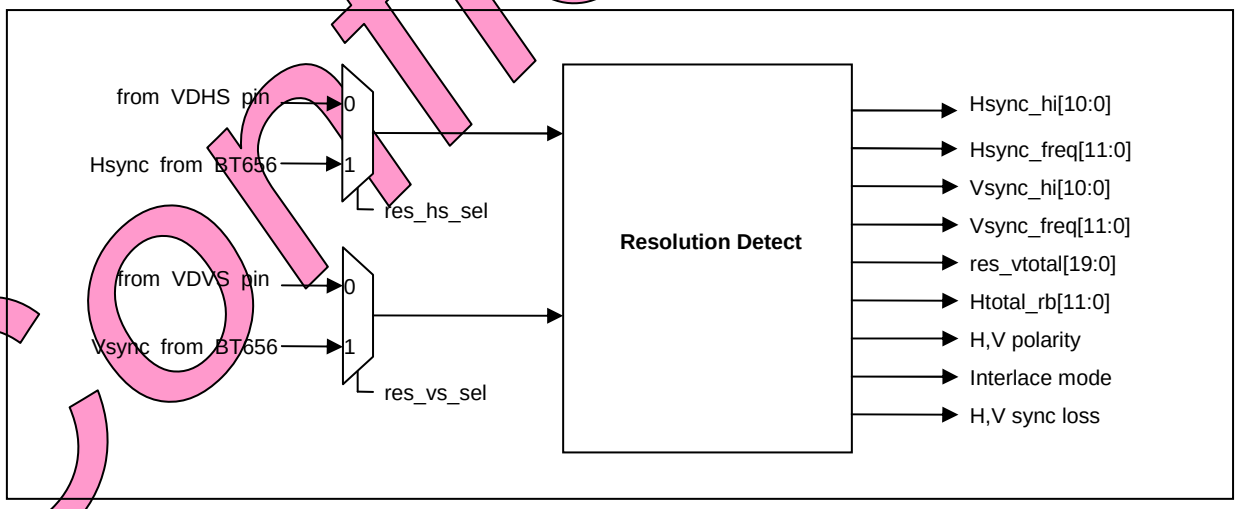



### 3.3.3. Resolution Detect

It measures input H/V timing and resolution, including

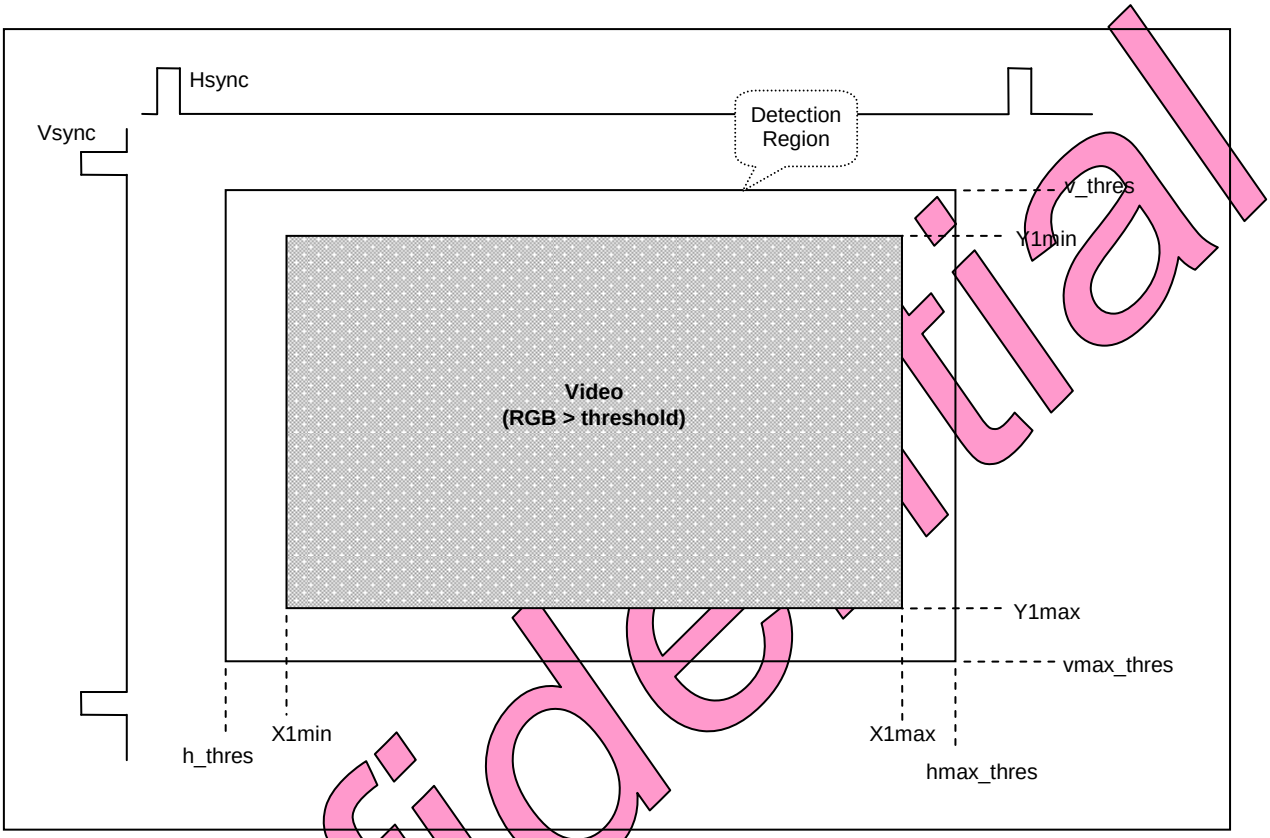
- Hsync pulse width and period, unit = system clock.
- Vsync pulse width and period, unit = line.
- Hsync pixel number, unit = input clock
- Vsync period, unit = system clock
- Hsync and Vsync polarity
- Odd or even frame
- Interlace or non-interlace

Input H/V timing is also monitored and will generate an interrupt when the frequency change is larger than preset range.



### 3.3.4. Active Video Region Detect

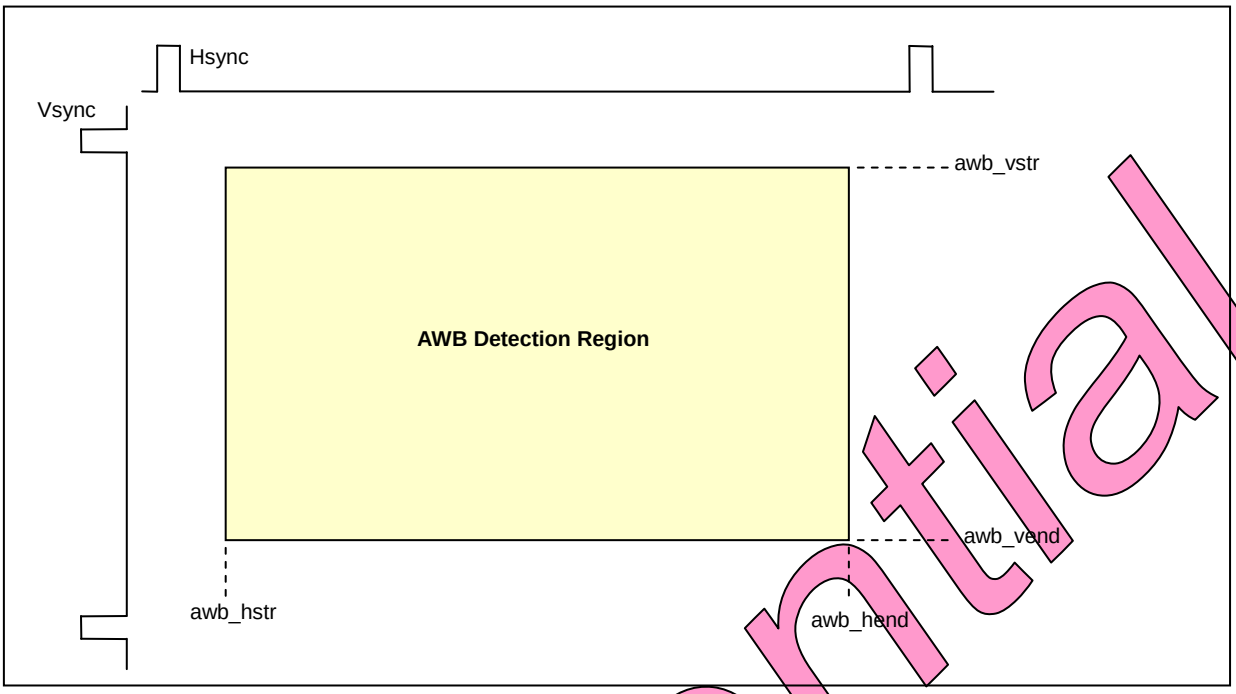
It detects active video boundary in an user-defined region. If the input signal amplitude is greater than the threshold, if will record the position and report the boundary.




### 3.3.5. Auto White Balance

Auto White Balance function records the maximum or minimum RGB value (from ADC) of the selected display region. After enable the function, it will start recording in next frame and set awb_done flag when it is done.

If also support user to get one pixel data when awb_data_type="1x".



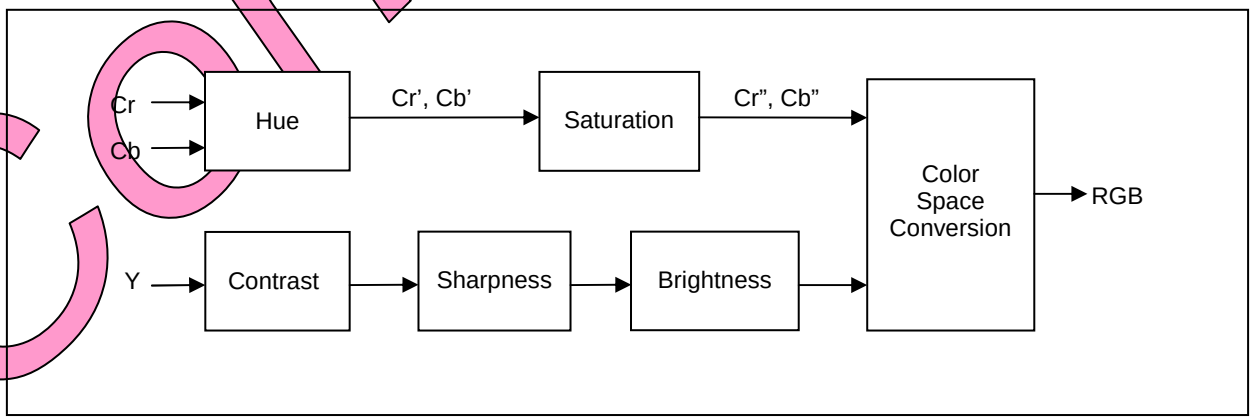

## 3.4. Scaler

Scaler is a zoom engine to convert input resolution to panel resolution. The scaling ratios, horizontal and vertical, are fully programmable. Therefore, supports different types of panel such as 320x234, 400x234, 480x234. 640x480, 800x600 and so on.

De-interlacing function is also implemented for improving picture quality.

## 3.5. Luminance and Chrominance Adjustment

Luminance and chrominance adjustment block is shown below. It contains hue, saturation, contrast, sharpness and brightness adjustment. The output is convert to RGB domain with a color space converter.



### 3.5.1. Hue

Hue adjustment allows user to change the hue angle.

Cb' = Cb·cos$\theta$ – Cr·sin$\theta$
Cr' = Cr·cos$\theta$ + Cb·sin$\theta$
where cos$\theta$ and **sin$\theta$** is set by registers.

### 3.5.2. Saturation

Saturation adjustment is done by multiplying Cb and Cr with a programmable coefficient.

Cb" = Cb'· sat_coef
Cr" = Cr'· sat_coef
The range of coefficient is 0 ~ 1.96875.

### 3.5.3. Contrast

Contrast adjustment is done by programming the Y transfer curve. Black and white level stretch can be done by setting this curve. It has 12 points to change the curve and get user favorite performance.

### 3.5.4. Sharpness

Sharpness adjustment is to increase the amplitude of high frequency luminance information. User can control the sharpness ratio and reduce the overshoot via register setting.

### 3.5.5. Brightness

Brightness adjustment is to add or subtract an offset to Y signal.

Yout = Yin ± offset

### 3.5.6. Color Space Conversion

Color space conversion converts YCbCr signal to RGB. Two standards are supported, BT.601 and BT.709.

SDTV-Computer System (BT.601)

$R = 1.164(Y_{601} - 16) + 1.596(Cr - 128)$
$G = 1.164(Y_{601} - 16) - 0.391(Cb - 128) - 0.813(Cr - 128)$
$B = 1.164(Y_{601} - 16) + 2.018(Cb - 128)$

HDTV-Computer System (BT.709)

$R = 1.164(Y_{709} - 16) + 1.793(Cr - 128)$
$G = 1.164(Y_{709} - 16) - 0.213(Cb - 128) - 0.534(Cr - 128)$
$B = 1.164(Y_{709} - 16) + 2.115(Cb - 128)$

## 3.6. On Screen Display (OSD)

OSD features :

- Font size : 12x18
- 9216x12 bits ROM, two banks, each bank stores 256 fonts
- 1280*24 bits RAM, stores user-defined fonts
- 512*16 bits Display RAM, stores character attributes
- Support RAM clear function
- Foreground and background color : selected from 32 colors look up table
- Programmable 1x, 2x, 3x and 4x for character width and height
- Support 2 display windows
- Support 1 programmable background windows
- Support shadow/border
- Support fade in/out effect
- Support blinking effect
- Support external OSD from other device

### 3.6.1. Character Attribute

Character attribute format

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Blink | 0 | CLUT index | | | | | BR | ROM font Index | | | | | | | |
| | Blink | 1 | CLUT index | | | | | 0 | User defined Font Index (1-bit/color) | | | | | | | |
| | Blink | 1 | CLUT index | | | | | 1 | 0 | User defined Font Index (2-bit/color) | | | | | | |

Each character has a 16-bit attribute.

Bit[15] : Blink

Blinking effect is enabled when it is “1”.

Bit[14] : Choose ROM font or RAM font

”0”: use ROM font

“1”: use RAM font

Bit[13:9] : Index to choose foreground/background color from CLUT.

Bit[8] :

If Bit[14]=0, border/shadow effect is enabled when it is “1”.

If Bit[14]=1, select 1-bit or 2-bit color font.

Bit[7:0] : character index to selected which character to be displayed

### 3.6.2. Display RAM

The display RAM stores the attribute of character which want to be displayed.

Display RAM Data Structure

| Address | Bit | Description |
|---|---|---|
| | 15……..……..0 | |
| DSP0_inx | character0 attribute of display window0 | Display Window0 Character Attribute |
| DSP0_inx +1 | character1 attribute of display window0 | |
| : | : | |

| | | |
|---|---|---|
| : | : | |
| : | : | |
| : | : | |
| DSP1_inx | character0 attribute of display window1 | Display Window1 Character Attribute |
| DSP1_inx +1 | character1 attribute of display window1 | |
| : | : | |
| : | : | |
| : | : | |
| : | : | |

Display RAM data mapping (512x16 bits, write only)

| RAM Addr. | Bit [15:8] | Bit [7:0] |
|---|---|---|
| 0 | Page= 0x20h, Register index= 01h | Page= 0x20h, Register index= 00h |
| 1 | Page= 0x20h, Register index= 03h | Page= 0x20h, Register index= 02h |
| : : | : : | : : |
| 128 | Page= 0x21h, Register index= 01h | Page= 0x21h, Register index= 00h |
| 129 | Page= 0x21h, Register index= 03h | Page= 0x21h, Register index= 02h |
| : : | : : | : : |
| 511 | Page= 0x23h, Register index= FFh | Page= 0x23h, Register index= FEh |

Display RAM clear procedure :

Set bit 5 of register 0x1Dh and clear this bit after 512 system clock cycles.

### 3.6.3. User-Defined Font RAM

UDF RAM Data Structure (1280x24 bits)

| Address | Bit[23:12] | Bit[11: 0] | Note |
|---|---|---|---|
| UDF_Inx0 | UDF1 character #0, Line 1 | UDF1 character #0, Line 0 | 1-bit color font |
| UDF_Inx0 +1 | UDF1 character #0, Line 3 | UDF1 character #0, Line 2 | |
| : | : | | |
| UDF_Inx0 + 8 | UDF1 character #0, Line 17 | UDF1 character #0, Line 16 | |
| : | : | | |
| UDF_Inx1 | UDF2 character #0, Line 0 | | 2-bit color font |
| UDF_Inx1 +1 | UDF2 character #0, Line 1 | | |
| : | : | | |
| UDF_Inx1 + 17 | UDF2 character #0, Line 17 | | |
| : | : | | |
| 0x4FFh | : | | |

User-Defined Font RAM data mapping (1280x24 bits, write only)

| RAM Addr. | Bit [23:16] | Bit [15:8] | Bit [7:0] |
|---|---|---|---|
| 0(0x000h) | Page= 0x2Ch, Reg index= 02h/03h | Page= 0x2Ch, Reg index= 01h | Page= 0x2Ch, Reg index= 00h |
| 1(0x001h) | Page= 0x2Ch, Reg index= 06h/07h | Page= 0x2Ch, Reg index= 05h | Page= 0x2Ch, Reg index= 04h |
| : : | : : | : : | : : |
| 256(0x100h) | Page= 0x30h, Reg index= 02h/03h | Page= 0x30h, Reg index= 01h | Page= 0x30h, Reg index= 00h |
| 257(0x101h) | Page= 0x30h, Reg index= 06h/07h | Page= 0x30h, Reg index= 05h | Page= 0x30h, Reg index= 04h |
| : : | : : | : : | : : |
| 512(0x200h) | Page= 0x34h, Reg index= 02h/03h | Page= 0x34h, Reg index= 01h | Page= 0x34h, Reg index= 00h |
| 513(0x201h) | Page= 0x34h, Reg index= 06h/07h | Page= 0x34h, Reg index= 05h | Page= 0x34h, Reg index= 04h |
| : : | : : | : : | : : |

| | | | |
|---|---|---|---|
| 1280(0x4FFh) | Page= 0x3Fh, Reg index= 3Eh/3Fh | Page= 0x3Fh, Reg index=3Dh | Page= 0x3Fh, Reg index= 3Ch |

User-Defined Font RAM clear procedure :
Set bit 6 of register 0x1Dh and clear this bit after 1280 system clock cycles.

### 3.6.4. Color Look-Up Table (CLUT)

Color Look-Up Table is a 32x24 bits RAM.

(1) Transparent :
Index “0” is defined to let OSD transparent

(2) 1-bit color :
Bit[23:12] stores foreground color and bit[11:0] stores background color. If bit[11:0]=”001h”, the background color is transparent.

| Foreground color | | | | | | | | | | | | Background color | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R7 | R6 | R5 | R4 | G7 | G6 | G5 | G4 | B7 | B6 | B5 | B4 | R3 | R2 | R1 | R0 | G3 | G2 | G1 | G0 | B3 | B2 | B1 | B0 |
| R7 | R6 | R5 | R4 | G7 | G6 | G5 | G4 | B7 | B6 | B5 | B4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Foreground color (font code=”1”)
RGB[23:0] = { R[7:4], R[7:4] , G[7:4] , G[7:4] , B[7:4] , B[7:4] }
Background color (font code=”0”)
RGB[23:0] = { R[3:0], R[3:0] , G[3:0] , G[3:0] , B[3:0] , B[3:0] }

(3) 2-bit color :
Bit[23:18] stores foreground color 2.
Bit[27:12] stores foreground color 1.
Bit[11:6] stores foreground color 0.
Bit[5:0] stores background color. If bit[5:0]=”000001”, the background color is transparent.

| Foreground color 2 | | | | | | Foreground color 1 | | | | | | Foreground color 0 | | | | | | Background color | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R7 | R6 | G7 | G6 | B7 | B6 | R5 | R4 | G5 | G4 | B5 | B4 | R3 | R2 | G3 | G2 | B3 | B2 | R1 | R0 | G1 | G0 | B1 | B0 |
| R7 | R6 | G7 | G6 | B7 | B6 | R5 | R4 | G5 | G4 | B5 | B4 | R3 | R2 | G3 | G2 | B3 | B2 | 0 | 0 | 0 | 0 | 0 | 1 |

Foreground color 2 (font code=”11”)
RGB[23:0] = { R[7:6], R[7:6], R[7:6], R[7:6], G[7:6], G[7:6], G[7:6], G[7:6], B[7:6], B[7:6], B[7:6], B[7:6] }
Foreground color 1 (font code=”10”)
RGB[23:0] = { R[5:4], R[5:4], R[5:4], R[5:4], G[5:4], G[5:4], G[5:4], G[5:4], B[5:4], B[5:4], B[5:4], B[5:4] }
Foreground color 0 (font code=”01”)
RGB[23:0] = { R[3:2], R[3:2], R[3:2], R[3:2], G[3:2], G[3:2], G[3:2], G[3:2], B[3:2], B[3:2], B[3:2], B[3:2] }
Background color (font code=”00”)
RGB[23:0] = { R[1:0], R[1:0], R[1:0], R[1:0], G[1:0], G[1:0], G[1:0], G[1:0], B[1:0], B[1:0], B[1:0], B[1:0] }

Note : Update CLUT during OSD is displaying is prohibited

CLUT RAM data mapping

| RAM Addr. | Bit [23:16] | Bit [15:8] | Bit [7:0] |
|---|---|---|---|
| 0(0x00h) | Page= 0x16h, Reg index= 02h/03h | Page= 0x16h, Reg index= 01h | Page= 0x16h, Reg index= 00h |
| 1(0x01h) | Page= 0x16h, Reg index= 06h/07h | Page= 0x16h, Reg index= 05h | Page= 0x16h, Reg index= 04h |
| : | : | : | : |
| : | : | : | : |

| | | | |
|---|---|---|---|
| 31(0x1Fh) | Page= 0x16h, Reg index= 7Eh/7Fh | Page= 0x16h, Reg index=7Dh | Page= 0x16h, Reg index= 7Ch |

CLUT RAM clear procedure :
Set bit 4 of register 0x1Dh and clear this bit after 32 system clock cycles.

### 3.6.5. Background Windows

There is one programmable background window provided. It has H_start, H_end, V_start and V_end to define window position and size. The color of background window is setting by register.

### 3.6.6. Fade in/out function

A programmable mask determines displayed OSD area. The mask is defined by H_start, V_start and H_end, V_end which can be automatically increment/decrement to perform fade in/out effect.

### 3.6.7. External OSD

External OSD can be mixed to the output. The display priority is *display window* > *background window* > *external OSD* > *video*.

## 3.7. Gamma Correction

Gamma correction is done by SRAM-based look-up table. Each color has a 256x8 bits RAM to give 1-to-1 transformation.

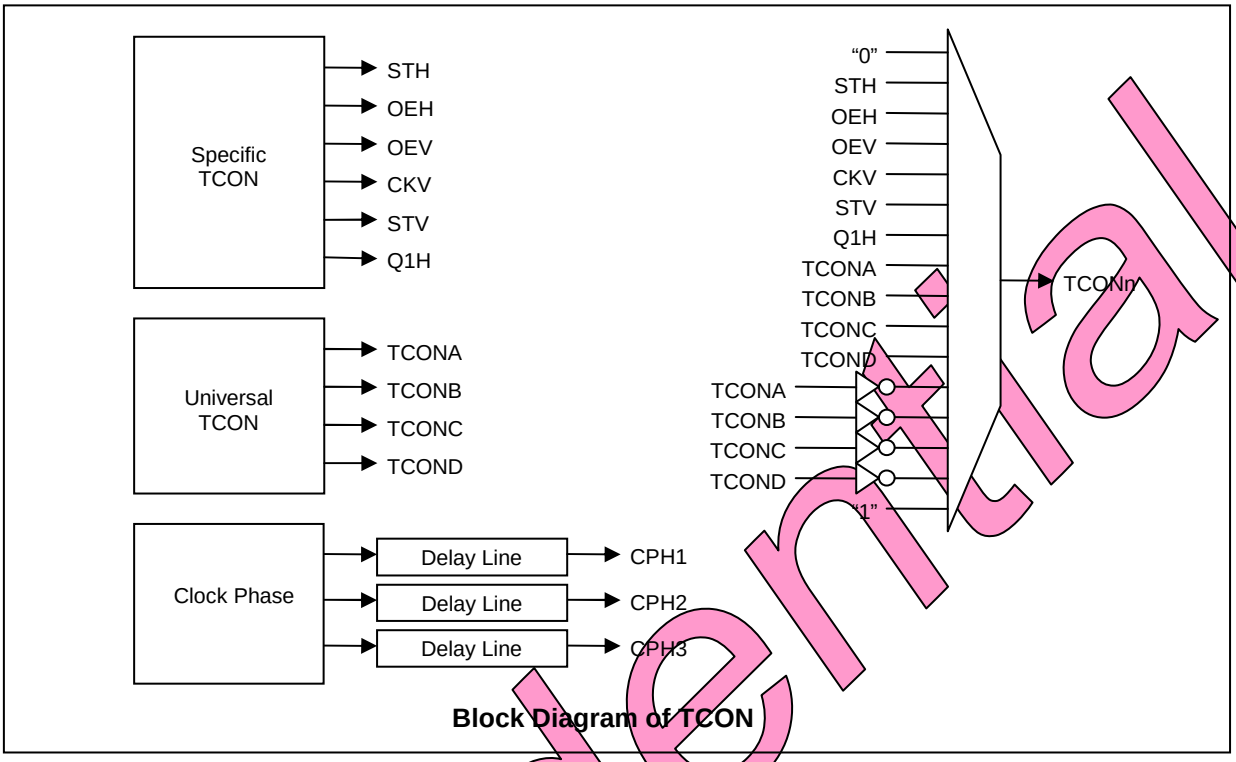
## 3.8. Dither

The dither function diffuses the errors when display panel is 6-bit.
An example of original 6-bit output and dithering 6-bit output (input = 8-bit)

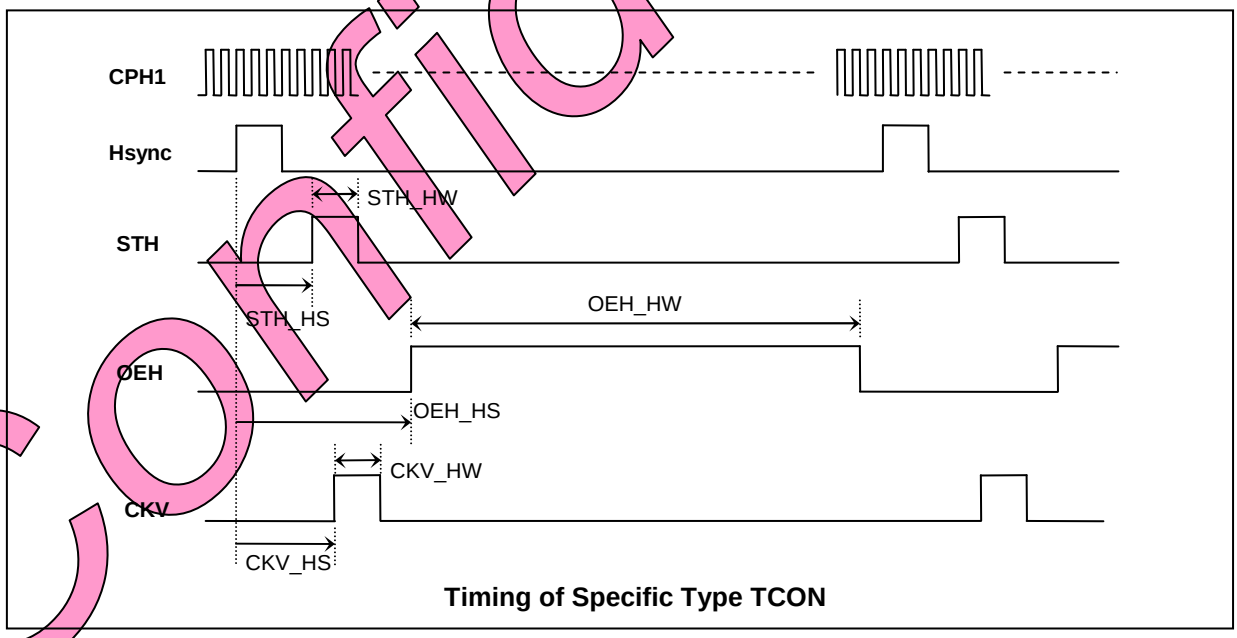
## 3.9. TCON and Panel Clock

There are two kinds of TCON signals supported : universal type and specific type. Specific type generates OEH, OEV, STH, STV, CKV and Q1H. Universal type generates signals which can be any combination of H and V timing.

Panel clock supports simultaneously and sequential mode for analog panel. Clock output can be fine tuned by programmable delay to get best timing margin.




**Block Diagram of TCON**




**Timing of Specific Type TCON**



## 3.10. Digital-to-Analog Converter

Analog RGB signals are output from triple 8-bit DACs. It can drive analog LCD panel directly without using external amplifiers. Amplitude of full scale swing is programmable, range is from 2.7V to 4.2V with 2.5V DC. Each channel output has a fine delay control for compensating differences of channel delay.

## 3.11. VCOM output

VCOM output amplitude is programmable. 5-bit register has 32 steps to fine tune the amplitude for analog panel. An external amplifier is needed to drive panel. The offset of VCOM can be generated from PWM .

## 3.12. Spread Spectrum PLL

The spread spectrum PLL generates the clock for panel. The modulation period and frequency deviation can be programmed to control the frequency spectrum for reducing EMI.

## 3.13. Keypad ADC

Keypad ADC is an 8-bit ADC with four inputs. It converts all inputs sequentially and clear the start bit when conversion is done.

## 3.14. PWM

### 3.14.1. PWM

PWM is 8-bit resolution and use BRM algorithm. Time base is 1MHz (if system clock=24MHz).

### 3.14.2. 10-bit PWM

One 10-bit PWM could output via PWM[3:0] by register setting. Time base is 1MHz (if system clock=24MHz).

### 3.14.3. Low Frequency PWM

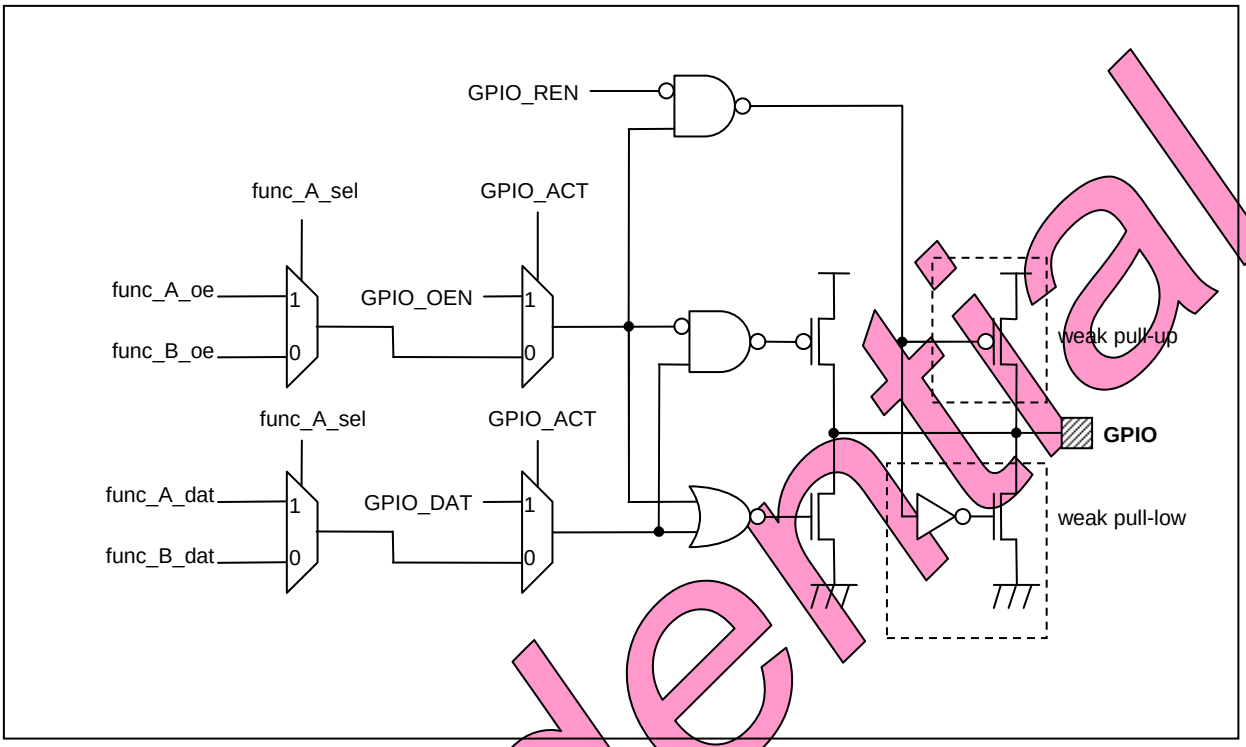
Low frequency PWM clock frequency is 1MHz ÷ (PWM_CLK[6:0]+1). Range is 30.52Hz ~ 3.90625khz And LPWM could output via PWM[3:0] by register setting or only internal use(for DC-DC).

## 3.15. Remote Control

Infra-red remote control is supported by using a 16-bit counter to measure high/low time interval. The clock source can be selected from 1μs, 64μs, 256μs or 1ms. Counter overflow value is programmable and with interrupt

## 3.16. GPIO

General purpose I/Os are shared with other functions. The structure is shown below. Pull-up or Pull-down can be turn off while not used.




## 3.17. Interrupt

Interrupt sources of internal MCU mode:

- Input processor, including H/V loss, timing change, Vsync edge
- Vsync output edge
- IR
- INT pin
- MCU timer/counter 0 and 1
- DC-to-DC power fail

## 3.18. ISP & ICE

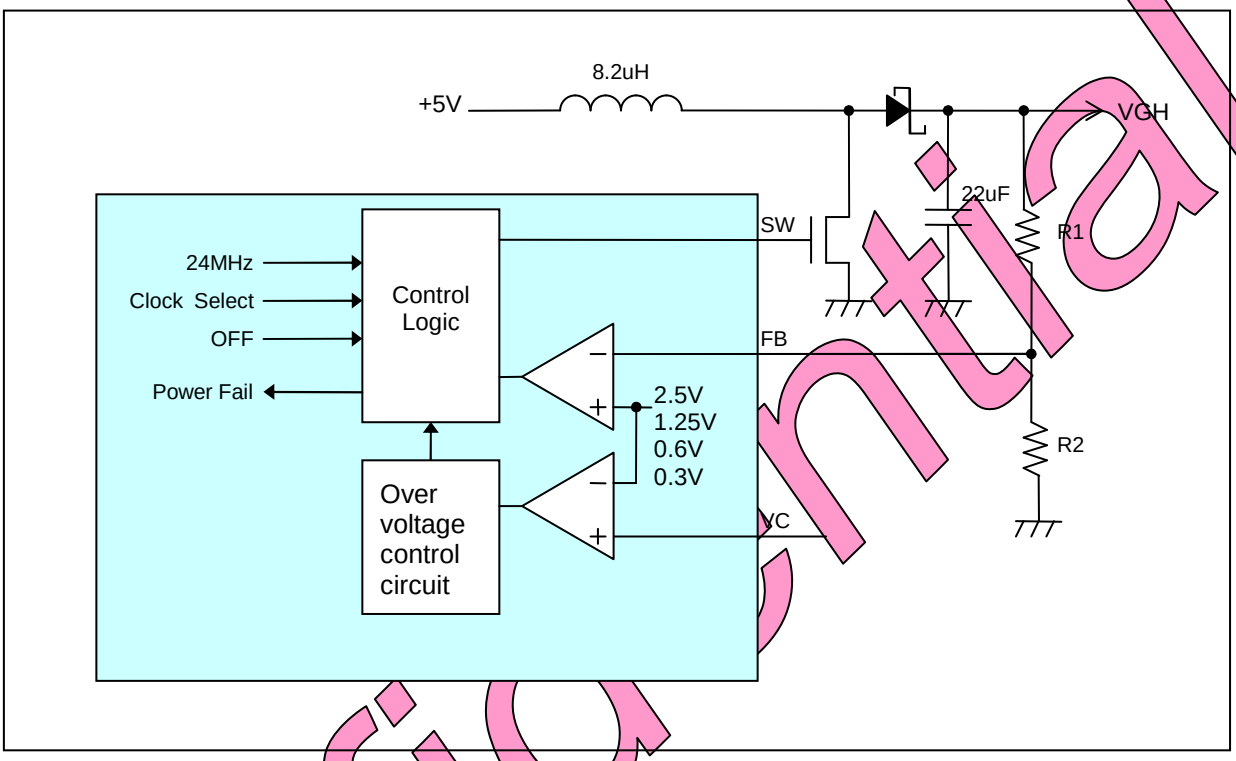
In-System-Programming (ISP) function is provided to program the external flash memory through $I^2C$ interface.

In-Circuit-Emulator (ICE) function is supported for debugging user program without using external ICE hardware.

Weltrend Development Kit supports ISP and ICE functions. Break points and single step execution are provided.

## 3.19. DC-to-DC Converter

DC-to-DC converter is PFM type with selectable switching frequency. A over-voltage-control circuit is built-in. Power failure signal is supported for MCU monitoring. Protection circuit is also implemented to protect power MOS while system clock fails. A backlight tuning function is built-in for LED application.




## 3.20. Reset

There are three sources can reset the whole chip.

- RESETB pin : A low level on this pin.
- 2.5V low voltage reset : When core logic power is under the threshold.
- 3.3V low voltage reset : When 3.3V pad power is under the threshold.

2.5V and 3.3V low voltage reset can be disabled by MCU.

# 4. Register List

All registers are 8-bit register with 16-bit address index. High byte of address is defined as page and low byte is index.

Below is a quick reference table for page information.

| Page | Function | Description |
|---|---|---|
| 0x00h | Global system control | I/O pin setting, power down mode, SS PLL |
| 0x01h | Input Processor | Input capture, resolution detect, reference timing, AWB |
| 0x02h | Reserved | |
| 0x03h | Scaler | Scaler control |
| 0x04h~0x09h | Reserved | |
| 0x0Ah | Chrominance and Luminance | Contrast, sharpness, brightness, hue, saturation |
| 0x0Bh | Reserved | |
| 0x0Ch | OSD control | OSD control |
| 0x0Dh | TCON | Panel timing control signal |
| 0x0Eh | Analog circuit | DAC, VCOM output, DC-to-DC converter |
| 0x0Fh | Output Processor | Output format, gamma, dither |
| 0x10h~0x12h | Reserved | |
| 0x13h | Miscellaneous | $I^2C$, IR, PWM, keypad ADC |
| 0x14h~0x15h | Reserved | |
| 0x16h | OSD CLUT | OSD color look-up table |
| 0x17~0x1F | Reserved | |
| 0x20~0x23 | OSD display RAM | RAM of OSD display |
| 0x24~0x2B | Reserved | |
| 0x2C~0x3F | OSD UDF RAM | RAM of OSD user defined font |
| 0x40 | Gamma table | Gamma table of red color |
| 0x41 | Reserved | |
| 0x42 | Gamma table | Gamma table of green color |
| 0x43 | Reserved | |
| 0x44 | Gamma table | Gamma table of blue color |
| 0x45~0x4F | Reserved | |
| 0x50~0x5F | Reserved | |
| 0x60 | Video Decoder | Video decoder |
| 0x61~0x6F | Reserved | |
| 0x70~0x75 | Reserved | |
| 0x76 | CPU RAM | RAM of MCU |
| 0x77~0xFF | Reserved | |

## 4.1. System Control

### 4.1.1. General Control

Page 0x00h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 00h | 03h | R/W | 7:0 | rev_id | Chip revision ID code |
| 01h | | | 7:4 | | Reserved |
| | 0 | R/W | 3 | osc_off | Shut down system clock, resumes when wake-up event (index-2) occurs.<br>Clear and set OSC_OFF to generate a rising edge to enable function |
| | 0 | R/W | 2 | rst_ndf | 0 = enable digital filter for system reset<br>1 = no digital filter for system reset |
| | 0 | R/W | 1 | lvr_33 | 0 = Enable Low Voltage Reset for 3.3V power |
| | 0 | R/W | 0 | lvr_25 | 0 =Enable Low Voltage Reset for 2.5V power |
| 02h | | | 7:5 | | Reserved |
| | | | 4 | wake_en_adc | wake-up enable for keypad-ADC<br>system suspends if OSC_OFF is turned on<br>system resumes if input data are changed from the status before suspend |
| | 0 | R/W | 3 | wake_en_mp1 | wake-up enable for MCU port-1 P1[3:0] |
| | 0 | R/W | 2 | wake_en_i2c | wake-up enable for $I^2C$ (including ISP_I2C, ICE_I2C, DVD_I2C and SLA_I2C) |
| | 0 | R/W | 1 | wake_en_sync | wake-up enable for CSYNC, VSYNC and HSYNC |
| | 0 | R/W | 0 | wake_en_int | wake-up enable for interrupt input |
| 03h | | | 7:0 | | Reserved |
| 04h | 0 | R/W | 7 | rst_global | F/W global reset (automatically cleared) |
| | | | 6:4 | | Reserved |
| | 0 | R/W | 3 | rst_cvd2 | reset video decoder |
| | 0 | R/W | 2 | rst_din | reset DI/BCA |
| | 0 | R/W | 1 | rst_sbs | reset scaler |
| | 0 | R/W | 0 | rst_do | reset OSD/DO/TCON |
| 05h | 0 | R/W | 7:6 | mux_adc | For IC test |
| | 0 | R/W | 5 | | Reserved |
| | 0 | R/W | 4 | mux_di | Input selection:<br>1= select ITU656 input, VDCK/VDHS/VDVS/VD[7:0] are inputs<br>0= if {EXT_OSD_EN, EXT_OSD_SEL} = "10", VDCK/VIN/HIN/VD[4:0]} acts as external OSD I/F, else VDCK/VIN/HIN/VD are decoder outputs |
| | 0 | R/W | 3 | demode_en | select scaler demo_de as reformat rfmt_de input<br>1 = connect demo_de to rfmt_de, disable GOB/DO demo function<br>0 = connect do_de to rfmt_de, enable GOB/DO demo function |
| | 000b | R/W | 2:0 | mux_rfmt | For IC test |
| 06h | | | 7:3 | | Reserved |
| | 1 | R/W | 2 | clkn_ rfmt | 1 = invert RFMT clock input |
| | 1 | R/W | 1 | clkn_ bca | 1 = invert BCA clock input |
| | 1 | R/W | 0 | clkn_ di | 1 = invert DI clock input |

### 4.1.2. Panel Clock Adjust

Page 0x00

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 07h | | | 7:5 | | Reserved |
| | 000b | R/W | 4:2 | daclk_sel | Panel clock phase selection |
| | 0 | R/W | 1 | cph_dp | 0 = analog panel<br>It also control the inversion function of panel data output. |
| | 0 | R/W | 0 | cph_phase | CPH/PCK phase inversion |
| 08h | | | 7:4 | | Reserved |
| | 0h | R/W | 3:0 | del_cph1 | CPH1 output delay selection |
| 09h | | | 7:4 | | Reserved |
| | 0h | R/W | 3:0 | del_cph2 | CPH2 output delay selection |
| 0Ah | | | 7:4 | | Reserved |
| | 0h | R/W | 3:0 | del_cph3 | CPH3 output delay selection |

### 4.1.3. Spread Spectrum PLL

Page 0x00

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 10h | | | 7 | | Reserved |
| | 0h | R/W | 6:4 | ss_prescale | VCO2 prescaler selection:<br>000= ÷2 100= ÷8<br>001= ÷3 101= ÷12<br>010= ÷4 110= ÷16<br>011= ÷6 111= ÷1 |
| | 0h | R/W | 1:0 | ss_finsel | FIN clock source selection<br>00= CKIN<br>01= REFCK<br>10= HSYNC<br>11= HS*NF2 |
| 11h | 0h | R/W | 7:4 | ss_T[3:0] | Modulation period (number of "freq" period) |
| | 0h | R/W | 3:0 | ss_stepn[3:0] | Spreading step number. Range : 1 ~15<br>Modulation Depth ~ ±((Delta*StepN)/ NF)*100% |
| 12h | | | 7:4 | | Reserved |
| | 0 | R/W | 3 | ss_tmode | For testing control |
| | 1 | R/W | 2 | ss_testb | For testing control. Keep “1” of normal use. |
| | 1 | R/W | 1 | ss_bypass | 1 =power down (PLL off) and force output to ground<br>0 = Enable SS PLL |
| | 1 | R/W | 0 | ss_onss | Spread enable |
| 13h | | | 7:4 | | Reserved |
| | 0h | R/W | 3:0 | ss_delta | Step size for NF spreading, i.e. add/sub value at one step from previous Spreaded NF<br>Range : 1 ~15 |
| 14h | 02h | R/W | 7:0 | ss_NI[7:0] | Dividing number of input divider, i.e. prescaler. |
| 15h | 00h | R/W | 1:0 | ss_NI[9:8] | |
| | | | 7:2 | | Reserved |
| 16h | 02h | R/W | 7:0 | ss_NF[7:0] | Dividing number of feedback divider.<br>Range : 2 ~1023<br>note: set SS_ONSS = '1' before programming SS_NF |
| 17h | 00h | R/W | 1:0 | ss_NF[9:8] | |
| | | | 7:2 | | Reserved |
| 18h | 02h | R/W | 7:0 | ss_NO[7:0] | Dividing number of output divider |
| 19h | 00h | R/W | 1:0 | ss_NO[9:8] | |
| | | | 7:2 | | Reserved |
| 1Ah | 02h | R/W | 7:0 | ss_NF2[7:0] | Dividing number of feedback divider II |
| 1Bh | 00h | R/W | 2:0 | ss_NF2[10:8] | |

| | | | | | |
|---|---|---|---|---|---|
| | | | 7:3 | | Reserved |

SS PLL output frequency can be calculated by the formula below

$$Fout = \frac{Fin * NF}{NI * NO}$$

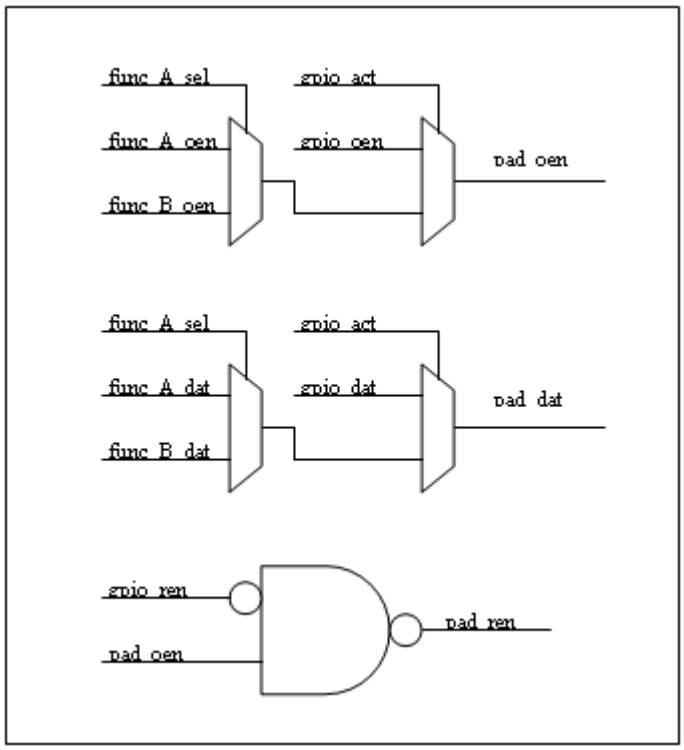
In order to have good performance of PLL, some criteria must be followed

(1) Fref: 1M~6M Hz

(2) Fosc: 350M~600M Hz

### 4.1.4. GPIO setting

Multi-Function I/O Definition




| func_A_sel | func_A | func_B | Description |
|---|---|---|---|
| REG_MP1_EN | MP1[3:0] | PWM[3:2]/ADC[1:0] | 8051 P1 via PWM[3:2] and ADC[1:0] |
| REG_EN_UART0 | TXD0/RXD0 | ADC[3:2] | 1st UART port via ADC[3:2] |
| REG_EN_UART1 | TXD1/RXD1 | TCON[1:0] | 2nd UART port via TCON[1:0] |
| REG_PWML_EN & REG_PWML_SEL[1:0] | Low frequency PWM | PWM[3:0] | Low frequency PWM output via PWM[3:0] pin |
| REG_PWM10_EN & REG_PWM10_SEL[1:0] | 10-bit PWM | PWM[3:0] | 10-bit PWM output via PWM[3:0] pin |
| EXT_OSD_EN = 1'b1 EXT_OSD_SEL = 1'b1 | {OSD_CK, OSD_VS, OSD_HS, OSD_DIN[4:0]} | TCON[7:0] | External OSD in/out pin via TCON[7:0] |
| MUX_DI = 1 'b0 EXT_OSD_EN = 1'b1 EXT_OSD_SEL= 1'b0 | {OSD_CK, OSD_VS, OSD_HS, XXX, OSD_DIN[4:0]} | ITU656 output for {VDCK, VSYNC, HSYNC, VD} | External OSD in/out pin via ITU656 in/out pins |

GPIO and Special Function Control Registers -- Page 0x00h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 20h | FFh | R/W | 7:0 | gpio_act_VD | Configuration of VD[7:0] pins.<br>1 = act as GPIO<br>0 = act as video data of BT.656 |
| 21h | | | 7:3 | | Reserved |
| | 1 | R/W | 2 | gpio_act_VC[2] | 1 = act as GPIO<br>0 = act as clock of BT.656 or BT.601 (VDCK) |

| | | | | | |
|---|---|---|---|---|---|
| | 1 | R/W | 1 | gpio_act_VC[1] | 1 = act as GPIO<br>0 = BT.601 VSYNC (VDVS) |
| | 1 | R/W | 0 | gpio_act_VC[0] | 1 = act as GPIO<br>0 = BT.601 HSYNC (VDHS) |
| 22h | FFh | R/W | 7:0 | gpio_act_TL[7:0] | 1 = act as GPIO<br>0 = TCON[7:0] |
| 23h | | | 7:6 | | Reserved |
| | 1 | R/W | 5:0 | gpio_act_TH[5] | 1 = act as GPIO<br>0 = act as vsync output (VSO) |
| | 1 | R/W | 4 | gpio_act_TH[4] | 1 = act as GPIO<br>0 = act as hsync output (HSO) |
| | 1111 | R/W | 3:0 | gpio_act_TH[3:0] | 1 = act as GPIO<br>0 = act as TCON[11:8] |
| 24h | | | 7:4 | | Reserved |
| | Fh | R/W | 3:0 | gpio_act_PWM | 1 = act as GPIO<br>0 = act as PWM[3:0] |
| 25h | | | 7:4 | | Reserved |
| | Fh | R/W | 3:0 | gpio_act_ADC | 1 = act as GPIO<br>0 = act as ADC[3:0] |
| 26h | | | 7:2 | | Reserved |
| | 0h | R/W | 1:0 | gpio_act_I2C | act as GPIO for {ICE_SCL, ICE_SDA}<br>note: only paired disable is allowed |
| 27h | | | 7:6 | | Reserved |
| | 1 | R/W | 5:0 | gpio_act_FLH[5] | act as GPIO for {IR, INT, FCSB, FCLK, FDO, FDI}<br>1 = act as GPIO<br>0 = act as infra red input (IR) |
| | 1 | R/W | 4 | gpio_act_FLH[4] | 1 = act as GPIO<br>0 = act as interrupt (INT) |
| | 1 | R/W | 3 | gpio_act_FLH[3] | 1 = act as GPIO<br>0 = act as flash chip select (FCSB) |
| | 1 | R/W | 2 | gpio_act_FLH[2] | 1 = act as GPIO<br>0 = act as flash clock (FCLK) |
| | 0 | R/W | 1 | gpio_act_FLH[1] | 1 = act as GPIO<br>0 = act as flash data output (FDO) |
| | 0 | R/W | 0 | gpio_act_FLH[0] | 1 = act as GPIO<br>0 = act as flash data input (FDI) |
| 28h | FFh | R/W | 7:0 | gpio_act_PDH | 1 = act as GPIO<br>0 = act as PD[23:16] |
| 29h | FFh | R/W | 7:0 | gpio_act_PDM | 1 = act as GPIO<br>0 = act as PD[15:8] |

note: keeping I2C active after initialization

GPIO Output Enable Control Registers -- Page 0x00

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 30h | FFh | R/W | 7:0 | gpio_oen_VD[7:0] | 0 = output enable for BT.656 data input bus VD[7:0] |
| 31h | | | 7:3 | | Reserved |
| | 1 | R/W | 2 | gpio_oen_VC[2] | 0 = output enable for VDCK pin |
| | 1 | R/W | 1 | gpio_oen_VC[1] | 0 = output enable for VDVS pin |
| | 1 | R/W | 0 | gpio_oen_VC[0] | 0 = output enable for VDHS pin |
| 32h | FFh | R/W | 7:0 | gpio_oen_TL[7:0] | 0 = output enable for TCON[7:0] pins |
| 33h | | | 7:6 | | Reserved |
| | 1 | R/W | 5 | gpio_oen_TH[5] | 0 = output enable for VSO pin |
| | 1 | R/W | 4 | gpio_oen_TH[4] | 0 = output enable for HSO pin |

| | | | | | |
|---|---|---|---|---|---|
| | 1111 | R/W | 3:0 | gpio_oen_TH[3:0] | 0 = output enable for TCON[11:8] pins |
| 34h | | | 7:4 | | Reserved |
| | 1111 | R/W | 3:0 | gpio_oen_PWM[3:0] | 0 = output enable for PWM[3:0] pins |
| 35h | | | 7:4 | | Reserved |
| | 1111 | R/W | 3:0 | gpio_oen_ADC[3:0] | 0 = output enable for keypad ADC[3:0] |
| 36h | | | 7:2 | | Reserved |
| | 1 | R | 1 | gpio_oen_I2C[1] | Input only |
| | 1 | | 0 | gpio_oen_I2C[0] | Input only |
| 37h | | | 7:6 | | Reserved |
| | 1 | R/W | 5 | gpio_oen_FLH[5] | 0 = output enable for IR pin |
| | 1 | R/W | 4 | gpio_oen_FLH[4] | 0 = output enable for INT pin |
| | 1 | R/W | 3 | gpio_oen_FLH[3] | 0 = output enable for FCSB pin |
| | 1 | R/W | 2 | gpio_oen_FLH[2] | 0 = output enable for FCLK pin |
| | 1 | R/W | 1 | gpio_oen_FLH[1] | 0 = output enable for FDO pin |
| | 1 | R/W | 0 | gpio_oen_FLH[0] | 0 = output enable for FDI pin |
| 38h | FFh | R/W | 7:0 | gpio_oen_PDH[7:0] | 0 = output enable for panel data output PD[23:16] |
| 39h | FFh | R/W | 7:0 | gpio_oen_PDM[7:0] | 0 = output enable for panel data output PD[15:8] |
| 3Bh | | | 7:4 | | Reserved |
| | 1 | R/W | 3 | gpio_oen_D2D[3] | 0 = output enable for VC2 pin |
| | 1 | R/W | 2 | gpio_oen_D2D[2] | 0 = output enable for FB2 pin |
| | 1 | R/W | 1 | gpio_oen_D2D[1] | 0 = output enable for FB1 pin |
| | 1 | R/W | 0 | gpio_oen_D2D[0] | 0 = output enable for VC1 pin |

GPIO Output Data Registers – Page 0x00h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 40h | FFh | R/W | 7:0 | gpio_dat_VD[7:0] | GPIO output data for VD[7:0] pins |
| 41h | | | 7:3 | | Reserved |
| | 7h | R/W | 2:0 | gpio_dat_VC[2:0] | GPIO output data for video control {VDCK, VSYNC, HSYNC} |
| 42h | FFh | R/W | 7:0 | gpio_dat_TL | GPIO output data for TCON[7:0] |
| 43h | | | 7:6 | | Reserved |
| | 3Fh | R/W | 5:0 | gpio_dat_TH | GPIO output data for {VSO, hSO, TCON[11:8]} |
| 44h | | | 7:4 | | Reserved |
| | Fh | R/W | 3:0 | gpio_dat_PWM | GPIO output data for PWM[3:0] |
| 45h | | | 7:4 | | Reserved |
| | Fh | R/W | 3:0 | gpio_dat_ADC | GPIO output data for keypad ADC[3:0] |
| 46h | | | 7:2 | | Reserved |
| | 3h | R/W | 1:0 | gpio_dat_I2C | GPIO output data for {ICE_SCL, ICE_SDA} |
| 47h | | | 7:6 | | Reserved |
| | 3Fh | R/W | 5:0 | gpio_dat_FLH | GPIO output data for {IR, INT, FCSB, FCLK, FDO, FDI} |
| 48h | FFh | R/W | 7:0 | gpio_dat_PDH | GPIO output data for panel data output PD[23:16] |
| 49h | FFh | R/W | 7:0 | gpio_dat_PDM | GPIO output data for panel data output PD[15:8] |
| 4Bh | | | 7:4 | | Reserved |
| | Fh | R/W | 3:0 | gpio_dat_D2D | GPIO output data for DC2DC pads {VC2, FB2, FB1, VC1} |

note: the read data is from pin, not registered value.

GPIO Pull up/down Control Registers – Page 0x00h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 50h | 00h | R/W | 7:0 | gpio_ren_VD[7:0] | 1 = turn off pull-down resistor of VD[7:0] pin<br>0 = turn on pull-down resistor of VD[7:0] pin |
| 51h | | R/W | 7:3 | | Reserved |
| | 0 | | 2 | gpio_ren_VC[2] | 1 = turn off pull-down resistor of VDCK pin<br>0 = turn on pull-down resistor of VDCK pin |
| | 0 | | 1 | gpio_ren_VC[1] | 1 = turn off pull-down resistor of VSYNC pin<br>0 = turn on pull-down resistor of VSYNC pin |

| | | | | | |
|---|---|---|---|---|---|
| | 0 | | 0 | gpio_ren_VC[0] | 1 = turn off pull-down resistor of HSYNC pin<br>0 = turn on pull-down resistor of HSYNC pin |
| 52h | 00h | R/W | 7:0 | gpio_ren_TL[7:0] | 1 = turn off pull-down resistor of TCON [7:0] pin<br>0 = turn on pull-down resistor of TCON [7:0] pin |
| 53h | | R/W | 7:6 | | Reserved |
| | 0 | | 5 | gpio_ren_TH[3:0] | 1 = turn off pull-down resistor of CPH2/PVS pin<br>0 = turn on pull-down resistor of CPH2/PVS pin |
| | 0 | | 4 | gpio_ren_TH[3:0] | 1 = turn off pull-down resistor of CPH3/PHS pin<br>0 = turn on pull-down resistor of CPH3/PHS pin |
| | 0h | | 3:0 | gpio_ren_TH[3:0] | 1 = turn off pull-down resistor of TCON [11:8] pin<br>0 = turn on pull-down resistor of TCON [11:8] pin |
| 54h | 0h | R/W | 3:0 | gpio_ren_PWM | 0 = turn on input pull-up for PWM[3:0]<br>1 = turn off input pull-up for PWM[3:0] |
| 55h | 0h | R/W | 3:0 | gpio_ren_ADC | 0 = turn on input pull-up for ADC[3:0]<br>1 = turn off input pull-up for ADC[3:0] |
| 56h | 0 | R/W | 1 | gpio_ren_I2C_SCL | 0 = turn on input pull-up for ICE_SCL<br>1 = turn off input pull-up for ICE_SCL |
| | 0 | R/W | 0 | gpio_ren_I2C_SDA | 0 = turn on input pull-up for ICE_SDA<br>1 = turn off input pull-up for ICE_SDA |
| 57h | | | 7:6 | | Reserved |
| | 0 | R/W | 5 | gpio_ren_IR | 0 = turn on input pull-up for IR pin<br>1 = turn off input pull-up for IR pin |
| | 0 | R/W | 4 | gpio_ren_INT | 0 = turn on input pull-up for INT pin<br>1 = turn off input pull-up for INT pin |
| | 0 | R/W | 3 | gpio_ren_FCSB | 0 = turn on input pull-up for FCSB pin<br>1 = turn off input pull-up for FCSB pin |
| | 0 | R/W | 2 | gpio_ren_FCLK | 0 = turn on input pull-up for FCLK pin<br>1 = turn off input pull-up for FCLK pin |
| | 0 | R/W | 1 | gpio_ren_FDO | 0 = turn on input pull-up for FDO pin<br>1 = turn off input pull-up for FDO pin |
| | 0 | R/W | 0 | gpio_ren_FDI | 0 = turn on input pull-up for FDI pin<br>1 = turn off input pull-up for FDI pin |
| 58h | 00h | R/W | 7:0 | gpio_ren_PDH | 0 = turn on input pull-up for PD[23:16] pin<br>1 = turn off input pull-up for PD[23:16] pin |
| 59h | 00h | R/W | 7:0 | gpio_ren_PDM | 0 = turn on input pull-up for PD[15:8] pin<br>1 = turn off input pull-up for PD[15:8] pin |
| 5Bh | | | 7:4 | | Reserved |
| | 0 | R/W | 3 | gpio_ren_VC2 | 0 = turn on input pull-up for VC2 pin<br>1 = turn off input pull-up for VC2 pin |
| | 0 | R/W | 2 | gpio_ren_FB2 | 0 = turn on input pull-up for FB2 pin<br>1 = turn off input pull-up for FB2 pin |
| | 0 | R/W | 1 | gpio_ren_FB1 | 0 = turn on input pull-up for FB1 pin<br>1 = turn off input pull-up for FB1 pin |
| | 0 | R/W | 0 | gpio_ren_VC1 | 0 = turn on input pull-up for VC1 pin<br>1 = turn off input pull-up for VC1 pin |

## 4.2. Input Processor

### 4.2.1. Video data/control signal handling

Page 0x01h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 01h | 0 | R/W | 7 | vcnt_rstedge | If xfr_vs_lock = 1'b1, then set Di_xfr_vcnt_rstedge.<br>Vcnt_rst will set at both rising and falling edge of vs input( this is vsyn_I for di_crtc0) |
| | 0 | R/W | 6 | tv_mode | Turn on TV mode |
| | 1 | R/W | 5 | vs_lock | Use external vs(vs_I of crtc0) as v counter reset source |

| | | | | | |
|---|---|---|---|---|---|
| | 1 | R/W | 4 | hs_lock | Use external hs(hs_I of crtc0) as h counter reset source |
| | 1 | R/W | 3 | tg_go | Turn on crtc0 module function to enable timing reference |
| | | | 2 | | Reserved |
| | 0 | R/W | 1 | data_24bit | 0 = 4:2:2 data from video decoder or external<br>1 = 4:4:4 data from video decoder |
| | 0 | R/W | 0 | din_rvs | Reverse input data bit order, i.e. data[7:0] will be data[0:7] |
| 02h | 0 | R/W | 7 | | Reserved |
| | 0 | R/W | 6 | | Reserved |
| | 1 | R/W | 5 | ck1_inv | Set ck1( di output clock) polarity inverse |
| | 0 | R/W | 4 | hsi_pol | Inverse input dinhs polarity |
| | 0 | R/W | 3 | vsi_pol | Inverse input dinvs polarity |
| | 0 | R/W | 2 | dei_pol | Inverse input dinde polarity |
| | 0 | R/W | 1 | fdi_pol | Inverse input dinfd polarity |
| | | R/W | 0 | | Reserved |
| 03h | 1 | R/W | 7 | dt_fd_sel2 | 1= select field from reference timing generator to di_clam<br>0= select field from dt_fd_sel1 |
| | 1 | R/W | 6 | dt_fd_sel1 | 1= select field from BT656 decoder<br>0= select field from external dinfd |
| | 1 | R/W | 5 | dt_de_sel2 | 1=select DE from reference timing generator<br>0= select DE from dt_de_sel1 |
| | 1 | R/W | 4 | dt_de_sel1 | 1= select DE from BT656 decoder<br>0= select DE from external dinde |
| | 1 | R/W | 3 | dt_vs_sel2 | 1= select vsync from reference timing generator<br>0= select vsync from dt_vs_sel1 |
| | 1 | R/W | 2 | dt_vs_sel1 | 1= select vsync from BT656 decoder<br>0= select vsync from VDVS pin |
| | 1 | R/W | 1 | dt_hs_sel2 | 1=select hsync from reference timing generator<br>0= select hsync from dt_hs_sel1 |
| | 1 | R/W | 0 | dt_hs_sel1 | 1= select hsync from BT656 decoder<br>0= select hsync from VDHS pin |
| 04h | 0 | R/W | 7 | res_hs_sel | Hsync source selection for resolution detect<br>1= from BT656 decoder<br>0= from VDHS pin |
| | 0 | R/W | 6 | res_vs_sel | Vsync source selection for resolution detect<br>1= from BT656 decoder<br>0= from VDVS pin |
| | 0 | R/W | 5 | tg_hs_sel | Hsync source selection for reference timing generator<br>1= from BT656 decoder<br>0= from VDHS pin |
| | 0 | R/W | 4 | tg_vs_sel | Vsync source selection for reference timing generator<br>1= from BT656 decoder<br>0= from VDVS pin |
| | 0 | R/W | 3:0 | sync_sel | Sync_sel[3] hcnt_rst sync to vsync_r<br>Sync_sel[2] de for crtc0(detect active region)<br>Sync_sel[1] de for crtc0(detect active region)<br>Sync_sel[0] pcnt_hs sel |
| 05h | 0 | | 7 | | Reserved |
| | 0 | R/W | 6 | average | Pcnt initial number for bt656 decoder |
| | 0 | | 5:2 | | Reserved |
| | 00 | R/W | 1:0 | pcnt_ini | Pcnt initial number for bt656 decoder |
| 06h | | | | | Reserved |
| 07h | | | 7 | | Reserved |

| | | | | | |
|---|---|---|---|---|---|
| | 000 | R/W | 6:4 | pat_sel | Test pattern select of input processor<br>000= bypass data<br>001= black<br>010=: white<br>011= dot pattern (dot → white)<br>100= horizontal strip (gray)<br>101= vertical ramp ( gray )<br>110= horizontal ramp ( gray )<br>111= color bar |
| | | | 3:0 | | Reserved |
| 08h | | | | | Reserved |
| 09h | | | | | Reserved |
| 0Ah | | | | | Reserved |
| 0Bh | 10h | R/W | 7:0 | xfr_mask_y | When mask Y's value |
| 0Ch | 80h | R/W | 7:0 | xfr_mask_cb | When mask Cb's value |
| 0Dh | 80h | R/W | 7:0 | xfr_mask_cr | When mask Cr's value |

### 4.2.2. Reference Timing Generation

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 20h | 00h | R/W | 7:0 | hsstrt[7:0] | After hcnt_rst, hsync will be set after "hsstrt" pixels |
| 21h | 0 | R/W | 3:0 | hsstrt[11:8] | |
| | | | 7:4 | | Reserved |
| 22h | 20h | R/W | 7:0 | hsend[7:0] | After hcnt_rst, hsync will be reset after "hsend" pixels |
| 23h | 0 | R/W | 3:0 | hsend[11:8] | |
| | | | 7:4 | | Reserved |
| 24h | 0 | R/W | 7:0 | vsstrt[7:0] | After vcnt_rst, vsync will be set after "Vsstrt" lines |
| 25h | 0 | R/W | 3:0 | vsstrt[11:8] | |
| | | | 7:4 | | Reserved |
| 26h | 03h | R/W | 7:0 | vsend[7:0] | After vcnt_rst, vsync will be reset after "vsend" lines |
| 27h | 0 | R/W | 3:0 | vsend[11:8] | |
| | | | 7:4 | | Reserved |
| 2Ch | B4h | R/W | 7:0 | htotal[7:0] | Total of pixels per line |
| 2Dh | 06h | R/W | 3:0 | htotal[11:8] | |
| | | | 7:4 | | Reserved |
| 2Eh | 06h | R/W | 7:0 | vtotal[7:0] | Total of lines per frame |
| 2Fh | 01h | R/W | 3:0 | vtotal[11:8] | |
| | | | 7:4 | | Reserved |
| 30h | Dch | R/W | 7:0 | hdisps[7:0] | Data enable start point (H direction) |
| 31h | 00h | R/W | 3:0 | hdisps[11:8] | |
| | | | 7:4 | | Reserved |
| 32h | 7Ch | R/W | 7:0 | hdispe[7:0] | Data enable end point (H direction) |
| 33h | 06h | R/W | 3:0 | hdispe[11:8] | |
| | | | 7:4 | | Reserved |
| 34h | 0Ch | R/W | 7:0 | vdisps[7:0] | Data enable start point (V direction) |
| 35h | 0 | R/W | 3:0 | vdisps[11:8] | |
| | | | 7:4 | | Reserved |
| 36h | FCh | R/W | 7:0 | vdispe[7:0] | Data enable end point (V direction) |
| 37h | 0 | R/W | 3:0 | vdispe[11:8] | |
| | | | 7:4 | | Reserved |
| 38h | FFh | R/W | 7:0 | hmasks[7:0] | Mask region start (H direction) |
| 39h | F | R/W | 3:0 | hmasks[11:8] | |
| | | | 7:4 | | Reserved |
| 3Ah | 0 | R/W | 7:0 | hmaske[7:0] | Mask region end (H direction) |

| | | | | | |
|---|---|---|---|---|---|
| 3Bh | 0 | R/W | 3:0 | hmaske[11:8] | |
| | | | 7:4 | | Reserved |
| 3Ch | FFh | R/W | 7:0 | vmasks[7:0] | Mask region start (V direction) |
| 3Dh | F | R/W | 3:0 | vmasks[11:8] | |
| | | | 7:4 | | Reserved |
| 3Eh | 0 | R/W | 7:0 | vmaske[7:0] | Mask region end (V direction) |
| 3Fh | 0 | R/W | 3:0 | vmaske[11:8] | |
| | | | 7:4 | | Reserved |

### 4.2.3. Resolution Detect

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 40h | 0 | R | 7:0 | hsync_hi[7:0] | Pulse width of hsync, unit = system clock. |
| 41h | 0 | R | 2:0 | hsync_hi[10:8] | |
| | 0 | | 7:3 | | Reserved |
| 42h | 0 | R | 7:0 | hsync_freq[7:0] | Period of Hsync, unit = system clock |
| 43h | 0 | R | 3:0 | hsync_freq[11:8] | |
| | 0 | | 7:4 | | Reserved |
| 44h | 0 | R | 7:0 | vsync_hi[7:0] | Pulse width of Vsync, unit = line. |
| 45h | 0 | R | 2:0 | vsync_hi[10:8] | |
| | 0 | | 7:3 | | Reserved |
| 46h | 0 | R | 7:0 | vsync_freq[7:0] | Period of Vsync, unit = line. |
| 47h | 0 | R | 3:0 | vsync_freq[11:8] | |
| | 0 | | 7:4 | | Reserved |
| 48h | 0 | R | 7:0 | res_vtotal[7:0] | Total of system clock per frame. |
| 49h | 0 | R | 7:0 | res_vtotal[15:8] | |
| 4Ah | 0 | R | 3:0 | res_vtotal[19:16] | |
| | 0 | | 7:4 | | Reserved |
| 4Bh | 0 | | 7:6 | | Reserved |
| | 0 | R | 5 | res_odd_even | Indicate current Field |
| | 0 | R | 4 | res_interlace | 1: interlace<br>0: progressive |
| | 0 | R | 3 | res_vs_neg_pol | 1: vs pol negative<br>0: vs pol positive |
| | 0 | R | 2 | res_hs_neg_pol | 1: hs pol negative<br>0: hs pol positive |
| | 0 | R | 1 | res_vsync_loss | 1: vcnt greater than range<br>0: vcnt within range |
| | 0 | R | 0 | res_hsync_loss | 1: hcnt greater then range<br>0: hcnt within range |
| 4Ch | 0 | R | 7:0 | htotl_rb[7:0] | Total pixels per line. Unit = input clock. |
| 4Dh | 0 | R | 3:0 | htotal_rb[11:8] | |
| | 0 | | 7:4 | | Reserved |

### 4.2.4. Active Region Detect

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 50h | 10h | R/W | 7:0 | r_thres[7:0] | Active region R threshold |
| 51h | 10h | R/W | 7:0 | g_thres[7:0] | Active region G threshold |
| 52h | 10h | R/W | 7:0 | b_thres[7:0] | Active region B threshold |
| 53h | 0 | R/W | 7:0 | h_thres[7:0] | H start of detect region |

| | | | | | |
|---|---|---|---|---|---|
| 54h | 0 | R/W | 7:0 | v_thres[7:0] | V start of detect region |
| 55h | | R | 7:0 | x1min[7:0] | Active region H min |
| 56h | | R | 3:0 | x1min[11:8] | |
| | | | 7:4 | | Reserved |
| 57h | | R | 7:0 | x1max[7:0] | Active region H max |
| 58h | | R | 3:0 | x1max[11:8] | |
| | | | 7:4 | | Reserved |
| 59h | | R | 7:0 | y1min[7:0] | Active region V min |
| 5Ah | | R | 3:0 | y1min[11:8] | |
| | | | 7:4 | | Reserved |
| 5Bh | | R | 7:0 | y1max[7:0] | Active region V max |
| 5Ch | | R | 3:0 | y1max[11:8] | |
| | | | 7:4 | | Reserved |
| 76h | FFh | R/W | 7:0 | hmax_thresh[7:0] | H end of detect region |
| 77h | Fh | R/W | 3:0 | hmax_thresh11:8] | |
| | | | 7:4 | | Reserved |
| 78h | FFh | R/W | 7:0 | vmax_thresh[7:0] | V end of detect region |
| 79h | Fh | R/W | 3:0 | vmax_thresh11:8] | |
| | | | 7:4 | | Reserved |

### 4.2.5. Auto White Balance

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 62h | 0 | R/W | 7:0 | awb_hstr[7:0] | H start point for AWB |
| 63h | 0 | R/W | 2:0 | awb_hstr[10:8] | |
| | 0 | | 7:3 | | Reserved |
| 64h | 0 | R/W | 7:0 | awb_vstr[7:0] | V start line for AWB |
| 65h | 0 | R/W | 2:0 | awb_vstr[10:8] | |
| | 0 | | 7:3 | | Reserved |
| 66h | 0 | R/W | 7:0 | awb_vend[7:0] | V end line for AWB |
| 67h | 0 | R/W | 2:0 | awb_vend[10:8] | |
| | 0 | | 7:3 | | Reserved |
| 70h | 0 | R/W | 7:0 | awb_hend[7:0] | H end point for AWB |
| 71h | 0 | R/W | 2:0 | awb_hend[10:8] | |
| | 0 | | 7:3 | | Reserved |
| 72h | 0 | | 7:6 | | Reserved |
| | 0 | R | 5 | awb_done | AWB done |
| | 0 | R/W | 4 | awb_en | AWB enable |
| | 0 | R/W | 3:2 | awb_data_type | 00 : min value<br>01 : max value<br>1x : capture value (the point at awb_hstr and awb_vstr) |
| | | | 1:0 | | Reserved |
| 73h | 0 | R | 7:0 | awb_data_r | Auto white balance data R |
| 74h | 0 | R | 7:0 | awb_data_g | Auto white balance data G |
| 75h | 0 | R | 7:0 | awb_data_b | Auto white balance data B |

### 4.2.6. Interrupt and region_mode setting

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 80h | 0 | | 7:6 | | Reserved |

| | | | | | |
|---|---|---|---|---|---|
| | 0 | R | 5 | int_flag_vsync | Interrupt flag of Vsync |
| | 0 | R | 4 | int_flag_timing | Interrupt flag of timing change |
| | 0 | R/W | 3 | region_mode | Active region de selector<br>0 : use threshold<br>1 : use active_de(sel from sync_sel[2:1]) |
| | 0 | R/W | 2 | int_v_edge | 0 : interrupt at rising edge of vsync<br>1 : interrupt t of vsync at falling edge of vsync |
| | 0 | R/W | 1 | int_en_vsync | Enable vsync interrupt |
| | 0 | R/W | 0 | int_en_timing | Enable timing interrupt |
| 81h | | R/W | 7:3 | | Reserved |
| | 0 | R/W | 2 | clr_vsync_int | Clear the int from vsync |
| | 0 | R/W | 1 | clr_timing_int | Clear the int from timing change interrupt |
| | 0 | R/W | 0 | clr_extr_vs_flag | Clear the extr vs indicator |
| 82h | 0 | R/W | 7:4 | h_diff | When resolution detect H change value bigger than H_diff will trigger int_flag_timing |
| | 0 | R/W | 3:0 | v_diff | When resolution detect V change value bigger than V_diff will trigger int_flag_timing |

## 4.3. Scaler

### 4.3.1. Scaler control

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 00h | 1 | R/W | 7 | scaler_ctl[7] | Timing repair |
| | 0 | R/W | 6 | scaler_ctl[6] | 1 = left/right mirror<br>0 = normal |
| | 1 | R/W | 5 | scaler_ctl[5] | Enable down scaling |
| | 0 | R/W | 4 | scaler_ctl[4] | Enable bypass pixel when down scaling |
| | 0 | R/W | 3 | scaler_ctl[3] | Enable horizontal non-linear scaling of up scaler |
| | 0 | R/W | 2 | scaler_ctl[2] | Enable horizontal non-linear scaling of down scaler |
| | 0 | R/W | 1 | scaler_ctl[1] | 0: Enable de_interlace start at odd field<br>1: Enable de_interlace start at field |
| | 1 | R/W | 0 | scaler_ctl[0] | Enable de-interlacer |
| 01h | 0 | R/W | 7 | go | Enable CRTC2 |
| | 0 | R/W | 6 | ext_hs | ext_hs_en |
| | 0 | R/W | 5 | ext_vs | ext_vs_en |
| | 1 | R/W | 4 | rev_odd_even | reverse odd/even field |
| | 1 | R/W | 3 | de_ctl | 1: use demo_de<br>0: use org_de |
| | | | 2:0 | | Reserved |
| 02h | | R/W | 7:5 | | Reserved |
| | 0 | R/W | 4 | frame_lock4 | Lock before Vsync |
| | 1 | R/W | 3 | frame_lock3 | Lock after Vsync |
| | 1 | R/W | 2 | frame_lock2 | Eq_htotal lock |
| | 0 | R/W | 1 | frame_lock1 | Frame lock with ext_hs1 |
| | 1 | R/W | 0 | frame_lock0 | Ext_vs1 lock |
| 03h | | | 7:1 | | Reserved |
| | 0 | R/W | 0 | pwr_dn | RAM Power down |

### 4.3.2. Scaling Coefficient

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 04h | 23h | R/W | 7:3 | | Reserved |
| | | | 2:0 | hs_ns_slt | H Non_linear scaling step Size<br>00: 1/32<br>01:1/64<br>02:1/128<br>03:1/256<br>04:1/512<br>05:1/1024<br>06:1/2048<br>07:1/4096 |
| 05h | 08h | R/W | 7:0 | | Reserved |
| 06h | 0 | R/W | 7 | FIX_HDWN_COEF | 0:original c1[23:16]<br>1:fixed c1[31:24] |
| | | R/W | 6:3 | | Reserved |
| | 0 | R/W | 2 | skip_mode | For v down scaler over |
| | 01b | R/W | 1:0 | qubic_ctl | Scaling coefficient select<br>00 : a= -0.2<br>01 : a= -0.6<br>10 : a= -1.0<br>11 : a= -2.0 |
| 07h | | | 7:3 | | Reserved |
| | 16h | R/W | 2:0 | pattern _select | 000: bypass<br>001: user defined color (register 35h, 36h and 37h)<br>010: V gray scale<br>011: H gray scale<br>100: gray bar<br>101: color bar<br>110: dot<br>111: color & gray bar |

### 4.3.3. Offset Settings of Scaler

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 08h | 2Eh | R/W | 7:0 | vs_offset1 [7:0] | Deinterlace odd vsync offset |
| 09h | | R/W | 1:0 | vs_offset1[9:8] | |
| | | | 7:2 | | Reserved |
| 0Ah | 2Eh | R/W | 7:0 | vs_offset2 [7:0] | Deinterlace even vsync offset |
| 0Bh | | R/W | 1:0 | vs_offset2[9:8] | |
| | | | 7:2 | | Reserved |
| 0Ch | 2Eh | R/W | 7:0 | hs_offset1[7:0] | Deinterlace odd Hsync offset |
| 0Dh | | R/W | 1:0 | hs_offset1[9:8] | |
| | | | 7:2 | | Reserved |
| 0Eh | 80h | R/W | 7:0 | hs_offset2 [7:0] | Deinterlace even Hsync offset |
| 0Fh | 10b | R/W | 1:0 | hs_offset2[9:8] | |
| | | | 7:2 | | Reserved |

### 4.3.4. Output Timing Settings of Scaler

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 10h | 00h | R/W | 7:0 | panel_htotal[7:0] | Total pixels per line of panel. |
| 11h | 4h | R/W | 1:0 | panel _htotal[9:8] | |
| | | | 7:2 | | Reserved |
| 12h | 0Ch | R/W | 7:0 | panel_hswdth [7:0] | Hsync pulse width of panel. |

| | | | | | |
|---|---|---|---|---|---|
| 13h | 0h | R/W | 1:0 | panel _hswdth[9:8] | |
| | | | 7:2 | | Reserved |
| 14h | 20h | R/W | 7:0 | panel _hdisps [7:0] | Horizontal display start, for line buffer read. |
| 15h | 0h | R/W | 1:0 | panel _hdisps [9:8] | |
| | | | 7:2 | | Reserved |
| 16h | 40h | R/W | 7:0 | panel _hdispe[7:0] | Horizontal display end, for line buffer read. |
| 17h | 3h | R/W | 1:0 | panel _hdispe [9:8] | |
| | | | 7:2 | | Reserved |
| 18h | 36h | R/W | 7:0 | panel_hwins [7:0] | Horizontal start for demo or pipeline DE |
| 19h | 0h | R/W | 1:0 | panel _hwins [9:8] | |
| | | | 7:2 | | Reserved |
| 1Ah | 56h | R/W | 7:0 | panel _hwine [7:0] | Horizontal end for demo or pipeline DE |
| 1Bh | 3h | R/W | 1:0 | panel _hwine [9:8] | |
| | | | 7:2 | | Reserved |

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 20h | 74h | R/W | 7:0 | panel_vtotal[7:0] | Total lines of Scaler output |
| 21h | 2h | R/W | 1:0 | panel_vtotal[9:8] | |
| | | | 7:2 | | Reserved |
| 22h | 03h | R/W | 7:0 | panel_vswdth [7:0] | Vsync pulse width of Scaler output. |
| 23h | 0h | R/W | 1:0 | panel_vswdth[9:8] | |
| | | | 7:2 | | Reserved |
| 24h | 07h | R/W | 7:0 | panel_vdisps [7:0] | Vertical display start, for line buffer read. |
| 25h | 0h | R/W | 1:0 | panel_vdisps [9:8] | |
| | | | 7:2 | | Reserved |
| 26h | 5Fh | R/W | 7:0 | panel_vdispe[7:0] | Vertical display end, for line buffer read. |
| 27h | 2h | R/W | 1:0 | panel_vdispe [9:8] | |
| | | | 7:2 | | Reserved |
| 28h | 07 | R/W | 7:0 | panel_vwins [7:0] | Vertical start for demo or pipeline DE |
| 29h | 0h | R/W | 1:0 | panel_vwins [9:8] | |
| | | | 7:2 | | Reserved |
| 2Ah | 5Fh | R/W | 7:0 | panel_vwine [7:0] | Vertical end for demo or pipeline DE |
| 2Bh | 2h | R/W | 1:0 | panel_vwine [9:8] | |
| | | | 7:2 | | Reserved |

### 4.3.5. Test Pattern Settings of Scaler

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 30h | 00h | R/W | 7:0 | crtc2_h_size [7:0] | For test pattern<br>Display H size |
| 31h | | R/W | 1:0 | crtc2_h_size [9:8] | |
| | | | 7:2 | | Reserved |
| 32h | 0Ch | R/W | 7:0 | grep_width [7:0] | For test pattern 03: define H grep width |
| 33h | 00h | R/W | 7:0 | pat_v_width [7:0] | For test pattern 07: define color & gray bar V width |
| 34h | | R/W | 1:0 | pat_v_width [9:8] | |
| | | | 7:2 | | Reserved |
| 35h | 03h | R/W | 7:0 | rgb_pattern [7:0] | User defined color for test pattern |
| 36h | 03h | R/W | 7:0 | rgb_pattern [7:0] | User defined color for test pattern |
| 37h | 03h | R/W | 7:0 | rgb_pattern [7:0] | User defined color for test pattern |

### 4.3.6. Scaling Ratio

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 40h | 99h | R/W | 7:0 | h_ratio [7:0] | Horizontal scaling ratio. |
| 41h | 39h | R/W | 6:0 | h_ratio [14:8] | |
| | | | 7 | | Reserved |
| 42h | 33h | R/W | 7:0 | v_ratio [7:0] | Vertical scaling ratio. |
| 43h | 03h | R/W | 6:0 | v_ratio [14:8] | |
| | | | 7 | | Reserved |
| 44h | | R/W | 7:0 | dh_ratio [7:0] | Horizontal down scaling ratio. |
| 45h | | R/W | 6:0 | dh_ratio [14:8] | |
| | | | 7 | | Reserved |
| 46h | | R/W | 7:0 | dh_x_ratio [7:0] | |
| 47h | | R/W | 7:0 | dh_x_ratio [15:8] | |

Up scaling ratio setting:

$$h\_ratio = \frac{H\_size_{input}}{H\_size_{panel}} \times 16384$$

$$v\_ratio = \frac{V\_size_{input}}{V\_size_{panel}} \times 16384$$

Down scaling ratio setting:

$$dh\_ratio = \frac{H\_size_{panel}}{H\_size_{input}} \times 16384$$

$$dh\_x\_ratio = \frac{H\_size_{input}}{H\_size_{panel}} \times 16384$$

Panel clock calculation :

$$f_{panel\_clk} = \frac{H\_total_{panel} * V\_size_{panel}}{H\_total_{input} * V\_size_{input}} * f_{input\_clk}$$

Voffset = ((PANEL_VSIZE/VI_ACTIVE)*(VI_DISP_STRT-VI_SYNC_STRT+Line_offset))-(PANEL_VSTART-1)

Hoffset = (voffset-VOFFSET)*PANEL_HTOTAL;

### 4.3.7. Scaler

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 48h | 07h | R/W | 7:0 | non _hstrt [7:0] | Non_linear H scaler start |
| 49h | 0 | R/W | 2:0 | non _hstrt [9:8] | |
| | | | 7:3 | | Reserved |
| 4Ah | 07h | R/W | 7:0 | non _hend [7:0] | Non_linear H scaler end |

| | | | | | |
|---|---|---|---|---|---|
| 4Bh | 0 | R/W | 2:0 | non _hend [9:8] | |
| | | | 7:3 | | Reserved |
| 50h | | R | 7:6 | overlap | The data must be 10 |
| | | R | 5:4 | even_overlap | The data must be 00 |
| | | R | 3:2 | odd_overlap | The data must be 00 |
| | | R | 1:0 | overlap | The data must be 00 |

## 4.4. Luminance and Chrominance Adjustment

### 4.4.1. Black/White Stretch

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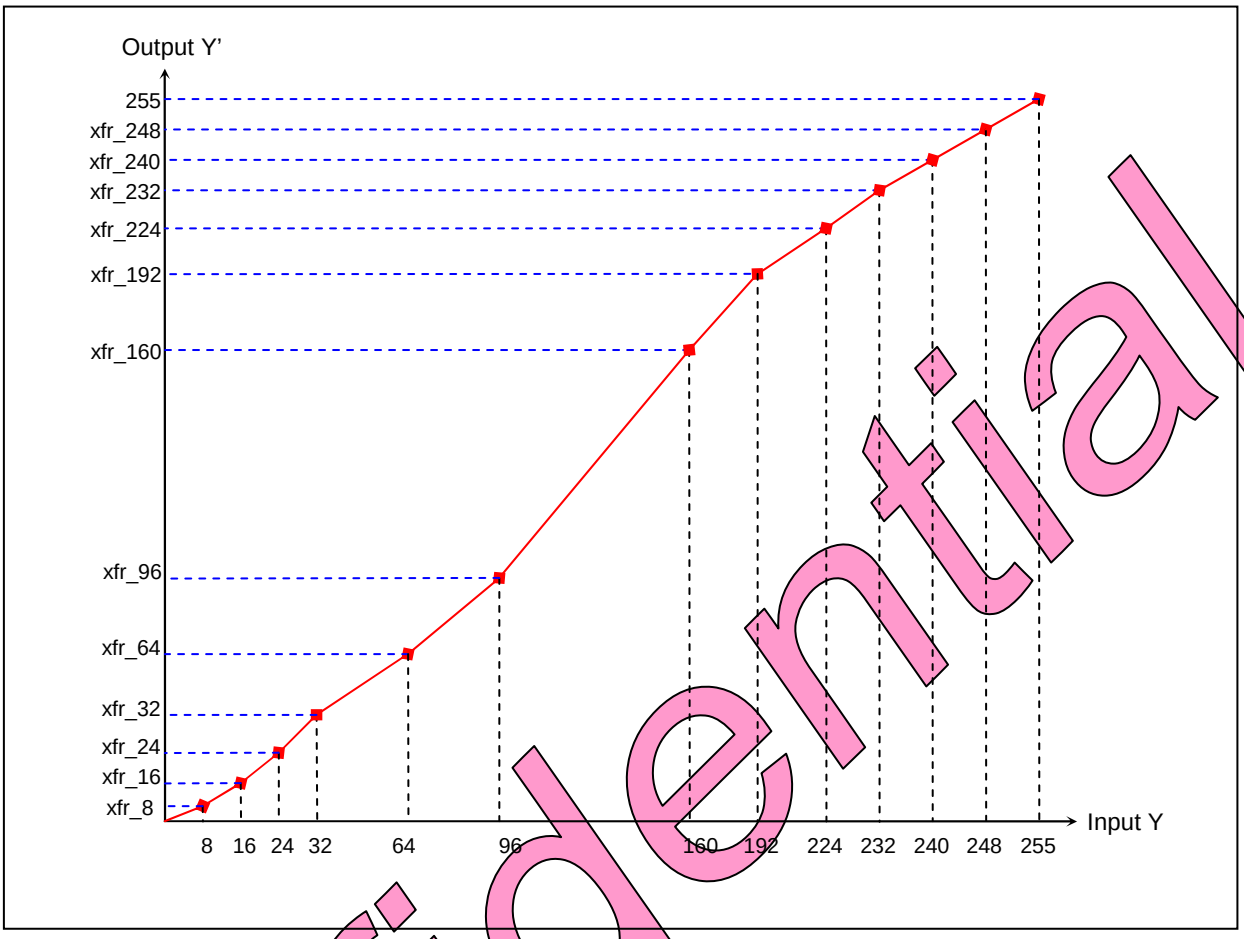
| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 00h | 00 | | 7:6 | | Reserved |
| | 0 | R/W | 0 | bw_en | Black/white stretch enable |
| 01h | 08h | R/W | 7:0 | xfr_8 | The luminance value after BW_strech when y input = 8 |
| 02h | 10h | R/W | 7:0 | xfr_16 | The luminance value after BW_strech when y input = 16 |
| 03h | 18h | R/W | 7:0 | xfr_24 | The luminance value after BW_strech when y input = 24 |
| 04h | 20h | R/W | 7:0 | xfr_32 | The luminance value after BW_strech when y input = 32 |
| 05h | 40h | R/W | 7:0 | xfr_64 | The luminance value after BW_strech when y input = 64 |
| 06h | 60h | R/W | 7:0 | xfr_96 | The luminance value after BW_strech when y input = 96 |
| 07h | A0h | R/W | 7:0 | xfr_160 | The luminance value after BW_strech when y input = 160 |
| 08h | C0h | R/W | 7:0 | xfr_192 | The luminance value after BW_strech when y input = 192 |
| 09h | E0h | R/W | 7:0 | xfr_224 | The luminance value after BW_strech when y input = 224 |
| 0Ah | E8h | R/W | 7:0 | xfr_232 | The luminance value after BW_strech when y input = 232 |
| 0Bh | F0h | R/W | 7:0 | xfr_240 | The luminance value after BW_strech when y input = 240 |
| 0Ch | F8h | R/W | 7:0 | xfr_248 | The luminance value after BW_strech when y input = 248 |

Note : must follow the rule below
xfr_248 ≥ xfr_240 ≥ xfr_232 ≥ xfr_224 ≥ xfr_192 ≥ xfr_160 ≥ xfr_96 ≥ xfr_64 ≥xfr_32 ≥ xfr_24 ≥ xfr_16 ≥ xfr_8






### 4.4.2. Brightness

Page 0x0A

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 60h | 0 | R/W | 7 | britnis_signed | Signed bit of brightness<br>0 = add<br>1 = subtract |
| | 00h | R/W | 6:0 | britnis_offset | Brightness value +/- (britnis_offset * 2) |

To bypass brightness, set this register to 00h.

### 4.4.3. Sharpness

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 10h | | | 7:5 | | Reserved |
| | 0 | R/W | 4 | div_4 | 1 = divide sharp_ratio by 4<br>0 = no operation |
| | 0 | R/W | 3 | div_8 | 1 = divide sharp_ratio by 8<br>0 = no operation |
| | 0 | R/W | 2 | div_16 | 1 = divide sharp_ratio by 16<br>0 = no operation |
| | 0 | R/W | 1 | overshoot_en | 0 = bypass overshoot point<br>1 = reduce overshoot sharpness ratio according to div_4, div_8 and div_16 settings |

| | | | | | |
|---|---|---|---|---|---|
| | 0 | R/W | 0 | sharp_en | 0 = Disable Sharpness<br>1 = Enable Sharpness |
| 11h | 00h | R/W | 7:0 | sharp_ratio | Sharpness Ratio |
| 12h | 00h | R/W | 7:0 | shrp_noise_thresh | Noise detected threshold<br>00h : disable noise detection<br>others : value of noise threshold |

### 4.4.4. Hue

Page 0x0Ah

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 20h | 00h | R/W | 7:0 | c0x[7:0] | hue **cosθ** coefficient.<br>c0x[11]: sign<br>c0x[10]: integer<br>c0x[9:0]: fraction |
| 21h | 4h | R/W | 3:0 | c0x[11:8] | |
| | | | 7:4 | | Reserved |
| 22h | 00h | R/W | 7:0 | c1x[7:0] | hue **sinθ** coefficient.<br>c1x[11]: sign<br>c1x[10]: integer<br>c1x[9:0]: fraction |
| 23h | 0h | R/W | 3:0 | c1x[11:8] | |
| | | | 7:4 | | Reserved |
| 24h | 00h | R/W | 7 | hue_en | hue enable |
| | | | 6:0 | | Reserved |

Degree Setting Table

| degree | cosθ | sinθ | degree | cosθ | sinθ |
|---|---|---|---|---|---|
| 0˚ | 400h | 000h | -0˚ | 400h | 000h |
| 1˚ | 400h | 012h | -1˚ | 400h | feeh |
| 2˚ | 3ffh | 024h | -2˚ | 3ffh | fdch |
| 3˚ | 3ffh | 036h | -3˚ | 3ffh | fcah |
| 4˚ | 3fdh | 047h | -4˚ | 3fdh | fb9h |
| 5˚ | 3fch | 059h | -5˚ | 3fch | fa7h |
| 6˚ | 3fah | 06bh | -6˚ | 3fah | f95h |
| 7˚ | 3f8h | 07dh | -7˚ | 3f8h | f83h |
| 8˚ | 3f6h | 08fh | -8˚ | 3f6h | f71h |
| 9˚ | 3f3h | 0a0h | -9˚ | 3f3h | f60h |
| 10˚ | 3f0h | 0b2h | -10˚ | 3f0h | f4eh |
| 11˚ | 3edh | 0c3h | -11˚ | 3edh | f3dh |
| 12˚ | 3eah | 0d5h | -12˚ | 3eah | f2bh |
| 13˚ | 3e6h | 0e6h | -13˚ | 3e6h | f1ah |
| 14˚ | 3e2h | 0f8h | -14˚ | 3e2h | f08h |
| 15˚ | 3ddh | 109h | -15˚ | 3ddh | ef7h |

### 4.4.5. Saturation

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 25h | 20h | | 7:6 | | Reserved |
| | | R/W | 5:0 | sat_coef[5:0] | saturation coefficient<br>sat_coef[5]: integer<br>sat_coef[4:0]: fraction |
| 26h | 0 | R/W | 7 | sat_en | 1= saturation enable<br>0= saturation disable |
| | | | 6:0 | | Reserved |

Magnitude Setting Table

| coeff. | value | coeff. | value |
|---|---|---|---|
| 1.0 | 20h | 1.5 | 30h |
| 1.1 | 23h | 1.6 | 33h |
| 1.2 | 26h | 1.7 | 36h |
| 1.3 | 2ah | 1.8 | 3ah |
| 1.4 | 2dh | 1.9 | 3dh |

### 4.4.6. Color Space Conversion

Page 0x0Ah

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 50h | 0 | R/W | 7 | cscb_en | 1: Enable color space conversion<br>0: Bypass color space conversion |
| | | | 6:1 | | Reserved |
| | 0 | R/W | 0 | hdtv_sel | 1: HDTV conversion (BT.709)<br>0: SDTV conversion (BT.601) |
| 51h | 0 | R/W | 7:4 | | Reserved |
| | | | 3:0 | bca_demo_en | demo enable:<br>bit-3: black/white stretch<br>bit-2: sharpness<br>bit-1: hue<br>bit-0: saturation |
| 52h | 0 | R/W | 7:0 | bca_demo_st[7:0] | BCA demo start, count from HS, it is 16 times of pixel count |
| 53h | 1Dh | R/W | 7:0 | bca_demo_sp[7:0] | BCA demo stop, count from HS, it is 16 times of pixel count |

## 4.5. OSD

### 4.5.1. OSD Display window 0

Page 0x0Ch

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 00h | 00h | R/W | 7:0 | osd0_hs[7:0] | OSD window0 Horizontal Start position |
| 01h | 00h | R/W | 2:0 | osd0_hs[10:8] | |
| 02h | 00h | R/W | 7:0 | osd0_vs[7:0] | OSD window0 Vertical Start position |
| 03h | 00H | R/W | 1:0 | osd0_vs[9:8] | |
| 04h | 00H | R/W | 5:0 | osd0_r_no[5:0] | OSD window0 Row numbers |
| 05h | 00H | R/W | 6:0 | osd0_c_no[6:0] | OSD window0 Character numbers each row |
| 06h | 0 | R/W | 7 | osd0_en | OSD window0 display enable |
| | 0 | R/W | 6 | osd0_fd | OSD window0 fade in/out function enable |
| | 0 | R/W | 5:4 | osd0_alpha[1:0] | OSD window0 display alpha blending<br>00= OSD only<br>01= OSD 3/4<br>10= OSD 2/4<br>11= OSD 1/4 |
| | 0 | R/W | 3:2 | osd0_hx[1:0] | OSD window0 character high magnify<br>00= 1X(18 scan lines)<br>01= 2X(36 scan lines)<br>10= 3X(54 scan lines)<br>11= 4X(72 scan lines) |
| | 0 | | 1:0 | osd0_wx[1:0] | OSD window0 character width magnify<br>00= 1X(12 pixels)<br>01= 2X(24 pixels)<br>10= 3X(36 pixels)<br>11= 4X(48 pixels) |

### 4.5.2. OSD Display window 1

Page 0x0Ch

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 08h | 00h | R/W | 7:0 | osd1_hs[7:0] | OSD window1 Horizontal Start position |
| 09h | 00h | R/W | 2:0 | osd1_hs[10:8] | |
| 0Ah | 00h | R/W | 7:0 | osd1_vs[7:0] | OSD window1 Vertical Start position |
| 0Bh | 00h | R/W | 1:0 | osd1_vs[9:8] | |
| 0Ch | 00h | R/W | 5:0 | osd1_r_no[5:0] | OSD window1 Row numbers |
| 0Dh | 00h | R/W | 6:0 | osd1_c_no[6:0] | OSD window1 Character numbers each row |
| 0Eh | 0 | R/W | 7 | osd1_en | OSD window1 display enable |
| | 0 | R/W | 6 | osd1_fd | OSD window1 fade in/out function enable |
| | 0 | R/W | 5:4 | osd1_alpha[1:0] | OSD window1 display alpha blending<br>00= OSD only<br>01= OSD 3/4<br>10= OSD 2/4<br>11= OSD 1/4 |
| | 0 | R/W | 3:2 | osd1_hx[1:0] | OSD window1 character high magnify<br>00= 1X(18 scan lines)<br>01= 2X(36 scan lines)<br>10= 3X(54 scan lines)<br>11= 4X(72 scan lines) |
| | 0 | R/W | 1:0 | osd1_wx[1:0] | OSD window1 character width magnify<br>00= 1X(12 pixels)<br>01= 2X(24 pixels)<br>10= 3X(36 pixels)<br>11= 4X(48 pixels) |

### 4.5.3. OSD Fade in/out

Page 0x0Ch

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 0Fh | 00h | R/W | 0 | LD_osd_de | Load OSD DE counter to start fade in/out function (0→1) |
| 10h | 00h | R/W | 7:0 | osd_de_hs[7:0] | OSD DataMaskEnable Horizontal Start position |
| 11h | 00h | R/W | 2:0 | osd_de_hs[10:8] | |
| 12h | 00h | R/W | 7:0 | osd_de_vs[7:0] | OSD DataMaskEnable Vertical Start position |
| 13h | 00h | R/W | 1:0 | osd_de_vs[9:8] | |
| 14h | 00h | R/W | 7:0 | osd_de_he[7:0] | OSD DataMaskEnable Horizontal End position |
| 15h | 00h | R/W | 2:0 | osd_de_he[10:8] | |
| 16h | 00h | R/W | 7:0 | osd_de_ve[7:0] | OSD DataMaskEnable Vertical End position |
| 17h | 00h | R/W | 1:0 | osd_de_ve[9:8] | |
| 18h | 0 | R/W | 7 | inc_hs | 1 = osd_de_hs add cnt_hs per frame<br>0 = osd_de_hs subtract cnt_hs per frame |
| | 00h | R/W | 6:0 | cnt_hs[6:0] | OSD DataMaskEnable Horizontal Start counter |
| 19h | 0 | R/W | 7 | inc_vs | 1 = osd_de_vs add cnt_vs per frame<br>0 = osd_de_vs subtract cnt_vs per frame |
| | 00h | R/W | 6:0 | cnt_vs[6:0] | OSD DataMaskEnable Vertical Start counter |
| 1Ah | 0 | R/W | 7 | inc_he | 1 = osd_de_he add cnt_he per frame<br>0 = osd_de_he subtract cnt_he per frame |
| | 00h | R/W | 6:0 | cnt_he[6:0] | OSD DataMaskEnable Horizontal End counter |
| 1Bh | 0 | R/W | 7 | inc_ve | 1 = osd_de_ve add cnt_ve per frame<br>0 = osd_de_ve subtract cnt_ve perh frame |
| | 00h | R/W | 6:0 | cnt_ve[6:0] | OSD DataMaskEnable Vertical End counter |

### 4.5.4. OSD Blinking

Page 0x0Ch

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 1Ch | 0h | R/W | 7:4 | BP[3:0] | Blinking period (Unit : frame)<br>BP[3] = 1 : 128 frames<br>BP[2] = 1 : 64 frames<br>BP[1] = 1 : 32 frames<br>BP[0] = 1 : 16 frames |
| | 0h | R/W | 3:0 | BD[3:0] | Blinking ON duty<br>BD[3] = 1 : 1/2 blinking period<br>BD[2] = 1 : 1/4 blinking period<br>BD[1] = 1 : 1/8 blinking period<br>BD[0] = 1 : 1/16 blinking period |

### 4.5.5. OSD RAM/ROM control

Page 0x0Ch

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 1Dh | 0 | R/W | 7 | rom_bank | Font ROM bank select |
| | 0 | R/W | 6 | udf_ram_clr | Clear UDF RAM, active high |
| | 0 | R/W | 5 | dsp_ram_clr | Clear DSP RAM, active high |
| | 0 | R/W | 4 | clut_ram_clr | Clear CLUT RAM, active high |
| | 0 | R/W | 3 | rom_pd | Font ROM power down, active high |
| | 0 | R/W | 2 | udf_ram _pd | UDF RAM power down, active high |
| | 0 | R/W | 1 | dsp_ram _pd | DSP RAM power down, active high |
| | 0 | R/W | 0 | clut_ram _pd | CLUT RAM power down, active high |

### 4.5.6. OSD Display Window Index

Page 0x0Ch

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 20h | 00h | R/W | 7:0 | dsp0_inx[7:0] | Display Window0 Index Address |
| 21h | 00h | R/W | 0 | dsp0_inx[8] | |
| 22h | 00h | R/W | 7:0 | dsp1_inx[7:0] | Display Window1 Index Address |
| 23h | 00h | R/W | 0 | dsp1_inx[8] | |

### 4.5.7. User-defined Font Index

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 24h | 00h | R/W | 7:0 | udf1_inx[7:0] | User define 1-bit color font Index Address |
| 25h | 00h | R/W | 2:0 | udf1_inx[10:8] | |
| 26h | 00h | R/W | 7:0 | udf2_inx[7:0] | User define 2-bit color font Index Address |
| 27h | 00h | R/W | 2:0 | udf2_inx[10:8] | |

### 4.5.8. OSD Shadow/Border

Page 0x0Ch

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 28h | 00h | R/W | 7 | char_tran_en | 1= Enable character transparent |
| | | R/W | 6 | char _bbr_md | 1= Shadow mode<br>0= Border mode |
| | | R/W | 5:0 | char _bdr_bg[5:0] | OSD ROM font character border's color |
| 29h | | | 7:5 | | Reserved |

| | | | | | |
|---|---|---|---|---|---|
| | | R/W | 4 | osd0_ bdr _md | OSD display window0 border mode; “0” Border, “1” Shadow |
| | 00h | R/W | 3:0 | osd0_ bdr _w[3:0] | OSD display window0 border width; “0000” disable |
| 2Ah | | | 7:6 | | Reserved |
| | 00h | R/W | 5:0 | osd0_ bdr _bg[5:0] | OSD display window0 border’s color |
| 2Bh | | | 7:5 | | Reserved |
| | 0 | R/W | 4 | osd1_ bdr _md | OSD display window1 border mode; “0” Border, “1” Shadow |
| | 0 | R/W | 3:0 | osd1_ bdr _w[3:0] | OSD display window1 border width; “0000” disable |
| 2Ch | | | 7:6 | | Reserved |
| | 00h | R/W | 5:0 | osd1_ bdr _bg[5:0] | OSD display window1 border’s color |

### 4.5.9. External OSD

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 2Dh | | | 7 | | Reserved |
| | 0 | R/W | 6 | ext_osd_en | 1= enable external OSD |
| | 0 | R/W | 5 | ext_osd_sel | 0= external OSD is from VD[6:0] |
| | 0 | R/W | 4 | ext_osd _int | Enable external OSD intensity input |
| | 0 | R/W | 3 | fast_bnk_pol | polarity of Fast blanking |
| | 0 | R/W | 2 | int_ pol | polarity of Intensity |
| | 0 | R/W | 1 | hv_ pol | polarity of H/V sync output |
| | 0 | R/W | 0 | clk_ pol | polarity of PCK output |

### 4.5.10. OSD Background Window

OSD Background Window
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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 30h | 00h | R/W | 7:0 | osd_win0_hs[7:0] | OSD Background window Horizontal Start position |
| 31h | 0 | R/W | 2:0 | osd_win0_hs[10:8] | |
| | | | 7:3 | | Reserved |
| 32h | 00h | R/W | 7:0 | osd_win0_vs[7:0] | OSD Background window Vertical Start position |
| 33h | 00h | R/W | 1:0 | osd_win0_vs[9:8] | |
| | | | 7:2 | | Reserved |
| 34h | 00h | R/W | 7:0 | osd_win0_he[7:0] | OSD Background window Horizontal End position |
| 35h | 0 | R/W | 2:0 | osd_win0_he[10:8] | |
| | | | 7:3 | | Reserved |
| 36h | 00h | R/W | 7:0 | osd_win0_ve[7:0] | OSD Background window Vertical End position |
| 37h | 0 | R/W | 1:0 | osd_win0_ve[9:8] | |
| | | | 7:2 | | Reserved |
| 38h | 0 | R/W | 7 | osd_win0_tran | Background window transparent when character BG is transparent |
| | 0 | R/W | 6 | osd_win0_ en | Enable Background window |
| | 0 | R/W | 5:0 | osd_win0_bg[5:0] | Background window color index<br>R[7:0] = { bit[5:4], bit[5:4], bit[5:4], bit[5:4] }<br>G[7:0] = { bit[3:2], bit[3:2], bit[3:2], bit[3:2] }<br>B[7:0] = { bit[1:0], bit[1:0], bit[1:0], bit[1:0] } |

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 3Ah | 00h | R/W | 7:0 | osd0_bg_r[7:0] | OSD display window0 background color R setting. |
| 3Bh | 00h | R/W | 7:0 | osd0_bg_g[7:0] | OSD display window0 background color G setting. |
| 3Ch | 00h | R/W | 7:0 | osd0_bg_b[7:0] | OSD display window0 background color B setting. |
| 3Dh | 00h | R/W | 7:0 | osd1_bg_r[7:0] | OSD display window1 background color R setting. |

| | | | | | |
|---|---|---|---|---|---|
| 3Eh | 00h | R/W | 7:0 | osd1_bg_g[7:0] | OSD display window1 background color G setting. |
| 3Fh | 00h | R/W | 7:0 | osd1_bg_b[7:0] | OSD display window1 background color B setting. |

bit[7] : 1 = Enable OSD display window background gradual color
bit[6] : 1= decrement color, 0= increment color
bit[5:4] :
00 = no inc./dec.
01 = inc/dec “2” every character
10 = inc/dec “4” every character
11 = inc/dec “6” every character
bit[3:0] : OSD display window background initial color
display window background color initial value = { bit[3], bit[3], bit[2], bit[2], bit[1], bit[1], bit[0], bit[0] }

## 4.6. TCON

Universal Type TCON setting

### 4.6.1. Universal Type TCON Settings

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 00h | 00h | R/W | 7:0 | tconA _hs[7:0] | TCONA Horizontal output star position |
| 01h | 00h | R/W | 2:0 | tconA _hs[10:8] | |
| | | | 7:3 | | Reserved |
| 02h | 00h | R/W | 7:0 | tconA_hw[7:0] | TCONA Horizontal output width |
| 03h | 00h | R/W | 2:0 | tconA_hw[10:8] | |
| | | | 7:3 | | Reserved |
| 04h | 00h | R/W | 7:0 | tconA_vs[7:0] | TCONA Vertical output star position |
| 05h | 00h | R/W | 1:0 | tconA_vs[9:8] | |
| | | | 7:2 | | Reserved |
| 06h | 00h | R/W | 7:0 | tconA_vw[7:0] | TCONA Vertical output width* |
| 07h | 0 | R/W | 7 | tconA_ctl[7] | “0” toggle follow active<br>“1” toggle follow vcnt bit0 |
| | 0 | R/W | 6 | tconA_ ctl[6] | “0” Reset toggle at Vsync falling edge<br>“1” Reset toggle at Vsync rising edge |
| | 0 | R/W | 5 | tconA_ ctl[5] | 0: Enable vertical component<br>1: Disable vertical component |
| | 0 | R/W | 4 | tconA_ ctl[4] | 0: Enable horizontal component<br>1: Disable horizontal component |
| | 0 | R/W | 3:2 | tconA_ ctl [3:2] | 11: TCONA, 1’b0 alternation each frame<br>10: TCONA ***OR*** 1’b0<br>01: TCONA ***AND*** 1’b0<br>00: TCONA |
| | 0 | R/W | 1 | tconA_ ctl[1] | 0: Output toggle disable<br>1: Output toggle enable |
| | 0 | R/W | 0 | tconA_ ctl[0] | 0: Output negative polarity<br>1: Output positive polarity |

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 08h | 00h | R/W | 7:0 | tconB _hs[7:0] | TCONB Horizontal output star position |
| 09h | 00h | R/W | 2:0 | tconB _hs[10:8] | |
| | | | 7:3 | | Reserved |
| 0Ah | 00h | R/W | 7:0 | tconB_hw[7:0] | TCONB Horizontal output width |
| 0Bh | 00h | R/W | 2:0 | tconB_hw[10:8] | |
| | | | 7:3 | | Reserved |
| 0Ch | 00h | R/W | 7:0 | tconB_vs[7:0] | TCONB Vertical output star position |
| 0Dh | 00h | R/W | 1:0 | tconB_vs[9:8] | |
| | | | 7:2 | | Reserved |
| 0Eh | 00h | R/W | 7:0 | tconB_vw[7:0] | TCONB Vertical output width* |
| 0Fh | 0 | R/W | 7 | tconB_ctl[7] | "0" toggle follow active<br>"1" toggle follow vcnt bit0 |
| | 0 | R/W | 6 | tconB_ ctl[6] | "0" Reset toggle at Vsync falling edge<br>"1" Reset toggle at Vsync rising edge |
| | 0 | R/W | 5 | tconB_ ctl[5] | 0: Enable vertical component<br>1: Disable vertical component |
| | 0 | R/W | 4 | tconB_ ctl[4] | 0: Enable horizontal component<br>1: Disable horizontal component |
| | 0 | R/W | 3:2 | tconB_ ctl [3:2] | 11: TCONB, TCONA alternation each fram<br>10: TCONB ***OR*** TCONA<br>01: TCONB ***AND*** TCONA<br>00: TCONB |
| | 0 | R/W | 1 | tconB_ ctl[1] | 0: Output toggle disable<br>1: Output toggle enable |
| | 0 | R/W | 0 | tconB_ ctl[0] | 0: Output negative polarity<br>1: Output positive polarity |

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 10h | 00h | R/W | 7:0 | tconC _hs[7:0] | TCONC Horizontal output star position |
| 11h | 00h | R/W | 2:0 | tconC _hs[10:8] | |
| | | | 7:3 | | Reserved |
| 12h | 00h | R/W | 7:0 | tconC_hw[7:0] | TCONC Horizontal output width |
| 13h | 00h | R/W | 2:0 | tconC_hw[10:8] | |
| | | | 7:3 | | Reserved |
| 14h | 00h | R/W | 7:0 | tconC_vs[7:0] | TCONC Vertical output star position |
| 15h | 00h | R/W | 1:0 | tconC_vs[9:8] | |
| | | | 7:2 | | Reserved |
| 16h | 00h | R/W | 7:0 | tconC_vw[7:0] | TCONC Vertical output width* |
| 17h | 0 | R/W | 7 | tconC_ctl[7] | "0" toggle follow active<br>"1" toggle follow vcnt bit0 |
| | 0 | R/W | 6 | tconC_ ctl[6] | "0" Reset toggle at Vsync falling edge<br>"1" Reset toggle at Vsync rising edge |
| | 0 | R/W | 5 | tconC_ ctl[5] | 0: Enable vertical component<br>1: Disable vertical component |
| | 0 | R/W | 4 | tconC_ ctl[4] | 0: Enable horizontal component<br>1: Disable horizontal component |

| | | | | | |
|---|---|---|---|---|---|
| | 0 | R/W | 3:2 | tconC_ ctl [3:2] | 11: TCONC, TCONB alternation each fram<br>10: TCONC ***OR*** TCONB<br>01: TCONC ***AND*** TCONB<br>00: TCONC |
| | 0 | R/W | 1 | tconC_ ctl[1] | 0: Output toggle disable<br>1: Output toggle enable |
| | 0 | R/W | 0 | tconC_ ctl[0] | 0: Output negative polarity<br>1: Output positive polarity |

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 18h | 00h | R/W | 7:0 | tconD _hs[7:0] | TCOND Horizontal output star position |
| 19h | 00h | R/W | 2:0 | tconD _hs[10:8] | |
| | | | 7:3 | | Reserved |
| 1Ah | 00h | R/W | 7:0 | tconD_hw[7:0] | TCOND Horizontal output width |
| 1Bh | 00h | R/W | 2:0 | tconD_hw[10:8] | |
| | | | 7:3 | | Reserved |
| 1Ch | 00h | R/W | 7:0 | tconD_vs[7:0] | TCOND Vertical output star position |
| 1Dh | 00h | R/W | 1:0 | tconD_vs[9:8] | |
| | | | 7:2 | | Reserved |
| 1Eh | 00h | R/W | 7:0 | tconD_vw[7:0] | TCOND Vertical output width* |
| 1Fh | 0 | R/W | 7 | tconD_ctl[7] | "0" toggle follow active<br>"1" toggle follow vcnt bit0 |
| | 0 | R/W | 6 | tconD_ ctl[6] | "0" Reset toggle at Vsync falling edge<br>"1" Reset toggle at Vsync rising edge |
| | 0 | R/W | 5 | tconD_ ctl[5] | 0: Enable vertical component<br>1: Disable vertical component |
| | 0 | R/W | 4 | tconD_ ctl[4] | 0: Enable horizontal component<br>1: Disable horizontal component |
| | 0 | R/W | 3:2 | tconD_ ctl [3:2] | 11: TCOND, TCONC alternation each fram<br>10: TCOND ***OR*** TCONC<br>01: TCOND ***AND*** TCONC<br>00: TCOND |
| | 0 | R/W | 1 | tconD_ ctl[1] | 0: Output toggle disable<br>1: Output toggle enable |
| | 0 | R/W | 0 | tconD_ ctl[0] | 0: Output negative polarity<br>1: Output positive polarity |

### 4.6.2. Specific Type TCON Settings

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 20h | 00h | R/W | 7:0 | STH_hs[7:0] | STH Horizontal output start position |
| 21h | 00h | R/W | 2:0 | STH_hs[10:8] | |
| | | | 7:3 | | Reserved |
| 22h | 00h | R/W | 7:0 | STH_hw[7:0] | STH Horizontal output width |
| 23h | 00h | R/W | 7:0 | OEH_hs[7:0] | OEH Horizontal output start position** |
| 24h | 00h | R/W | 7:0 | OEH_hw[7:0] | OEH Horizontal output width |
| 25h | 00h | R/W | 7:0 | OEV_hs[7:0] | OEV Horizontal output start position |

| | | | | | |
|---|---|---|---|---|---|
| 26h | 00h | R/W | 7:0 | OEV_hw[7:0] | OEV Horizontal output width |
| 27h | 00h | R/W | 7:0 | CKV_hs[7:0] | CKV Horizontal output start position |
| 28h | 00h | R/W | 7:0 | CKV_hw[7:0] | CKV Horizontal output width |
| 29h | 00h | R/W | 2:0 | CKV_hw[10:8] | |
| | | | 7:3 | | Reserved |
| 2Ah | 00h | R/W | 7:0 | STV_vs[7:0] | STV Vertical output start position*** |
| 2Bh | 00h | R/W | 7 | Q1H_polarity | Q1 initial polarity |
| | | R/W | 6:0 | Q1H_hs[6:0] | Q1(VCOM digital output) Horizontal output start position**** |
| 2Ch | | | 7:3 | | Reserved |
| | 0 | R/W | 2 | vS_edge_Sel | 0 = Reset Q1H at Vsync falling edge<br>1 = Reset Q1H at Vsync rising edge |
| | 0 | R/W | 1:0 | Q1H_rft_sel | 00 = Q1H_RFT same as Q1H<br>01 = Q1H_RFT same as Q1H<br>10 = Q1H_RFT same as TCONB<br>11 = Q1H_RFT same as TCOND |

### 4.6.3. Specific Type TCON Output Selection

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 30h | 0 | R/W | 3:0 | tcon0_sel[3:0] | 0000= Low;<br>0001= STH;<br>0010= OEH;<br>0011= OEV;<br>0100= CKV;<br>0101= STV;<br>0110= Q1H;<br>0111= TCONA;<br>1000= TCONB;<br>1001= TCONC;<br>1010= TCOND;<br>1011= invert TCONA;<br>1100= invert TCONB;<br>1101= invert TCONC;<br>1110= invert TCOND;<br>1111= High; |
| | 0 | R/W | 7:4 | tcon1_sel[3:0] | |
| 31h | 0 | R/W | 3:0 | tcon2_sel[3:0] | |
| | 0 | R/W | 7:4 | tcon3_sel[3:0] | |
| 32h | 0 | R/W | 3:0 | tcon4_sel[3:0] | |
| | 0 | R/W | 7:4 | tcon5_sel[3:0] | |
| 33h | 0 | R/W | 3:0 | tcon6_sel[3:0] | |
| | 0 | R/W | 7:4 | tcon7_sel[3:0] | |
| 34h | 0 | R/W | 3:0 | tcon8_sel[3:0] | |
| | 0 | R/W | 7:4 | tcon9_sel[3:0] | |
| 35h | 0 | R/W | 3:0 | tcon10_sel[3:0] | |
| | 0 | R/W | 7:4 | tcon11_sel[3:0] | |

## 4.7. DAC

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 00h | 1 | R/W | 7 | dac_pd | DAC power down control.<br>0 = normal<br>1 = power down |
| | | | 6:0 | | Reserved |
| | | | 7:5 | | Reserved |
| | 1 | R/W | 4 | dac_bsel | DAC bias current selection |
| 01h | 0011 | R/W | 3:0 | dac_isel[3:0] | Output driving current selection.<br>0000 : minimum current<br>:<br>1111 : maximum current |
| 02h | | | 7:4 | | Reserved |

| | | | | | |
|---|---|---|---|---|---|
| | 0h | R/W | 3:0 | dac_dr[3:0] | R-channel clock delay select<br>0000 = minimum delay<br>:<br>1111 = maximum delay |
| 03h | | | 7:4 | | Reserved |
| | 0h | R/W | 3:0 | dac_dg[3:0] | G-channel clock delay select |
| 04h | | | 7:4 | | Reserved |
| | 0h | R/W | 3:0 | dac_db[3:0] | B-channel clock delay select |
| 05h | | | 7:4 | | Reserved |
| | Dh | R/W | 3:0 | dac_vref[3:0] | Output amplitude control.<br>0000 : 2.7V swing (1.15V ~ 3.85V)<br>0001 : 2.8V swing (1.10V ~ 3.90V)<br>:<br>1111 : 4.2V swing (0.4V ~ 4.6V) |

## 4.8. VCOM

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 10h | 1 | R/W | 7 | vcom_pd | VCOM output power down control.<br>0 = normal<br>1 = power down |
| | | | 6:5 | | Reserved |
| | 10h | R/W | 4:0 | vcom_vsel[4:0] | VCOM output amplitude selection<br>00000 : 2.2V<br>00001 : 2.25V<br>:<br>11111 : 3.75V |

## 4.9. DC-to-DC

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 20H | 1 | R/W | 7 | OFF2 | ON/OFF control of DC-DC2. Set OFF2=1 to turn off DC-DC2. |
| | 1 | R/W | 6 | OFF1 | ON/OFF control of DC-DC1. Set OFF1=1 to turn off DC-DC1. |
| | -- | -- | 5-0 | Reserved | |
| 21H | 0010 | R/W | 7-4 | PG_CNT2 | Defines power-fail-2 criteria. If there is no switching within the counter period, power-fail-2 will be set. |
| | 0010 | R/W | 3-0 | PG_CNT1 | Defines power-fail-1 criteria. If there is no switching within the counter period, power-fail-1 will be set. |
| 22H | -- | R | 7 | PGOOD2 | power good status of DC2DC-2<br>0 = power fail<br>1 = power good |
| | -- | R | 6 | PGOOD1 | power good status of DC2DC-1<br>0 = power fail<br>1 = power good |
| | -- | R | 5 | OVF2 | DC-DC2 over voltage flag |
| | -- | R | 4 | OVF1 | DC-DC1 over voltage flag |
| | -- | -- | 3-2 | Reserved | |
| | 0 | R/W | 1 | BLT2 | Enable DC-DC2 backlight tuning. |
| | 0 | R/W | 0 | BLT1 | Enable DC-DC1 backlight tuning |
| 23H | 0 | W | 7 | pfail2_int_clr | Clear power fail interrupt of DC-DC-2, generate a falling edge to clear power fail flag |
| | 0 | W | 6 | Pfail1_int_clr | Clear power fail interrupt of DC-DC-1, generate a falling edge to clear power fail flag |
| | 10 | R/W | 5-4 | VS2 | DC-DC2 reference voltage selection<br>00 = 0.3 V<br>01 = 0.6 V<br>10 = 1.25V<br>11 = 2.5 V |
| | 10 | R/W | 3-2 | VS1 | DC-DC1 reference voltage selection<br>00 = 0.3 V<br>01 = 0.6 V<br>10 = 1.25V<br>11 = 2.5 V |
| | 0 | R/W | 1 | EOV2 | DC-DC2 over voltage enable |
| | 0 | R/W | 0 | EOV1 | DC-DC1 over voltage enable |
| 24H | 000 | R/W | 7-5 | DCDCFS2 | DC-DC2 clock and frequency selection. SCK=24MHz.<br>000 = SCK/6/16 = 250KHz<br>001 = SCK/4/16 = 375KHz<br>010 = SCK/3/16 = 500KHz<br>011 = SCK/2/16 = 750KHz<br>100 = VCK/4/16<br>101 = VCK/3/16<br>110 = VCK/2/16<br>111 = VCK/16 |
| | 00 | R/W | 4-3 | DCDCDS2 | DC-DC2 clock duty cycle selection, generated by 4-bit PWM.<br>00 = 50% ( 8/16 )<br>01 = 56.25% ( 9/16 ) |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | 10 = 62.5% ( 10/16 )<br>11 = 68.75% ( 11/16 ) |
| | -- | -- | 2-0 | Reserved | |
| 25H | 000 | R/W | 7-5 | DCDCFS1 | DC-DC2 clock and frequency selection. SCK=24MHz.<br>000 = SCK/6/16 = 250KHz<br>001 = SCK/4/16 = 375KHz<br>010 = SCK/3/16 = 500KHz<br>011 = SCK/2/16 = 750KHz<br>100 = VCK/4/16<br>101 = VCK/3/16<br>110 = VCK/2/16<br>111 = VCK/16 |
| | 00 | R/W | 4-3 | DCDCDS1 | DC-DC2 clock duty cycle selection, generated by 4-bit PWM.<br>00 = 50% ( 8/16 )<br>01 = 56.25% ( 9/16 )<br>10 = 62.5% ( 10/16 )<br>11 = 68.75% ( 11/16 ) |
| | -- | -- | 2-0 | Reserved | |

## 4.10. Output Processor

### 4.10.1. Gain and Offset

Page 0x0Bh

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 00h | 1 | R/W | 7 | g0x[7] | Gain coefficient for data_i[23:16] (red)<br>g0x[7]: integer<br>g0x[6:2]: fraction |
| | 0 | R/W | 6:2 | g0x[6:2] | |
| | | | 1:0 | | Reserved |
| 01h | 1 | R/W | 7:2 | g1x[7] | Gain coefficient for data_i[15:8] (green)<br>g1x[7]: integer<br>g1x[6:2]: fraction |
| | 0 | R/W | | g1x[6:2] | |
| | | | 1:0 | | Reserved |
| 02h | 1 | R/W | 7:2 | g2x[7] | Gain coefficient for data_i[7:0] (blue)<br>g2x[7]: integer<br>g2x[6:2]: fraction |
| | 0 | R/W | | g2x[6:2] | |
| | | | 1:0 | | Reserved |
| 03h | 0 | R/W | 7:0 | b0x[7:0] | Offset coefficient for data_i[23:16]<br>b0x[7]: sign<br>b0x[6:0]: integer |
| 04h | 0 | R/W | 7:0 | b1x[7:0] | offset coefficient for data_i[15:8] |
| 05h | 0 | R/W | 7:0 | b2x[7:0] | offset coefficient for data_i[7:0] |
| 06h | 0 | R/W | 7 | gob_en | Gain/offset enable<br>1 = enable<br>0 = disable |
| | | | 6:0 | | Reserved |

Formula of gain and offset adjustment:

```
R' = g0x * R + b0x
G' = g1x * G + b1x
B' = g2x * B + b2x
```

### 4.10.2. Gamma Correction

Page 0x0Fh

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 08h | 0 | R/W | 7 | gma_en | Gamma correction enable |
| | 0 | R/W | 6 | gma_pd | Gamma RAM power down<br>0 = RAM enable<br>1 = RAM disable |
| | 0 | R/W | 5 | gma_demo_en | Gamma function demo enable<br>0 = mask demo signal from scaler<br>1 = demo enable |
| | | | 4:0 | | Reserved |

note:
clear gma_en before R/W gamma RAM

Gamma RAM address :
Page 0x40h : Red gamma table for 00h~FFh
Page 0x42h : Green gamma table for 00h~FFh
Page 0x44h : Blue gamma table for 00h~FFh

### 4.10.3. Dithering

Page 0x0Fh

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 09h | 0 | R/W | 7 | dith_en | 0 = dithering disable<br>1 = dithering enable |
| | 0 | R/W | 6 | dith_pd | Dither RAM power down<br>0 = RAM enable<br>1 = RAM disable |
| | 0 | R/W | 5 | dith_demo_en | dither function demo enable<br>0 = mask demo signal from scaler<br>1 = demo enable |
| | 0 | R/W | 4 | dith_static | static randoming enable<br>0 = random stream is continuous<br>1 = random stream is reset for each frame |
| | | | 3:2 | | Reserved |
| | 0 | R/W | 1 | difu_en | error diffusion dithering enable |
| | 0 | R/W | 0 | rand_en | random dithering enable |

### 4.10.4. Output Formatter

Page 0x0Fh

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 0AH | 0 | R/W | 6 | even_swap | bit order swap for even pixel (single pixel mode) |
| | 0 | R/W | 5 | clk_inv | clock inversion<br>0: vs/hs/de/data change at rising edge<br>1: vs/hs/de/data change at falling edge |
| | 0 | R/W | 3 | data_toggle_switch | data toggle switch:<br>0: analog panel data toggle for even/odd lines<br>1: digital panel data toggle for even/odd lines |
| | | R/W | 2 | data_toggle_selection | 0: data output inversion if q1h = '1'<br>1: data output inversion if q1h = '0' |
| | 0 | R/W | 1 | data_shift | data shift for 6-bit panel:<br>0: output to data[7:2]<br>1: output to data[5:0] |
| | 0 | R/W | 0 | panle_width | panel data width:<br>0: 8-bit panel<br>1: 6-bit panel |
| 0BH | 0 | R/W | 2 | vs_inv | panel VS polarity inversion (0: active high) |
| | 0 | R/W | 1 | hs_inv | panel HS polarity inversion (0: active high) |
| | 0 | R/W | 0 | de_inv | panel DE polarity inversion (0: active high) |
| 0CH | 0 | R/W | 6 | delta_en | delta panel support, set to '1' will force all RGB output to be sequential RRR->GGG->BBB |
| | 0 | R/W | 5:3 | output_seq_1 | RGB output sequence configuration for q1h = '1'<br>101: BGR<br>100: BRG<br>011: GRB<br>010: GBR<br>001: RBG<br>000: RGB |
| | 0 | R/W | 2:0 | output_seq_0 | RGB output sequence configuration for q1h = '0'<br>101: BGR<br>100: BRG<br>011: GRB<br>010: GBR<br>001: RBG<br>000: RGB |

## 4.11. MCU and Miscellaneous Functions

SFR Mapping

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| F8 | | | | | | | | | FF |
| F0 | B | | | | | | | | F7 |
| E8 | T3CON | | RCAP3L | RCAP3H | TL3 | TH3 | | | EF |
| E0 | ACC | | | | | | | | E7 |
| D8 | SCON1 | SBUF1 | SBRG1 | | | | | | DF |
| D0 | PSW | | | | | | | | D7 |
| C8 | T2CON | | RCAP2L | RCAP2H | TL2 | TH2 | | | CF |
| C0 | XICON | | | | | | | | C7 |
| B8 | IP | | | | | | | | BF |
| B0 | *P3* | | | | | | | | B7 |
| A8 | IE | | | | | | | | AF |
| A0 | *P2* | | | | | | | | A7 |
| 98 | SCON | SBUF | SBRG0 | | | | | | 9F |
| 90 | *P1* | | | | | | | | 97 |
| 88 | TCON | TMOD | TL0 | TL1 | TH0 | TH1 | CKSEL | | 8F |
| 80 | *P0* | SP | DPL | DPH | | | | PCON | 87 |

☝ bit addressable

**Interrupt information**

| Interrupt Source | Vector Address | Polling Sequence within Priority level | Enabled required settings | Interrupt type edge/level |
|---|---|---|---|---|
| External Interrupt 0 | 03H | 0 (highest) | IE.0 | TCON.0 |
| Timer/Counter 0 | 0BH | 1 | IE.1 | -- |
| External Interrupt 1 | 13H | 2 | IE.2 | TCON.2 |
| Timer/Counter 1 | 1BH | 3 | IE.3 | -- |
| Serial Port 0 (1st UART) | 23H | 4 | IE.4 | -- |
| Timer/Counter 2 | 2BH | 5 | IE.5 | -- |
| Serial Port 1 (2nd UART) | 33H | 6 | IE.6 | -- |

IE (8052 interrupt enable register) Address : A8H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EA | ES1 | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

"ES1" :IE.6, Enables/disables the Serial Port 1 interrupt. If ES1 = 0, the Serial Port 1 interrupt is disabled.

IP (8052 interrupt priority register) Address : B8H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | PS1 | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

"PS1" : IP.6, Define the serial port 1 interrupt priority level. PS1 = 1 program it to higher priority level.

**SCON1 (8052 2nd UART control register) Address : D8H**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SM1_1 | SM1_2 | SM1_3 | REN_1 | TB8_1 | RB8_1 | TI_1 | RI_1 |

The additional serial port is similar as 8052's UART.

**SBUF1 (8052 2nd UART buffer) Address : D9H**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SBUF1.7 | SBUF1.6 | SBUF1.5 | SBUF1.4 | SBUF1.3 | SBUF1.2 | SBUF1.1 | SBUF1.0 |

**PCON (8052 power control register) Address : 87h**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SMOD | SMOD2 | | | GF1 | GF0 | PD | IDL |

**SBRG0 (8052 1st UART baud rate control register) Address : 9Ah**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SBRG0EN | SBRG0.6 | SBRG0.5 | SBRG0.4 | SBRG0.3 | SBRG0.2 | SBRG0.1 | SBRG0.0 |

**SBRG1 (8052 2nd UART baud rate control register) Address : DAh**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SBRG1EN | SBRG1.6 | SBRG1.5 | SBRG1.4 | SBRG1.3 | SBRG1.2 | SBRG1.1 | SBRG1.0 |

Baud Rate Generation for UART0

| SBRG0EN (SBRG0.7)) | SMOD1 (PCON.7) | SMOD2 (PCON.6) | TCS1 (CKSEL.2) | Baud Rate for UART0 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | $\frac{1}{32}\times\frac{f_{osc}}{12\times(256-TH1)}$ |
| | | | 1 | $\frac{1}{32}\times\frac{f_{osc}}{3\times(256-TH1)}$ |
| 0 | SMOD1 or SMOD2 = 1 | | 0 | $\frac{1}{16}\times\frac{f_{osc}}{12\times(256-TH1)}$ |
| | | | 1 | $\frac{1}{16}\times\frac{f_{osc}}{3\times(256-TH1)}$ |
| 0 | 1 | 1 | 0 | $\frac{1}{8}\times\frac{f_{osc}}{12\times(256-TH1)}$ |
| | | | 1 | $\frac{1}{8}\times\frac{f_{osc}}{3\times(256-TH1)}$ |
| 1 | 0 | 0 | X | $\frac{1}{32}\times\frac{f_{osc}}{(SBRG0[6:0]+1)}$ |
| 1 | SMOD1 or SMOD2 = 1 | | X | $\frac{1}{16}\times\frac{f_{osc}}{(SBRG0[6:0]+1)}$ |
| 1 | 1 | 1 | X | $\frac{1}{8}\times\frac{f_{osc}}{(SBRG0[6:0]+1)}$ |

Baud Rate Generation for UART1

| SBRG1EN (SBRG1.7)) | SMOD2 (PCON.6) | TCS2 (CKSEL.3) | Baud Rate for UART1 |
|---|---|---|---|
| 0 | 0 | 0 | $\frac{1}{16}\times\frac{f_{osc}}{12\times(65536-RCAP2)}$ |
| | | 1 | $\frac{1}{16}\times\frac{f_{osc}}{3\times(65536-RCAP2)}$ |
| 0 | 1 | 0 | $\frac{1}{8}\times\frac{f_{osc}}{12\times(65536-RCAP2)}$ |

| | | | |
|---|---|---|---|
| | | 1 | $\frac{1}{8}\times\frac{f_{osc}}{3\times(65536-RCAP2)}$ |
| 1 | 0 | X | $\frac{1}{16}\times\frac{f_{osc}}{(SBRG1[6:0]+1)}$ |
| 1 | 1 | X | $\frac{1}{8}\times\frac{f_{osc}}{(SBRG1[6:0]+1)}$ |

misc. control register - Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 00H | 0 | R/W | 7 | mcu_ram_pd | 1: power down mcu ram. |
| | 0 | | 6-3 | en_p1[3:0] | 1: Enable 8051 P1.0-P1.3 |
| | 0 | | 2 | | RSV |
| | 0 | | 1 | en-uart1 | 1: Enable 8051 UART1(via TCON[1:0]) |
| | 0 | | 0 | en-uart0 | 1: Enable 8051 UART0(via ADC[3:2]) |

Flash control register - Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 01H | 00 | R/W | 7-0 | ferom_enbyte1 | enable flash-eeprom verify byte1 (0x55h) |
| 02H | 00 | R/W | 7-0 | ferom_enbyte2 | enable flash-eeprom verify byte2 (0xAAh) |
| 03H | 00 | R/W | 7-0 | ferom_adr[23:16] | flash-eeprom address[23:16] |
| 04H | 00 | R/W | 7-0 | ferom_adr[15:8] | flash-eeprom address[16:8] |
| 05H | 00 | R/W | 7-0 | ferom_adr[7:0] | flash-eeprom address[7:0] |
| 06H | 0 | R/W | 7 | ferom_start | flash-eeprom command execute (auto-clear) |
| | 0 | | 6-3 | reserved | |
| | 0 | | 2 | ferom_erase | flash-eeprom sector erase (auto-clear) |
| | 0 | | 1 | ferom_program | flash-eeprom byte program (auto-clear) |
| | 0 | | 0 | ferom_read | flash-eeprom byte read (auto-clear) |
| 07H | 00 | R/W | 7-0 | ferom_data | flash-eeprom I/O data |
| 08H | D8 | R/W | 7-0 | ferom_ercmd | flash-eeprom sector erase command |
| 09H | 9F | R/W | 7-0 | ferom_rdcmd | flash-eeprom read ID command |

Enable Flash-EEPROM by write register 0x01 data 0x55 and register 0x02 data 0xAA.
Set Flash-EEPROM address by write register 0x03 ~ 0x05
Erase Flash-EEPROM by write register 0x06 data 0x84
Program Flash-EEPROM one-byte data :

1. set Flash-EEPROM program address.
2. set program data by write register 0x07.
3. write register 0x06 data 82 to start program.

Read Flash-EEPROM one-byte data :

1. set Flash-EEPROM program address.
2. write register 0x06 data 81 to start read.
3. read register 0x07 to get Flash-EEPROM data

Write register 0x08 data 0x20 to support 8K-sector erase (MXIC).

### 4.11.1. I²C

Slave I2C status register - Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 20h | 0 | R | 7 | di2c_int_rt | This bit is set when data is received, transmitted.<br>(The data depend on di2c_rt_slt) |
| | 0 | R | 6 | di2c_int_stop | 1: STOP phase interrupt. |
| | 0 | R | 5 | di2c_first | 1: First phase |
| | 0 | R | 4 | di2c_alrw | 1: Read phase, 0:Write phase. |

| | | | | | |
|---|---|---|---|---|---|
| | 0 | R | 3 | di2c_rxnak | 1: NACK, 0:ACK (receive ack bit) |
| | 0 | R | 2 | di2c_rx_ful | 1: RX FIFO full |
| | 1 | R | 1 | di2c_tx_empt | 1: TX FIFO empty |
| | 0 | R | 0 | di2c_bb | 1: SCL & SDA busy |
| 21h | 0 | R | 7 | di2c_slv | 1: receive slave address |
| | | | 6:0 | | Reserved |

Slave I2C control registers - Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 22h | 0 | R/W | 7 | di2c_en | 1= slave i2c enable |
| | 0 | R/W | 6 | di2c_clr_rt | 1= Clear transmit/receive interrupt |
| | 0 | R/W | 5 | di2c_clr_stp | 1= Clear STOP phase interrupt |
| | 0 | R/W | 4 | di2c_clr_rx | 1= Clear RX FIFO index |
| | 0 | R/W | 3 | di2c_clr_tx | 1= Clear TX FIFO index |
| | 0 | R/W | 2 | di2c_wait | 1= enable pull low scl when 9th bit |
| | 1 | R/W | 1 | di2c_txnak | 1= NACK<br>0= ACK (Transmit ACK bit) |
| | 0 | R/W | 0 | | Reserved |
| 23h | 0 | R/W | 7:6 | di2c_rt_slt | 00= don't enable int_rt when received the data.<br>01= one byte (The int_rt will be set when one byte data is received, transmitted).<br>10= two bytes (The int_rt will be set when two bytes data is received, transmitted).<br>11= four bytes (The int_rt will be set when four bytes data is received, transmitted). |
| | | | | | |

Slave I2C Receive & Transmit Buffer Registers - Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 24h | FFh | R/W | 7:0 | di2c_dtx | Transmit buffer |
| 25h | FFh | R | 7:0 | di2c_drx | Receive buffer |
| 26h | | | 7:4 | | Reserved |
| | 0h | R | 3:0 | di2c_dtx_idx | Transmit buffer index |
| 27h | | | 7:4 | | Reserved |
| | 0h | R | 3:0 | di2c_drx_idx | Receive buffer index |

Slave I2C Address Register - Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 28h | A0H | R/W | 7:1 | di2c_sadr | Slave address |

### 4.11.2. IR

Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 30h | 0 | R/W | 7 | en_ir | Enable IR |
| | 0 | R/W | 6 | ir_sedg | 0 = trigger at both edge<br>1 = single edge trigger |
| | 0 | R/W | 5 | ir_rf | 0 = falling edge trigger<br>1 = rising edge trigger |
| | 0 | R/W | 4 | en_ov_int | Enable over flow interrupt |
| | 0 | R/W | 3:2 | pre_scal[1:0] | pre-scaler of IR counter clock<br>00 = 64us<br>01 = 1us<br>10 = 256us<br>11 = 1ms |
| | 0 | R/W | 1 | clr_ir_int | Clear interrupt "ir_int" "(write '1" & "0") |

| | | | | | |
|---|---|---|---|---|---|
| | | | 0 | | Reserved |
| 31h | | | 7:3 | | Reserved |
| | | R | 2 | ir_hl | Read IR input H/L |
| | | R | 1 | ir_ovflw | IR over flow interrupt |
| | | R | 0 | ir_int | IR interrupt = edge trigger + overflow |
| 32h | 00h | R | 7:0 | ir_cnt[7:0] | IR counter value |
| 33h | 00h | R | 7:0 | ir_cnt[15:8] | |
| 34h | 00h | R/W | 7:0 | ir_ov_cnt[7:0] | IR overflow counter low byte |
| 35h | 02h | R/W | 7:0 | ir_ov_cnt[15:8] | If ir_cnt = ir_ov_cnt → ir_ovflw =1 |

### 4.11.3. PWM

Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 40h | 80h | R/W | 7:0 | pwm0[7:0] | PWM0 output data |
| 41h | 80h | R/W | 7:0 | pwm1[7:0] | PWM1 output data |
| 42h | 80h | R/W | 7:0 | pwm2[7:0] | PWM2 output data |
| 43h | 80h | R/W | 7:0 | pwm3[7:0] | PWM3 output data |
| 44h | 0 | R/W | 7 | | Reserved |
| | 0 | R/W | 6 | PWML_OE | "0" PWML for DCDC(internal) only<br>"1" PWML could output via PWM[x] pin |
| | 0 | R/W | 5-4 | PWML_SEL[1:0] | "00" PWML output via PWM[0]<br>"01" PWML output via PWM[1]<br>"10" PWML output via PWM[2]<br>"11" PWML output via PWM[3] |
| 45h | 0 | R/W | 7 | enpwml | 1 = enable low frequency PWM at PWM0<br>0 = normal PWM |
| | 00h | R/W | 6:0 | pwm_clk[6:0] | Select low frequency PWM clock.<br>The clock is 1MHz ÷ (PWM_CLK[6:0] +1). |
| 46h | 00h | R/W | 7:0 | pwml[7:0] | PWML output data |
| 47H | 0 | R/W | 7 | | Reserved |
| | 0 | R/W | 6 | pwm_10_OE | 10 bit PWM output enable |
| | 00 | R/W | 5-4 | pwm10_SEL [1:0] | "00" PWM10 output via PWM[0]<br>"01" PWM10 output via PWM[1]<br>"10" PWM10 output via PWM[2]<br>"11" PWM10 output via PWM[3] |
| | 0 | R/W | 3-2 | | Reserved |
| | 10h | R/W | 1-0 | pwm10l[9:8] | 10-bit PWM MSB |
| 48H | 00h | R/W | 7-0 | pwm10l[7:0] | 10-bit PWM LSB |

### 4.11.4. Keypad ADC

Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 50h | 1 | R/W | 7 | pd_ladc | power down keypad ADC |
| | 0 | R/W | 6 | str_cvt | Start ADC conversion when set to "1". It will be cleared to "0" when conversion is done. |
| | 0 | R/W | 5 | adc_clk | ADC clock source.<br>0: 3MHz<br>1: 1MHz |
| | | | 4 | | Reserved |
| | 0 | R/W | 3 | en_ad[3] | Enable channel 3 when it is set. |
| | 0 | R/W | 2 | en_ad[2] | Enable channel 2 when it is set. |
| | 0 | R/W | 1 | en_ad[1] | Enable channel 1 when it is set. |

| | | | | | |
|---|---|---|---|---|---|
| | 0 | R/W | 0 | en_ad[0] | Enable channel 0 when it is set. |
| 51h | 00h | R | 7:0 | ad_chA[7:0] | KPADC channel 0 data |
| 52h | 00h | R | 7:0 | ad_chB[7:0] | KPADC channel 1 data |
| 53h | 00h | R | 7:0 | ad_chC[7:0] | KPADC channel 2 data |
| 54h | 00h | R | 7:0 | ad_chD[7:0] | KPADC channel 3 data |
| 55h | 0 | R/W | 7 | adc_big | select ADC compare bigger |
| | | | 6:4 | | Reserved |
| | 0h | R/W | 3:0 | adc_wk_ch[3:0] | ADC keep "ADC_WK_V[7:0]" voltage to monitor ADC channel "ADC_WK_CH[3:0]" |
| 56h | 80h | R/W | 7:0 | adc_wk_v[3:0] | ADC wake up voltage |

### 4.11.5. Interrupt

Interrupt1 Enable Register
Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 60h | 0 | R/W | 7 | ie_din | Enable DIN interrupt include H V loss, resolution change VIN rising/falling… |
| | 0 | R/W | 6 | ie_vso | Enable VS output rising or falling edge interrupt |
| | 0 | | 5 | | Reserved |
| | 0 | R/W | 4 | ie_ir | Enable IR detection interrupt |
| | 0 | R/W | 3 | ie_di2c | Enable slave $I^2C$ interrupt |
| | 0 | R/W | 2 | ie_int | Enable external INT interrupt |
| | 0 | R/W | 1 | ie_tc0 | Enable TC0 interrupt |
| | 0 | R/W | 0 | ie_tc1 | Enable TC1 interrupt |
| 61h | 0 | R/W | 7:6 | ie_pfail[1:0] | Enable power fail [1:0] (dc to dc) interrupt |
| | 0 | R/W | 5 | ie_kpadc | Enable KPADC interrupt |

Interrupt1 Flag Register
Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 62h | 0 | R | 7 | if_din | Interrupt Flag of DIN interrupt include H V loss, resolution change VIN rising/falling… |
| | 0 | R | 6 | if_vso | Interrupt Flag of VS output rising or falling edge interrupt |
| | 0 | | 5 | | Reserved |
| | 0 | R | 4 | if_ir | Interrupt Flag of IR detection |
| | 0 | R | 3 | if_di2c | Interrupt Flag of slave $I^2C$ |
| | 0 | R | 2 | if_int | Interrupt Flag of external INT interrupt |
| | 0 | R | 1 | if_tc0 | Interrupt Flag of TC0 interrupt |
| | 0 | R | 0 | if_tc1 | Interrupt Flag of TC1 interrupt |
| 63h | 0 | R | 7:6 | if_pfail[1:0] | Interrupt Flag of power fail [1:0] (dc to dc) interrupt |
| | 0 | R | 5 | if_kpadc | Interrupt Flag of kpadc |
| | 0 | R | 4:0 | if_blk[4:0] | Reserved for further use. |

Polling Flag Register
Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 64h | 0 | R | 7 | evt_vso | Event of VS output rising or falling edge |
| | | | 6:0 | | Reserved |
| 65h | 0 | R | 7 | evt_int | Event of external INT |
| | | | 6:0 | | Reserved |

Clear Polling Flag Register
Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 66h | 0 | R/W | 7 | clr_vso_ris | Clear event of VS output rising or falling edge |
| | | | 6:0 | | Reserved |
| 67h | 0 | R/W | 7 | clr_int | Clear event of external INT |
| | | | 6:0 | | Reserved |

VSO & INT Interrupt Edge Control Register
Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 68h | 0 | R/W | 7 | vso_int_edge | 0 = rising edge trigger<br>1 = falling edge trigger |
| | 0 | | 6:0 | | Reserved |
| 69h | 0 | R/W | 7 | int_chg | 0 = single edge trigger, depends on int_edge.<br>1 = rising & falling trigger |
| | 0 | | 6:0 | | Reserved |
| 6Ah | 0 | R/W | 7 | int_edge | 0 = rising edge trigger<br>1 = falling edge trigger |
| | 0 | | 6:0 | | Reserved |

### 4.11.6. Watchdog

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| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 70h | ABh | R/W | 7:0 | wd_timer[7:0] | Write **0xAB** will reset the timer for **2 seconds**.<br>Write **0xAA** will reset the timer for **1.5 seconds**.<br>Write **0xA9** will reset the timer for **1.0 second**.<br>Write **0xA8** will reset the timer for **0.5 seconds**.<br>Write **0x55** will **stop** the timer.<br>Write other values will **resume** the timer.<br>Stop or resume the timer will not clear the timer. |

Timer
Page 0x13h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 80h | 1 | R/W | 7 | tc0_en | 1= enable Timer 0<br>0= disable Timer 0 |
| | 1 | R/W | 6 | tc1_en | 1= enable Timer 1<br>0= disable Timer 1 |
| | | | 5:4 | | Reserved |
| | 0 | R/W | 3 | clr_tc0 | 1= clear TC0 interrupt |
| | 0 | R/W | 2 | clr_tc1 | 1= clear TC1 interrupt |
| | | | 1:0 | | Reserved |
| 81h | 55h | R/W | 7:0 | tc0[7:0] | TC0 Low byte data |
| 82h | 0 | R/W | 7:0 | tc0[15:8] | TC0 High byte data |
| 83h | AAh | R/W | 7:0 | tc1[7:0] | TC1 Low byte data |
| 84h | 0 | R/W | 7:0 | tc1[15:8] | TC1 High byte data |

Note: Time base is 1us

## 4.12. Video Decoder

### 4.12.1. Video Decoder Register Summary

| Index | R/W | Default | Bit 7 | Bit 6 | Bit 5 | Bit4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | R/W | 00h | hv_delay | hpixel | | vline_625 | colour_mode | | | yc_src |
| 0x01 | R/W | 01h | Reserved | | luma_notch_bw | | chroma_bw_lo | | chroma_burst5or10ped | ped |
| 0x02 | R/W | 4Fh | hagc_field | mv_hagc | dc_clamp_mode | | dagc_en | agc_half_en | cagc_en | hagc_en |
| 0x03 | R/W | 00h | ntsc443_mode | Reserved | | | colour_trap | adaptive_mode | | |
| 0x04 | R/W | DDh | hagc | | | | | | | |
| 0x05 | R/W | 32h | noise_thresh | | | | | | | |
| 0x06 | R/W | 0Ah | adc_updn_swap | adc_input_swap | adc_cbcr_pump_swap | agc_gate_thresh | | | | |
| 0x07 | R/W | A0h | ccir656_en | cbcr_swap | blue_mode | | yc_delay | | | |
| 0x08 | R/W | 80h | contrast | | | | | | | |
| 0x09 | R/W | 20h | brightness | | | | | | | |
| 0x0A | R/W | 80h | saturation | | | | | | | |
| 0x0B | R/W | 00h | hue | | | | | | | |
| 0x0C | R/W | 8Ah | cagc | | | | | | | |
| 0x0D | R/W | 07h | user_ckill_mode | | vbi_ckill | hlock_ckill | chroma_kill | | | |
| 0x0E | R/W | 06h | vnon_std_threshold | | | | hnon_std_threshold | | | |
| 0x0F | R/W | 2Ch | nstd_hysis | | fixed_burstgate | cautopos | | | | |
| 0x10 | R/W | 0Ah | Reserved | agc_peak_nominal | | | | | | |
| 0x11 | R/W | 89h | agc_gate_vsync_coarse | agc_gate_vsync_stip | agc_gate_kill_mode | | agc_peak_en | agc_peak_cntl | | |
| 0x12 | R/W | 05h | Reserved | | | | | agc_gate_start[10:8] | | |
| 0x13 | R/W | C8h | agc_gate_start[7:0] | | | | | | | |
| 0x14 | R/W | 38h | agc_gate_width | | | | | | | |
| 0x15 | R/W | 58h | agc_bp_delay | | | | | | | |
| 0x16 | R/W | 74h | locked_count_noisy_max | | | | locked_count_clean_max | | | |
| 0x17 | R/W | CBh | hlock_vsync_mode | | hstate_fixed | disable_hfine | hstate_unlocked | hstate_max | | |
| 0x18 | R/W | 26h | cdto_fixed | Reserved | cdto_inc[29:24] | | | | | |
| 0x19 | R/W | 2Eh | cdto_inc[23:16] | | | | | | | |
| 0x1A | R/W | 8Bh | cdto_inc[15:8] | | | | | | | |
| 0x1B | R/W | A2h | cdto_inc[7:0] | | | | | | | |
| 0x1C | R/W | 24h | hdto_fixed | Reserved | hdto_inc[29:24] | | | | | |
| 0x1D | R/W | 00h | hdto_inc[23:16] | | | | | | | |
| 0x1E | R/W | 00h | hdto_inc[15:8] | | | | | | | |
| 0x1F | R/W | 00h | hdto_inc[7:0] | | | | | | | |
| 0x20 | R/W | 3Eh | hsync_rising | | | | | | | |
| 0x21 | R/W | 3Eh | hsync_phase_offset | | | | | | | |
| 0x22 | R/W | 00h | hsync_gate_start | | | | | | | |
| 0x23 | R/W | 80h | hsync_gate_end | | | | | | | |
| 0x24 | R/W | E9h | hsync_tip_start | | | | | | | |
| 0x25 | R/W | 0Fh | hsync_tip_end | | | | | | | |
| 0x26 | R/W | 2Dh | hsync_rising_start | | | | | | | |
| 0x27 | R/W | 50h | hsync_rising_end | | | | | | | |
| 0x28 | R/W | 22h | backporch_start | | | | | | | |

| Index | R/W | Default | Bit 7 | Bit 6 | Bit 5 | Bit4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x29 | R/W | 4Eh | backporch_end | | | | | | | |
| 0x2A | R/W | D6h | hsync_filter_start | | | | | | | |
| 0x2B | R/W | 4Eh | hsync_filter_end | | | | | | | |
| 0x2C | R/W | 32h | burst_gate_start | | | | | | | |
| 0x2D | R/W | 46h | burst_gate_end | | | | | | | |
| 0x2E | R/W | 82h | hactive_start | | | | | | | |
| 0x2F | R/W | 50h | hactive_width | | | | | | | |
| 0x30 | R/W | 22h | vactive_start | | | | | | | |
| 0x31 | R/W | 61h | vactive_height | | | | | | | |
| 0x32 | R/W | 70h | Reserved | vsync_h_min | | | | | | |
| 0x33 | R/W | 0Eh | Reserved | vsync_h_max | | | | | | |
| 0x34 | R/W | 6Ch | Reserved | vsync_agc_min | | | | | | |
| 0x35 | R/W | D0h | vsync_clamp_mode | | vsync_agc_max | | | | | |
| 0x36 | R/W | 7Ah | Reserved | vsync_vbi_min | | | | | | |
| 0x37 | R/W | 20h | vlock_wide_range | vsync_vbi_max | | | | | | |
| 0x38 | R/W | 00h | vsync_cntl | | vsync_thresh | | | | | |
| 0x39 | R/W | 0Ah | field_pol | flip_field | veven_delayed | vodd_delayed | field_detect_mode | | vloop_tc | |
| 0x3A | R | X | mv_cstripes | | | mv_vbi_detected | chromalock | vlock | hlock | no_signal |
| 0x3B | R | X | Reserved | | | | | vnon_standard | hnon_standard | proscan_detected |
| 0x3C | R | X | vcr_rew | vcr_ff | vcr_trick | vcr | noisy | 625lines_detected | SECAM_detected | PAL_detected |
| 0x3D | R/W | 00h | debugmux_en | debugmux | | | | | | |
| 0x3F | W | 00h | Reserved | | | | | | | soft_rst |
| 0x70 | R | X | Reserved | | status_hdto_inc[29:24] | | | | | |
| 0x71 | R | X | status_hdto_inc[23:16] | | | | | | | |
| 0x72 | R | X | status_hdto_inc[15:8] | | | | | | | |
| 0x73 | R | X | status_hdto_inc[7:0] | | | | | | | |
| 0x74 | R | X | Reserved | | status_cdto_inc[29:24] | | | | | |
| 0x75 | R | X | status_cdto_inc[23:16] | | | | | | | |
| 0x76 | R | X | status_cdto_inc[15:8] | | | | | | | |
| 0x77 | R | X | status_cdto_inc[7:0] | | | | | | | |
| 0x78 | R | X | status_agc_again | | | | | | | |
| 0x79 | R | X | status_agc_dgain | | | | | | | |
| 0x7A | R | X | status_cmag | | | | | | | |
| 0x7B | R | X | Reserved | | status_cgain[13:8] | | | | | |
| 0x7C | R | X | status_cgain[7:0] | | | | | | | |
| 0x7D | R | X | status_cordiq_freq | | | | | | | |
| 0x7F | R | X | status_noise | | | | | | | |
| 0x80 | R/W | 04h | Reserved | secam_ybw | peak_range | | peak_gain | | | peak_en |
| 0x82 | R/W | 82h | sv_bf | Reserved | | | | | palsw_level | |
| 0x83 | R/W | 6Fh | lose_chromalock_count | | | | lose_chromalock_level | | | lose_chromalock_ckill |
| 0x84 | R/W | 0h | | | vsync_derived_sel | | | vsync_real_sel | | |
| 0x85 | R | X | Reserved | y_sat_abs_level_latch | | | | | | |

| Index | R/W | Default | Bit 7 | Bit 6 | Bit 5 | Bit4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x86 | R | X | Reserved | cb_sat_abs_level_latch | | | | | | |
| 0x87 | R | X | Reserved | cr_sat_abs_level_latch | | | | | | |
| 0x8A | R/W | 0Ah | Reserved | | | | cstate | | | fixed_cstate |
| 0x8B | R/W | 01h | Reserved | | | | sogin_sel | ext_hsync_pol | ext_vsync_pol | hresampler_2up |
| 0x8D | R/W | 0Ah | cpump_delay_en | cpump_adjust_polarity | cpump_adjust_delay | | | | | |
| 0x8E | R/W | C8h | cpump_adjust | | | | | | | |
| 0x8F | R/W | B9h | cpump_delay | | | | | | | |
| 0x90 | R/W | 04h | auto_mode_time_constant | | | | | | | |
| 0x91 | R/W | 03h | reserved | | iir_filter_sel | | reserved | clamp_scale | | |
| 0x92 | R/W | 00h | adc_clamp_restore_thr | | | | | | | |
| 0xAF | R/W | 0Ah | noise_th_en | noise_th | | | | | | |
| 0xB0 | R/W | FAh | horiz_diff_cgain | | horiz_diff_ygain | | chroma_vdiff_gain | | lowfreq_vdiff_gain | |
| 0xB1 | R/W | FFh | vadap_burst_noise_th_gain | | burst_noise_th_gain | | c_noise_th_gain | | y_noise_th_gain | |
| 0xB2 | R/W | 10h | lbadrgen_rst | comb2d_only | pal_chroma_level | | | | | |
| 0xB5 | R/W | 43h | chroma_peak_en | chroma_coring_en | Reserved | | | | chroma_peak | |
| 0xB6 | R/W | 02h | ldpause_threshold | | | | Reserved | | vf_nstd_en | vcr_auto_switch_en |
| 0xB7 | R/W | 00h | Reserved | notch_gain | | | Reserved | comb_gain | | |
| 0xBA | R/W | 21h | vactive_fb_start | | | | | | | |
| 0xBB | R/W | 61h | vactive_fb_height | | | | | | | |
| 0xBC | R/W | 00h | Reserved | | | | hsync_pulse_width | | | |
| 0xBD | R/W | 10h | no_signal_path_sel | free_run_27m | Reserved | VBI_in_CCIR656 | CCIR656_eav_sav_phase | vsync_out_polarity | hsync_out_polarity | clk_out_polarity |
| 0xBE | R/W | 00h | Reserved | | | | | | vactive_out_sel | hactive_out_sel |
| 0xC0 | R/W | 08h | adc_resample_clk_sel | rgb_input | cvbs_out_disable | cvbs_out_sel | | chb_sel | cha_sel | |
| 0xC1 | R/W | B9h | adc_current_sel | | cb_ch_sel | | c_ch_sel | | y_ch_sel | |
| 0xC2 | R/W | 54h | Reserved | chc_on | Reserved | chb_on | Reserved | cha_on | adc_sample_clk | |
| 0xC3 | R/W | 04h | Reserved | | edge_enhance_range | | edge_enhance_gain | | | edge_enhance_en |
| 0xC4 | R/W | 00h | pre_coast | | | | | | | |
| 0xC5 | R/W | 00h | post_coast | | | | | | | |
| 0xC6 | R/W | 00h | luma_coring_en | Reserved | | | | luma_coring_ threshold | | |
| 0xC7 | R/W | 00h | blue_stretch_en | blue_stretch_luma threshold | | blue_stretch_chroma_ threshold | | blue_stretch_amount | | |
| 0xC8 | R/W | 00h | skin_tone_adj_en | Reserved | | | | | skin_tone_type sel | |
| 0xC9 | R/W | 08h | Reserved | | | en_vos | Reserved | adc_hsync_backup_en | Reserved | lbf_filter_en |
| 0xCA | R/W | 14h | fix_sog_setting | sog_amplifier | sog_threshold | | | | | |
| 0xCB | R/W | 10h | ad_clplace | | | | | | | |
| 0xCC | R/W | 10h | ad_cldur | | | | | | | |
| 0xCD | R/W | FFh | adc_gain | | | | | | | |
| 0xD0 | R/W | 1Fh | Reserved | | ch_a_offset | | | | | |
| 0xD1 | R/W | 1Fh | Reserved | | ch_b_offset | | | | | |
| 0xD2 | R/W | 1Fh | Reserved | | ch_c_offset | | | | | |

| Index | R/W | Default | Bit 7 | Bit 6 | Bit 5 | Bit4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0xD3 | R/W | 00h | hsync_path_sel | adc_hsync_polarity | half_delay_sel | hactive_path_sel | sog_hsync_delay_pulse_width | | | |
| 0xD4 | R/W | 00h | hs_del[7:0] | | | | | | | |
| 0xD5 | R/W | 04h | adc_clamp_hsync_sel | sync_sep_hsync_polarity | Reserved | | | hsync_path_sel_pll27m | hs_del[9:8] | |
| 0xD6 | R/W | 00h | self_test_pattern_en | Reserved | | | | self_test_pattern | | |
| 0xD7 | R/W | 00h | Reserved | | | | | adc_clamp_time_const | | |
| 0xD8 | R/W | 80h | ccir656_hactive_width | | | | | | | |
| 0xD9 | R/W | B4h | NF27M[7:0] | | | | | | | |
| 0xDA | R/W | 02h | Reserved | | | | | | NF27M[9:8] | |
| 0xDB | R/W | 00h | Reserved | auto_detection_en | special_reset_en | Reserved | | | | pd |
| 0xDC | R/W | 0Ah | adc_clamp_threshold_en | adc_clamp_threshold | | | | | | |
| 0xDD | R | X | status_sync_sep_no_signal | status_amplifier | status_sog_threshold | | | | | |
| 0xDE | R/W | 88h | adc_clamp_in_non_active_en | Reserved | adc_clamp_in_non_active_width | | | | | |
| 0xDF | R/W | 1Ch | Reserved | rgb_input_hsync_height | | | | | | |
| 0xEC | R/W | 05h | vcr_mode_dis | reserved | vcr_free_run_27m_en | no_clamp | auto_no_clamp_en | | | |
| 0xED | R/W | 1Fh | rainbow_suppress_en | y_up_lo_diff_threshold | | | | | | |
| 0xEE | R/W | 09h | rainbow_band_coef | y_ri_le_diff_threshold | | | | | | |
| 0xEF | R/W | 00h | reserved | pal_fix_en | reserved | weight_en | bpf_en | 443m_sel | wide_bw_sel | |
| 0xF3 | R/W | EAh | auto_mode_FcMore_up_threshold | | | | | | | |
| 0xF4 | R/W | 20h | auto_mode_FcLess_lo_threshold | | | | | | | |
| 0xF5 | R/W | 40h | auto_mode_FcLess_up_threshold | | | | | | | |
| 0xF6 | R/W | D0h | auto_mode_FcMore_lo_threshold | | | | | | | |
| 0xF7 | R/W | 00h | reserved | | | | | peaking_strength | peaking_soften | |
| 0xFF | R | 02h | standard_states | | | | chip_revision | | | |

## 4.12.2. Video Decoder Registers

Control Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 00h | 0 | R/W | **7** | hv_delay | This bit emulates the HV-delay mode found on Sony studio monitors.<br>0 = disabled (default)<br>1 = enabled |
| | 00b | R/W | **6:5** | hpixel | These bits select the output display format.<br>00 : 858 pixels/line - NTSC, PAL(M)<br>01 : 864 pixels/line - PAL(B,D,G,H,I,N,CN),SECAM<br>10 : 780 pixels/line - NTSC Square Pixel, PAL(M) Square Pixel<br>11 : 944 pixels/line - PAL(B,D,G,H,I,N) Square Pixel |
| | 0 | R/W | **4** | vline_625 | This bit selects the number of scan lines per frame.<br>0 = 525 (default)<br>1 = 625 |

| | | | | | |
|---|---|---|---|---|---|
| | 000b | R/W | **3:1** | colour_mode | These bits select video colour standard.<br>000 = NTSC (default)<br>001 = PAL (I,B,G,H,D,N)<br>010 = PAL (M)<br>011 = PAL (CN)<br>100 = SECAM |
| | 0 | R/W | **0** | yc_src | This bit selects input video format.<br>0 = composite (default)<br>1 = S-Video (separated Y/C) |
| 01h | | R/W | **7:6** | | Reserved |
| | 00b | R/W | **5:4** | luma_notcha_bw | These bits select luma notch width<br>00 = none (default)<br>01 = narrow<br>10 = medium<br>11 = wide |
| | 00b | R/W | **3:2** | chroma_bw_lo | This bit set the chroma low pass filter to wide or narrow<br>0 = narrow (default)<br>1 = wide<br>2 = extra wide |
| | 0 | R/W | **1** | chroma_burst5or10 | This bit selects the burst gate width<br>0 = 5 subcarrier clock cycles (default)<br>1 = 10 subcarrier clock cycles |
| | 1 | R/W | **0** | ped | This bit enables black level correction for 7.5 blank-to-black setup (pedestal).<br>0 = no pedestal subtraction<br>1 = pedestal subtraction (default) |
| 02h | 0 | R/W | **7** | hagc_field | When this bit is "0" (the default), then the gain is updated once per line, after DC clamping. When this bit is set, then the gain is only updated once per field, at the start of vertical blank.<br>0 = off (default)<br>1 = on |
| | 1 | R/W | **6** | my_hagc | This bit, when set, automatically reduces the gain (set in register 4) by 25% when<br>macro-vision encoded signals are detected<br>0 = off<br>1 = on (default) |
| | 00b | R/W | **5:4** | dc_clamp_mode | This bit sets the mode for the analog front end DC clamping<br>00 = auto (default)<br>01 = backporch only<br>10 = synctip only<br>11 = off |
| | 1 | R/W | **3** | dagc_en | This bit, when set, enables the digital AGC. The digital AGC is used in series with the analog gain.<br>0 = off<br>1 = on (default) |
| | 1 | R/W | **2** | agc_half_en | This bit, when set, enables the half gain mode, when unlocked, for the analog front end.<br>0 = off<br>1 = on (default) |
| | 1 | R/W | **1** | cagc_en | This bit when set enables the chroma AGC. If disabled, then the AGC target is used to drive directly the AGC gain.<br>0 = off<br>1 = on (default) |
| | 1 | R/W | **0** | hagc_en | This bit when set enables the luma/composite AGC. If disabled, then the AGC target (register 04h) is used to drive directly the AGC gain.<br>0 = off<br>1 = on (default) |

YC Separation Control Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 03h | 0 | R/W | **7** | ntsc443_mode | This bit enable the NTSC443 input mode<br>Default=0 |
| | | | **6:4** | | Reserved |
| | 0 | R/W | **3** | colour_trap | This bit enables the notch-filter at the luma path after the comb filter. This filter can be turned on or off irrespective of the adaptive mode setting.<br>0 = Disabled<br>1 = Enabled |
| | 000b | R/W | **2:0** | adaptive_mode | These bits select modes for the composite signal's luma (Y) and chroma (C) separation before colour demodulation.<br>For NTSC Mode<br>000 = fully adaptive comb (2-D adaptive comb) (default)<br>001 = vertical adaptive comb only (1-D adaptive comb)<br>010 = Reserved<br>011 = basic luma notch filter mode (for very noisy and unstable pictures)<br>100 = simple 2-tap comb<br>101 = simple 3-tap comb<br>110 = Reserved<br>111 = Reserved<br><br>For PAL Mode<br>000 = fully adaptive comb (2-D adaptive comb) (default)<br>001 = basic luma notch filter mode WITH handover bar suppression<br>010 = 5-Tap comb filter mode WITHOUT handover bar suppression<br>011 = basic luma notch filter mode WITHOUT handover bar suppression<br>100 = luma notch and fixed-chroma comb<br>101 = simple 3-tap comb<br>110 = 5-Tap hybrid comb filter mode WITH handover bar suppression<br>111 = Reserved |

Luma AGC Value Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 04h | DDh | R/W | 7:0 | hagc | These bits specify the luma AGC target value. The gain of the AGC is modified until the horizontal sync height is equal to this value. Note that if a MacroVision signal is detected and "mv_hagc_mode" (02.6h) is set, then this value is automatically reduced by 25%.<br>Standard — Programming Value<br>NTSC M — DDh (221d)<br>NTSC J — CDh (205d)<br>PAL B,D,G,H,I, COMB N, SECAM — DCh (220d)<br>PAL M,N — DDh (221d)<br>NTSC M (MACROVISIOIN) — A6h (166d)<br>PAL B,D,G,H,I, COMB N (MACROVISION) — AEh (174d)<br>If "hagc_en" (register 02.0h) is "0", then "hagc" is used to directly drive the analog gain.<br>In this case, a value of 64 represents a unity gain, 32 represents a one-half gain, and 128 denotes a double gain. |

Noise Threshold Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 05h | 32h | R/W | 7:0 | noise_thresh | This value sets the noise value at which the circuit considers a signal noisy. The detected noise value may be read back through register 7Fh ("status_noise"). If the detected noise value is greater than "noise_thresh", then register bit 3C.3h ("noisy") is set. Larger values of "status_noise" indicate noisier signals, so larger values of |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | "noise_thresh" decreases the likelihood of "noisy" being set while smaller values of "noise_thresh" increases the likelihood of "noisy" being set. |

AGC_GATE_THRESHOLD and ADC_SWAP Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 06h | 0 | R/W | **7** | adc_updn_swap | This bit swaps the DC clamp up/down controls to the analog front-end.<br>0 = Disabled (default)<br>1 = Enabled |
| | 0 | R/W | **6** | adc_input_swap | This bit swaps the MSBs and LSBs from the analog front-end's ADC<br>0 = Disabled (default)<br>1 = Enabled |
| | 0 | R/W | **5** | adc_cbcr_pump_swap | This bit swaps the Pb/Pr charge pump pairs to the analog front-end<br>0 = Disabled (default)<br>1 = Enabled |
| | 0Ah | R/W | **4:0** | agc_gate_thresh | This specifies the threshold at which the rough gate generator creates a sync gate. |

Output Control Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 07h | 1 | R/W | **7** | ccir656_en | This bit enable the CCIR656 output |
| | 0 | R/W | **6** | cbcr_swap | This bit swaps Cb/Cr outputs.<br>0 = don't swap Cb/Cr (default)<br>1 = swap Cb/Cr |
| | 10b | R/W | **5:4** | blue_mode | This bit controls the blue screen mode.<br>00 = Disabled<br>01 = Enabled<br>10 = Auto (Default)<br>11 = Reserved |
| | 0 | R/W | **3:0** | yc_delay | This 2's complement number controls the output delay between luma and chroma.<br>Negative values shift luma outputs to the left while positive values shift luma values to the right. The range is [-5, 7]. |

Luma Contrast Adjustment Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 08h | 80h | R/W | 7:0 | contrast | These bits control the adjustable gain to the luma output path. |

Luma Brightness Adjustment Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 09h | 20h | R/W | 7:0 | brightness | These bits control the adjustable brightness level to the luma output path. This value is offset by -32, i.e., a value of 32 (the default) implies a brightness level of 0, and a value of 0 implies a brightness level of -32. |

Chorma Saturation Adjustment Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 0Ah | 80h | R/W | 7:0 | saturation | These bits adjust the colour saturation (default = 128). |

Chorma Hue Phase Adjustment Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 0Bh | 00h | R/W | 7:0 | hue | This 2's complement number adjusts the hue phase offset. |

Chorma AGC Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 0Ch | 8Ah | R/W | 7:0 | cagc | These bits set the chroma AGC target (default = 138). |

Chorma Kill Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 0Dh | 00b | R/W | 7:6 | user_ckill_mode | Mode 0 uses auto hardware chroma kill, Mode 1 forces chroma kill on and Mode 2 forces chroma kill off (default=0) |
| | 0 | R/W | 5 | vbi_ckill | When set, chroma is killed during VBI (default = 0) |
| | 0 | R/W | 4 | hlock_ckill | When set, chroma is killed whenever horizontal lock is lost (default = 0) |
| | 7h | R/W | 3:0 | chroma_kill | These bits set the chroma kill level (default = 7) |

Non-Standard H/V Config Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 0Eh | 0h | R/W | 7:4 | vnon_std_threshold | These bits specify the threshold value for when WT8871S-C/WT8871S-E will consider the vertical frequency input signal a non-standard signal. This will turn-on the vnon_standard status register bit and can be use to turn off the 3D comb filter. (default = 0) |
| | 6h | R/W | 3:0 | hnon_std_threshold | These bits specify the threshold value for when WT8871S-C/WT8871S-E will consider the horizontal frequency input signal is a non-standard signal. This will turn-on the hnon_standard status register bit and can be use to turn off the 3D comb filter. (default = 6) |

Chorma Auto Position Registe - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 0Fh | 00b | R/W | 7:6 | nstd_hysis | These bits specified the hystersis loop use for the non-standard signal detection. These bits should be use together with the "non_standard_threshold" register. This register sets the number of continuous lines use to determine the status of non-standard signal detection. This is use to reduce the frequent change in the non-standard signal status flag due to weak and noisy signal.<br>When nstd_hysis =<br>0x00 = 256 lines (defaults)<br>0x01 = 512 lines<br>0x10 = 768 lines<br>0x11 = 1024 lines |
| | 1 | R/W | 5 | fixed_burstgate | When set, this bit disables the burst gate autoposition. The manual burstgate window position is defined by the burst_gate_start (0x2c) and burst_gate_end (0x2d) register.<br>(default = 1) |
| | 0Ch | R/W | 4:0 | cautopos | These bits set the chroma burst gate position relative to the auto centre position<br>(default = 12) |

AGC Peak Nominal Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 10h | | | 7 | | Reserved |
| | 0Ah | R/W | 6:0 | agc_peak_nominal | These bits set the luma peak white detection's AGC nominal peak white value.<br>This value is added to 128 and then the result is multiplied by 4 (default = 10) |

AGC Peak and Gate Controls Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 11h | 1 | R/W | **7** | agc_gate_vsync_coarse | This bit forces coarse sync-tip and backporch gates to be used during vsync when VCRs are detected (default = 1). |
| | 0 | R/W | **6** | agc_gate_vsync_stip | This bit forces sync-tip clamping during vsync (default = 0). |

| | | | | | |
|---|---|---|---|---|---|
| | 00b | R/W | **5:4** | agc_gate_kill_mode | These bits determine the method that sync-tip and backporch gates are suppressed:<br>00 = off (default)<br>01 = enabled – if sync-tip gate is killed, kill backporch gate<br>10 = enabled – if sync-tip gate is killed, kill backporch gate, except during vsync<br>11 = enabled – if sync-tip gate is killed, do not kill backporch gate |
| | 1 | R/W | **3** | agc_peak_en | This bit enables the AGC peak white detector (default = 1) |
| | 001b | R/W | 2:0 | agc_peak_cntl | These bits set the time constant for the AGC peak white detector (default = 1) |

AGC_GATE_START Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 12h | | | 7:3 | | Reserved |
| | 101b | R/W | **2:0** | agc_gate_start[10:8] | These high-order bits set the delay from the detected hsync for the rough gate generator |
| 13h | C8h | R/W | **7:0** | agc_gate_start[7:0] | These low-order bits set the delay from the detected hsync for the rough gate generator.<br>Default = C8h |

AGC_GATE_WIDTH Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 14h | | | 7 | | Reserved |
| | 38h | R/W | 6:0 | agc_gate_width | These bits set the width of the rough gates.<br>Default = 38h |

AGC_BP_DELAY Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 15h | 58h | R/W | 7:0 | agc_bp_delay | These bits set the time delay from the sync tip gate to the backporch gate for the rough gate generator. |

Lock Count Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 16h | 7h | R/W | 7:4 | locked_count_noisy_max | These bits set the max value of the hlock sensor for noisy signals. 8 is added to this value. (default = 7 →15) |
| | 4h | R/W | 3:0 | locked_count_clean_max | These bits set the max value of the hlock sensor for clean signals. 8 is added to this value. (default = 4 →12) |

H Loop MaxState Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 17h | 11b | R/W | 7:6 | hlock_vsync_mode | These bits control hsync locking during vsync:<br>00 = disabled<br>01 = enabled<br>10 = enabled except for noisy signals<br>11 = enabled only for VCR signals (default) |
| | 0 | R/W | 5 | hstate_fixed | This bit when set forces the state machine to remain in the state set in “hstate_max”<br>(default = 0) |
| | 0 | R/W | 4 | disable_hfine | This bit, when set, disables the fine mode of the HPLL phase comparator. (default = 0) |
| | 1 | R/W | 3 | hstate_unlocked | This bit sets the state when unlocked (default = 1) |
| | 011b | R/W | 2:0 | hstate_max | These bits set the maximum state for the horizontal PLL state machine. The range of this register is 0 to 5, inclusive. Higher states have a finer PLL control. Values of “0” and “1” should not programmed into this register. If “hstate_fixed” is set, then this register is used to force the state. (default = 3). |

Chroma DTO Increment Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 18h | 0 | R/W | 7 | cdto_fixed | This bit, when set, fixes the chroma DTO at its centre frequency. |
| | | | 6 | | Reserved |
| | 26h | R/W | 5:0 | cdto_inc[29:24] | These bits contain bits 29:0 of the 30-bit-wide chroma DTO increment. |
| 19h | 2Eh | R/W | 7:0 | cdto_inc[23:16] | |
| 1Ah | 8Bh | R/W | 7:0 | cdto_inc[15:8] | |
| 1Bh | A2h | R/W | 7:0 | cdto_inc[7:0] | |

Horizontal Sync Increment Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 1Ch | 0 | R/W | 7 | hdto_fixed | This bit, when set, fixes the horizontal sync DTO at its centre frequency (default = 0) |
| | 0 | | 6 | | Reserved |
| | 24h | R/W | 5:0 | hdto_inc[29:24] | These bits contain bits 29:0 of the 30-bit-wide horizontal sync DTO increment. |
| 1Dh | 00h | R/W | 7:0 | hdto_inc[23:16] | |
| 1Eh | 00h | R/W | 7:0 | hdto_inc[15:8] | |
| 1Fh | 00h | R/W | 7:0 | hdto_inc[7:0] | |

Horizontal Sync Rising-Edge Occurrence Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 20h | 3Eh | R/W | 7:0 | hsync_rising | These bits set the position of the expected hsync rising edge. It is used by the fine hsync detector. The fine detector uses this time position to sample the video signal for the rising edge of the hsync. (Default = 62) |

Horizontal Sync Phase Offset Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 21h | 3Eh | R/W | 7:0 | hsync_phase_offset | This register sets the offset value between the coarse hsync detector and the fine hsync detector. Nominally set to 62. The course detector actually finds the middle of the hsync so we need to subtract the nominal hsync width to find the beginning of the hsync. (Default = 62) |

Horizontal Sync Detect Window Start Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 22h | 00h | R/W | 7:0 | hsync_gate_start | These bits control the PLL horizontal sync detect window for coarse sync detection.<br>This specifies the beginning of the window. |

Horizontal Sync Detect Window End Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 23h | 80h | R/W | 7:0 | hsync_gate_end | These bits control the PLL horizontal sync detect window for coarse sync detection.<br>This specifies the end of the window. (Default = 128) |

Horizontal Sync Tip Detect Window Start Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 24h | E9h | R/W | 7:0 | hsync_tip_start | These bits control the PLL horizontal sync tip detect window used for AGC control. This specifies the beginning of the window.<br>MSB is sign bit, “0” means positive, “1” means negative (Default = -23) |

Horizontal Sync Tip Detect Window End Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| 25h | 0Fh | R/W | 7:0 | hsync_tip_end | These bits control the PLL horizontal sync tip detect window used for AGC control. This specifies the end of the window. (Default = 15) |

Horizontal Sync Rising-Edge Detect Window Start Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 26h | 2Dh | R/W | 7:0 | hsync_rising_start | These bits provide a programmable start time of the window that looks for the rising edge of the hsync. This is used by the coarse hsync detector. (Default = 45) |

Horizontal Sync Rising-Edge Detect Window End Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 27h | 50h | R/W | 7:0 | hsync_rising_end | These bits provide a programmable end time for the window which spans across the rising-edge of the horizontal sync pulse. (Default = 80) |

Backporch Interval Start Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 28h | 22h | R/W | 7:0 | backporch_start | These bits control the backporch detect window. This specifies the beginning of the window. (Default = 34) |

Backporch Interval End Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 29h | 4Eh | R/W | 7:0 | backporch_end | These bits control the backporch detect window. This specifies the end of the window. (Default = 78) |

Hsync Filter Gate Start Time Register Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 2Ah | D6h | R/W | 7:0 | hblank_start | These bits specify the beginning of the horizontal-blank-interval window. (Default = -42) |

Hsync Filter Gate End Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 2Bh | 4Eh | R/W | 7:0 | hblank_end | These bits specify the end of the horizontal-blank-interval window. (Default = 78) |

Chroma Burst Gate Start Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 2Ch | 32h | R/W | 7:0 | burst_gate_start | This specifies the beginning of the burst gate window. Note that this window is set to be bigger than the burst. The automatic burst position tracker finds the burst within this window. (Default = 50) |

Chroma Burst Gate End Time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 2Dh | 46h | R/W | 7:0 | burst_gate_end | These bits specifies the end of the burst gate window. (Default = 70) |

Active video Horizontal start time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 2Eh | 82h | R/W | 7:0 | hactive_start | These bits control the active video line time interval. This specifies the beginning of active line. This register is used to centre the horizontal position, and should *not* be used to crop the image to a smaller size. (default = 130) |

Active video Horizontal Width Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 2Fh | 50h | R/W | 7:0 | hactive_width | These bits control the active video line time interval. This register |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | specifies the width of the active line, and should *not* be used to crop the image to a smaller size. The value 640 is added to this register. (default = 80 → 640+80=720) |

Active video vertical start time Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 30h | 22h | R/W | 7:0 | vactive_start | These bits control the first active video line in a field.<br>This specifies the number of half lines from the start of a field.<br>(Default = 34) |

Active video vertical height Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 31h | 61h | R/W | 7:0 | vactive_height | These bits control the active video height. This specifies the height by the number of half lines. The value 384 is added to this register. (default = 97 → 394+97=481 half lines) |

Vsync H Lockout Start Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 32h | | | 7 | | Reserved |
| | 70h | R/W | 6:0 | vsync_h_min | This register defines the number of half-lines before the vsync that the hsync detector circuit is disabled. This is to make sure that the HPLL is not confused by the equalization pulses and the broad pulses. Also in VCR trick modes the VSYNC is just one 3 line wide pulse with no hsync structure so it must be ignored.<br>(Default = -16) |

Vsync H Lockout End Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 33h | | | 7 | | Reserved |
| | 0Eh | R/W | 6:0 | vsync_h_max | This register defines the number of half-lines after the vsync that the hsync detector circuit is re-enabled. (Default = 14) |

Vsync AGC Lockout Start Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 34h | | | 7 | | Reserved |
| | 6Ch | R/W | 6:0 | vsync_agc_min | This register defines the number of half-lines before the vsync that the AGC, SYNCTIP, and BACKPORCH gates are disabled.<br>(Default = -20) |

Vsync AGC Lockout End Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 35h | 11b | R/W | 7:6 | vsync_clamp_mode | These bits control DC clamping during the vertical blanking interval.<br>00 = disabled<br>01 = enabled<br>10 = enabled except for noisy signals<br>11 = enabled except for noisy signals and VCRs (default) |
| | 10h | R/W | 5:0 | vsync_agc_max | This register defines the number of half-lines after the vsync that the AGC, SYNCTIP, and BACKPORCH gates are re-enabled.<br>(Default = 16) |

Vsync VBI Lockout Start Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 36h | | | 7 | | Reserved |
| | 7Ah | R/W | 6:0 | vsync_vbi_min | This register defines the number of half-lines before the VSYNC that VBI data is valid. (Default = -16) |

Vsync VBI Lockout END Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 37h | 0 | R/W | 7 | vlock_wide_range | This register controls whether a wide or a narrow vertical locking range should be used:<br>Default = 0 (narrow) |
| | 20h | R/W | 6:0 | vsync_vbi_max | This register defines the number of half-lines after the VSYNC that VBI data is valid. (Default = 14 ??) |

VSYNC_CNTL Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 38h | 00b | R/W | 7:6 | vsync_cntl | These bits set the vsync output mode<br>00 = output the vertical PLL vsync when the signal is noisy; otherwise use directly derived vsync (default)<br>01 = output the directly detected vsync<br>10 = output the vertical PLL derived vsync<br>11 = output the PLL vsync in alternate mode |
| | 00h | R/W | 5:0 | vsync_thresh | This register specifies a relative threshold to add to the slice level for the purpose of vsync detection.<br>Default = 0 (2's complement value) |

VSYNC_TIME_CONSTANT Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 39h | 0 | R/W | 7 | field_polarity | This bit sets the output field polarity.<br>0 → field=1 for odd fields, field=0 for even fields (default)<br>1 → field=0 for odd fields, field=1 for even fields |
| | 0 | R/W | 6 | flip_field | This bit flips even/odd fields |
| | 0 | R/W | 5 | veven_delayed | This bit delays detection of even fields by 1 vertical line (default = 0) |
| | 0 | R/W | 4 | vodd_delayed | This bit delays detection of odd fields by 1 vertical line (default = 0) |
| | 10b | R/W | 3:2 | field_detect_mode | These bits control the field detection logic. (default = 2) |
| | 10b | R/W | 1:0 | vloop_tc | These bits set the vertical PLL time constant<br>0 = fast. Only useful if the vloop_cntl register is not 11. Internal values are 2 and 1.<br>1 = moderate. Internal values are 1 and ¼.<br>2 = slow. Internal values are ½ and 1/16 (default)<br>3 = very slow. Most useful for noisy signals. Internal values are ¼ and ½ |

Status Register 1 Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 3Ah | | R | 7:5 | mv_colourstripes | Macrovision colour stripes detected. The number indicates the number of colour stripe lines in each group |
| | | R | 4 | mv_vbi_detected | MacroVision VBI pseudo-sync pulses detection<br>1 = Detected<br>0 = Undetected |
| | | R | 3 | chromalock | Chroma PLL locked to colour burst<br>1 = Locked<br>0 = Unlocked |
| | | R | 2 | Vlock | Vertical lock<br>1 = Locked<br>0 = Unlocked |
| | | R | 1 | Hlock | Horizontal line locked<br>1 = Locked<br>0 = Unlocked |
| | | R | 0 | no_signal | No signal detection<br>1 = No Signal Detected<br>0 = Signal Detected |

Status Register 2 Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 3Bh | | R | 7:3 | | Reserved |
| | | R | 2 | vnon_standard | Vertical frequency non-standard input signal Detected |
| | | R | 1 | hnon_standard | Horizontal frequency non-standard input signal Detected |
| | | R | 0 | proscan_detected | Progressive Scan Detected |

Status Register 3 Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 3Ch | | R | 7 | vcr_rew | VCR Rewind Detected |
| | | R | 6 | vcr_ff | VCR Fast-Forward Detected |
| | | R | 5 | vcr_trick | VCR Trick-Mode Detected |
| | | R | 4 | vcr | VCR Detected |
| | | R | 3 | noisy | Noisy Signal Detected. This bit is set when the detected noise value (status register 7Fh) is greater than the value programmed into the “noise_thresh” register (05h). |
| | | R | 2 | 625lines_detected | 625 Scan Lines Detected |
| | | R | 1 | SECAM_detected | SECAM Colour Mode Detected |
| | | R | 0 | PAL_detected | PAL Colour Mode Detected |

Horizontal Sync DTO Increment Status Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 70h | | | 7:6 | | Reserved |
| | | R | 5:0 | status_hdto_inc[29:24] | These bits contain status of the 30-bit-wide horizontal sync DTO increment. |
| 71h | | R | 7:0 | status_hdto_inc[23:16] | |
| 72h | | R | 7:0 | status_hdto_inc[15:8] | |
| 73h | | R | 7:0 | status_hdto_inc[7:0] | |

Chorma Sync DTO Increment Status Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 74h | | | 7:6 | | Reserved |
| | | R | 5:0 | status_cdto_inc[29:24] | These bits contain status of the 30-bit-wide chroma sync DTO increment. |
| 75h | | R | 7:0 | status_cdto_inc[23:16] | |
| 76h | | R | 7:0 | status_cdto_inc[15:8] | |
| 77h | | R | 7:0 | status_cdto_inc[7:0] | |

AGC Analog Gain Status Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 78h | | R | 7:0 | status_agc_again | These bits contain the analog AGC gain value. |

AGC Digital gain Status Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 79h | | R | 7:0 | status_agc_dgain | These bits contain the digital AGC gain value. |

Chroma magnitude Status Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 7Ah | | R | 7:0 | status_cmag | These bits contain the chroma magnitude. |

Chroma Gain Status Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 7Bh | | | 7:6 | | Reserved |
| | | R | 5:0 | status_cgain[13:8] | These bits contain the 14 bits data of the chroma gain. |
| 7Ch | | R | 7:0 | status_cgain[7:0] | |

CORDIC Frequency Status Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 7Dh | | R | 7:0 | status_cordiq_frerq | These bits contain the SECAM cordic frequency. |

Noise Status Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 7Fh | | R | 7:0 | status_noise | This registers indicates how noisy the signal is. Larger values indicate noisier signals. This register is used in conjunction with programmable register 05h, "noise_thresh" and status bit 3C.3h, "noisy". |

Luma Peaking Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 80h | | R/W | 7 | | Reserved |
| | 0 | R/W | 6 | secam_ybw | These bit set the SECAM luma notch filter bandwidth<br>0 = narraw (default)<br>1 = wide |
| | 00b | R/W | 5:4 | peak_range | These bits set the range of peak_gain.<br>Setting peak_range value<br>00 1 (default)<br>01 2<br>10 4<br>11 8<br>Ypeak = Y + YH *(peak_gain/peak_range) where Y is the luma and YH is the high frequency luma only |
| | 010b | R/W | 3:1 | peak_gain | These bits set the gain for the luma horizontal peaking control. This allows adjustable gain to the luma around the colour subcarrier frequency (default = 2). |
| | 0 | R/W | 0 | peak_en | This bit enables the luma horizontal peaking control around the colour subcarrier<br>frequency<br>0 = Disabled (default)<br>1 = Enabled |

Comb Filter Config Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 82h | 1 | R/W | 7 | sv_bf | This bit is used to enable the chroma signal to bypass the bandpass filter in the YC separator during s-video mode. When set to 1, the chroma signal will run through the bandpass filter, when set to 0, the chroma signal will bypass the bandpass filter. For composite video mode. This bit should always set to 1. (default=1) |
| | | | 6:2 | | Reserved |

| | | | | | |
|---|---|---|---|---|---|
| | 10b | R/W | 1:0 | palsw_level | This bit is used to determine how many incorrect lines are used for the pal switch circuit before switching. Use a higher level for noisy signals. (default = 2). |

Chroma_Lock_Config Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 83h | 6h | R/W | 7:4 | lose_ chromalock_ count | This register is used to tune the chromakill, higher values are more sensitive to losing lock (default = 6). |
| | 111b | R/W | 3:1 | lose_ chromalock_ level | Set the level for chromakill (default = 7). |
| | 1 | R/W | 0 | lose_ chromalock_ ckill | When set, chroma is killed whenever chromlock is lost (default = 1). |

Vsync select Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 84h | | | 7:6 | | Reserved |
| | 0 | R/W | 5:3 | vsync_derived_sel | 0: counter - 80<br>1: counter<br>2: counter – 1<br>3: counter – 2 (recommend)<br>4~: counter - 4 |
| | 0 | R/W | 2:0 | vsync_real_sel | 0: counter - 80<br>1: counter<br>2: counter – 1<br>3: counter – 2 (recommend)<br>4~: counter - 4 |

Y Clamp UP/DN Value Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 85h | | | 7 | | Reserved |
| | | R | 6:0 | y_sat_abs_level_latch | Y clamp up or down value within a line |

CB Clamp UP/DN Value Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 86h | | | 7 | | Reserved |
| | | R | 6:0 | cb_sat_abs_level_latch | Cb clamp up or down value within a line |

CR Clamp UP/DN Value Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 87h | | | 7 | | Reserved |
| | | R | 6:0 | cr_sat_abs_level_latch | Cr clamp up or down value within a line |

Chroma Loop Filter State Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 8Ah | | | 7:4 | | Reserved |
| | 101b | R/W | 3:1 | cstate | This register sets the chroma loopfilter bandwidth state, larger state has a slower response. (default = 5) |
| | 0 | R/W | 0 | Fixed_cstate | This register fixes the state of chroma loopfilter to cstate. (default=0) |

External Hin/Vin Control Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 8Bh | | | 7:6 | | Reserved |
| | 0 | R/W | 3 | sogin_sel | Enable external sync input |
| | 0 | R/W | 2 | est_hsync_pol | Polarity select |
| | 0 | R/W | 1 | ext_vsync_pol | Polarity select |
| | 1 | R/W | 0 | Hreasampler_2up | Upsample the chroma by 2 before going into the hresampler. (default = 1) |

Charge Pump Delay Control Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 8Dh | 0 | R/W | 7 | cpump_delay_en | Enable delay of charge-pump up/down pulses.<br>Default = 0 (disabled) |
| | 0 | R/W | 6 | cpump_adjust_polarity | Polarity of adjustment used to compensate for possible visible artefacts caused by charge-pump pulses.<br>Default = 0 (normal polarity). |
| | 0Ah | R/W | 5:0 | cpump_adjust_delay | Delay, relative to charge-pump pulses, before adjustment, used to compensate for possible visible artefacts caused by charge-pump pulses, is applied.<br>Default = 10. |

Charge Pump Adjustment Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 8Eh | C8h | R/W | 7:0 | cpump_adjust | Value used to compensate for possible visible artefacts caused by charge-pump pulses. (Default = 200) |

Charge Pump Delay Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 8Fh | B9h | R/W | 7:0 | cpump_delay | If “cpump_delay_en == 1”, then the charge pump up/down pulses are delayed by “4 x cpump_delay” output pixels.<br>Default = 185→740 output pixel delay. |

RESET Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 3Fh | | | 7:1 | | Reserved |
| | 0 | W | 0 | soft_rst | Soft Reset |

Auto Mode Detection Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 90h | 04h | R/W | 7:0 | auto_mode_time_constant | the number of vsync delays for auto mode change |

Clamping Noise Reduction Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 91h | | | 7:6 | | Reserved |
| | 0 | W | 5:4 | iir_filter_sel | Clamping noise reduction filter selection |
| | | | 3 | | Reserved |
| | 3h | W | 2:0 | clamping scale | The amount of clamping up/dn |

Clamping Noise Reduction Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| 92h | 0 | R/W | 7:0 | adc_clamp_restore_thr | The threshold to enable clamping up/du mechanism |

2D Comb Noise Threshold Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| AFh | 0 | R/W | 7 | noise_th_en | This bit enable the use of the noise detector value as the threshold value used to determine the best set of adaptive coefficients to be used. (Default = 0) |
| | 0Ah | R/W | 6:0 | noise_th | These register bits specified the noise threshold used to determine the set of adaptive coefficients to be used. If the noise_th_en bit is disabled, this value is directly used as the threshold value. If the nosie_th_en bit is enable, this value is added to the value from the noise detector before it is used. (Default = 10) |

2D Comb Adaptive Gain Control Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| B0h | 11b | R/W | 7:6 | horiz_diff_cgain | These register bits specified the weight for the chroma change in horizontal chroma transition to be used in the adaptive algorithm. Increase this value will make the adaptive comb filter to be more sensitive to the horizontal chroma change such as vertical color bar test pattern. This will tune the adaptive comb filter to be more favourable to the vertical comb filter mode for the chroma output. (Default = 3) |
| | 11b | R/W | 5:4 | horiz_diff_ygain | These register bits specified the weight for the luma change in horizontal luma transition to be used in the adaptive algorithm. Increase this value will make the adaptive comb filter to be more sensitive to the horizontal luma change such as vertical black and write bar test pattern. This will tune the adaptive comb filter to be more favourable to the vertical comb filter mode for the luma output. (Default = 3) |
| | 10b | R/W | 3:2 | chroma_vdiff_gain | These register bits specified the weight for the chroma change in vertical color transition. Increase this value will make the adaptive comb filter to be more sensitive to the vertical chroma change such as horizontal color bar test pattern. This will tune the adaptive comb filter to be more favourable to the bandpass filter mode. (Default = 2) |
| | 10b | R/W | 1:0 | lowfreq_vdiff_gain | These register bits specified the weight for the low frequency luma change in vertical luma transition to be used in the adaptive algorithm. Increase this value will make the adaptive comb filter to be more sensitive to the vertical low frequency luma change such as horizontal black and write bar test pattern. This will tune the adaptive comb filter to be more favourable to the notch filter mode. (Default = 2) |

2D Comb Adaptive Gain Control Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| B1h | 11b | R/W | 7:6 | vadap_burst_noise_th_gain | These register bits specified the weight of chroma noise threshold especially for luma burst signal and B/W signal. Increase for noisy signal. Default = 3 |
| | 11b | R/W | 5:4 | burst_noise_th_gain | These register bits specified the weight of luma noise threshold especially for luma burst signal and B/W signal. Increase for noisy signal. Default = 3 |
| | 11b | R/W | 3:2 | c_noise_th_gain | These register bits specified the weight of chroma path noise threshold. Increase for noisy signal. Default = 3 |
| | 11b | R/W | 1:0 | y_noise_th_gain | These register bits specified the weight of luma path noise threshold. Increase for noisy signal. Default = 3 |

Chroma Edge Enhancement Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| B5h | 0 | R/W | 7 | chroma_peak_en | This register bit enable the chroma edge enhancement cirucit. (Default = 0) |
| | 1 | R/W | 6 | chroma_coring_en | This register bit enables the coring function circuit which is used to eliminate the low level chroma noise such that the low amplitude noise will not be amplified. (Default = 1) |
| | | R/W | 5:2 | | Reserved |
| | 11b | R/W | 1:0 | chroma_peak | These register bits specified the peak gain for the chroma edge enhancement. Increase this value will increase the sharpness of the chroma edge. (Default = 3) |

Control Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| B6h | 0h | R/W | 7:4 | ldpause_threshold | These bits specify the threshold value for when WT8871S-C/WT8871S-E will consider the input signal a non-standard signal. This will turn-on the non_standard status register bit and can be use to turn off the 3D comb filter. (default = 0) |
| | | R/W | 3:2 | | Reserved |
| | 1 | R/W | 1 | vf_nstd_en | This bit enables the vertical frequency non-standard signal detection. If non-standard signals detected, the 3D-comb filter will be turned off automatically. (Default = 1) |
| | 0 | R/W | 0 | vcr_auto_switch_en | This bit enables the auto 3D comb filter turnoff mode when VCR signal detected. (Default = 0) |

2D Comb Filter and Notch Filter Gain Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| B7h | | R/W | 7 | | Reserved |
| | 000b | R/W | 6:4 | notch_gain | These register bits specified the gain for the notch filter in the luma path. Increase this value will increase the notch strength on the luma output at the expense of more dot crawl might be seen on the horizontal color transition and blurry image such as the vertical color bar test pattern. (Default = 0) |
| | | R/W | 3 | | Reserved |
| | 000b | R/W | 2:0 | comb_gain | These register bits specified the gain for the comb filter in the luma path. Increase this value will increase the comb strength on the luma ouput at the expense of more dot-crawl might be seen on the vertical color transition such as the horizontal color bar test pattern. (Default = 0) |

Active Video Vertical Start for Frame Buffer Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| BAh | 21h | R/W | 7:0 | vactive_fb_start | These bits control the first active video line in a field to write to the field buffer memory for the 3D comb filter. This specifies the number of half-lines from the start of a field. (Default = 33) |

Active Video Vertical Height for rame Buffer Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| BBH | 60h | R/W | 7:0 | vactive_fb_height | These bits control the active video height for data writing to the field buffer memory for the 3D comb filter. This specifies the height by the number of half lines. The value 384 is added to this register.<br>(default = 97 → 384+97=481 half lines) |

Hsync Pulse Config Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| BCh | | | 7:4 | | Reserved |
| | 0h | R/W | 3:0 | hsync_pulse_width | These bits define the width of the output hysnc pulse |

VBI WSS Data 0 Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| BDh | 0 | R | 7 | no_signal_path_sel | no signal selection for sync separator block itself<br>0 = no_signal generated from sync separator itself<br>1 = no_signal status bit from register 0x3A[0] |
| | 0 | R | 6 | free_run_27m | clock output selection<br>0 = line locked clock<br>1 = free run clock |
| | 0 | | 5 | | Reserved |
| | 1 | R | 4 | VBI_in_CCIR656 | Insert VBI raw data in CCIR656 ancillary data portion<br>0 = disabled<br>1 = enabled |
| | 0 | R | 3 | CCIR656_eav_sav_phase | CCIR656 vibration absorption selection<br>0 = line vibration absorption from eav to sav<br>1 = line vibration absorption from eav to sav |
| | 0 | R | 2 | vsync_out_polority | Inverse VOUT, vsync output polarity |
| | 0 | R | 1 | hsync_out_polority | Inverse HOUT, hsync output polarity |
| | 0 | R | 0 | clk_out_polority | Inverse 13.5/27M clock output polarity |

VBI WSS DATA 0 Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| BEh | | | 7:2 | | Reserved |
| | 0 | R/W | 1 | vactive_out_sel | Enable vactive output from DA1 |
| | 0 | R/W | 0 | hactive_out_sel | Enable hactive output from DA0 |

Input Level 1 Selection Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| C0h | | | 7 | | Reserved |
| | 0 | R/W | 6 | rgb_input | R/G/B input enable<br>0 = CVBS, S-video, Y/Pb/Pr input<br>1 = R/G/B input |
| | 0 | R/W | 5 | cvbs_out_disable | CVBS_OUT pin disable<br>0 = enable CVBS_OUT<br>1 = disable CVBS_OUT |
| | 01b | R/W | 4:3 | cvbs_out_sel | CVBS_OUT pin output selection<br>00 = from SOGI pin<br>01 = from channel A input<br>10 = from channel B input<br>11 = from channel C input |
| | 0 | R/W | 2 | chb_sel | Channel B of the first input level selection<br>0 = select AIN1 pin input (default)<br>1 = select AIN3 pin input |

| | | | | | |
|---|---|---|---|---|---|
| | 0 | R/W | 1:0 | cha_sel | Channel A of the first input level selection<br>00 = select AIN0 pin input (default)<br>01 = select AIN2 pin input<br>10 = select AIN4 pin input<br>11 = reserved |

Input Level 2 Selection Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| C1h | 10b | R/W | 7:6 | adc_current_sel | ADC drive current selection<br>00 = 25%<br>01 = 50%<br>10 = 75% (default)<br>11 = 100%l |
| | 11b | R/W | 5:4 | cb_ch_sel | Cb channel of the second input level selection<br>00 = reserved<br>01 = select CH a<br>10 = select CH b<br>11 = select CH c (default) |
| | 10b | R/W | 3:2 | c_ch_sel | C channel of the second input level selection<br>00 = reserved<br>01 = select CH a<br>10 = select CH b (default)<br>11 = select CH c |
| | 01b | R/W | 1:0 | y_ch_sel | Y channel of the second input level selection<br>00 = reserved<br>01 = select CH a (default)<br>10 = select CH b<br>11 = select CH c |

Output Selection Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| C2h | | R/W | 7 | | Reserved |
| | 1 | R/W | 6 | chc_on | CH c enable<br>0 = disable<br>1 = enable (default) |
| | | R/W | 5 | | Reserved |
| | 1 | R/W | 4 | chb_on | CH b enable<br>0 = disable<br>1 = enable (default) |
| | | R/W | 3 | | Reserved |
| | 1 | R/W | 2 | cha_on | CH a enable<br>0 = disable<br>1 = enable (default) |
| | 00b | R/W | 1:0 | adc_sample_clk | ADC sampling clock selection:<br>00 = 48MHz (default)<br>01 = 48Mhz<br>10 = 48MHz<br>11 = 96MHz |

Luma Enhancement Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| C3h | | R/W | 7:6 | | Reserved |

| | | | | | |
|---|---|---|---|---|---|
| | 00b | R/W | 5:4 | y_edge_enhance_range | These bits set the range of y_edge_enhance.<br>Setting edge_enhance_range value<br>00 1 (default)<br>01 2<br>10 4<br>11 8<br>Yedge_enhance = Y + YH *(edge_enhance_gain/edge_enhance_range) where Y is the luma and YH is the high frequency luma only |
| | 010b | R/W | 3:1 | y_edge_enhance_gain | These bits set the gain for the luma edge enhancement control. This allows adjustable gain (default = 2). |
| | 0 | R/W | 0 | y_edge_enhance_en | This bit enables the luma edge enhancement<br>0 = Disabled (default)<br>1 = Enabled |

Sync Separator Pre-coast Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| C4h | 00h | R/W | 7:0 | pre_coast | The sync separator hsync output is from virtual hsync but not source signals in the period of number of lines before Vsync (default = 0) |

Sync Separator Post-coast Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| C5h | 00h | R/W | 7:0 | post_coast | The sync separator hsync output is from virtual hsync but not source signals in the period of number of lines during Vsync (default = 4) |

Luma Peaking Coring Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| C6h | 0 | R/W | 7 | luma_coring_enable | Luma peaking coring enable<br>0 = disable (default)<br>1 = enable |
| | | R/W | 6:3 | | Reserved |
| | 000b | R/W | 2:0 | luma coring threshold | Luma peaking coring threshold level selection<br>000 = coring threshold level is set to 8<br>001 = coring threshold level is set to 16<br>010 = coring threshold level is set to 24<br>011 = coring threshold level is set to 32<br>100 = coring threshold level is set to 40<br>101 = coring threshold level is set to 48<br>110 = coring threshold level is set to 56<br>111 = coring threshold level is set to 64 |

Blue Stretch Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| C7h | 0 | R/W | 7 | blue_stretch_en | Blue stretch enable<br>0 = disable (default)<br>1 = enable |
| | 00b | R/W | 6:5 | blue_stretch_luma_threshold | Threshold level is selected for luma (Y) specifically.<br>00 = threshold level is set to 832 (decimal)<br>01 = threshold level is set to 768 (decimal)<br>10 = threshold level is set to 704 (decimal)<br>11 = threshold level is set to 640 (decimal) |

| | | | | | |
|---|---|---|---|---|---|
| | 00b | R/W | 4:3 | blue_stretch_ chroma_ threshold | Threshold level is selected for Cb / Cr specifically.<br>00 = threshold level is set to 16 ( 512 ± 16 )<br>01 = threshold level is set to 32 ( 512 ± 32 )<br>10 = threshold level is set to 48 ( 512 ± 48 )<br>11 = threshold level is set to 64 ( 512 ± 64 ) |
| | 000b | R/W | 2:0 | blue_stretch_ amount | Blue stretching amount to be processed.<br>000 = amount is set to 16<br>001 = amount is set to 32<br>010 = amount is set to 48<br>011 = amount is set to 64<br>100 = amount is set to 80<br>101 = amount is set to 96<br>110 = amount is set to 112<br>111 = amount is set to 128 |

Skin Tone Adjustment Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| C8h | 0 | R/W | 7 | skin_tone_adj _en | Skin tone adjustment enable<br>0 = disable (default)<br>1 = enable |
| | | | 6:2 | | Reserved |
| | 00b | R/W | 1:0 | skin_tone_typ e sel | Skin tone adjustment type selection<br>00 = type 1 - window (0, -0.5, 0.3, 0.6)<br>01 = type 2 - window (0, -0.5, 0.3, 0.6) + (0, -0.25, 0.2, 0.8)<br>10 = type 3 - window (0, -0.5, 0.3, 0.6) + (0, -0.25, 0.2, 0.8) + (0, -0.6, 0.3, 0.5)<br>11 = type 4 - window (0, -0.5, 0.3, 0.6) + (0, -0.25, 0.2, 0.8) + (0, -0.6, 0.3, 0.5) + (0, -0.7, 0.4, 0.5) |

ADC Control Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| C9h | | | 7:5 | | Reserved |
| | 0 | R/W | 4 | en_vos | Enable offset voltage |
| | 1 | | 3 | | Reserved |
| | 0 | R/W | 2 | adc_hsync_ba ckup_en | Clamped Y signal's hsync tip source<br>0 = original ADC's signal (default)<br>1 = hsync sync tip is made by SOG's estimation |
| | | | 1 | | Reserved |
| | 0 | R/W | 0 | lbf_filter_en | Enable input low pass filter |

SOG Control Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| CAh | 0 | R/W | 7 | fix_sog_settin g | fix_sog sog_threshold and sog_amplifier settings<br>0 = disable, the sog_threshold and sog_amplifier are auto set by hardware (default)<br>1 = enable, the settings are fixed by sog_threshold and sog_amplifier registers |
| | 00b | R/W | 6:5 | sog_amplifier | SOG amplifier multiple<br>00 = multiply 3 (default)<br>01 = multiply 5<br>10 = multiply 9<br>11 = multiply 17 |
| | 14h | R/W | 4:0 | sog_threshold | SOG threshold. (default=14 h) |

ADC Clamp Placement Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| CBh | 10h | R/W | 7:0 | ad_clplace | Clamp Placement |

ADC Clamp Duration Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| CCh | 10h | R/W | 7:0 | ad_cldur | Clamp Duration |

ADC Channel A Gain Adjust Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| CDh | FFh | R/W | 7:0 | adc_gain | ADC gain adjust |

ADC Channel A Offset Adjust Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| D0h | | | 7:6 | | Reserved |
| | 1Fh | R/W | 5:0 | ch_a_offset | Channel A offset adjust |

ADC Channel B Offset Adjust Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| D1h | | | 7:6 | | Reserved |
| | 1Fh | R/W | 5:0 | ch_b_offset | Channel B offset adjust |

ADC Channel C Offset Adjust Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| D2h | | | 7:6 | | Reserved |
| | 1Fh | R/W | 5:0 | ch_c_offset | Channel C offset adjust |

Hsync_feedback Pulse Control Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| D3h | 0 | R/W | 7 | hsync_path_sel | Hsync Path Select for CCIR656 encoder and scaler<br>0 = original Hsync_27M (cvd2 path) (default)<br>1 = Hsync_feedback + HS_DEL (SOG, PLL path) |
| | 0 | R/W | 6 | adc_hsync_polarity | ADC Hsync Polarity control, Hi for positive, Lo for negative (edge as starting counting for ClPlace[7:0] |
| | 0 | R/W | 5 | half_delay_sel | Hsync path delay for CCIR656 encoder and scaler to enhance Hsync robustness<br>0 = No delay (default)<br>1 = 0.5 clock cycle (27M) delay |
| | 0 | R/W | 4 | hactive_path_sel | hactive Path Select<br>0 = original hactive_27M (cvd2 path) (default)<br>1 = Hsync_feedback + HS_DEL + hactive_start_pll + hactive_width_pll (SOG, PLL path) |
| | 0h | R/W | 3:0 | sog_hsync_delay_pulse_width | pulse width control for Hsync_feedback (SOG, PLL path), working associated with HS_DEL register |

HS_DEL Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| D4h | 00h | R/W | 7:0 | HS_DEL[7:0] | Number of clocks delay applied for Hsync (SOG, PLL path), working associated with Hsync Pulse Control register (0xD3), it's working when bit 7 and bit 6 of register 0xD3 are set |

HS_DEL and MISC Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| D5h | 0 | R/W | 7 | adc_clamp_hsync_sel | ADCs clamp hsync source selection:<br>0 = select Sync Seperator hsync<br>1 = select internal hsync |
| | 0 | R/W | 6 | Sync_sep_hsync_polarity | Hsync Polarity control for Sync Separator output for PLL27M<br>0 = Sync Separator output positive Hsync (active high) (default)<br>1 = Sync Separator output negative Hsync (active low) |
| | | R/W | 5:3 | | Reserved |
| | 1 | R/W | 2 | hsync_path_sel_pll27M | hsync Path Select for PLL27M<br>0 = select hsync decoded from SOG path<br>1 = select hsync decoded from cvd2 path (default) |
| | 00b | R/W | 1:0 | HS_DEL[9:8] | Number of clocks delay applied for Hsync (SOG, PLL path), working associated with Hsync Pulse Control register (0xD3), it's working when bit 7 and bit 6 of register 0xD3 are set |

Self Test Pattern Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| D6h | 0 | R/W | 7 | self_test_pattern_en | CCIR656 self test pattern selection enable:<br>0 = disable (default)<br>1 = enable |
| | | R/W | 6:3 | | Reserved |
| | 000b | R/W | 2:0 | self_test_pattern | CCIR656 self test pattern selection:<br>000 = colour bar (default)<br>001 = grey level<br>002 = white screen<br>003 = black screen<br>004 = red screen<br>005 = green screen<br>006 = blue screen |

Digital ADC Clamp Time Constant Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| D7h | | R/W | 7:3 | | Reserved |
| | 000b | R/W | 2:0 | adc_clamp_time_const | Time constant to adjust ADC clamp via digital method, smaller value get quicker clamping to correct level<br>0 = adjust every 1 pulse (Up / Down pulses)<br>1 = adjust every 2 pulses<br>2 = adjust every 4 pulses<br>3 = adjust every 8 pulses<br>4 = adjust every 16 pulses<br>5 = adjust every 32 pulses<br>6 = adjust every 64 pulses<br>7 = adjust every 128 pulses |

CCIR656 Width Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| D8h | 80h | R/W | 7:0 | ccir656_hactive_width | These bits control the active video line time interval for CCIR656 format output. This register specifies the width of the active line, and should *not* be used to crop the image to a smaller size. The value 640 is added to this register.<br>(default = 128 → 640+128=768) |

PLL_27M Divider Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| D9h | B4h | R/W | 7:0 | NF27M [7:0] | The 10 bits divider of PLL_27M |
| DAh | 01b | R/W | 1:0 | NF27M [9:8] | |
| | | | 7:2 | | Reserved |

The formula of this PLL_27M is

output freq. = ( NF27M[9:0] + 1024 ) * freq. of Hsync

| | Input Hsync | hpixel | Divider | Program value for AFE NF27M[9:0] | PLL output frequency | Remark |
|---|---|---|---|---|---|---|
| NTSC | 15.734 KHz | 00 | 1716 | 1716 – 1024 = 692 = 0x2B4h | 27 MHz | 13.5 MHz 525-line non-square pixel |
| | | 10 | 1560 | 1560 – 1024 = 536 = 0x218h | 24.54 MHz | 12.27 MHz 525-line square pixel |
| PAL / SECAM | 15.625 KHz | 01 | 1728 | 1728 – 1024 = 704 =0x2C0h | 27 MHz | 13.5 MHz 625-line non-square pixel |
| | | 11 | 1888 | 1888 – 1024 = 864 = 0x360h | 29.5 MHz | 14.75 MHz 625-line square pixel |

The actual divider is a 11-bit counter. MSB (bit 10) is always set, bit 9:0 are programmable. So the frequency multiplification range is from 1024 to 2047.

Misc. Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| DBh | | | 7 | | Reserved |
| | 0 | R/W | 6 | auto_detection_en | TV mode auto detection<br>0 = disable (default)<br>1 = enable |
| | 0 | R/W | 5 | special_reset_en | Automatic soft reset when vsync or hsync or chroma is unlock or no signal<br>0 = disable (default)<br>1 = enable |
| | 0 | | 4:1 | | Reserved |
| | 0 | R/W | 0 | pd | Power down mode<br>0 = disable (default)<br>1 = enable, enter power down mode<br>During power down mode only I2C, registers, XTAL alive |

Digital ADC Clamp Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| DCh | 0 | R/W | 7 | adc_clamp_threshold_en | The ADC clamp up/down pulse limit<br>0 = disable (default)<br>1 = enable |
| | 0Ah | R/W | 6:0 | adc_clamp_threshold | The limit value for the ADC clamp up/down pulse length that is valid when adc_clamp_threshold_en = 1 |

Digital ADC Clamp Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| DDh | | R | 7 | status_sync_sep_no_signal | no signal statue bit which is detected by sync_seperator |

| | | | | | |
|---|---|---|---|---|---|
| | | R | 6:5 | status_amplifier | These bits contain status bits of hardware SOG amplifier multiplier<br>00 = multiply by 3<br>01 = multiply by 5<br>10 = multiply by 9<br>11 = multiply by 17 |
| | | R | 4:0 | status_sog_threshold | These bits contain status bits of hardware SOG slice level automatic adjustment |

Digital ADC Clamp Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| DEh | 1 | R/W | 7 | adc_clamp_in_non_active_en | adc clamp during non active video region<br>0 = adc clamp in every hsync<br>1 = adc clamp only in hsync of non active |
| | | R/W | 6:4 | | Reserved |
| | 8h | R/W | 3:0 | adc_clamp_in_non_active_width | When the register adc_clamp_in_non_active_en = , this register sets the number of hsyncs before active video, during these hsyncs, the adc clamp up/dn is actived |

RGB Input Sync Height Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| DFh | | | 7:5 | | Reserved |
| | 1Ch | R/W | 4:0 | rgb_input_hsync_height | When R/G/B input, this register sets the height of the sync height |

Misc. Register - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| ECh | 0 | R/W | 7 | vcr_mode-dis | Disable this flag |
| | | | 6:3 | | Reserved |
| | 1 | R/W | 2 | vcr_free_run_27m_en | When VCR mode detected, the output clock are forced to free run 27MHz clock:<br>0 = disable<br>1 = enable |
| | 0 | R/W | 1 | no_clamp | ADC clamp behaviour selection:<br>0 = ADC with clamp<br>1 = ADC without clamp |
| | 1 | R/W | 0 | auto_no_clamp | No clamp during vsync for ADC selection:<br>0 = disable, the ADCs are always clamped<br>1 = enable, the ADCs are not clamped during vsync |

Rainbow Pattern Suppression Registers - Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| EDh | 0 | R/W | 7 | rainnow_suppress_en | Enabled to suppress rainbow pattern |
| | 05h | R/W | 6:0 | y_up_lo_diff_threshold | When the luma upper and lower pixels difference is larger than this value, the rainbow pattern suppression is activated |
| EEh | 0 | R/W | 7 | rainbow_band_coef | The 2D Y/C separation's bandpass filter coefficient is used as a factor to adjust rainbow pattern |
| | 05h | R/W | 6:0 | y_ri_le_diff_threshold | When the luma right and left pixels difference is larger than this value, the rainbow pattern suppression is activated |
| EFh | | | 7:6 | | Reserved |
| | 0 | R/W | 5 | pal_fix_en | PAL mode bug-fix enable |
| | | | 4 | | Reserved |

| | | | | | |
|---|---|---|---|---|---|
| | 0 | R/W | 3 | weight_en | weighting detection enable, uses weighting factor to select filter bandwidth automatically |
| | 0 | R/W | 2 | bpf_en | BPF enable (it should be turned off for S-video mode) |
| | 0 | R/W | 1 | 443m_sel | 4.43MHz/3.58MHz central freq. Selection |
| | 0 | R/W | 0 | wide_bw_sel | wide/narrow bandwidth selection |

Auto Mode Detection Registers- Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| F3h | EAh | R/W | 7:0 | auto_mode_FcMore_up_threshold | For adjust auto mode detection FcMore upper threshold |
| F4h | 20h | R/W | 7:0 | auto_mode_FcLess_lo_threshold | For adjust auto mode detection FcLess lower threshold |
| F5h | 40h | R/W | 7:0 | auto_mode_FcLess_up_threshold | For adjust auto mode detection FcLess upper threshold |
| F6h | D0h | R/W | 7:0 | auto_mode_FcMore_lo_threshold | For adjust auto mode detection FcMore lower threshold |

Misc. Registers- Page 0x60h

| Index | Default | R/W | Bit | Name | Description |
|---|---|---|---|---|---|
| FFh | 0h | R | 7:4 | standard_states | Auto standard mode detection results:<br>1 = YPbPr525<br>2 = YPbPr625<br>3 = NTSC<br>4 = PALI<br>5 = PALCN<br>6 = PALM<br>7 = PAL60<br>8 = NTSC443<br>9 = SECAM<br>Others = reserved |
| | 2h | R | 3:0 | chip_revision | Chip version |

# 5. Electrical Characteristics

## 5.1. Absolute Maximum Ratings

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| 5V Power supply voltage | -0.5 | 6.0 | V |
| 3.3V Power supply voltage | -0.5 | 3.8 | V |
| 2.5V Power supply voltage | -0.5 | 3.0 | V |
| DC voltage on I/O | $V_{SS}$ – 0.5 | $V_{DD33}$ + 0.5 | V |
| Operating ambient temperature (commercial use) | 0 | + 70 | ˚C |
| Operating ambient temperature (extending temp. range) | -20 | +80 | ˚C |
| Storage temperature | - 40 | +120 | ˚C |

***Note: Any other outside extending temp. range, please contact and discuss with us. Besides temperature, stresses above those listed may cause permanent damage to the devices.**

## 5.2. DC Characteristics

Ta=25℃

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD25}$ | 2.5V Supply Voltage | | 2.3 | 2.5 | 2.7 | V |
| $V_{DD33}$ | 3.3V Supply Voltage | | 3.1 | 3.3 | 3.5 | V |
| $V_{CC}$ | 5V Supply Voltage | | 4.75 | 5.0 | 5.25 | V |
| $I_{DD25}$ | 2.5V Operating current | | | 170 | | mA |
| $I_{DD33}$ | 3.3V Operating current | | | 10 | | mA |
| $I_{DD5}$ | 5V Operating current | | | 25 | | mA |
| $V_{IH}$ | Input high voltage | | $0.7V_{DD}$ | – | $V_{DD}$+0.3 * | V |
| $V_{IL}$ | Input low voltage | | $V_{SS}$-0.3 | – | $0.3V_{DD}$ | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = -6mA; $V_{DD33}$=3.3V | 2.4 | | | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 6mA; $V_{DD33}$=3.3V | | | 0.4 | V |
| $I_{OZ}$ | Tri-state leakage current | | – | – | ±1 | μA |

All GPIOs are CMOS 3-state output and 5V-tolerant input(except KP_ADC[3:0])

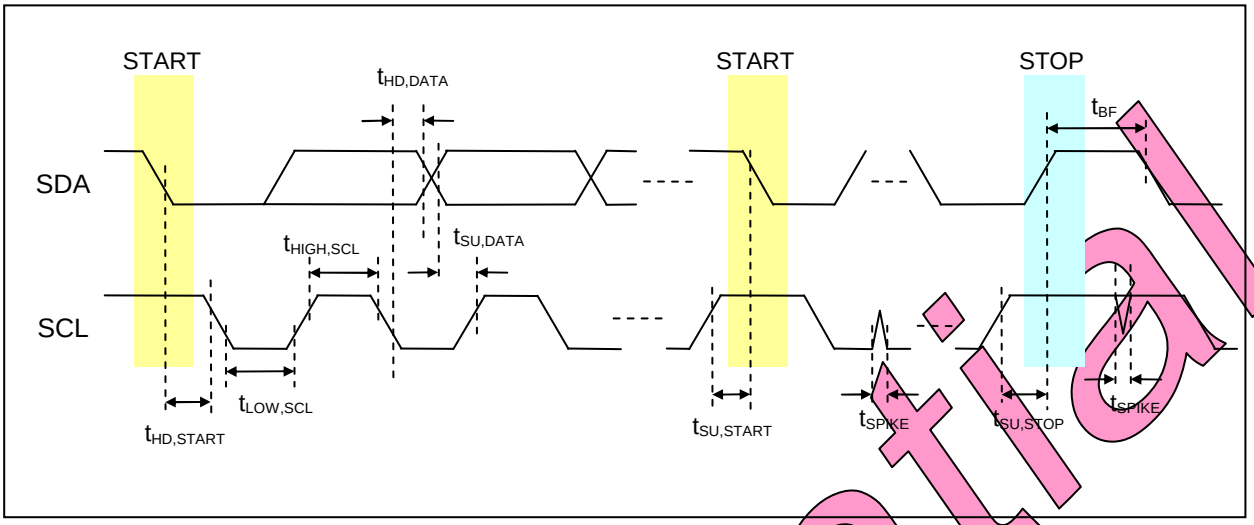
## 5.3. AC Characteristics

### 5.3.1. General

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| fosc | Oscillator frequency | | | 24 | | MHz |

### 5.3.2. $I^2C$ Interface

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL input clock frequency | 0 | - | 400 | KHz |
| $t_{BF}$ | Bus free time | 1 | – | – | us |
| $t_{HD,START}$ | Hold time for START condition | 0.6 | – | – | us |
| $t_{SU,START}$ | Set-up time for START condition | 0.6 | – | – | us |
| $t_{HIGH,SCL}$ | SCL clock high time | 0.6 | – | – | us |
| $t_{LOW,SCL}$ | SCL clock low time | 0.6 | – | – | us |
| $t_{HD,DATAI}$ | Hold time for DATA input | 0 | – | – | ns |
| $t_{HD,DATAO}$ | Hold time for DATA output | 80 | – | – | ns |
| $t_{SU,DATAI}$ | Set-up time for DATA input | 20 | – | – | ns |
| $t_{SU,DATAO}$ | Set-up time for DATA output | 100 | – | – | ns |
| $t_{RISE,I2C}$ | SCL and SDA rise time | – | – | 1 | us |
| $t_{FALL,I2C}$ | SCL and SDA fall time | – | – | 300 | ns |
| $t_{SU,STOP}$ | Set-up time for STOP condition | 0.6 | – | – | us |
| $t_{SPIKE}$ | Pulse width of spike that suppressed by input filter | – | – | 50 | ns |




### 5.3.3. BT.656 Input

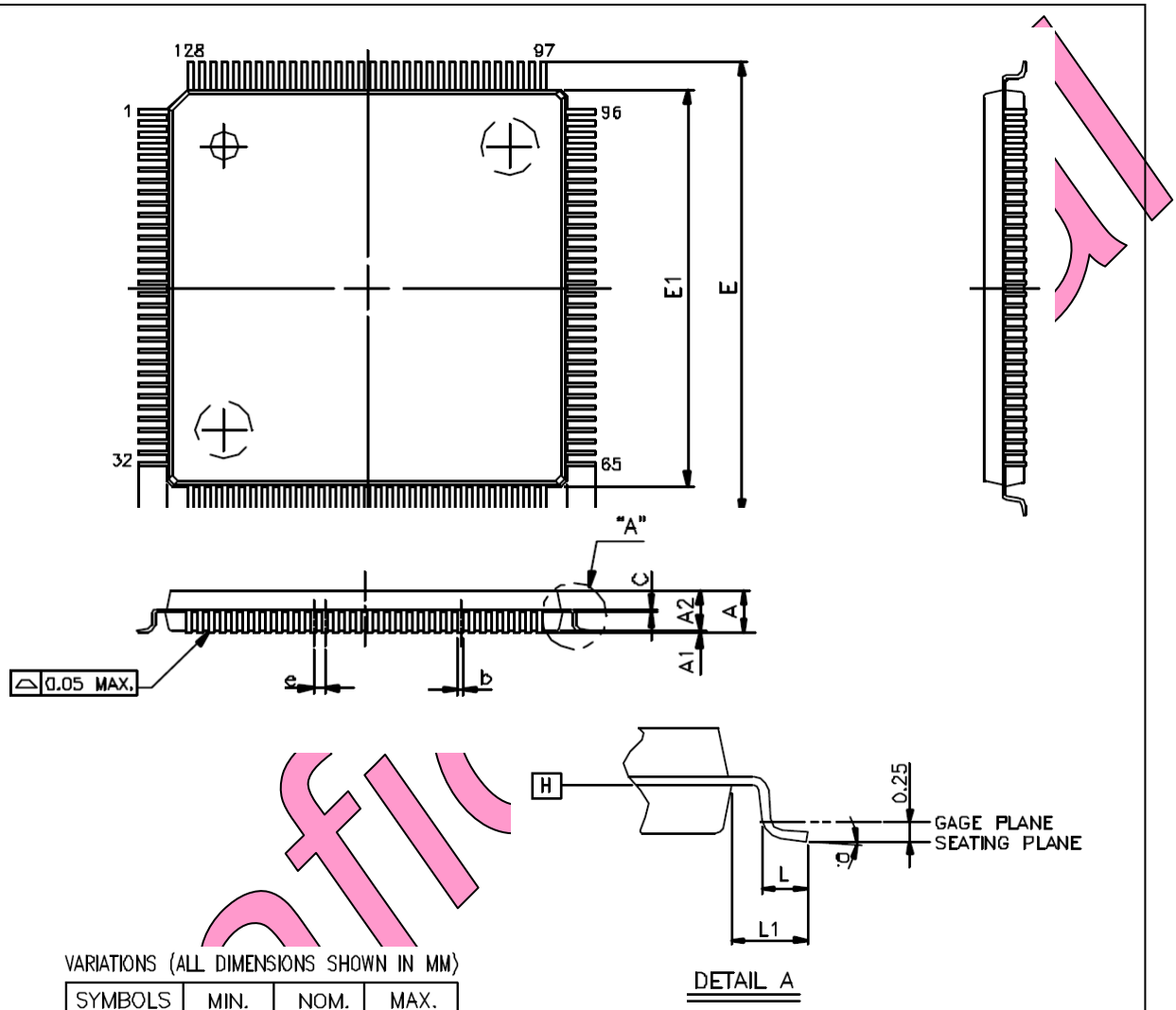
| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{CLK,656}$ | BT.656 clock frequency | | 27 | | MHz |
| $t_{SU,656}$ | BT.656 data setup time | 2 | – | – | ns |
| $t_{HD,656}$ | BT.656 data hold time | 2 | – | – | ns |

## 5.4. DAC Characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $INL_{DAC}$ | Integral nonlinearity | | | | ±1 | LSB |
| $DNL_{DAC}$ | Differential nonlinearity | | | | ±1 | LSB |

# 6. Package Outline

LQFP 128 pin : 14mm(W) x 14mm(L) x 1.4mm(H)




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.13 | 0.18 | 0.23 |
| c | 0.09 | -- | 0.20 |
| D | 16.00 BSC | | |
| D1 | 14.00 BSC | | |
| E | 16.00 BSC | | |
| E1 | 14.00 BSC | | |
| e | 0.40 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| θ | 0° | 3.5° | 7° |

NOTES:

1. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.