VP77

Video Decoder for Portable LCD Display

(Preliminary)

Version: 0.96

Date : Apr. 7, 2005

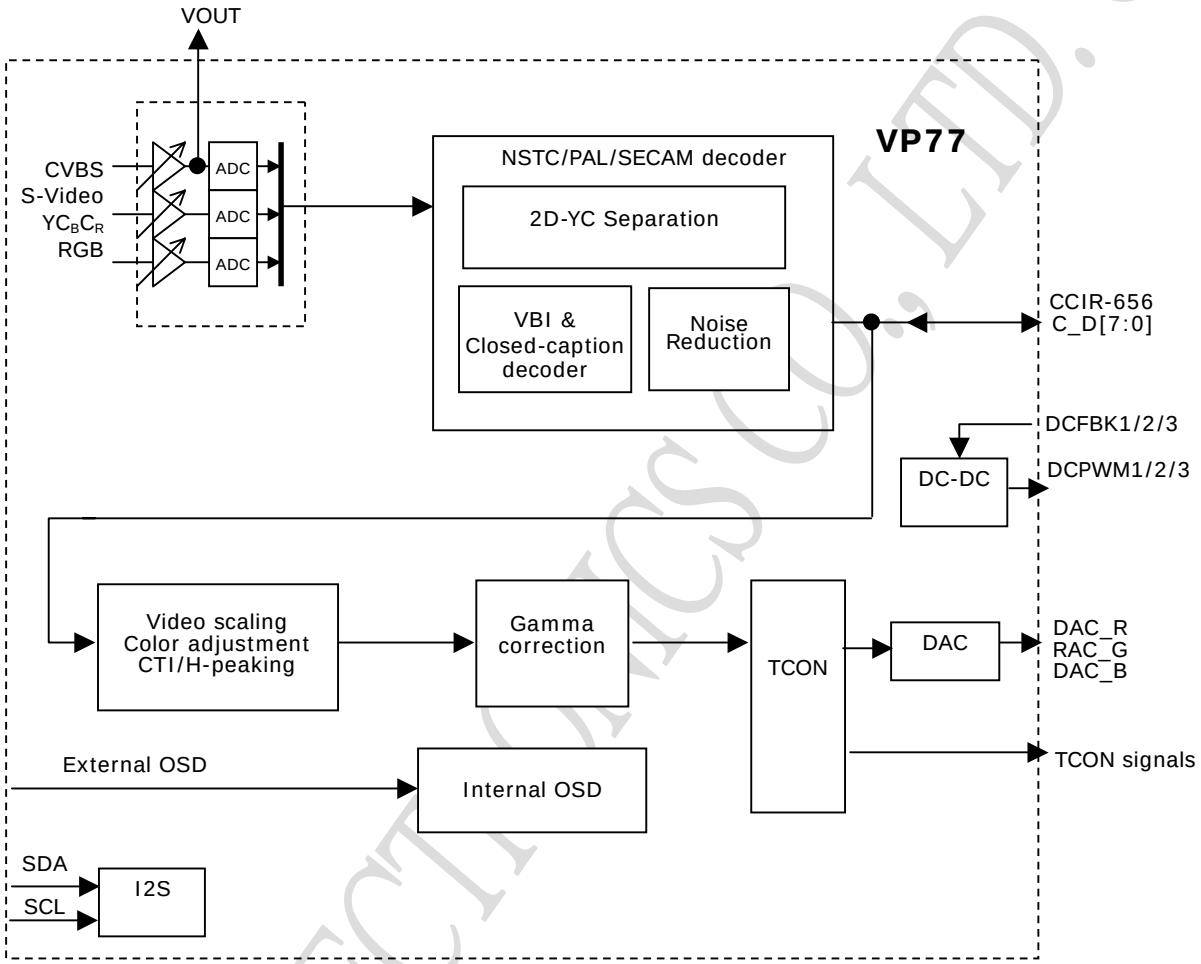
VP77 Data Sheet

1. Features

The VP77, is an one-chip video decoder with integrated scalar, OSD function, TCON, and DAC, which can drives small size 4, 5.6, 7-inch TFT-LCD panel with analog interlace. For analog panels, VP77 can support the display resolutions of 1440x234, 1200x234, or 960x234.

- ☐ Support inputs:
  - Composite video (CVBS) input
  - S-video input
  - Component video input
  - Analog RGB input
  - Digital CCIR-656 input
- ☐ Video decoder
  - Supporting NTSC/PAL/SECAM standard
  - 2D comb filter
  - 2D noise reduction
  - Closed-caption/font-rendering
  - Macro-vision copy protection
  - Selectable CCIR-656 output
- ☐ Video Scaling
  - Horizontal scaling
  - Vertical scaling
  - 4:3 to/from 16:9 conversion
- ☐ OSD
  - The normal font size of 12x16
  - 127-downloadable fonts and one space code
  - Alpha blending, blinking
  - Maximum display dimension is 16(row) by 31(column)
  - Flexible memory partition to allocated normal character fonts (with 16 foreground colors and 8 background colors) and graphic character fonts (with 8 colors per dot)
  - Programmable character height, width, row space, column space
- ☐ Built-in RGB-to-YUV matrix for RGB input signal
- ☐ Brightness, contrast, tint, and color adjustment
- ☐ Auto-adjustment for phase, frequency, H/V position, and white balance
- ☐ Programmable gamma correction
- ☐ H-peaking and CTI
- ☐ Hardware mode detection support
- ☐ RGB-YUV and YUV-RGB matrix conversion
- ☐ Support free-run mode if the sync signal is missing
- ☐ Programmable TCON
- ☐ Three PWM's
- ☐ DC-DC control signals
- ☐ On-chip triple video DAC's
- ☐ 128-pin LQFP package

2. Block Diagram



3. Pinning diagram

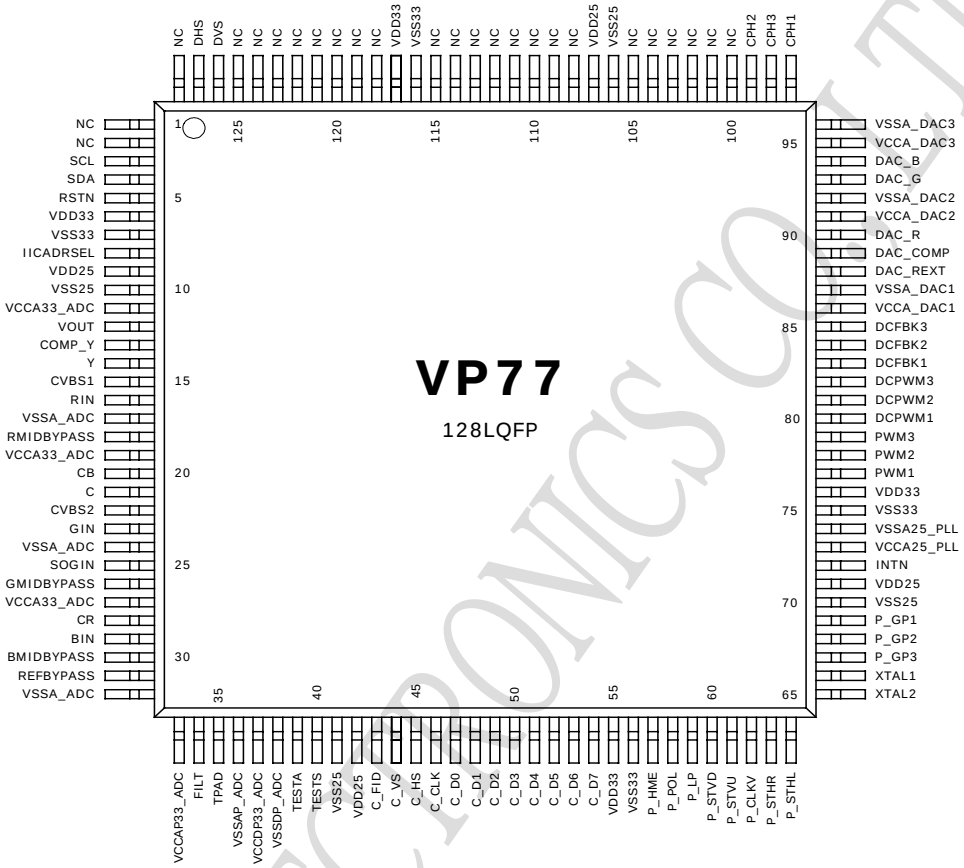


Fig.3.1 VP77 pinning diagram for 128-lead LQFP

4. Pin Assignment

PIN NAME	PIN TYPE	PIN#	DESCRIPTION
COMP_Y	A	13	Y of Component video
Y	A	14	Luma of S-Video Input
CVBS1	A	15	Composite video input 1
RAIN	A	16	Red Channel Analog Input
RMIDBYPASS	A	18	R channel internal midscale voltage bypass (default to be ground)
CB	A	20	C_B of Component video
C	A	21	Chroma of S-Video Input
CVBS2	A	22	Composite video input 2
GAIN	A	23	Green Channel Analog Input
GMIDBYPASS	A	26	G channel internal midscale voltage bypass (default to be ground)
CR	A	28	C_R of Component video
BAIN	A	29	Blue Channel Analog Input
BMIDBYPASS	A	30	B channel internal midscale voltage bypass (default to be ground)
SOGIN	A	24	Sync-on-Green slicer input
REFBYPASS	A	31	Internal reference bypass
FILT	A	34	External filter connection for PLL
DHS	I(SMT, PD)	127	VGA input H sync
DVS	I(SMT, PD)	126	VGA input V sync
VOUT	A	12	Buffered composite video output
TPAD	A	35	Test mode output
C_VS/OVR	IO(PD4)	44	Vertical sync of video port / Overlay color select R input of external OSD
C_HS/OVG	IO(PD4)	45	Horizontal sync of video port / Overlay color select G input of external OSD
C_FID/OVB	IO(PD4)	43	Field ID/ Overlay color select B input of external OSD
C_CLK/OVCLK	IO(PD4)	46	Clock for video port/ Overlay clock of external OSD
C_D[7:4], C_D3/OVS, C_D2/OHS, C_D1/OVI, C_D0/OVFB	IO(PD4)	54~51, 50, 49, 48, 47	YUV data of video port bit 7~0/ YUV bit-3 alternative to Overlay VSYNC of ext-OSD/ YUV bit-2 alternative to Overlay HSYNC of ext-OSD/ YUV bit-1 alternative to Overlay intensity of ext- OSD/ YUV bit-0alternative to Overlay fast blanking of ext-OSD
SDA	IO(SMT, PU4)	4	Serial I/F data in/out
SCL	IO(SMT, PU4)	3	Serial I/F clock
IICADRSEL	I(PD)	8	Serial I/F sub-address setting
TESTA	I(PD)	39	Test pin A
TESTS	I(PD)	40	Test pin S
XTAL1	I	66	Input external free-run clock of 20 MHz
XTAL2	O	65	Output external free-run clock of 20 MHz
RSTN	I(SMT)	5	Reset signal (active low)
PWM1	O(PD4)	77	PWM output 1
PWM2	O(PD4)	78	PWM output 2

PWM3	O(PD4)	79	PWM output 3
DCPWM1	O(PD4)	80	DC-DC control PWM output 1
DCPWM2	O(PD4)	81	DC-DC control PWM output 2
DCPWM3	O(PD4)	82	DC-DC control PWM output 3
DCFBK1	A	83	DC-DC feedback input 1
DCFBK2	A	84	DC-DC feedback input 2
DCFBK3	A	85	DC-DC feedback input 3
INTN	O(PU8)	72	Interrupt to host (active low)
CPH1	O(PD4)	97	Clock phase 1 output for sourced river IC
P_STHL	O(PD4)	64	Start pulse for source driver IC; Active when scan from L to R, and tri-state when scan from R to L
P_STHR	O(PD4)	63	Start pulse for source driver IC; Active when scan from R to L, and tri-state when scan from L to R
P_CLKV	O(PD4)	62	Clock for gate driver IC
P_STVU	O(PD4)	61	Start pulse for gate driver; Active when scan from U to D, and tri-state when scan from D to U
P_STVD	O(PD4)	60	Start pulse for gate driver; Active when scan from D to U, and tri-state when scan from U to D
P_LP/OEH	O(PD4)	59	Latch pulse for source driver IC
P_POL/PFRP	I(PD4)	58	Polarity for source driver IC
P_HME	O(PD4)	57	Data inversion control for source driver IC
P_GP1/OEV	O(PD4)	69	TCON GPO1
P_GP2/Q1H	O(PD4)	68	TCON GPO2
P_GP3	O(PD4)	67	TCON GPO3
NC	O(PD4)	1	No connection
NC	O(PD4)	2	No connection
NC	O(PD4)	128	No connection
CPH2	O(PD4)	99	Clock phase 2 for source driver IC
CPH3	O(PD4)	98	Clock phase 3 for source driver IC
NC		105~100	No connection
NC		115~108	No connection
NC		125~118	No connection
DAC_R	A	90	Red channel DAC output
DAC_G	A	93	Green channel DAC output
DAC_B	A	94	Blue channel DAC output
DAC_REXT	A	88	External resistor input for DAC
DAC_COMP	A	89	Compensation pin of DAC
VCCA_DAC1	P	86	Dedicated Analog VCC (3.3V) for DAC
VSSA_DAC1	P	87	Dedicated Analog Ground for DAC
VCCA_DAC2	P	91	Dedicated Analog VCC (3.3V) for DAC
VSSA_DAC2	P	92	Dedicated Analog Ground for DAC
VCCA_DAC3	P	95	Dedicated Analog VCC (3.3V) for DAC
VSSA_DAC3	P	96	Dedicated Analog Ground for DAC
VCCA25_PLL	P	73	Analog VDD (2.5V) for PLL clock generator
VSSA25_PLL	P	74	Analog Ground for PLL clock generator
VCCDP33_ADC	P	37	ADC/PLL digital core (3.3V)
VSSDP_ADC	P	38	ADC/PLL digital core ground
VCCAP33_ADC	P	33	ADC/PLL analog core (3.3V)
VSSAP_ADC	P	36	ADC/PLL analog core ground
VCCA33_ADC	P	11,19,27	AVDD (3.3V) for ADC analog core

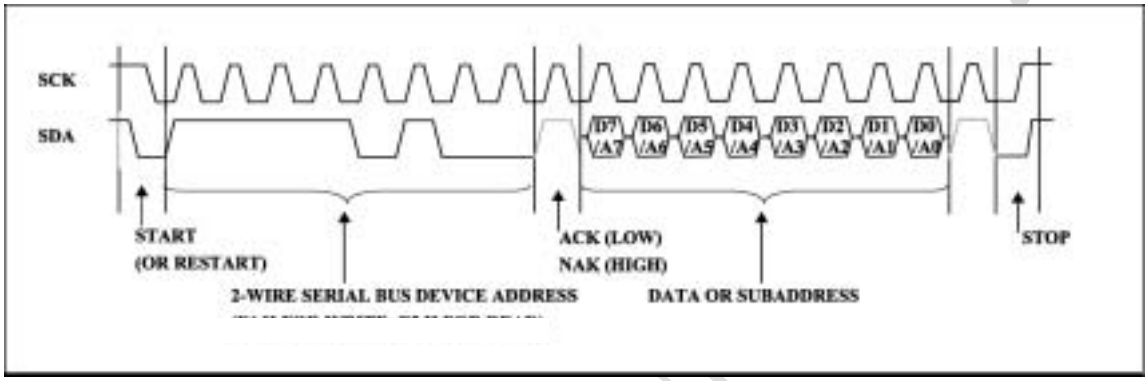
VSSA_ADC	P	17,25,32	Ground for ADC analog core
VDD33	P	6,55,76,117	VDD (3.3V) for IO
VSS33	P	5,56,75,116	Ground for IO
VDD25	P	9,42,71,107	VDD (2.5V) for digital core
VSS25	P	10,41,70,106	Ground for digital core

- SMT: Schmitt Trigger in input
- I: Input
- O: Output
- IO: In/out
- OD: Open-drain
- PU: Pull-up in input (not valid for chip external)
- PD: Pull-down in input (not valid for chip external)
- PD4: Pull-down with 4 mA driving capability in output
- PU4: Pull-up with 4 mA driving capability in output
- PU8: Pull-up with 8 mA driving capability in output
- P: Power
- A: Analog IO

5. System Description

5.1 2-wire serial bus interface

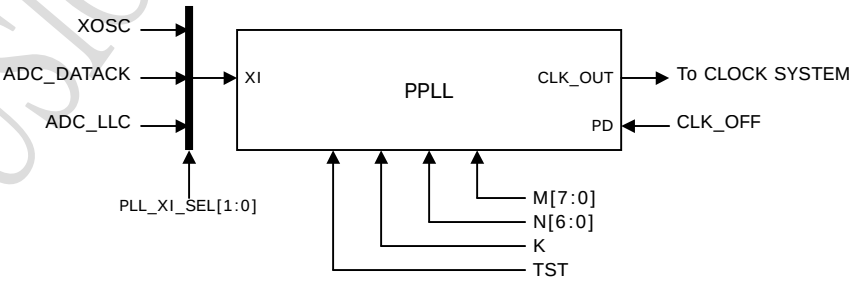
This chip supports the industrial standard 2-wire serial bus interface, which consists of SDA bi-directional data line and SCL clock line. The 2-wire serial bus slave addresses(also known as device address) of this chip are described in the below table. The definition of the basic 2-wire serial bus interface protocol is illustrated as follows. For detailed timing and operation protocol, please refer to the standard 2-wire serial bus specification.



VP77 has four slave serial-bus devices. The slave addresses table is shown as belows:

Device name	IICADRSEL	Slave Address (hex) [6:0],0
Video decoder (VDEC)	0	40
	1	48
ADC	0	42
	1	4A
Scalar System	0	F4
	1	FC
TCON	0	F6
	1	FE

5.2 Panel PLL (PPLL) Setup



VP77 has one PLL for PCLK generation. PCLK is used for display panel clocking. The PLL output frequency,

CLK_OUT, is determined by the ratio set between the value set in the input divider and the feedback divider. PLL output frequency CLK_OUT is calculated from the following equations:

CLK_OUT = XI * (M/N) * [1/(1+K)]

where:

M = 2~255 (feedback divider value)
N = 2~127 (input divider value)
K = 0,1 (post divider for output clock)

XI= 20MHz in default (2~50MHz can be valid), and the following conditions must be satisfied to have a qualified CLK_OUT:

1. 1MHz ≦ (XI/N) ≦ 15MHz
2. 100MHz ≦ [CLK_OUT * (1+K)] ≦ 450MHz

PPLL0 (PPLL Control Register 0, BAH)			Default
7:0	M	feedback divider value	63h

PPLL1 (PPLL Control Register 1, BBH)			Default
7	K	post divider for output clock	1
6:0	N	input divider value	11h

PPLL2 (PPLL Control Register 2, BEH)			Default
7~6	-	Reserved	00
5	TST	PPLL test mode	0
4	PLL_PREDIV4	PPLL pre-divide 4	0
3~2	PLL_XI[1:0]	00: select XOSC as PPLL source clock 01: select ADC's DATACK as PPLL source clock 10: select ADC's LLC as PPLL source clock 11: reserved	00
1	PLL_DIV6	PPLL output divide by 6 after "pre-divide 4"	1
0	PLL_DIV4	PPLL output divide by 4	0

5.3 Reset System

A reset is accomplished by holding the RSTN pin LOW (LOW ACTIVE) for at least 1us while the crystal oscillator is running in XTAL1 and XTAL2. An automatic reset can be obtained by switching on VCC, if the RSTN pin is connected to GROUND via a capacitor and to the VDD via a resistor. The VDD rise time must not exceed 10 ms and the capacitor should be at least 10 uF. The increase of the RSTN pin voltage depends on the capacitor and the external resistor.

5.4 ADC Front End

The 10bit AD converter is shown in Fig.5.3. It employs three 10-bit ADCs and a PLL timing generator. The ADC sampling clock can be derived from either an external source or incoming horizontal signal using internal, PLL. Output data are 30-bit RGB and 1-channel VIDEO_OUT. Input amplitude range is 500~1000mV at RGB mode, 650~1300mV at video mode, and programmable through the 8-bit gain control. Input offset voltage of each converter is programmable through the 7-bit offset control.

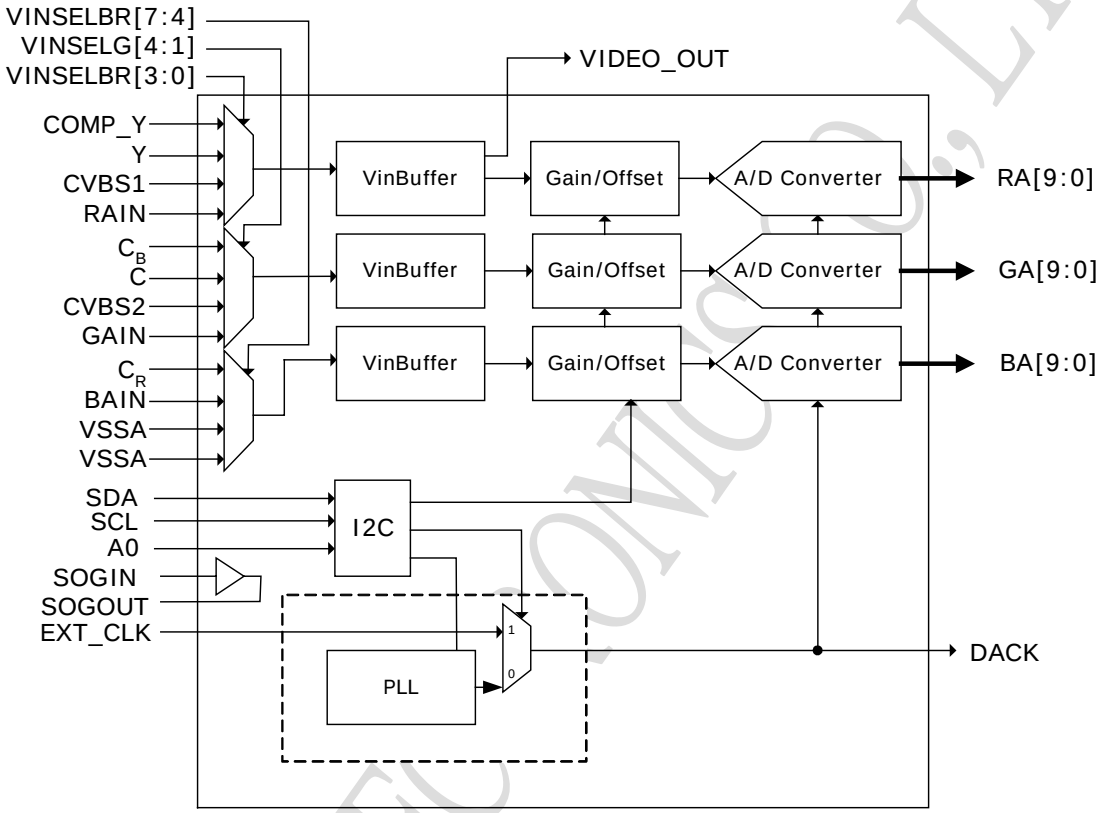


Fig. 5.4.1 ADC Block Diagram

00H		PLL Divider MSB Register	
Bit	ACCESS	SYMBOL	Description
[7:0]	R/W	PLLDIV[11:4]	This register is used for bits 11-4 of PLL divider. The PLL divider has total of 12 bits value (default at 1693). Larger value means that the PLL will operate at a higher rate. This register should be loaded in the beginning before any change is needed. (PLLDIV[11:4] is default to 69H)

01H	PLL Divider LSB Register

Bit	ACCESS	SYMBOL	Description
[7:4]	R/W	PLLDIV[3:0]	This register is used for bits 3-0 of PLL divider. The PLL divider has total of 12 bits value (default at 1693). (PLLDIV[3:0] is default to 0DH)
[3:0]	R/W	RESERVED	

02H		Red Gain Control Register	
Bit	ACCESS	SYMBOL	Description
[7:0]	R/W	RGAIN	This register controls the Red color ADC input range (i.e. Contrast). Smaller values give more contrast. (deafult to 80H)

03H		Green Gain Control Register	
Bit	ACCESS	SYMBOL	Description
[7:0]	R/W	GGAIN	This register controls the Green color ADC input range (i.e. Contrast). Smaller values give more contrast. (deafult to 80H)

04H		Blue Gain Control Register	
Bit	ACCESS	SYMBOL	Description
[7:0]	R/W	BGAIN	This register controls the Blue color ADC input range (i.e. Contrast). Smaller values give more contrast. (deafult to 80H)

05H		Red offset Control Register	
Bit	ACCESS	SYMBOL	Description
[7:1]	R/W	ROFF	This register controls the Red color DC offset (i.e. Brightness). Smaller values give a brighter image (default to 1000000b)
[0]	R/W	RESERVED	

06H		Green offset Control Register	
Bit	ACCESS	SYMBOL	Description
[7:1]	R/W	GOFF	This register controls the Green color DC offset (i.e. Brightness). Smaller values give a brighter image. (default to 1000000b)
[0]	R/W	RESERVED	

07H		Blue offset Control Register	
Bit	ACCESS	SYMBOL	Description
[7:1]	R/W	BOFF	This register controls the Blue color DC offset (i.e. Brightness). Smaller values give a brighter image. (default to 1000000b)
[0]	R/W	RESERVED	

08H		Clamp Placement Register	
Bit	ACCESS	SYMBOL	Description

[7:0]	R/W	CLPL	This register is used to place the CLAMP signal an integer number of clock periods after the railing edge of the HSYNC signal. This register can be programmed to any value between 1 and 255. (default to 80H)

09H		Clamp duration Register	
Bit	ACCESS	SYMBOL	Description
[7:0]	R/W	CLDU	This register is used to control the number of clock periods that the CLAMP signal is active clamping. (default to 80H)

0AH		Control Register	
Bit	ACCESS	SYMBOL	Description
[7:6]	R/W	CTRL[7:6]	Default: 2'b11
5	R/W	CTRL[5]	**HSYNC Polarity** Changes the polarity of the incoming HSYNC signal. 0b: Active Low (HSYNC is negative-going pulse) 1b: Active High (HSYNC is positive-going pulse) →(default)
4	R/W	CTRL[4]	**COAST Polarity** Changes the polarity of external COAST signal. 0b: Active Low 1b: Active High →(default)
3	R/W	CTRL[3]	**CLAMP Source** Selects HSYNC for generating internal clamp signal or selects external CLAMP signal for clamping. 0b: Uses HSYNC as clamping signal →(default) 1b: Select External Clamping Signal
2	R/W	CTRL[2]	**CLAMP Polarity** Changes the polarity of external CLAMP signal. Only valid with external CLAMP signal. 0b: Active Low 1b: Active High →(default)
1	R/W	CTRL[1]	**PLL Bypass @ RGB Mode** Selects the internal PLL or the External clock input. 0b: Use Internal PLL →(default) 1b: Use External Clock Input & Shut down the internal PLL
0	R/W	RESERVED	

0BH		Phase Adjust Register	
Bit	ACCESS	SYMBOL	Description
[7:3]	R/W	PHASE	This register is used to adjust the clock phase for ADC. Larger values mean more delay (1 LSB = T/32). (deafult to 11110b)
[2:0]	R/W	RESERVED	

0CH		VCO/CPMP Register	
Bit	ACCESS	SYMBOL	Description

[7]	R/W	RESERVED	
[6:5]	R/W	VCOCP[4:3]	**VCO Range** Selects VCO frequency range. 00b: 20 ~ 60 MHz 10b: 80 ~ 120 MHz 01b: 50 ~ 90 MHz → (default) 11b: 110 ~ 140 MHz
[4:2]	R/W	VCOCP[2:0]	**Charge Pump Current** Changes the driving current to the low pass filter. 000b: 50 uA 100b: 350 uA 001b: 100 uA → (default) 101b: 500 uA 010b: 150 uA 110b: 750 uA 011b: 250 uA 111b: 1500 uA
[1:0]	R/W	RESERVED	

0DH		Red Midscale Voltage Level Control Register	
Bit	ACCESS	SYMBOL	Description
[7:1]	R/W	RBOFF	This register controls the Red channel midscale voltage level for mid-level clamping use. (default to 1000000b)
[0]	R/W	RESERVED	

0EH		Green Midscale Voltage Level Control Register	
Bit	ACCESS	SYMBOL	Description
[7:1]	R/W	GBOFF	This register controls the Green channel midscale voltage level for mid-level clamping use. (default to 1000000b)
[0]	R/W	RESERVED	

0FH		Blue Midscale Voltage Level Control Register	
Bit	ACCESS	SYMBOL	Description
[7:1]	R/W	BBOFF	This register controls the Blue channel midscale voltage level for mid-level clamping use. (default to 1000000b)
[0]	R/W	RESERVED	

10H		SYNC Routing Select & Output Control Register	
Bit	ACCESS	SYMBOL	Description
[7:4]	R/W	RESERVED	
[3]	R/W	HREFSEL	The Reference clock for PLL can be external HSYNC/composite sync or SOG input. 0: External HSYNC/Composite sync (Default) 1: SOG
[2]	R/W	CSTSEL	Two types of input can be applied into COAST for PLL to lock on current frequency. 0: Coast input pin (Default) 1: Using VSYNC
[1:0]	R/W	RESERVED	

11H		YUV Clamping & SOG Threshold Control Register	
Bit	ACCESS	SYMBOL	Description

[7:6]	R/W	HSY	Default: 10b
[5:4]	R/W	SOG	Default: 01b
[3]	R/W	COMP	Mid-level clamping op-amp compensation enable signal. Default: 1 (enabled)
[2]	R/W	RCLAMPSEL	When RAIN / GAIN / BAIN is connected to analog video signal, RCLAMPSEL / GCLAMPSEL / BCLAPMSEL can be used to clamp video to 00H or 10H (midscale). 0: Clamp to groud (Default) 1: Clamp to midscale
[1]	R/W	GCLAMPSEL	
[0]	R/W	BCLAPMSEL	

16H		Video Input Select Register	
Bit	ACCESS	SYMBOL	Description
[7:6]	R/W	-	**Reserved** Default:00
5	R/W	CLP_PUMPB	**Video DC Restore Method** Selects the DC restore method for video input. 0b: Charge pump → (default) 1b: Clamping
4	R/W	VINSELG[4]	**GAIN Input Selection on Green Channel** Default: 0
3	R/W	VINSELG[3]	**CVBS2 Input Selection on Green Channel** Default: 0
2	R/W	VINSELG[2]	**C Input Selection on Green Channel** Default: 0
1	R/W	VINSELG[1]	**CB Input Selection on Green Channel** Default: 1
0	R/W	VMODE	**ADC Video Mode Selection** Select between RGB mode and Video mode input. 0b: RGB mode → (default) 1b: Video mode

17H		Video power down Register	
Bit	ACCESS	SYMBOL	Description
[7]	R/W	VTST[7]	0: Reference clock and feedback clock are the same frequency 1: Reference clock is twice the feedback clock frequence (Default = 0)
[6]		VTST[6]	Reserved
[5]	R/W	CBPD	Power down Blue channel (Default = 0)
[4]	R/W	CRPD	Power down Red channel (Default = 0)
[3]	R/W	YPD	Power down Green channel (Default = 0)
[2]	R/W	SOGPD	Power down SOG Function (Default = 0)
[1]	R/W	GCLP256	(Default = 0)
[0]	R/W	RCLP256	(Default = 0)

Clamp to	xCLAMPSEL	xCLP256
GND	0	x
Mid	1	0
256	1	1

18H		Hsync Pulse Width Counter Register	
Bit	ACCESS	SYMBOL	Description
[7:0]	R/W	HSCOUNT	Counter for adjusting the pulse width of the internally-generated HSOUT signal (Default = 80H)

19H		Hsync Test Mode Register	
Bit	ACCESS	SYMBOL	Description
[7:2]	R/W	HSTEST[7:2]	reserved
[1:0]	R/W	HSTEST[1:0]	Keep HSOUT frequency during COAST period (Default = 00H)

1AH		Speed Register	
Bit	ACCESS	SYMBOL	Description
[7]	R/W	RESERVED	
[6]	R/W	PLL_VMODE	**ADC Clock Source Selection** Select between RGB mode and Video mode clock function. 0b: RGB mode, ADC clock uses PLL clock → (default) 1b: Video mode, ADC clock uses external clock
[5:0]	R/W	RESERVED	

1BH		Speed Register	
Bit	ACCESS	SYMBOL	Description
[7:4]	R/W	BC[3:0]	ADC bias current, default: 1000b
[3:0]	R/W	TEST	

20H		Video Sync Tip Control 1 Register	
Bit	ACCESS	SYMBOL	Description
[7:0]	R/W	YPUMPCTRL[7:0]	**Charge Pump Current for Y (Green Channel)** Changes the DC restore current for video mode. 01h: 25 uA 10h: 250 uA 02h: 50 uA 20h: 300 uA 04h: 100 uA 40h: 350 uA 08h: 200 uA 80h: 400 uA (default = 00H)

21H		Video Sync Tip Control 2 Register	
Bit	ACCESS	SYMBOL	Description
[7:0]	R/W	CRPUMPCTRL[7:0]	**Charge Pump Current for CR (Red Channel)** Changes the DC restore current for video mode. 01h: 25 uA 10h: 250 uA 02h: 50 uA 20h: 300 uA 04h: 100 uA 80h: 400 uA 08h: 200 uA 40h: 350 uA (default = 00H)

22H		Video Sync Tip Control 3 Register	
Bit	ACCESS	SYMBOL	Description
[7:0]	R/W	CBPUMPCTRL[7:0]	**Charge Pump Current for CB (Blue Channel)** Changes the DC restore current for video mode. 01h: 25 uA 10h: 250 uA 02h: 50 uA 20h: 300 uA 04h: 100 uA 40h: 350 uA 08h: 200 uA 80h: 400 uA (default = 00H)

23H		Input Select Register (default = 00H)	
Bit	ACCESS	SYMBOL	Description
[7]	R/W	VINSELBR[7]	VSSA input switch on B channel
[6]	R/W	VINSELBR[6]	VSSA input switch on B channel
[5]	R/W	VINSELBR[5]	BAIN input switch on B channel
[4]	R/W	VINSELBR[4]	CR input switch on B channel
[3]	R/W	VINSELBR[3]	RAIN input switch on R channel
[2]	R/W	VINSELBR[2]	CVBS1 input switch on R channel
[1]	R/W	VINSELBR[1]	Y input switch on R channel
[0]	R/W	VINSELBR[0]	COMP_Y input switch on R channel

25H		Power management Register	
Bit	ACCESS	SYMBOL	Description
[7:1]	R/W	RESERVED	
[0]	R/W	PDADC_B	Power down ADC, Low-active signal. Default:0

5.5 Video Decoder (VDEC)

VP77's VDEC is a high quality NTSC, PAL, and SECAM video decoder plus YPbPr component inputs designed for video applications. Minimum external components are required due to its integrated analog front-end containing AGC, clamping, and three high speed ADCs. For composite inputs, an adaptive 2D comb filter and luma/chroma processing produce exceptionally high quality pictures for Y/C separation. Furthermore, 2D noise reduction which provide good video quality especially when the source is from a noisy VCR tape are included.

5.5.1 VDEC Control Register

00h	**VDEC CONTROL0**						
7	6	5	4	3	2	1	0
IFMT	DFMT		V625	CMODE			RSVD

Mnemonic	**Type**	**Description**
IFMT	R/W	This bit selects input video format. 0 = composite (default) 1 = S-Video (separated Y/C)
CMODE	R/W	These bits select video colour standard. 000 = NTSC (default) 001 = PAL (I,B,G,H,D,N) 010 = PAL (M) 011 = PAL (CN) 100 = SECAM
V625	R/W	This bit selects the number of scan lines per frame. 0 = 525 (default) 1 = 625
DFMT	R/W	These bits select the output display format. Standard — pixels/line — bit-setting NTSC, PAL(M) — 858 — 00 (default) PAL(B,D,G,H,I,N,CN),SECAM — 864 — 01 NTSC Square Pixel, PAL(M) Square Pixel — 780 — 10 PAL(B,D,G,H,I,N) Square Pixel — 944 — 11
Bit 0	R/W	Reserved (default to 0)

01h	**VDEC CONTROL1**						
7	6	5	4	3	2	1	0
COMPVI	COMPV	LNOWD		CHROMALPF		BURSTWDH	PED

Mnemonic	**Type**	**Description**
PED	R/W	This bit enables black level correction for 7.5 blank-to-black setup (pedestal). 0 = no pedestal subtraction 1 = pedestal subtraction (default)
BURSTWDH	R/W	This bit selects the burst gate width 0 = 5 subcarrier clock cycles (default) 1 = 10 subcarrier clock cycles
CHROMALPF	R/W	This bit set the chroma low pass filter to wide or narrow 0 = narrow (default) 1 = wide 2 = extra wide

LNOWDH	R/W	These bits select luma notch width 00 = none (default) 01 = narrow 10 = medium 11 = wide
COMPV	R/W	This bit enables the component video input format. 0 = Disable the component video input (default) 1 = Component-Video (Y,Pb,Pr)
COMPVI	R/W	This bit inverts the select signal for the analog input multiplexer during component video mode. 0 = not inverted (default) 1 = inverted

02h	**VDEC CONTROL2**						
7	6	5	4	3	2	1	0
LAGCFLD	MVAGC	CLAMPMD		RSVD	RSVD	CAGCEN	LAGCEN
Mnemonic	**Type**	**Description**					
LAGCEN	R/W	This bit when set enables the luma/composite AGC. If disabled, then the AGC target (register 04h) is used to drive directly the AGC gain. 0 = off 1 = on (default)					
CAGCEN	R/W	This bit when set enables the chroma AGC. If disabled, then the AGC target is used to drive directly the AGC gain. 0 = off 1 = on (default)					
Bit 2	R/W	Reserved (Default to 1)					
Bit 3	R/W	Reserved (Default to 1)					
CLAMPMD	R/W	This bit sets the mode for the analog front end DC clamping 00 = auto (default) 01 = backporch only 10 = synctip only 11 = off					
MVAGC	R/W	This bit, when set, automatically reduces the gain (set in register 4) by 25% when macro-vision encoded signals are detected 0 = off 1 = on (default)					
LAGCFLD	R/W	When this bit is “0” (the default), then the gain is updated once per line, after DC clamping. When this bit is set, then the gain is only updated once per field, at the start of vertical blank. 0 = off (default) 1 = on					

03h	**YC-SEPARATION CONTROL**						
7	6	5	4	3	2	1	0
N443	RSVD			CTRAP	ADAPMD		
Mnemonic	**Type**	**Description**					
ADAPMD	R/W	For NTSC Mode → set to 000b For NTSC443 mode → set to 110b For PAL 60 Mode → set to 011b For other PAL modes → set to 110b (Default = 000b)					

CTRAP	R/W	This bit enables the notch-filter at the luma path after the comb filter. This filter can be turned on or off irrespective of the adaptive mode setting. 0 = Disabled (default) 1 = Enabled
N443	R/W	This bit enable the NTSC443 input mode (Default=0)

04h	**LUMA AGC VALUE**						
7	6	5	4	3	2	1	0
LAGC							

Mnemonic	**Type**	**Description**
LAGC	R/W	Set Luma AGC control level : Standard — Programming Value NTSC M — DDh (221d) (default) NTSC J — CDh (205d) PAL B,D,G,H,I, COMB N, SECAM — DCh (220d) PAL M,N — DDh (221d) NTSC M (MACROVISIOIN) — A6h (166d) PAL B,D,G,H,I, COMB N (MACROVISION) — AEh (174d) LAGC is used when LAGCEN bit is 0 (REG 02H/bit-0)

06h	**ADC_SWAP**						
7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	AGCG_THD				

Mnemonic	**Type**	**Description**
AGCG_THD	R/W	This specifies the threshold at which the rough gate generator creates a sync gate. Default = 10
Bit 7	R/W	Reserved
Bit 6	R/W	Reserved
Bit 5	R/W	Reserved

08h	**LUMA CONTRAST ADJUSTMENT**						
7	6	5	4	3	2	1	0
Contrast							

Mnemonic	**Type**	**Description**
Contrast	R/W	These bits control the adjustable gain to the luma output path (default = 128).

09h	**LUMA BRIGHTNESS ADJUSTMENT**						
7	6	5	4	3	2	1	0
Brightness							

Mnemonic	**Type**	**Description**
Brightness	R/W	This 2's complement number control the adjustable brightness level to the luma output path. (default = 32)

0Ah	**CHROMA SATURATION ADJUSTMENT**						
7	6	5	4	3	2	1	0
saturation							

Mnemonic	Type	Description
saturation	R/W	These bits adjust the colour saturation (default = 128).

0Bh	CHROMA HUE PHASE ADJUSTMENT						
7	6	5	4	3	2	1	0
hue							

Mnemonic	Type	Description
Hue	R/W	This 2's complement number adjusts the hue phase offset (default = 0).

0Ch	CHROMA AGC						
7	6	5	4	3	2	1	0
cagc							

Mnemonic	Type	Description
Cagc	R/W	These bits set the chroma AGC target (default = 138)

12h	AGC control 1						
7	6	5	4	3	2	1	0

Mnemonic	Type	Description
agc_control_1	R/W	Default to 0C6H, and set to 34H for the XTAL clock of 20MHz

13h	AGC control 2						
7	6	5	4	3	2	1	0

Mnemonic	Type	Description
agc_control_2	R/W	Default to 82H, and set to 0D2H for the XTAL clock of 20MHz

14h	AGC control 3						
7	6	5	4	3	2	1	0

Mnemonic	Type	Description
agc_control_3	R/W	Default to 64, and set to 2FH for the XTAL clock of 20MHz

15h	AGC control 4						
7	6	5	4	3	2	1	0

Mnemonic	Type	Description
agc_control_4	R/W	Default = 64H, and set to 4AH for the XTAL clock of 20MHz

17h	H LOOP MAXSTATE						
7	6	5	4	3	2	1	0
hlock_vsync_mode		hstate_fixed	disable_hfine	hstate_unlocked	hstate_max		

Mnemonic	Type	Description
hstate_max	R/W	These bits set the maximum state for the horizontal PLL state machine. If "hstate_fixed" is set, then this register is used to force the state. (default = 3).
hstate_unlocked	R/W	This bit sets the state when unlocked (default = 1)

disable_hfine	R/W	This bit, when set, disables the fine mode of the HPLL phase comparator. (default = 0)
hstate_fixed	R/W	This bit when set forces the state machine to remain in the state set in "hstate_max" (default = 0)
hlock_vsync_mode	R/W	These bits control hsync locking during vsync: 00 = disabled 01 = enabled 10 = enabled except for noisy signals 11 = enabled only for VCR signals (default)

18h	**CHROMA DTO INCREMENT**						
31	30	29	28	27	26	25	24
cdto_fixed	*Reserved*	cdto_inc[29:24]					

Mnemonic	**Type**	**Description**
cdto_fixed	R/W	This bit, when set, fixes the chroma DTO at its centre frequency (default = 0)
cdto_inc[29:24]	R/W	These bits contain bits 29:24 of the 30-bit-wide chroma DTO increment.

19h	**CHROMA DTO INCREMENT**						
23	22	21	20	19	18	17	16
cdto_inc[23:16]							

Mnemonic	**Type**	**Description**
cdto_inc[23:16]	R/W	These bits contain bits 23:16 of the 30-bit-wide chroma DTO increment.

1Ah	**CHROMA DTO INCREMENT**						
15	14	13	12	11	10	9	8
cdto_inc[15:8]							

Mnemonic	**Type**	**Description**
cdto_inc[15:8]	R/W	These bits contain bits 15:8 of the 30-bit-wide chroma DTO increment.

1Bh	**CHROMA DTO INCREMENT**						
7	6	5	4	3	2	1	0
cdto_inc[7:0]							

Mnemonic	**Type**	**Description**
cdto_inc[7:0]	R/W	These bits contain bits 7:0 of the 30-bit-wide chroma DTO increment.

1Ch	**HORIZONTAL SYNC DTO INCREMENT**						
31	30	29	28	27	26	25	24
hdto_fixed	*Reserved*	hdto_inc[29:24]					

Mnemonic	**Type**	**Description**
hdto_fixed	R/W	This bit, when set, fixes the horizontal sync DTO at its centre frequency (default = 0)
hdto_inc[29:24]	R/W	These bits contain bits 29:24 value of the 30-bit-wide horizontal sync DTO increment.

1Dh	HORIZONTAL SYNC DTO INCREMENT						
23	22	21	20	19	18	17	16
hdto_inc[23:16]							

Mnemonic	Type	Description
hdto_inc[23:16]	R/W	These bits contain bits 23:16 value of the 30-bit-wide horizontal sync DTO increment.

1Eh	HORIZONTAL SYNC DTO INCREMENT						
15	14	13	12	11	10	9	8
hdto_inc[15:8]							

Mnemonic	Type	Description
hdto_inc[15:8]	R/W	These bits contain bits 15:8 value of the 30-bit-wide horizontal sync DTO increment.

1Fh	HORIZONTAL SYNC DTO INCREMENT						
7	6	5	4	3	2	1	0
hdto_inc[7:0]							

Mnemonic	Type	Description
hdto_inc[7:0]	R/W	These bits contain bits 7:0 value of the 30-bit-wide horizontal sync DTO increment.

28h	BACKPORCH INTERVAL START TIME						
7	6	5	4	3	2	1	0
backporch_start							

Mnemonic	Type	Description
backporch_start	R/W	These bits control the backporch detect window. This specifies the beginning of the window. (Default = 34)

29h	BACKPORCH INTERVAL END TIME						
7	6	5	4	3	2	1	0
backporch_end							

Mnemonic	Type	Description
backporch_end	R/W	These bits control the backporch detect window. This specifies the end of the window (Default = 78)

2Ch	CHROMA BURST GATE START TIME						
7	6	5	4	3	2	1	0
burst_gate_start							

Mnemonic	Type	Description
burst_gate_start	R/W	This specifies the beginning of the burst gate window. Note that this window is set to be bigger than the burst. The automatic burst position tracker finds the burst within this window. (Default = 50)

2Dh	CHROMA BURST GATE END TIME						
7	6	5	4	3	2	1	0
burst_gate_end							

Mnemonic	Type	Description
burst_gate_end	R/W	These bits specifies the end of the burst gate window (Default = 70)

2Eh	ACTIVE VIDEO HORIZONTAL START_TIME						
7	6	5	4	3	2	1	0
hactive_start							

Mnemonic	Type	Description
hactive_start	R/W	These bits control the active video line time interval. This specifies the beginning of active line. This register is used to centre the horizontal position, and should *not* be used to crop the image to a smaller size. (default = 130)

2Fh	ACTIVE VIDEO HORIZONTAL WIDTH						
7	6	5	4	3	2	1	0
hactive_width							

Mnemonic	Type	Description
hactive_width	R/W	These bits control the active video line time interval. This register specifies the width of the active line, and should *not* be used to crop the image to a smaller size. The value 640 is added to this register. (default = 80, and so the total width is 640+80=720)

30h	ACTIVE VIDEO VERTICAL START						
7	6	5	4	3	2	1	0
vactive_start							

Mnemonic	Type	Description
vactive_start	R/W	These bits control the first active video line in a field. This specifies the number of half lines from the start of a field. (Default = 34).

31h	ACTIVE VIDEO VERTICAL HEIGHT						
7	6	5	4	3	2	1	0
vactive_height							

Mnemonic	Type	Description
vactive_height	R/W	These bits control the active video height. This specifies the height by the number of half lines. The value 384 is added to this register. (default = 97 , and 394+97=481 half lines)

34h	VSYNC AGC LOCKOUT START						
7	6	5	4	3	2	1	0
Reserved	vsync_agc_min						

Mnemonic	Type	Description
vsync_agc_min	R/W	This register defines the number of half-lines before the vsync that the AGC, SYNCTIP, and BACKPORCH gates are disabled. (Default = -20)

35h	**VSYNC AGC LOCKOUT END**						
7	6	5	4	3	2	1	0
vsync_clamp_mode		vsync_agc_max					

Mnemonic	**Type**	**Description**
vsync_agc_max	R/W	This register defines the number of half-lines after the vsync that the AGC, SYNCTIP, and BACKPORCH gates are re-enabled. (Default = 16)
vsync_clamp_mode	R/W	These bits control DC clamping during the vertical blanking interval. 00 = disabled 01 = enabled 10 = enabled except for noisy signals (default) 11 = enabled except for noisy signals and VCRs

38h	**VSYNC_CNTL**						
7	6	5	4	3	2	1	0
vsync_cntl		vsync_thresh					

Mnemonic	**Type**	**Description**
vsync_thresh	R/W	This register specifies a relative threshold to add to the slice level for the purpose of vsync detection. (Default = 0 with 2's complement value)
vsync_cntl	R/W	These bits set the vsync output mode 00 = output the vertical PLL vsync when the signal is noisy; otherwise use directly derived vsync (default) 01 = output the directly detected vsync 10 = output the vertical PLL derived vsync 11 = output the PLL vsync in alternate mode

39h	**VSYNC_TIME_CONSTANT**						
7	6	5	4	3	2	1	0
field_pol	flip_field	veven_dly	vodd_dly	field_detect_mode		vloop_tc	

Mnemonic	**Type**	**Description**
vloop_tc	R/W	These bits set the vertical PLL time constant 0 = fast. Only useful if the vloop_cntl register is not 11. Internal values are 2 and 1. 1 = moderate. Internal values are 1 and 1/4. 2 = slow. Internal values are 1/2 and 1/16 (default) 3 = very slow. Most useful for noisy signals. Internal values are 1/4 and 1/2
field_detect_mode	R/W	These bits control the field detection logic. (default = 2)
vodd_dly	R/W	This bit delays detection of odd fields by 1 vertical line (default = 0)
veven_dly	R/W	This bit delays detection of even fields by 1 vertical line (default = 0)
flip_field	R/W	This bit flips even/odd fields
field_polarity	R/W	This bit sets the output field polarity. 0 field=1 for odd fields, field=0 for even fields (default) 1 field=0 for odd fields, field=1 for even fields

3Ah	**VDEC STATUS REGISTER 1**						
7	6	5	4	3	2	1	0
mv_cstripes			mv_vbi_det	chromalock	vlock	hlock	no_signal

Mnemonic	Type	Description
no_signal	R	No signal detection 1 = No Signal Detected 0 = Signal Detected
Hlock	R	Horizontal line locked 1 = Locked 0 = Unlocked
Vlock	R	Vertical lock 1 = Locked 0 = Unlocked
chromalock	R	Chroma PLL locked to colour burst 1 = Locked 0 = Unlocked
mv_vbi_det	R	MacroVision VBI pseudo-sync pulses detection 1 = Detected 0 = Undetected
mv_colourstripes	R	Macrovision colour stripes detected. The number indicates the number of colour stripe lines in each group

3Bh	VDEC STATUS REGISTER 2						
7	6	5	4	3	2	1	0
reserved			-	no_colorburst	vnon_standard	hnon_standard	proscan_detected

Mnemonic	Type	Description
proscan_detected	R	Progressive Scan Detected
hnon_standard	R	Horizontal frequency non-standard input signal Detected
vnon_standard	R	Vertical frequency non-standard input signal Detected
no_colorburst	R	No colorburst detect

3Ch	VDEC STATUS REGISTER 3						
7	6	5	4	3	2	1	0
vcr_rew	vcr_ff	vcr_trick	vcr	noisy	625_det	SECAM_det	PAL_det

Mnemonic	Type	Description
PAL_det	R	PAL Mode Detected
SECAM_det	R	SECAM Mode Detected
625_det	R	625 Scan Lines Detected
noisy	R	Noisy Signal Detected.
vcr	R	VCR Detected
vcr_trick	R	VCR Trick-Mode Detected
vcr_ff	R	VCR Fast-Forward Detected
vcr_rew	R	VCR Rewind Detected

3Fh	VDEC RESET REGISTER						
7	6	5	4	3	2	1	0
Reserved							soft_rst

Mnemonic	Type	Description
soft_rst	W	Soft Reset

5.5.2 VBI Decoder Registers

40h	VDEC TELETEXT VBI FRAME CODE REGISTER						
7	6	5	4	3	2	1	0
reserved					SLVL_EN	ST_ERR	VBI_EN

Mnemonic	Type	Description
VBI_EN	R/W	This bit enable the VBI decoder 0 = off (default) 1 = on
ST_ERR	R/W	When this is 1, it will allow one bit error in the stat code detection. When this bit is 0, all the start-code-bits must be correct during vbi line detection. 0 = off (default) 1 = on
SLVL_EN	R/W	When it is enable, the slicer level is auto determined. When is disable, the slicer level is specified by the VBI_DATA_HLVL register. 0 = off 1 = on (default)

42h	VDEC DATA HIGH LEVEL REGISTER						
7	6	5	4	3	2	1	0
VBI_DATA_HLVL							

Mnemonic	Type	Description
VBI_DATA_HLVL	R/W	These bits specified the VBI data high level

51h	VDEC VBI DATA TYPE CONFIGURATION REGISTER FOR LINE 21						
7	6	5	4	3	2	1	0
VBIL21E				VBIL21O			

Mnemonic	Type	Description
VBIL21O	R/W	Set VBI data type for odd field
VBIL21E	R/W	Set VBI data type for even field (Line 284 for 525 system, Line 334 for 625 system)

VBI Data Type	Programming Value
Closed Caption (US)	0001b
reserved	others

5.5.3 Status Registers 2

70h	HORIZONTAL SYNC DTO INCREMENT STATUS						
31	30	29	28	27	26	25	24
Reserved		status_hdto_inc[29:24]					

Mnemonic	Type	Description
status hdto_inc[29:24]	R	These bits contain status bits 29:24 of the 30-bit-wide horizontal sync DTO increment.

71h	HORIZONTAL SYNC DTO INCREMENT STATUS						
23	22	21	20	19	18	17	16

status_hdto_inc[23:16]		
Mnemonic	**Type**	**Description**
status_ hdto_inc[23:16]	R	These bits contain status bits 23:16 of the 30-bit-wide horizontal sync DTO increment.

72h	**HORIZONTAL SYNC DTO INCREMENT STATUS**						
15	14	13	12	11	10	9	8
status_hdto_inc[15:8]							
Mnemonic	**Type**	**Description**					
status_ hdto_inc[15:8]	R	These bits contain status bits 15:8 of the 30-bit-wide horizontal sync DTO increment.					

73h	**SYNC-TIP LEVEL DATA**						
7	6	5	4	3	2	1	0
synctip_level[9:2]							
Mnemonic	**Type**	**Description**					
synctip_level[9:2]	R	These bits contain status bits [9:2] of the 10-bit sync-tip level data					

77h	**BLANK LEVEL DATA**						
7	6	5	4	3	2	1	0
blank_level[9:1]							
Mnemonic	**Type**	**Description**					
blank_level[9:2]	R	These bits contain status bits [9:2] of the 10-bit blank level data					

7Dh	**BLANK/SYNC-TIP DATA**						
7	6	5	4	3	2	1	0
Reserved				synctip_level[1:0]		blank_level[1:0]	
Mnemonic	**Type**	**Description**					
blank_level[1:0]	R	These bits contain status bits [1:0] of the 10-bit blank level data					
synctip_level[1:0]	R	These bits contain status bits [1:0] of the 10-bit sync-tip level data					

80h	**VDEC LUMA PEAKING REGISTER**						
7	6	5	4	3	2	1	0
Reserved	secam_ybw	peak_range		peak_gain			peak_en
Mnemonic	**Type**	**Description**					
peak_en	R/W	This bit enables the luma horizontal peaking control around the colour subcarrier 0 = Disabled (default) 1 = Enabled					
peak_gain	R/W	These bits set the gain for the luma horizontal peaking control. This allows adjustable gain to the luma around the colour subcarrier frequency (default = 2).					
peak_range	R/W	These bits set the range of peak_gain Setting — peak_range value 00 — 1 (default) 01 — 2 10 — 4 11 — 8					

secam_ybw	R/W	These bit set the SECAM luma notch filter bandwidth 0 = narraw (default) 1 = wide

83h	**VDEC CHROMA_LOCK_CONFIG**						
7	6	5	4	3	2	1	0
lose_chromalock_count				lose_chromalock_level			lose_chroma lock_ckill

Mnemonic	**Type**	**Description**
lose_chromalock_ckill	RW	When set, chroma is killed whenever chromlock is lost (default = 1).
lose_chromalock_level	RW	Set the level for chromakill (default = 7).
lose_chromalock_count	RW	This register is used to tune the chromakill, smaller values are more sensitive to losing lock (default = 6).

5.5.4 VDEC Input and ADC/VDEC Output Control Register

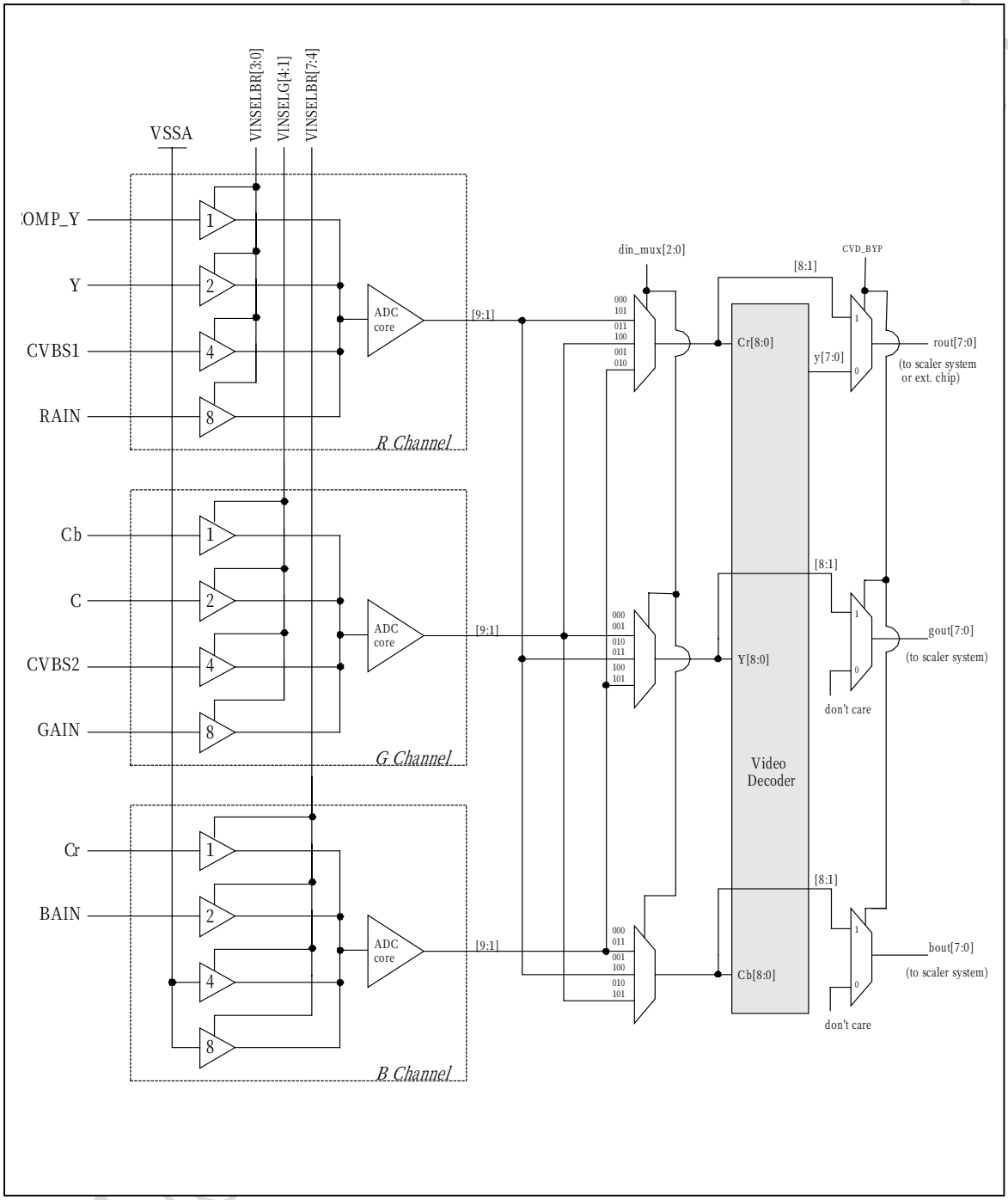
A0h	**OUTPUT_CONTROL**						
7	6	5	4	3	2	1	0
ccir656_en	cbcr_swap	blue_mode		yc_delay			

Mnemonic	**Type**	**Description**
yc_delay	R/W	This 2's complement number controls the output delay between luma and chroma. Negative values shift luma outputs to the left while positive values shift luma values to the right. The range is [-5,7]., and the default = 0
blue_mode	R/W	This bit controls the blue screen mode. 00 = Disabled 01 = Enabled 10 = Auto (Default) 11 = reserved
cbcr_swap	R/W	This bit swaps Cb/Cr outputs. 0 = don't swap Cb/Cr (default) 1 = swap Cb/Cr
ccir656_en	R/W	This bit enable the CCIR656 output

A1h	**OUTPUT_CONTROL**						
7	6	5	4	3	2	1	0
reserved	din_mux			flip_yuv	output_format	ofid_pol	blank_mask_en
	000			0	0	0	0

Mnemonic	**Type**	**Description**
blank_mask_ en	R/W	Force the output data during blanking interval to be zeros 0: non-mask the output data 1: mask the output data
ofid_pol	R/W	Vdec output fid pin polarity
output_format	R/W	Select the output data format 0: 8 bits data output 1: 16 bit data ouput
flip_yuv	R/W	Swap the output data of Y and U/V

din_mux	R/W	The digital switches for the mapping of ADC output to YCbCr digital input. Y Cb Cr 000 : G B R 001 : G R B 010 : R G B 011 : R B G 100 : B R G 101 : B G R



ADC/Video-decoder output multiplexing

5.5.5 Y/C Separation Register

AFh	**Y/C separation control 1**						
7	6	5	4	3	2	1	0

Mnemonic	**Type**	**Description**
Y/C control 1	R/W	Default is 0AH, and set to 05H for NTSC mode, and 0AH for PAL mode

B0h	**Y/C separation control 2**						
7	6	5	4	3	2	1	0

Mnemonic	**Type**	**Description**
Y/C control 2	R/W	Default is 0FAH, and set to 0FAH for NTSC mode, and 0FH for PAL mode

B5h	**VDEC chroma edge enhancement REGISTER**						
7	6	5	4	3	2	1	0
chroma_peak_en	chroma_coring_en	*reserved*				chroma_peak	

Mnemonic	**Type**	**Description**
chroma_peak	R/W	These register bits specified the peak gain for the chroma edge enhancement. Increase this value will increase the sharpness of the chroma edge. Default = 3
chroma_coring_en	R/W	This register bit enables the coring function circuit which is used to eliminate the low level chroma noise such that the low amplitude noise will not be amplified. Default = 1
chroma_peak_en	R/W	This register bit enable the chroma edge enhancement circuit. Default = 0

B7h	**Y/C control 3**						
7	6	5	4	3	2	1	0

Mnemonic	**Type**	**Description**
Y/C control 3	R/W	Default is 0H, and set to 04H for NTSC mode, and 34H for PAL mode

BBh	**VDEC MISC CONTROLLER REGISTER 1**						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
reserved						byp_adc	byp_vd
						0	0

Mnemonic	**type**	**description**
byp_vd	R/W	Bypass the digital part of Vdec and use ADC only.
byp_adc	R/W	Bypass internal ADC. (debug test use only)

BEh	**VDEC MISC CONTROLLER REGISTER 2**

7	6	5	4	3	2	1	0

Mnemonic	type	description
MISC 2	R/W	Default is 00H, and set to 08H

5.5.6 Noise Reduction Registers

CFh	VDEC NR CONTROL REGISTER 1						
7	6	5	4	3	2	1	0
reserved				nr_demo_mode		nr_mode	
				00		00	

Mnemonic	type	description
nr_mode	R/W	For noise reduction, 00 = none(default) 01 = processed with 2d noise reduction others reserved
nr_demo_mode	R/W	For noise reduction, 0x = normal(default) 10 = demo by horizontal 11 = demo by vertical

E0h	VDEC NR CONTROL REGISTER 2						
7	6	5	4	3	2	1	0
reserved						nr_ outcode	nr_incode
						0	0

Mnemonic	type	description
nr_incode	R/W	This bit shows the input yuv format for noise reduction. 0 = unsigned(default) 1 = signed
nr_outcode	R/W	Set the desired the yuv output format from noise reduction. 0 = unsigned(default) 1 = signed

E1h	VDEC NR CONTROL REGISTER 3						
7	6	5	4	3	2	1	0
nr2d_thrd							
0000-0100							

Mnemonic	type	description
nr2d_thrd	R/W	Threshold for 2d noise reduction

EBh	VDEC NR CONTROL REGISTER 4						
7	6	5	4	3	2	1	0
reserved			cr_sel	nr_demo_ch	reserved		
			0	0			

Mnemonic	type	description
nr_demo_ch	R/W	0 = left/up part is processed 1 = right/down part is processed

cr_sel	R/W	For component video, select Pb_valid at the chip

ECh	VDEC NR CONTROL REGISTER 5						
7	6	5	4	3	2	1	0
reserved					weight_method	nr2d_yc	
					0	11	

Mnemonic	type	description
nr2d_yc	R/W	Whether processed by 2d noise reduction 00 = none(default) 10 = luma only 01 = chroma only 11 = both
weight_method	R/W	

5.5.7 Closed Caption Registers

F0h	VDEC CC CONTROL REGISTER 1						
7	6	5	4	3	2	1	0
Reserved	cc_timer_erase			cc_mode			
	000			0000			

Mnemonic	type	description
cc_mode	R/W	Data display mode. 0000 = CC1{odd field, channel 1}(default) 0001 = CC2{odd field, channel 2} 0010 = CC3{even field, channel 1} 0011 = CC4{even field, channel 2} 0100 = T1{odd field, channel 1} 0101 = T2{odd field, channel 2} 0110 = T3{even field, channel 1} 0111 = T4{even field, channel 2} 1xxx = XDS data and odd field mode can work at the same time
cc_timer_erase	R/W	Timer erase select 000 = disable 110 = enable

F1h	VDEC CC CONTROL REGISTER 2						
7	6	5	4	3	2	1	0
reserved		cc_external	uv_swap	bypass_cc	erase_memory	underline	osd_flipfield
		1	0	0	0	0	0

Mnemonic	Type	description
osd_flipfield	R/W	Flip OSD field 0: don't flip(default) 1: flip field
underline	R/W	Force display underline 0: don't force(default) 1: force display underline

erase_memory	R/W	Erase display memory 0: don't erase(default) 1: erase memory
bypass_cc	R/W	Bypass CC display 0: don't bypass(default) 1: bypass
uv_swap	R/W	Swap U V 0: don't swap(default) 1: swap
cc_external	R/W	Decide CC display data from internal decoder or insertion port 0: internal decoder 1: insertion port(default)

F2h	**VDEC CC CONTROL REGISTER 3**						
7	6	5	4	3	2	1	0
roll_up_speed		roll_up	roll_up_setting				
00		0	0-0000				

Mnemonic	**Type**	**description**
roll_up_setting	R/W	Roll-up method select (suggest 01)
roll_up	R/W	Force roll up 0: don't set(default) 1: roll up one row
roll_up_speed	R/W	Adjust roll up speed 00:roll up one line every field(default) 01:roll up one line every two fields 10:roll up one line every three fields 11:roll up one line every four fields

F3h	**VDEC CC CONTROL REGISTER 4**						
7	6	5	4	3	2	1	0
debug_fifo	disable_transparent	erase_screen_en	backspace	user_input	cc_test_mode	delay_fb	
0	0	0	0	0	0	00	

Mnemonic	**Type**	**description**
delay_fb	R/W	Adjust the position of fast_blanking 00: original(default) 01: delay 1 clk 10: delay 2 clk 11: delay 3 clk
cc_test_mode	R/W	CC test mode, when set ,it will automatically fill display memory. 0: don't set(default) 1: set
user_input	R/W	User can input 2 bytes CC data from I2C. 0: don't set(default) 1: User input mode
backspace	R/W	Force backspace 0: don't work(default) 1: erase one character

erase_scereen_en	R/W	When this bit is set, the display data will be erase during pause, forward and backward. 0: don't set(default) 1: set
disable_transparent	R/W	Disable transparent char 0: don't disable transparent 1: disable transparent
debug_fifo	R/W	Store CC data into XDS_FIFO for debug 0: don't store cc data into xds_fifo 1: store cc data into xds_fifo

F4h	**VDEC CC CONTROL REGISTER 5**						
7	6	5	4	3	2	1	0
background				color			
0000				0000			

Mnemonic	**Type**	**description**
color	R/W	Force foreground color. 0xxx = define by CC control code 1000 = Black 1001 = Blue 1010 = Green 1011 = Cyan 1100 = Red 1101 = Magenta 1110 = Yellow 1111 = White
background	R/W	Force background color. 0000 = define by CC control code 0000 = Black 0001 = Blue 0010 = Green 0011 = Cyan 0100 = Red 0101 = Magenta 0110 = Yellow 0111 = White 1xxx = opaque

F5h	**VDEC ERASE TIME REGISTER**						
7	6	5	4	3	2	1	0
Reserved	zero_time	erase_time		Reserved			
	0	00					

Mnemonic	**Type**	**description**
erase_time	R/W	If no cc signal during erase_time ,screen will be erase 00: 2sec(default) 01: 4sec 10: 6sec 11: 8sec
zero_time	R/W	Get zero data during 8sec, screen will be erase 0: disable 1: enable

F6h	VDEC XDS_FIFO_STATUS REGISTER						
7	6	5	4	3	2	1	0
reserved					xds_fifo_rdy	xds_ fifo_empty	xds_ fifo_full
					0	0	0

Mnemonic	Type	description
xds_fifo_full	R	XDS fifo status 0: fifo is not full 1: fifo is full
xds_fifo_empty	R	XDS fifo status 0: fifo is not empty 1: fifo is empty
xds_fifo_rdy	R	XDS fifo can be read 0: fifo is not ready, it can't be read 1: fifo is ready

F7h	VDEC XDS_DATA REGISTER						
7	6	5	4	3	2	1	0
xds_data							
0000-0000							

Mnemonic	Type	description
xds_data	R	XDS data read from I2C

F8h	VDEC USER INPUT REGISTER 1						
7	6	5	4	3	2	1	0
user_ccdata1							
0000-0000							

Mnemonic	Type	description
user_ccdata1	R/W	User can input cc data from i2c (byte1)

F9h	VDEC USER INPUT REGISTER 2						
7	6	5	4	3	2	1	0
user_ccdata2							
0000-0000							

Mnemonic	Type	description
user_ccdata2	R/W	User can input cc data from i2c (byte2)

FAh	VDEC CC HORIZONTAL POSITION REGISTER						
7	6	5	4	3	2	1	0
cc_h_start							
0000-0000							

Mnemonic	Type	description
cc_h_start	R/W	CC display horizontal position

FBh	VDEC CC VERTICAL POSITION REGISTER						
7	6	5	4	3	2	1	0
reserved		xds_wr_en	cc_v_start				
		0	0-0000				

Mnemonic	Type	description
cc_v_start	R/W	CC display vertical position
xds_wr_en	R/W	XDS fifo enable 0: XDS data can't write to fifo 1: XDS data can write to fifo

FFh	VDEC VERSION NUMBER REGISTER						
7	6	5	4	3	2	1	0
version_number							
0000-0001							

Mnemonic	Type	description
version_number	R	

5.6 Scalar System (SC)

The VP77 scalar system receives the CCIR656/YUV444/RGB signals and performs image scaling on the digitized RGB data. An auto adjustment function provides automatic frequency, phase, H&V position, saturation, and white balance tuning in graphics mode. It also contains display mode auto detection circuitry that provides accurate H and V timing detection for all display modes (including Sync-On-Green signals). VP77 contains an on chip OSD (On Screen Display) logic together with an overlay port for external OSD signals interface.

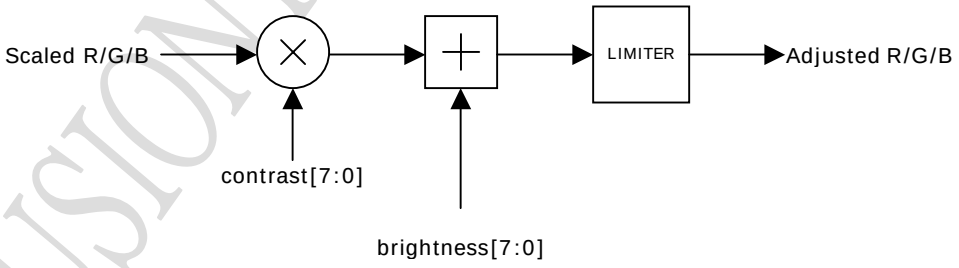
5.6.1 Color Adjust

VP77 supports the contrast control useng a 8-bit signal to set a multiply value from 2 to 0 (in fact, the 256 choices are 255/128, 254/128, ..., 128/128, .., 1/128, 0). The brightness correction uses a 8-bit signal to set an offset value from 127 to -128 (the 256 choices are 127, 126, ..., 1, 0, -1, ..., -127, -128). The control signals BRIGHTNESS[7:0] and CONTRAST[7:0] are programmable via serial interface. The formula to set CONTRAST[7:0] value is ((CONTRAST+128) mod 256)/128 where CON-TRAST is in the range of [255,0]. For brightness control, the signal BRIGHTNESS[7:0] is interpreted as a 2s complement value.

TABLE 5.5.3. Contrast & Brightness definition

Contrast correction for MSB=0						
contrast[7:0]	7f(hex)	7e	.....	02	01	00
multiply value	255/128	254/128	.....	130/128	129/128	128/128
Contrast correction for MSB=1						
contrast[7:0]	ff(hex)	fe	.....	82	81	80
multiply value	127/128	126/128	.....	2/128	1/128	0/128

Brightness correction for MSB=0							
brightness[7:0]	7f(hex)	7e	7d	.....	02	01	00
offset value	127	126	125 .	.....	2	1	0
Brightness correction for MSB=1							
brightness[7:0]	ff(hex)	fe	fd	.....	82	81	80
offset value	-1	-2	-3	.....	-126	-127	-128



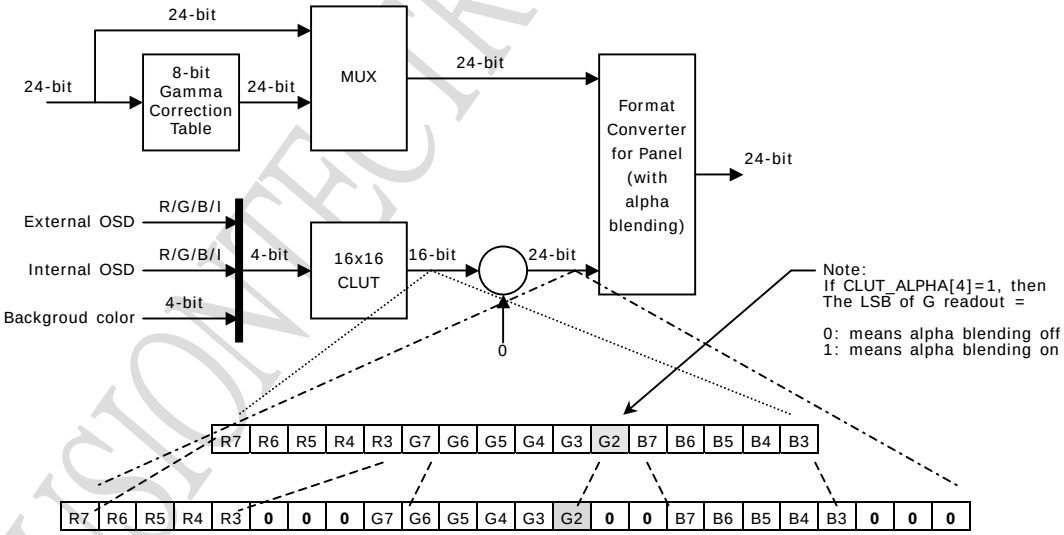
5.6.2 Gamma Correction RAM Tables

Gamma correction RAM tables are implemented after the Brightness/Contrast block to provide the color-mapping of the RGB data. The tables can be activated by setting GAMMAUSE (MSB of OUTCTR1 or 04 hex) bit = 1. We can also by-pass the gamma correction function by resetting the GAMMAUSE bit = 0. Through three gamma table registers (GRWADDR, GGWADDR and GBWADDR) the data representing gamma curves can be put into the RAMs sequentially.

5.6.3 OSD, CLUT

This VP77 embeds an On Screen Display function for human interfacing. It is designed to display colored patterns, icons or characters onto the screen. A 127 character fonts (downloadable from MCU) are provided for the application of Multi-language TV/Monitor. The Graphic Character Fonts can produce the effect of the pixel based graphic display, which allows the impressive display of the customized pattern or logos. The OSD provides plentiful features to enhance the appearance of the displayed character fonts. Each character can have its own colors (up to 16 colors) and blinking option. Up to 10 shadowing modes (including bordering, boxing etc.) are provided together with 16 background colors. The versatile choice for display font color, background/shadow/window color, and shadow modes (including bordering and graphic character mode) leads to a unique OSD style. Some dynamic features, such as built-in see-through curtain effect, two-direction wipe in/out, character basis blinking, hardware overlapping windows etc. also enhance the image of OSD menu.

There is a 16x16 CLUT (color look-up table) which provides a programmable color palette for internal/external OSD and background color. The color index bus, namely R/G/B/I, is used as the address to the CLUT which defines the 16 colors for OSD and background color. The content and the index selection of CLUT are programming via serial interface. The mapping of the 16-bit RGB565 color to 24-bit true color is depicted as the following figure.



Scalar's 2-wire serial bus registers table

ADDR (hex) H\L	0	1	2	3	4	5	6	7
0	ID_VER	INCTR0	INCTR1	OUTCTR0	OUTCTR1	OUTCTR2	INCTR2	INCTR3
1	IH_ASTART		IH_AWIDTH		IH_TOTAL		IV_ASTART	
2	AWIVSTA		IH_AWIDTH		IH_TOTAL		IV_ASTART	
3	PH_ASTART		PH_AWIDTH				PV_AWIDTH	
4	BH_ASTART		BH_END			RESET_REG		
5	PBV_AOFFSET_EVEN		PBV_AOFFSET_ODD		PBV_AWIDTH		OSD_FONT_ADR	OSD_FONT_LSB
6	OFFSET_NO		SYNC_DISTANCE		LINE_MARGIN		IHSC_AWDITH	
7	VDENO	SDNHDX	SDHDY	SDNHHINC	FREAD_R	FREAD_G	FREAD_B	
8	RGB_OV	RGB_MIN	AW2VSTA		AW2VEND			
9	HEND		HSR	HSG	HSB	HER	HEG	HEB
A	ICLK_MEAS		PCLK_MEAS		IH_TOTAL_MEAS		PWG_OUTSC1	PWG_OUTSC2
B	GCONTRSAST	GBRIGHTNESS	GRWADDR	GGWADDR	GBWADDR	LUTWADDR	CLUT_ALPHA	BCONTRAST
C			OSD_SYS_CTRL		PH_TOTAL		PH_DELAY	
D	HWDCNT	INTSRC	SYNC_STATUS	HPERIOD		VPERIOD		PULCNT
E	PEAK_CTRL1	PEAK_CTRL2	PEAK_CTRL3	PEAK_CTRL4	PEAK_CTRL5	PEAK_CTRL6		
F	OSD_FONT_ADR2	OSD_DISP_OP1		OSDLUT			AW2HSTA	

ADDR (hex) H\L	8	9	A	B	C	D	E	F
0	MISCTR2	MISCTR3	MISCTR0	MISCTR1	MISCTR4	STATUS1	INTCTR	MISCTR5
1	IV_AWIDTH		IV_TOTAL		IH_PULW		IVS_DELAY	VS_FPORCH
2	ASUM				ASOD			
3	PV_TOTAL		PH_PULW	PV_PULW	OLHNV		GRAPHICS_STR (OSD)	GRAPHICS_END (OSD)
4	CTI_CTRL1	CTI_CTRL2	CTI_CTRL3	CTI_CTRL4		SINHUE	COSHUE	BLACK
5	OSD_FONT_MSB	OSD_FONT_ATTR	OSD_FONT_CODE	OSD_DRAM_ADR0	OSD_DRAM_ADR1	PWM0_PULH	PWM0_PERIOD	
6		VDX		VDY		VHINC	ALGO_SD	VNUME
7	SOD_MASK	PWM0_PULH	CLAMP_START	CLAMP_WIDTH	IV_WRAP		IH_WRAP	
8	MLNUM		VSTART		VEND		HSTART	
9	LNUM		PDFVADDR		PDFHSTART		LB_MARGIN	
A	PWG_OUTSC3	PX_AS_ALINE			AML_OVERFLOW		RCONTRAST	RBRIGHTNESS
B	BBRIGHTNESS	GCSTART	PLLCTRL0	PLLCTRL1	AUXIDL	AUXIDH	PLLCTRL2	
C		IV_SFDL	OSD_SPDEF	OSD_DISP_OPT0	OSD_HPOS	OSD_VPOS	OSDCTR0	OSDCTR1
D	HVPWTH	POUTPOLPOS	HMDMisc	HfpHigh	HVfpLoe	VfpHigh	VsepProgLo	VsepProgHi
E		FREAD (Freeze Line)	FVADDR (Freeze Line)		FHSTART (Freeze Line)			VsPd_with_Hs
F	AW2HEND		PWG_OUTCTR1	PWG_OUTCTR2	PWG_OUTCTR3	PWM1PULH	PWM2PULH	

SC's I/O and Misc. Registers Descriptions:

REGISTER FUNCTION	ADDR (hex)	D7	D6	D5	D4	D3	D2	D1	D0
Chip ID and Version (ID_VER)	00H	ID_VER[7:0]							
Input Control Register 0 (INCTR0)	01H (R/W)	DIS_IHSPOL	IHS_POL	IVS_SELECT	IVS2PVS		AVREF_USE	AHREF_USE	RGB_ORDER
Input Control Register 1 (INCTR1)	02H (R/W)	ICLK_INV	IACLK_DELAY[2:0]			LLCK_DELAY[1:0]		OSD_CLK_EN	IRGBEN
Output Control Register 0 (OUTCTR0)	03H (R/W)	DITHER_ON	CHP1_CTR1	PCLKIN_EXT	PCLK_INV	PCLK_OP[2:0]			
Output Control Register 1 (OUTCTR1)	04H (R/W)	GAMMA_USE	RST_GT_ADR	CPH1_CTR2	BKFRC	BKCOL[3:0]			
Output Control Register 2 (OUTCTR2)	05H (R/W)	OVCLK_DELAY[2:0]				PVS_POL	PHS_POL	PDE_POL	POUT_OFF
Input Control Register 2 (INCTR2)	06H (R/W)	SWAP_RB	MATRIX_ON	RY_SEL	RGB_INVM	EXT_VIDEO	UTI_YUV656	EN_FREEZE	RE_FHADDR
Input Control Register 3 (INCTR3)	07H (R/W)	YUV444	ODD_POL	INCODE	INTERLACE_SEN	IV_INV	IH_INV	FID_MSEL	FID_ESEL
Misc. Control Register 2 (MISCTR2)	08H (R/W)	VCLKO_MODE[3:0]				CPH_MODE[3:0]			
Misc. Control Register 3 (MISCTR3)	09H (R/W)	PLL_54M_EN	USB_DATCK	27M_SEL	XOSC2ADC_DIV2_EN	ADC_ICLK_MODE[3:0]			
Misc. Control Register 0 (MISCTR0)	0AH (R/W)	ADC_TST	PWD_EN	XTAL_PULSE_SEL[1:0]		VHSYN_SEL	DACTST	FREERUN_N	RGB_OUT_DIS
Misc. Control Register 1 (MISCTR1)	0BH (R/W)	OSDLUT_RELOAD	OVS_VACTIVE	EOSD_EN	EOSDFR	EOSD_SYNSEL	CLAMP_OFF	ACLK_SEL	IIC_ACT_DIRECT
Misc. Control Register 4 (MISCTR4)	0CH (R/W)	VIDEO_PIN_IN_EN	VIDEO_PIN_OUT_EN	SC_OUT2D_EN	SC_OUT2A_EN	ADC_PLL_CLK_OFF	PWG_CLK_OFF	BYP_CVD	CPH_OFF
Status Register (STATUS1)	0DH (R)						APXL_RESORT	ASOD_RDY	AML_RDY
Interrupt Control Register (INTCTR)	0EH (W)	INTEN							
Misc. Control Register 5 (MISCTR5)	0FH (R/W)	DAC_CLKX3_EN	CPH_OUT_EN	DCPWMOUT_OFF	DAC_EN				DAC_INVERT

ID_VER (Chip ID and Version, 00H)			Default
7-0	ID_VER for VP77	01100010	62

INCTR0(INput Control Register 0, 01H)			Default
7	DIS_IHSPOL	0: Auto detecting function of the polarity of HS of input video will be checked automatically 1: Auto detecting function of the polarity of HS of input video will be disabled Note: The polarity of VS of input video will be checked automatically	0
6	IHS_POL	0: The rising edge of input HS will be used as the start of the sync pulse 1: The falling edge of input HS will be used as the start of the sync pulse	0
5	IVS_SELECT	Input VS source selection. 0: from external IVS, 1: from internal mode detection circuit.	0
4	IVS2PVS	PVS generation using the rising/falling edge of IVS (For the case PVS is generated by free-running, this control bit is invalid) 0: falling edge. 1: rising edge.	0
3	-	reserved	0
2	AVREF_USE	1: scalar use VREF from external scalar 0: scalar use VREF from internal scalar	0
1	AHREF_USE	1: scalar use HREF from external scalar 0: scalar use HREF from internal scalar	0
0	RGB_ORDER	1: RGB[7:0] output changed to RGB[1,0,7~2]; 0: no change, [7:0]	0

INCTR1(INput Control Register 1, 02H) Default			Default
7	INCLK_INV	INCLK invert enable 0: normal input clock 1: invert input clock	0
6:4	IACLK_DELAY[2:0]	Programmable delay for IACLK 000 ~ 111: 0 to 7 unit delay	000
3:2	LLCK_DELAY[1:0]	Programmable delay for LLCK 00 ~ 11: 0 to 3 unit delay	0
1	OSD_CLK_EN	0: internal OSD clock inactive 1: internal OSD clock active	1
0	IRGBEN	0: video input 1: RGB input	1

OUTCTR0(Output Control Register 0, 03H) (This register can be read and write)			Default
7	DITHER_ON	0: no dithering (for the panel with 8 bit color depth per R/G/B) 1: 2 bit dithering (for the panel with 6 bit color depth per R/G/B)	0
6	CHP1_CTR1	0: CHP1 source is from PCLKI 1: CHP1 source is from PCLK6I (PCLKI div6)	0
5	PCLKIN_EXT	The way PCLK, panel clock, is generated. 0: PCLK is generated by internal PLL. 1: PCLK is fed from PCLKIN pin (by external source).	0
~~4~~	PHCLK_INV	0: Normal PHCLK clock output to panel 1: Inverted PHCLK clock output to panel (The relationship of PHCLK and PCLK is also defined by PHCLK_OP(1:0))	1
~~3:1~~	PHCLK_OP (2:0)	Phase deviation of PHCLK with respect to PCLK 000: No delay 001: Delay 1 unit	000

		010: Delay 2 units 011: Delay 3 units 100: Delay 4 units 101: Delay 5 units 110: Delay 6 units 111: Delay 7 units (The relationship of PHCLK and PCLK is also defined by PHCLK_INV.)	

OUTCTR1 (OUTput Control Register 1, 04H)			
7	GAMMA_USE	Use GAMMA correction table for each R,G, and B. 0: Bypass the GAMMA table 1: Use the GAMMA look-up table	0
6	RST_GT_ADR	Reload Gamma Table starting address control bit The Gamma Table starting address is reloaded to the value defined by Reg GCSTART (B9h)while there is a low to high transition	0
5	CHP1_CTR2	0: CHP1 use original source as CPH2/3 1: CHP1 use new source sync. with scalar clock phase	0
4	BKFRC	Panel output Force to Background color 0: Normal Panel output 1: Output Panel is forced to Background color, the color is selected by BKCOL[3:0]	0
3:0	BKCOL[3:0]	Panel output Background color select signals. These signals share the look-up table with OSD to generate colors.	000

OUTCTR2 (OUTput Control Register 2, 05H)			
7:5	OVCLK_DELAY[2:0]	OVCLK phase deviation for the nominal clock reference phase. OVCLK_DELAY[2]: 0: OVCLK for OSD output is not inverted, 1: OVCLK for OSD output is inverted. Besides, there are delays defined by OVCLK_DELAY[1:0] as follows: OVCLK_DELAY[1:0]: 00: 0 unit delay, 01: 1 unit delay, 10: 2 units delay, 11: 3 units delay.	000
3	PVS_POL	PVS output polarity (inside use active High) 0: Negative polarity (active Low) 1: Positive polarity (active High)	0
2	PHS_POL	PHS output polarity (inside use active High) 0: Negative polarity (active Low) 1: Positive polarity (active High)	0
1	PDE_POL	0: active High for display data enable output to panel 1: active Low for display data enable output to panel	0
0	POUT_OFF	Panel output control & data disable 0: PHS, PVS, PDE, PARED/PAGRN/PABLU, and PBRED/PBGRN/PBBLU output are enabled. 1: PHS, PVS, PDE, PARED/PAGRN/PABLU, and PBRED/PBGRN/PBBLU output are set to weak pull low.	0

INCTR2(INput Control Register 2, 06H)			Default
7	SWAP_RB	Input R channel and B channel can be swapped by setting this bit	0
6	MATRIX_ON	0: YUV2RGB matrix disable 1: YUV2RGB matrix enable	0
5	RY_SEL	0: color adjust based on RGB 1: color adjust based on YUV	0
4	RGB_INVM	0: RGB2YUV matrix disable 1: RGB2YUV matrix enable	0
3	EXT_VIDEO	0: scalar's video signal comes from internal video decoder	0

		1: scalar's video signal comes from external chip	
2	UTI_YUV656	0: scalar's video input is not CCIR656 encoded 1: scalar's video input is CCIR656 encoded	0
1	EN_FREEZE	0: disable freeze 1: enable freeze	0
0	RE_FHADDR	Reload freeze H start address	0

INCTR3 (INput Control Register 3, 07H)			
7	YUV444	0: scalar's video input format is not YUV444 1: scalar's video input format is YUV444	0
6	ODD_POL	0: scalar selects 1st field is ODD and ODD is active HIGH 1: scalar selects 1st field is ODD and ODD is active LOW	0
5	INCODE	0: scalar's video input format is binary 1: scalar's video input format is 2's complement	0
4	INTERLACE_SEN	1: interlace shift enable; 0: disable	0
3	IV_INV	0: normal 1: scalar selects inverse input video VS	0
2	IH_INV	0: normal 1: scalar selects inverse input video HS	0
1	FID_MSEL	1: scalar selects from HMD FID 0: scalar selects from internal FID	0
0	FID_ESEL	1: scalar selects from external FID_ODD 0: scalar selects internal FID	0

MISCTR2(Misc. Control Register 2, 08 hex)			Default
7:4	VCLKO_MODE[3:0]	Programmable delay(VCLK_DELAY) for VCLKO (video clock output from VDEC) VCLKO_MODE[2:0]: 000 ~ 111: 0 ~ 7 unit delay VCLKO_MODE[3]: 0: no delay after VCLK_DELAY 1: more half of VCLK delay after VCLK_DELAY	0000
3:0	CPH_MODE[3:0]	Programmable delay(CPH_DELAY) for CPH1/2/3 (analog panel clock) CPH_MODE[2:0]: 000 ~ 111: 0 to 7 unit delay CPH_MODE[3]: 0: no delay after CPH_DELAY 1: more half of CPH delay after CPH_DELAY	0000

MISCTR3(Misc. Control Register 3, 09 hex)			Default
7	PLL_54M_EN	See clock system	0
6	USE_DATCK	See clock system	0
5	27M_SEL	See clock system	0
4	XOSC2ADC_DIV2_EN	See clock system	0
3:0	ADC_ICLK_MODE[3:0]	Programmable delay(ADC_ICLK_DELAY) for ADC input clock ADC_ICLK_MODE[2:0]: 000 ~ 111: 0 to 7 unit delay ADC_ICLK_MODE[3]: 0: no delay after ADC_ICLK_DELAY 1: more half of ADC_ICLK delay after ADC_ICLK_DELAY	0000

MISCTR0(Misc. ConTrol Register 0, 0AH) (This register can be read and write)			Default
7	ADCTST	0: ADC test mode inactive 1: ADC test mode active	0
6	PWD_EN	0: VP77 is alive (CLK_OFF=0) 1: VP77 is in power down mode (CLK_OFF=1)	0
5:4	XTAL_PULSE_SEL	Crystal clock pulse selection. This clock pulse will then be counted by ICLK and PCLK. 00: 1024 crystal clocks. 01: 2048 crystal clocks. 10: 3072 crystal clocks. 11: 4096 crystal clocks.	0
3	VHSYN_SEL	Port A VS & HS synchronization edge 0: Use ACLK rising edge 1: Use ACLK falling edge	0
2	DACTST	0: DAC test mode inactive 1: DAC test mode active	0
1	BYPASS(Output Free-Run Mode)	0: (default) Panel VS and HS (PVS & PHS) free-runs and acts as a sync master. 1: In this mode, the input and output frames are synchronized. In a sense, IVS & IHS are the sync master that generate PVS & PHS. Note: In order to activate free-run mode, micro-controller should choose BYPASS = 0. To this, the input data can be ignored, if necessary, by setting BKFRC= 1 so background colors are sent to panel.	0
0	RGB_OUT_DIS	0:RGB 24 bits output pins active 1:RGB 24 bits output pins inactive	0

MISCTR1(Misc. ConTrol Register 1, 0B hex)			Default
7	OSDLUT_RELOAD	Reload OSD LUT from address F3H 0: inactive. 1: active.	0
6	OVS_VACTIVE	The OSD VS output is generated using 0: Overlay VS as in Zurac1. 1: Vertical display active signal.	0
5	EOSD_EN	0: External OSD will be disabled 1: External OSD will be enabled (The internal OSD can be enabled by IOSD_EN in bit 0 of OSDCTR1 register)	0
3	EOSD_SYNSEL	0: EOSD data latch uses OVCLK 1: EOSD data latch uses the inverse of OVCLK	0
2	CLAMP_OFF	CLAMP pulse will be generated according to the register 7A and 7B (hex) 0: clamp pulse is sent out. 1: clamp pin is in tri-state	0
1	ACLK_SEL	ACLK_SEL is for IACLK selection. 0: ICLK = IACLK/2 (for LLC2) 1: ICLK = IACLK	1
0	IIC_ACT_DIRECT	0: 2-wire serial bus parameters are activated until next VS retrace period. 1: 2-wire serial bus parameters are activated upon data received	1

MISCTR4(Misc. ConTrol Register 4, 0C hex)			Default
7	VIDEO_PIN_IN_EN	0: Video signal input from pins disable 1: Video signal input from pins enable	0
6	VIDEO_PIN_OUT_EN	0: Video signal output to pins disable	0

		1: Video signal output to pins enable	
5	SC_OUT2D_EN	0: scalar output for digital LCD panel disable 1: scalar output for digital LCD panel enable	0
4	SC_OUT2A_EN	0: scalar output for analog LCD panel disable 1: scalar output for analog LCD panel enable	0
3	ADC_PLL_CLK_OFF	See clock system	0
2	PWG_CLK_OFF	See clock system	0
1	BYP_CVD	See clock system	0
0	CPH_OFF	See clock system	0

STATUS1 (Status Register 0, 0DH) (read only)			Default	R/W
7:3	Reserved			
2	APXL_REPORT	For auto adjustment, by setting to 0, the PXL_REPORT function will be performed. This status bit will be set to 1 as the function is completed. This is a RD/WR bit. The PXL_REPORT function can read the pixel value via PXL_Value (x74 ~ x76) of specified position via PXL_Address (x9A ~ 9D).		R/W
1	ASOD_RDY	For auto adjustment, by setting to 0, the SOD (sum or sum of difference) function will be performed. This status bit will be set to 1 as the function is completed. This is a RD/WR bit.	1	R/W
0	AML_RDY	For auto adjustment, by setting to 0, the Mth line function will be performed. This status bit will be set to 1 as the function is completed.	1	R/W

INTCTR (Interrupt Control Register, 0EH)			Default
7	INTEN	0: Disable all interrupt 1: Enable all interrupt	1
6:0	Reserved		

MISCTR5(Misc. ConTrol Register 5, 0F hex)			Default
7	DAC_CLKX3_EN	0: internal DAC clock frequence x1 (DAC_CLK_f * 1) 1: internal DAC clock frequence x3 (DAC_CLK_f * 3)	0
6	CPH_OUT_EN	0: analog panel clock output to pins disable 1: analog panel clock output to pins enable	0
5	DCPWMOUT_OFF	0: DCDC PWM output to pins disable 1: DCDC PWM output to pins enable	0
4:1	DAC_EN	DAC_EN[1]: (DAC global power control) 0: DAC enable 1: DAC disable DAC_EN[4:2]: (DAC sub-channel power control) 001: R channel disable 010: G channel disable 100: B channel disable 000: no disable	0000
0	DAC_INVERT	0: DAC input clock no invert 1: DAC input clock invert	0

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	**Description**

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	Description
INPUT WINDOW PARAMETER				
Input Horizontal Active Start(IH_ASTART[10:0])	11,10	01,28	W	This value should be at least larger than six.
Input Horizontal Active Width (IH_AWIDTH[10:0])	13,12	04,00	W	All default values are setting for test purpose
Input Hsync TOTAL (IH_TOTAL[10:0])	15,14	05,40	W	Input Hsync TOTAL
Input Vertical Active Start (IV_ASTART[10:0])	17,16	00,23	W	Input Vertical Active Start
Input Vertical Active Width (IV_AWIDTH[10:0])	19,18	03,00	W	Input Vertical Active Width
Input Vsync TOTAL (IV_TOTAL[10:0])	1B,1A	03,26	W	Input Vsync TOTAL
Input Hsync Pulse Width (IH_PULW[7:0])	1C	44	W	This register specifies the pulse width of the input Hsync. Within this region the input video data are forced to zero by the internal circuit. The max. allowed value is 255 (in the unit of iclk).
Input VS Delay (VS_EQ_VREF, IVS_DELAY[3:0])	1E	00	W	The input VS delay. The LSB 4-bit is used. By programming these bits, the input VS signal will be delayed by IVS_DELAY*16 or IVS_DELAY*32 pixels (depends on IRGB24=1 or 0, see INCTR1 at register 02H). IVS_DELAY=00 (default) means no delay. The bit higher than IVS_DELAY[3:0] is used for VS_EQ_VREF. Or the generation of internal VS signal for video display. 0: (default) Internal VS is different from VREF input. 1: Internal VS is equal to VREF input.
VS_FPORCH[7:0]	1F	00	W	Define the vertical front porch width when scalar's input video is encoded CCIR656 format
Input Vsync Delay for Wrap Around (IV_DELAY4WRAP[10:0])	7D,7C	00,02	W	The V delay for VGA input. The value 2 (default) means no delay and 3 means one H line delay, and so on (0 and 1 are not allowed.)
Input Hsync Delay for Wrap Around (IH_DELAY4WRAP[10:0])	7F,7E	00,01	W	The H delay for VGA input. The value 1 (default) means no delay and 2 means one pixel delay, and so on (0 is not allowed.)
OUTPUT WINDOW PARAMETER				
Panel Horizontal Active Start(PH_ASTART[10:0])	31,30	01,28	W	Please refer to the figure of Output Window
Panel Horizontal Active Width(PH_AWIDTH[10:0])	33,32	04,00	W	Panel Horizontal Active
Panel Vertical Active Width (PV_AWIDTH[10:0])	37,36	03,00	W	Panel Vertical Active Width
Panel Vsync EVEN TOTAL (PV_TOTAL_EVEN[10:0])	39,38	03,26	W	This 10-bit register defines the Panel Vertical Active Total Lines for non- interlaced video or the Even Field Active Total Lines for interlaced video.
Panel Hsync Pulse Width (PH_PULW[7:0])	3A	88	W	Panel Hsync Pulse Width
Panel Vsync Pulse Width (PV_PULW[7:0])	3B	06		Panel Vsync Pulse Width

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	Description
OLHNVL[10:0]	3D,3C		R	Report the offset between the last PHS to next PVS; MSB:x3D[2:0]; LSB:x3C[7:0]
BACKGROUND WINDOW PARAMETER				
Background Horizontal Start (BH_START[10:0])	41,40	01,28	W	Please refer to the figure of Output Window ALL default values are setting for 1024*768@60Hz
Background Horizontal End (BH_END[10:0])	43,42	05,28	W	
RESERVED	44		W	
RESET_PWM[6:1]	45	02	W	RESET_PWM [1] : RESET_SCALAR reset the rest of blocks (except I2C, PWM, HMD) RESET_PWM [2] : PWM0_OUT_EN 0 : PWM0 output is enable 1 : PWM0 output is disable RESET_PWM [3] : PWM1_OUT_EN 0 : PWM1 output is enable 1 : PWM1 output is disable RESET_PWM [5] : PWM2_OUT_EN 0 : PWM2 output is enable 1 : PWM2 output is disable RESET_PWM [6] : OUTPUT_SWAP 1 : Swap the A/B port output
CTI Control PARAMETER				
CTI_CTRL1	48	06	W	CTI_CTRL1[7]: 0: disable CTI 1: enable CTI CTI_CTRL1[3]: 0: disable the pre-filter 1: enable the pre-filter CTI_CTRL1[2:0]: CTI filter type
CTI_CTRL2	49	42	W	CTI_CTRL2[6:4]: 000: filter_out x1 001: filter_out x2 010: filter_out x3 011: filter_out x4 100: filter_out x5 101: filter_out x6 110: filter_out x7 111: filter_out x8 CTI_CTRL2[1:0]: 00: divided by one 01: divided by two others: divided by four

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	Description
CTI_CTRL3	4A	C1	W	CTI_CTRL3[7]: 0: discontinues coring 1: continuous coring CTI_CTRL3[6:4]: 000: no coring others: 2*CTI_CTRL3 CTI_CTRL3[1:0]: 00: one 01: two 10: three 11: four
CTI_CTRL4	4B	78	W	CTI_CTRL4[7]: 0: disable pre-dcti 1: enable pre-dcti CTI_CTRL4[6]: 0: disable pre-dcti filter1 1: enable pre-dcti filter1 CTI_CTRL4[5]: 0: disable pre-dcti filter2 1: enable pre-dcti filter2 CTI_CTRL4[4]: 0: disable pre-dcti filter3 1: enable pre-dcti filter3 CTI_CTRL4[3]: 0: type 1 of filter1 1: type 2 of filter1
HUE Saturation Control				
SINHUE	4D	00	W	The register defines the SAT_SINHUE setting for YUV domain color adjustment.
COSHUE	4E	80	W	The register defines the SAT_COSHUE setting for YUV domain color adjustment.
BLACK	4F	00	W	The register defines the BLACK setting for YUV domain luminance adjustment. NOTE: During the YUV-domain color setting, the contrast and brightness of R, G and B should be set to the same values.
PANEL BACKGROUND PARAMETER				
Panel background active offset for even field (PB_LEAD_LAG_EN, PBV_AOFFSET_EVEN[9:0])	51, 50	00,00	W	The LSB 10-bit defines the offset of panel background active region for even field. The Value is counted from the PV_ASTART. The MSB, PB_LEAD_LAG_EN, defines lead or lag to PV_ASTART.PB_LEAD_LAG_EN = 1 is lag, otherwise (default) lead.
Panel background active offset for odd field (PB_LEAD_LAG_OD, PBV_AOFFSET_ODD[9:0])	53, 52	00,00	W	The LSB 10-bit defines the offset of panel background active region for odd field. The value is counted from the PV_ASTART. The MSB, PB_LEAD_LAG_OD, defines lead or lag to PV_ASTART.PB_LEAD_LAG_OD = 1 is lag, otherwise (default) lead.
Panel background active width	55, 54	00,00	W	The LSB 11-bit defines the width of panel

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	Description
(PBV_AWIDTH[10:0])				background active region.
OSD control register				
GRAPHIC_START(OSD)	3E	FF	W	Graphic font starting
GRAPHIC_END(OSD)	3F	FF	W	Graphic font ending
OSD Font address [6:0]	56	00	W	Font RAM write address (auto increment). There are 127 (0x00 ~ 0x7E) address for the downloadable fonts. Address 0x7F is the space code.
OSD FONT LSB [7:0]	57	00	W	Font LSB, each font is composed of 20x12 bits
OSD FONT MSB [11:8]	58	00	W	Font MSB
OSD attribute for FONT Code(OSD_AT[7:0])	59	00	W	Font code attribute
OSD FONT code address (OSD_DT[6:0])	5A	00	W	Font code address
OSD Display RAM address 0~255 (OSD_AD0[7:0])	5B	00	W	Display RAM address, range (0-255)
OSD Display RAM address 256-511 (OSD_AD1[7:0])	5C	00	W	Display RAM address, range (256-511)
OSD Display RAM address 512-639 (OSD_AD2[7:0])	F0	00	W	Display RAM address, range (512-639)
OSD System Control	C2	00	W	Bit0~bit1:bits for dot rate selection 00,01: divided by 1 02: divided by 2 03: divided by 3 Bit2:Vint enable interrupt signal to MCU Bit3:WinFB_N drive pin FB 0 or 1 Bit5:VintOrEndL selection between the leading edge of Vsync and the last scanning line Bit6:faderate determine the fade rate 0:0.5 sec / 1:0.25 sec Bit7:WinMask determine whether the outer of OSD window is displayed (WinMask=0) or not(WinMsk=1).
OSD default setting for space code color (OSD_SPDEF])	CA	00	W	Bit0:intensity color of space code Bit1:blue color of space code Bit2:green color of space code Bit3:red color of space code Bit5~bit4:Veritical position step Bit7~bit6:Horziontal position step
OSD DISPLAY OPTION0 (DISPLAY_OPTION0)	CB	00	W	Bit7~5:column space 000:no space 001 ~ 111:1 to 7 dot Bit4~0:Point to the first display row in the display RAM
OSD Horizontal Start in	CC	FF	W	The horizontal starting position

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	**Description**
Window(OSD_HPOS[7:0])				
OSD Vertical Start in Window(OSD_VPOS[7:0])	CD	FF	W	The vertical starting position
OSD control register2 (OSD_CTRL2)	CE	01	W	Bit0:intensity color of monitor mode Bit1:blue color of monitor mode Bit2:green color of monitor mode Bit3:red color of monitor mode Bit4:NOT used Bit5:wipe enable bit Bit6:wipe In/Out Bit7:wipe direction
OSD control register (OSD_CTRL)	CF	1C	W	Bit0:OSD enable bit Bit1:select blinking rarte Bit2:the polarity of R,G,B,I,FB Bit3:Vsync polarity Bit4:Hysnc polarity Bit5:**character font downloadable** 0: disable 1: enable Bit6:half-tone/see through-effect enable bit Bit7:determine if background color can be spilt
OSD DISPLAY OPTION (DISPLAY_OPTION1[2:0])	F1	00	W	Bit0: horizontal mirror font Bit1: vertical mirror font Bit2: rotate font
Address port to address OSD window registers OSDWindow_Addr[6:0]	F4	00	W	Bit4~0:OSD window registers address port Bit5: Vertical position bit 8 Bit6: Horizontal position bit 8
Data port to write OSD window registers OSDWindow_Data[7:0]	F5	00	W	OSD window registers data port
*Those registers are used to define 4 OSD windows. They are programmed through address port (OSDWindow_Addr[6:0], F4h) and data port (OSDWindow_Data[7:0], F5h) using indirect addressing mode				
Win1VS Win2VS Win3VS Win4VS	Ind(00)* Ind(05)* Ind(0A)* Ind(0F)*	00	W	Bit4-Bit0:The display starting row of Window 1,2,3,4
Win1VE Win2VE Win3VE Win4VE	Ind(01)* Ind(06)* Ind(0B)* Ind(10)*	00	W	Bit4-Bit0:The display ending row of Window 1,2,3,4
Win1HS Win2HS Win3HS Win4HS	Ind(02)* Ind(07)* Ind(0C)* Ind(11)*	00	W	Bit0: The Intensity color of window color index Bit1: Window 1 halftone enable bit Bit2: Window 1 enable bit Bit7-bit3: The display starting column of Window 1,2,3,4
WIn1HE Win2HE Win3HE	Ind(03)* Ind(08)* Ind(0D)*	00	W	Bit0: The Blue color of window color index Bit1: The Green color of window color index Bit2: The Red color of window color index

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	Description
Win4HE	Ind(12)*			Bit7-bit3:The display ending column of Window 1,2,3,4
WIn1SH Win2SH Win3SH Win4SH	Ind(04)* Ind(09)* Ind(0E)* Ind(13)*	00	W	Bit1-Bit0: The height of the window shadow Bit3-Bit2: The width of the window shadow Bit4: If set, enable the window shadow If cleared, disable the window shadow Bit7-bit5: The color index of the window shadow The actual color is defined by CLUT.
PWM				
PWM1_HIGH_PERIOD[15:0]	79,5D	00	W	Define the duty ratio of PWM. Duty Ratio = PWM_HIGH_PERIOD / PWM_PERIOD Note: MSB should be programed first. LSB is located at x79[7:0]. The smallest value of PWM_HIGH_PERIOD is 1.
PWM0_PERIOD[15:0]	5F,5E	00,FF	W	Define the freqnency of PWM. PWM frequency = 14.318MHz/ 4 /PWM_PREIOD Note: MSB should be programed first. PWM_PERIOD should be greater than PWM_HIGH_PERIOD. So this PWM can be programed from 55Hz to 1.7MHz.
PWM1[7:0]	FD	00	W	The default value 00 means a low output while the value FF(hex) can be integrated by a capacitor for an almost high signal
PWM2[7:0]	FE	00	W	The default value 00 means a low output while the value FF(hex) can be integrated by a capacitor for an almost high signal
SCALING PARAMETER				
OFFSET_NO	60	00	W	Specify the number of m lines among n lines from which PH_TOTAL is compensated by value 2 (works together with reg. LINE_MARGIN)
SYNC_DISTANCE	63,62		R	Report the distance between last IHS to next PHS from where the output starts to display
LINE_MARGIN	65,64		R	Report the offset pixel number for last synchronized PHS
IH_ACTIVE_SC	67,66		W	For scaling factor calculation, to have a fixed scaling factor
SVdx[7:0], SVdy[7:0], SVhinc[6:0]	69,6B,6D	01,00, 80	W	SVhinc= floor(32/Vsf), Vdy/Vdx= 32/Vsf - SVhinc. These parameters are used for both scaling up and down
ALGO_SD[7:4]	6E	80	W	The MSB 2-bit of ALGO_SD is defined as algorithm for scaling algorithm selection, where SALGO = 0 chooses linear interpolation, SALGO = 1 selects bell shape interpolation,

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	Description
				SALGO = 2 selects SINC (default), SALGO = 3 chooses pixel replicate. The bit 5 V_SD_ON, is used for enabling V scaledown operations, i.e. VSD_ON=0 (default) for scaling up, VSD_ON=1 for scaling down The bit 4 H_SD_ON, is used for enabling H scaledown operations, i.e. HSD_ON=0 (default) for scaling up, HSD_ON=1 for scaling down
VNEMU(6:0)	6F	01	W	Vnume/Vdeno = Vsf
VDENO(6:0)	70	01	W	
SDNHdx[6:0], SDNHdy[6:0], SDNHhinc[5:0]	71,72,73	01,00, 08	W	For scaling down, SDNHhinc= floor(8/Hsf), SDNHdy/SDNHdx= 8/Hsf - SDNHhinc. Note that we should set SHdx[6:0]=01, SHdy[6:0]=00, and SHhinc[5:0]=20 for scaling down operation. Also note that SDNHdx[6:0]=01, SDNHdy[6:0]=00, and SDNHhinc[5:0] =08 should be set for scaling up operation.
FREAD	E9	00	R	Read out the freezed data
FVADDR	EB,EA	00	W	Freeze vertical start address
FHADDR	ED,EC	00	W	Freeze horizontal start address
Registers 74-78 are for Auto Adjustments				
MISC				
Clamp pulse starting setting register (CLAMP_STA)	7A	8A	W	The starting point of clamp pulse setting. Counted from the falling edge of sync pulse by IACLK.
Clamp pulse width setting register (CLAMP_WIDTH)	7B	80	W	The width of clamp pulse by IACLK (1.2us is suggested)
AUTO Adjust Register				
The 1st line of the window for SOD calculation (AWV1START[10:0])	21,20	00,00	W	Define the range of intra-frame SOD operation. Note that AWVSTART and AWHSTART are counted from the starting edge of input VSync/HSync pulse. AWVSTART should be larger than 3 and AWHSTART should be larger than 6.
The last line of the window for SOD calculation (AWV1END[10:0])	23,22	00,00	W	
The 1st pixel of the window for SOD calculation (AWH1START[10:0])	25,24	00,00	W	
The last pixel of the window for SOD calculation (AWH1END [10:0])	27,26	00,00	W	
The 1st line of the window for SOD calculation (AWV2START[10:0])	83,82	00,00	W	Define the range of intra-frame SOD operation. Note that AWVSTART and AWHSTART are counted from the starting edge of input VSync/HSync pulse. AWVSTART should be larger than 3 and AWHSTART should be larger
The last line of the window for SOD calculation (AWV2END[10:0])	85,84	00,00	W	
The 1st pixel of the window for SOD calculation (AWH2START[10:0])	F7,F6	00,00	W	

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	Description
The last pixel of the window for SOD calculation (AWH2END [10:0])	F9,F8	00,00	W	than 6.
The resulting value of the sum of the SOD calculation (ASUM[31:0])	28,29, 2A,2B	00,00	R	The resulting value of the sum of the SOD calculation.
The resulting value of sum of difference of the SOD calculation (ASOD[31:0])	2C,2D 2E,2F	00,00	R	
PXL Value	76,75,74	00,00	R	Report the data value of specified position in PXL_Address (x9A~9D) 74 : R 75 : G 76 : B
Reserved	77	00	W	
SOD Mask Register (SODMASK[7:0])	78	00	W	The MSB 3 bit of SODMASK[7:0], SOD_MASK_BIT[2:0], is used to select the number of MSB bits for SOD operation. The default state is all channels are calculated.
Registers 79-7B (PWM and clamp) are described at MISC, and Registers 7C-7F (IHV_DELAY4WRAP) are described at INPUT WINDOW.				
Maximum Threshold (ARGB_MAX[7:0])	80	7F	W	Designate the threshold value for R, G, and B. The result will be available at AML_OVERFLOW (Reg. 0xAC)
Minimum Threshold (ARGB_MIN[7:0])	81	00	W	Designate the threshold value for either R, G, or B
The Mth line chosen to check the horizontal start & end (AMLNUM[10:0])	89,88	00,00	R/W	Designated by host, the auto adjust function searches (horizontally) the starting and ending pixels along the Mth line. If 00 are programmed, the entire screen is covered for H_start and H_end points searching.
The 1st line exceeds ARGB_MIN (AVSTART[10:0])	8B,8A	00,00	R	The 1st line exceeds ARGB_MIN.
The last line exceeds ARGB_MIN (AVEND[10:0])	8D,8C	00,00	R	The last line exceeds ARGB_MIN.
The 1st pixel exceeds ARGB_MIN position at Mth line (AMLHSTA[10:0])	8F,8E	00,00	R	The 1st pixel exceeds ARGB_MIN position at Mth line
The last pixel of the Mth line exceeds ARGB_MIN position (AMLHEND[10:0])	91,90	00,00	R	If SOD_INTRA = 1 (SOD, sum of difference), the number read should minus one.
The RGB value of the 1st pixel of the Mth line that exceeds ARGB_MIN (AMLHSTAR[7:0],AMLHSTAG[7:0],AMLHSTAB[7:0])	92,93,94	00,00,00	R	If SOD_INTRA = 1 (SOD, sum of difference), the values are not available.
The RGB value of the last pixel of the Mth line that exceeds ARGB_MIN(AMLHENDR[7:0],AMLHENDG[7:0], AMLHENDB[7:0])	95,96,97	00,00,00	R	If SOD_INTRA = 1 (SOD, sum of difference), the values are not available

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	Description
RESERVED	98		W	
VHPERLOW_16BIT	99	00		The MSB 4-bit of Reg 99 is Vperiod[3:0] and the LSB 4-bit is Hperiod[3:0]
PXL Address	9B,9A 9D,9C		W	The PXL_REPORT function (xOD[2]) can read the pixel value via PXL_Value (x74 ~ x76) of specified postion via PXL_Address (x9A ~ 9D). Note: 9A 9B V position (Y) 9C 9D H position (X) The position are counted and aligned to V/Hsync.
VSEP_SPT	9F,9E	00,60	R	programmable sampling point, this is a 12-bits register for Csync separation
Registers A0-A7 are for ICLK/PCLK Measurement				
RESERVED	A8		R	
PX_AS_ALINE[3:0]	A9	02	W	The threshold of number of pixels that will be treated as an active line. The LSB 4-bit will be used. The default number is at least 2 pixels will be treated as an active line.
-	AB, AA	00,10	R	reserved
An overflow had been detected on the M-th line (AML_OVERFLOW) (0: B channel, 1: G channel, 2: R channel, other bits are reserved)	AC	00	R	An overflow (a value larger or equal to ARGB_MAX[7:0] at Reg 0x80) of color value in R, G, or B has been detected on Mth line
ICLK/PCLK MEASURE PARAMETER				
ICLK MEASURE (XPULSE_BY_ICLK[15:0])	A1,A0	00,00	R	The number the XTAL pulse (programmable at the length of 1K, 2K, 3K,and 4K) counted by the ICLK.
PCLK MEASURE (XPULSE_BY_PCLK[15:0])	A3,A2	00,00	R	The number the XTAL pulse (programmable at the length of 1K, 2K, 3K,and 4K) counted by the PCLK.
-	A5,A4	00,00	R	reserved
Brightness, Contrast, Gamma, CLUT, and ALPHA BLENDING				
RCONTRAST[7:0]	AE	00	W	256 level contrast control for R
RBRIGHTNESS[7:0]	AF	00	W	256 level brightness control for R
GCONTRAST[7:0]	B0	00	W	256 level contrast control for G
GBRIGHTNESS[7:0]	B1	00	W	256 level brightness control for G
GAMMA table R write Address (GRWADDR[7:0])	B2	00	W	Each gamma-correction table is a 256x8 LUT (look-up table) which can be updated by writing to these ports. By programming this port 256 times the 256x8 LUT is updated completely.
GAMMA table G write Address (GGWADDR[7:0])	B3	00	W	Same as R channel.
GAMMA table B write Address (GBWADDR[7:0]) (The table write address will be auto increased upon each writing)	B4	00	W	Same as R channel.

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	Description
CLUT write address (CLUTWADDR[7:0])	B5	00	W	The 16x16 Color LUT can be written by host from this port. First the lower byte data are sent to an entity, then followed by the higher byte data, color index 0 is filled followed by color index 1 until color index 15, the final one. The 16-bit output of this color LUT will be interpreted as the RGB565 format, i.e. the MSB 5 bits are for R, the middle 6 bits for G, and the LSB 5 bits for B.
Starting address of OSD Look Up Table OSD_LUT_ADDR[3:0]	F3	00	w	The starting address for OSD Look Up Table to be updated
CLUT alpha blending (CLUT_ALPHA[4:0])	B6	00	W	The MSB of CLUT_ALPHA is used indirectly for the interpretation of the I signal of OSD, while CLUT_ALPHA[3:0] is used to select the blending factor between the output of the CLUT and the output of the dithered video. CLUT_ALPHA[4]= 0: The content of CLUT is RGB565. 1: The content of CLUT is RGB555. And the LSB of G will be interpreted as LSB of G of CLUT read out =0: means alpha blending off. =1: means alpha blending on. If alpha blending is on and any one of the internal/external OSD/background color is activated, the final video of panel out will be equal to Video*CLUT_ALPHA[3:0]/16+CLUT*(1-CLUT_ALPHA[3:0]/16). For the case that CLUT_ALPHA[3:0]=0, the final video of panel is directly from the output of CLUT. And for CLUT_ALPHA[3:0]=6, the final video is Video*6/16+CLUT*12/16.
BCONTRAST[7:0]	B7	00	W	256 level contrast control for B The input signal is multiplied by a value ((CONTRAST+128) mod 256)/128 where CONTRAST is in the range of [255,0].
BBRIGHTNESS[7:0]	B8	00	W	256 level brightness control for B 7f ->127,..., 01 -> 1, 00 -> 0, ff -> -1,..., 80 -> -128 i.e. The input data is added by a 2,s complement value
GCSTART[7:0]	B9	00		Define Gamma Table Starting Address
PPLL program parameter				
Registers 0xBA,0xBB,OxBE, please refer to the Section of Clock System for PPLL setting.				
IN/OUT HS/VS PARAMETER				

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	**Description**
Panel HSync total (PH_TOTAL[10:0])	C5,C4	00,00	W	The LSB 11-bit defines the total value of LCD panel HS. The value is counted by PCLK. Using the results of ICLK/PCLK measurement (see Reg. A0-A3), this parameter can be calculated via IH_TOTAL * ICLK_Period = Vsf * PH_TOTAL * PCLK_Period.
Panel HSync delay (PH_DELAY[10:0])	C7,C6	00,00	W	The LSB 11-bit defines the delay of display output HS from IVS. The value is counted by PCLK.
Input SFDL delay (IV_SFDL[5:0])	C9	01	W	The register defines the value of line delay of an internal signal SFDL. The value is counted from the falling edge of input VS by IHS. This delayed signal is used to synchronize the panel VS.
Registers CA-CF are described in OSD Parameters				
Registers D0-DF are described in Hardware Mode Detection Parameters				
PEAKING Control				
PEAK_CTRL1	E0	1A	W	PEAK_CTRL1[7]: 0: disable peaking function 1: enable peaking function PEAK_CTRL1[6]: 0: normal hactive output 1: delay hactive 1 clock than normal PEAK_CTRL1[5:4]: Gain of BPF1 00: divided by four 01: divided by two others: divided by one PEAK_CTRL1[3:2]: Gain of BPF2 00: divided by four 01: divided by two others: divided by one PEAK_CTRL1[1:0]: Gain of HPF 00: divided by four 01: divided by two others: divided by one

REGISTER FUNCTION	ADDR(HEX) MSB:ODD LSB:EVEN	RESET VALUE (hex)	R/W	**Description**
PEAK_CTRL2	E1	44	W	{PEAK_CTRL2[7], PEAK_CTRL2[3], PEAK_CTRL3[7]} : 000: all frame are processed by peaking 001: not processed at frame edge within 4 pixels 010: not processed at frame edge within 5 pixels 011: not processed at frame edge within 6 pixels 100: not processed at frame edge within 7 pixels 101: not processed at frame edge within 8 pixels 110: not processed at frame edge within 9 pixels 111: not processed at frame edge within 10 pixels PEAK_CTRL2[6:4]/PEAK_CTRL[2:0]: Gain of filter1 and filter2 000: zero 001: filter_out / 4 010: filter_out / 2 011: filter_out *3 / 4 100: filter_out 101: filter_out *5 /4 110: filter_out *6 /4 111: filter_out *2
PEAK_CTRL3	E2	44	W	PEAK_CTRL3[7]: described in E1h PEAK_CTRL3[6:4]: Gain of filter3 000: zero 001: filter_out / 4 010: filter_out / 2 011: filter_out *3 / 4 100: filter_out 101: filter_out *5 /4 110: filter_out *6 /4 111: filter_out *2 PEAK_CTRL3[3:0]: Coring value 0000: zero 1000: 64 0001: 8 1001: 72 0010: 16 1010: 80 0011: 24 1011: 88 0100: 32 1100: 96 0101: 40 1101: 104 0110: 48 1110: 112 0111: 56 1111: 120
PEAK_CTRL4	E3	A0	W	PEAK_CTRL4[7]: reg_dec_en 0: without mapping 1: with mapping PEAK_CTRL4[6:0]: Curve1 of Mapping range1
PEAK_CTRL5	E4	40	W	PEAK_CTRL5[7]: reserved PEAK_CTRL5[6:0]: Curve2 of Mapping range1
PEAK_CTRL6	E5	60	W	PEAK_CTRL6[7]: reserved PEAK_CTRL6[6:0]: Curve3 of Mapping range1

The register map of Hardware Mode Detector:

Name: (bit)	7	6	5	4	3	2	1	0
HWDCNT(D0H)	Enhwd	SelDE	Hwd_inten	Vint_ren	Vint_fen	Vcnt-Sel	HVsep1	HVsep0
83H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
IntSrc(D1H)	-	-	Vint_R	Vint_F	VfChanged	Vpolcha	HfChanged	Hpolcha
00H	-	-	R	R	R	R	R	R
SyncStatus(D2H)	-	Falt	FwHalf	Odd_Even	Vpresence	Hpresence	Vpolarity	Hpolarity
00H	-	R	R	R	R	R	R	R
HperHigh(D3H)	Hper15	Hper14	Hper13	Hper12	Hper11	Hper10	Hper9	Hper8
00H	R	R	R	R	R	R	R	R
HperLow(D4H)	Hper7	Hper6	Hper5	Hper4	Hper3	Hper2	Hper1	Hper0
00H	R	R	R	R	R	R	R	R
VperHigh(D5H)	Vper15	Vper14	Vper13	Vper12	Vper11	Vper10	Vper9	Vper8
00H	R	R	R	R	R	R	R	R
VperLow(D6H)	Vper7	Vper6	Vper5	Vper4	Vper3	Vper2	Vper1	Vper0
00H	R	R	R	R	R	R	R	R
PulCnt(D7H)	EnVout	EnHout	VoutMode1	VoutMode0	HoutMode1	HoutMode0	Htolerance1	Htolerance0
C0H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HVPwth(D8H)	VPW4	VPW3	VPW2	VPW1	VPW0	HPW2	HPW1	HPW0
43H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PoutPolPos(D9H)	Vshift5	Vshift4	Vshift3	Vshift2	Vshift1	Vshift0	VoutPol	HoutPol
00H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HMDMisc(DAH)	-	MacVis_ON	VFrmCnt1	VFrmCnt0	VCDelay1	VCDelay0	FIDPol	EOEnable
60H	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HfpHigh(DBH)	Hfp9	Hfp8	Hfp7	Hfp6	Hfp5	Hfp4	Hfp3	Hfp2
4AH	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
HVfpLow(DCH)	Vtolerance1	Vtolerance0	Vfp3	Vfp2	Vfp1	Vfp0	Hfp1	Hfp0
18H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VfpHigh(DDH)	Vfp11	Vfp10	Vfp9	Vfp8	Vfp7	Vfp6	Vfp5	Vfp4
32H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VsepProgLo(DEH)	Vsep_spt7	Vsep_spt6	Vsep_spt5	Vsep_spt4	Vsep_spt3	Vsep_spt2	Vsep_spt1	Vsep_spt0
32H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VsepProgHi(DFH)	Vsync_dly3	Vsync_dly2	Vsync_dly1	Vsync_dly0	Vsep_spt11	Vsep_spt10	Vsep_spt9	Vsep_spt8
32H	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

IA-Hardware Mode Detector Control Register, 0xD0 ~ 0xDF			
HWDCNT (Hardware Mode Detector Control Register, 0xD0)			Default
7	Enhwd	Enable Hardware mode detectorEnable 0: Disabled; (clock is sleeping also to save power) 1: Enabled	1
6	SelDE	Selection between DE and Csync input (DE and Csync are mutually exclusive) (if SelDE = 1, HVsep is automatically set as 00) 0: Csync is selected 1: DE is selected	0
5	Hwd_inten	Enable interrupt from one of Sync signal changes: H/V frequency or Polarity change 0: Disabled 1: Enabled	0
4	Vint_ren	Enable interrupt at Vsync leading edge 0: Disabled 1: Enabled	0

3	Vint_fen	Enable interrupt at Vsync trailing edge 0: Disabled 1: Enabled	0
2	Vcnt_Sel	Select Vperiod count by time or by line number 0: By time; i.e. Vclk (Hclk/11) 1: By H line	0
1~0	HVsep1-HVsep0	Multiplexer to select Vsync source: 00: Csync/DE + VsyncSep 01: Hsync + VsyncSep 10: Hsync + VsyncSep XOR Vsync 11: Hsync + Vsync (if SelDE = 1, 00 is chosen, i.e. DE is treated as one kind of Csync)	11
IntSrc (Interrupt Source, 0xD1)			Default
5	Vint_R	Interrupt is caused by Vsync leading edge 0: Vsync leading edge not happened 1: Vsync leading edge happened	0
4	Vint_F	Interrupt is caused by Vsync trailing edge 0: Vsync trailing edge not happened 1: Vsync trailing edge happened	0
3	VfChanged	Interrupt is caused by V frequency change 0: V frequency not changed 1: V frequency changed	0
2	VpolCha	Interrupt is caused by V polarity change 0: V polarity not changed 1: V polarity changed	0
1	HfChanged	Interrupt is caused by H frequency change 0: H frequency not changed 1: H frequency changed	0
0	HpolCha	Interrupt is caused by H polarity change 0: H polarity not changed 1: H polarity changed	0
SyncStatus (H/V sync signals status, 0xD2)			Default
6	Falt	Indicate whether Field contains alternating n / n+1 lines 0: Not this format 1: Yes	0
5	FwHalf	Indicate whether Field contains n+1/2 lines (half line) 0: Not this format 1: Yes	0
4	Odd_Even	Indicate current field is Odd field or Even field 0: odd field/1st field; with earlier H sync 1: even field/2nd field; with lagged H sync	0
3	Vpresence	The presence status of Vsync 0: Not present 1: Present	0
2	Hpresence	The presence status of Hsync/Csync 0: Not present 1: Present	0
1	Vpolarity	The polarity of Vsync 0: Positive polarity (Pulse width smaller than 1/4 of Vperiod) 1: Negative polarity (Pulse width larger than 3/4 of Vperiod)	0
0	Hpolarity	The polarity of Hsync 0: Positive polarity (Pulse width smaller than 1/4 of Hperiod) 1: Negative polarity (Pulse width larger than 3/4 of Hperiod)	0
Hperiod (0xD3, 0xD4)			Default
15~0	Hperiod	64 Hsync line periods	Hx0000
Vperiod (0xD5, 0xD6)			Default

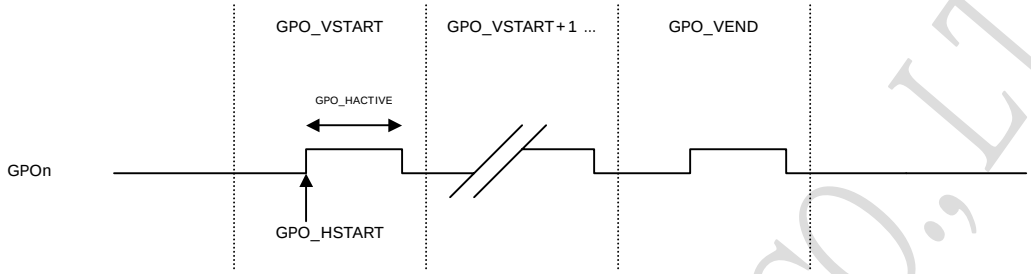
15~0	Vperiod	Vsync period (the period of one frame)	Hx2000
PulCnt (H/V output pulse control register, 0xD7)			Default
7	EnVout	Enable VsyncOut pulse 0: Disabled; VsyncOut is kept low 1: Enabled	1
6	EnHout	Enable HsyncOut pulse 0: Disabled; HsyncOut is kept low 1: Enabled	1
5~4	VoutMode1 - VoutMode0	**00 (FreeRun)**: The period of VsyncOut is programmed by 12-bit counter, Vfper. **01 (Loopth_st)**: The leading edge of VsyncOut will be roughly close to the incoming Vsync, however, snapped to the leading edge of incoming HsyncOut. **10 (R_aligned)**: The leading edge of VsyncOut will be shifted ahead or after the leading edge of Vsync based on the programmed value, however, snapped to the leading edge of incoming HsyncOut. **11 (Loopth)**: Completely copy the shape of the incoming Vsync	00
3~2	HoutMode1 - HoutMode0	**00 (FreeRun)**: The period of HsyncOut is programmed by 10-bit counter, Hfper. The pulse width is programmed by 3-bit register, HPW. **01 (Loopth_st)**: The HsyncOut will be snapped to the rising/falling edge of incoming Hsync; if the pulse of incoming Hsync is missing, an artificial pulse will be inserted with pulse width defined by HPW. **10 (R_aligned)**: The leading edge of the output Hsync is aligned with the incoming Hsync. However, the pulse width is defined by HPW. **11 (Loopth)**: Completely copy the shape of the incoming Hsync	00
1~0	Htolerance1 - Htolerance0	The definition of H frequency/count deviation is programmable: 00: +/- 4 counts 01: +/- 8 counts 10: +/- 16 counts	00
HVPwth (The Pulse Width of H/V sync output, 0xD8)			Default
7~3	Vpw4 -Vpw0	There are 16 programmable values to set the pulse width of VsyncOut 2 * (Vpw + 1) => 2, 4, 6, ... 30, 32 H lines.	01000
2~0	Hpw2 - Hpw0	The pulse width of Hsync Output: 000: 4(0.28us) 001: 8(0.59us) 010: 16(1.12us) 011: 20(1.40us) 100: 24(1.68us) 101: 28(1.96us) 110: 32(2.23us) 111: 36(2.51us)	011
PoutPolPos (The polarity of H/V sync output and the position of VsyncOut, 0xD9)			Default
7~2	Vshift5 - Vshift0	Vshift(5) = 1 (Leading edge of VsyncOut ahead the incoming Vsync): Vshift4 - Vshift0= 00000 ~ 11111 : Ahead 1 ~ 32 H lines Vshift(5) = 0 (Leading edge of VsyncOut lag the incoming Vsync): Vshift4 - Vshift0= 00000: Kept at the same position as incoming Vsync 00001 ~ 11111 : After 1 ~ 31 H lines	000000
1	VoutPol	The polarity of VsyncOut 0: Positive polarity (Pulse width smaller than 1/4 of VsyncOut) 1: Negative polarity (Pulse width larger than 3/4 of VsyncOut)	0
0	HoutPol	The polarity of HsyncOut 0: Positive polarity (Pulse width smaller than 1/4 of HsyncOut) 1: Negative polarity (Pulse width larger than 3/4 of HsyncOut)	0
HMDMisc (HMD misc register, 0xDA)			Default
6	MacVis_ON	Macro vision on 0: turn off 1: turn on	0
5~4	VFrmCnt	Vertical frame counter set (iteration check value if have any change)	11
3~2	VCDelay	Delay counter set of VsyncOut (Delay output is VCDelayout)	00

1	FID_POL	Field Polarity 0: (default) keep the original field polarity 1: inverse the current field polarity	0
0	EOEnable	The selection of even/odd flag. 0: (default) even/odd flag will be disabled. 1: even/odd flag will be readable and used	0
HfpHigh (0xDB)			Default
7~0	Hfperiod9 - Hfperiod2	The high nibble of H free run period (9 - 0)	01001010
HVfpLow (0xDC)			Default
7~6	Vtolerance1 - Vtolerance0	The definition of V frequency/count deviation is programmable: 00: +/- 4 counts 01: +/- 8 counts 10: +/- 16 counts 11: +/- 88 counts	00
5~2	Vfperiod3 - Vfperiod0	The low nibble of V free run period (11 - 0)	0110
1~0	Hfperiod1 - Hfperiod0	The low nibble of H free run period (9 - 0)	00
VfpHigh (0xDD)			Default
7~0	Vfperiod11 - Vfperiod4	The high nibble of V free run period (11 - 0)	00110010
VSepProgLo (0xDE)			Default
7~0	Vsep_spt_L	The low nibble of Vsync separation position (7 - 0) from Csync	01100000
VSepProgHi (0xDF)			Default
7~4	Vsync_dly	Process Vsync with clock delay	0000
3~0	Vsep_spt_M	The high nibble of Vsync separation position (11 - 8) from Csync	0000

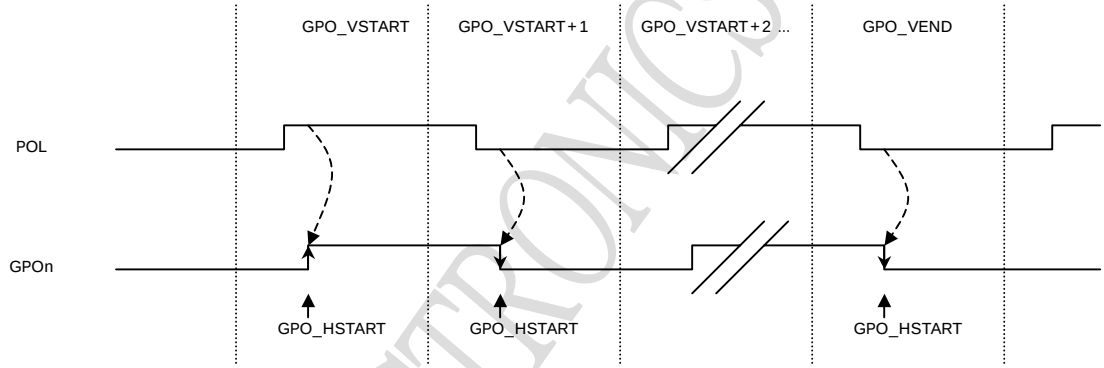
5.7 TCON

5.7.1 The TCON example timing for GPO[0,1,2]

*for the mode of no logical operation :

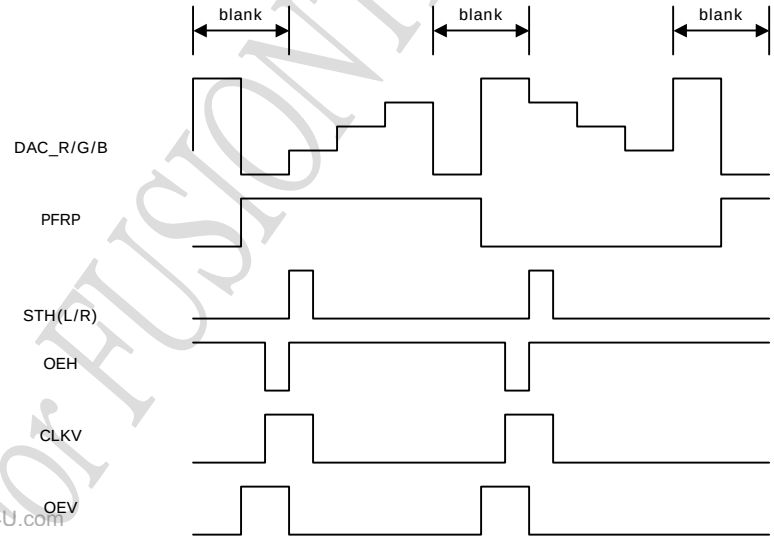


*for the mode with latched POL's value :



5.7.2 TCON timing

- The TCON horizontal timing relationship of data, starting and other related signals



5.7.2.1 Register definition for TCON

The 2-wire serial bus slave address of this chip is 1111011b or 1111111b. The table is listed:

	LOW NIBBLE OF SUBADDRESS															
	Addr (hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
HIGH NIBBLE	0	Reserved		TC_ MAJ OR1	TC_ MAJ OR2		TC_ MAJ OR4	TC_ MAJ OR5									
	1	GPO0 Programming Registers									Reserved	LP Programming Registers					
	2	GPO1 Programming Registers									Reserved	CLKV Programming Registers					
	3	STH Programming				POL Programming				CLKH Programming Registers							
	4	STV Programming and CLKV_VSTART					Ahead_DE		STH width	Reserved							
	5	GPO2 Programming Registers								Reserved							
	6	Reserved															
	7~F	Reserved															

TC_MAJOR1 (TCON MAJOR control register 1, 02H)			Default
7	LP_PHASE	The phase selection of the edges of LP pulse signal with respect to the internal pixel clock. 0: (default) Aligned with the rising edge of CLKH. 1: Aligned with the falling edge of CLKH. NOTE: Internal pixel clock, CLKH, will send to Pin 63 which can be inverted with programmable delay. Please refer to PHCLK_INV and PHCLK_OP in Register OUTCTR0 or 03hex.	0
6	TI_MODE	STV start position (This bit also defines the CLKV start position) 0: (default) Normal start. 1: Late start.	0
5	POL_MODE	The toggle duration of POL (polarity output signal) pin 0: (default) toggle per H line. 1: toggle per 2H lines	0
4	CLKH_OFF	The CLKH signal can be turned off during the non-active display period. 0: (default) CLKH output signal is always available. 1: CLKH signal will be turned off during the non-active display period. The duration is defined by the TC_CLKH_VSTART, TC_CLKH_VACTIVE, TC_CLKH_HSTART, and TC_CLKH_HACTIVE registers.	0

TC_MAJOR1 (TCON MAJOR control register 1, 02H)			Default
3	RGB_BUS_SKEW	Data bus group delay for EMI reduction. 0: (default) The data bus of RGB signals are distributed as 0.0/1.0/2.0ns. 1: The data bus of RGB signals are distributed as 0.0/2.0/4.0ns.	0
2	DIR_SCMD	The driver IC R/L direction control. 0: Start pulse for gate driver(Active L to R), STHL output , STHR High impedance. 1: Start pulse for gate driver(Active R to L), STHL High impedance , STHR output.	0
1	INVERSE_HMS	The inversion of HMSO and HMSE signals.	0

		0: (default) No inversion. 1: The HMSO and HMSE signals will be inversed	
0	ENABLE_HMS	The operation of HMSO and HMSE signals. 0: The HMSO and HMSE signals will be kept at high or low (In a word, HMSO=HMSE=INVERSE_HMS). 1: (default) The operation of HMSO and HMSE is enabled.(Note: HMSO and HMSE will be calculated separately)	1

TC_MAJOR2 (TCON MAJOR control register 2, 03H)			Default
7	INVERSE_CLKV	The inversion of CLKV clock. 0: (default) No inversion. 1: Inversed CLKV.	0
6	TCON_8BIT	TCON can be configured for 8-bit or 6-bit (for each RGB) TFT-LCD panel 0: (default) TCON is configured for 8-bit (for each RGB) panel. 1: TCON is configured for 6-bit (for each RGB) panel	0
5	SINGLE_HMS	This register defines the operation of HMS is based on two single port (24/18 bits) or one dual port (48/36 bits) 0 : EVEN/ODD is calculated separately 1 : EVEN/ODD is calculated together	0
1	PHSI_POL	This bit control the phs in 0: (default) PHS IN 1: invert PHS IN	0
0	TCON_EN	This bit control the TCON function. 0: disable TCON 1: enable TCON	0
TC_MAJOR4 (TCON MAJOR control register4, 05H)			Default
7	DIR_SCMD2	The gate IC U/D direction control. 0: Start pulse for gate driver(Active U to D), STVU output , STVD High impedance. 1: Start pulse for gate driver(Active D to U), STVU High impedance , STVD output.	0
6	PHSO_POL	Panel H sync output POL 0: (default) PHS 1: invert PHS	0
5	PVSO_POL	Panel H sync output POL 0: (default) PVS 1: invert PVS	0
4	LP_POL	Latch pulse POL 0: (default) LP 1: invert LP	0
3	FRN_FID_POL	FRN Field ID POL 0: Field = 0 1: Field = 1	0
2	EXT_FID_POL	EXT Field ID POL 0: (default) Fid in 1: invert Fid in	0
1	FID_SEL	Field ID select 0: free-run. 1: external	0
0	PIXC_FHSREDGE	pixel count from HS rising edge 0: falling 1: rising	0
TC_MAJOR5 (TCON MAJOR control register5, 06H)			Default
7	LKILL_EN	Line drop enable	0

		0: (default) disable 1: enable	
6,5	LK_MODE	Line drop mode 00: (default) –1 line number 01: same line number 10: +1 line number 11: reserved	0
2	R_B_SWAP	R/B channel swap 0: (default) original RGB channel 1: swap R/B channel	0
1	FRN_GRADIENT	Free run gradient pattern select 0: Normal (no free run gradient pattern 1: free run gradient pattern enable	0
0	POL_INV_RGB	RGB inverted by POL 0: (default) disable 1: enable (invert RGB)	0

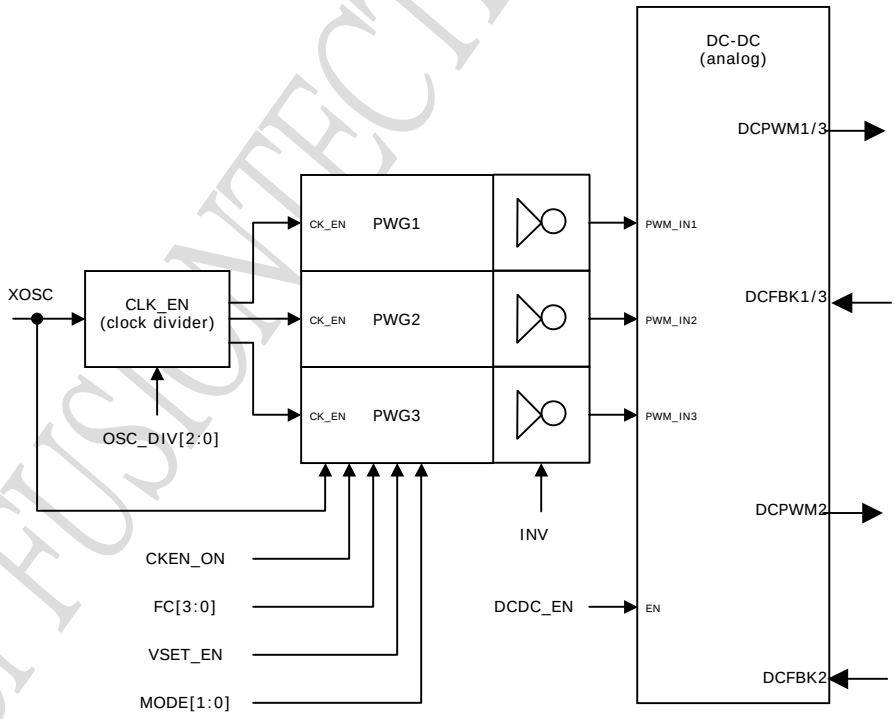
REGISTER FUNCTION	ADDR (HEX) MSB:ODD LSB:EVEN	RESET VALUE	R/W	Description
Timing Control Parameter		hex		
Reserved	00-01	00	W	
Major feature Control Register TC_MAJOR1[7:0]	02	00	W	Major programming features of the timing controller 1
Major feature Control Register TC_MAJOR2[7:0]	03	00	W	Major programming features of the timing controller 2
Major feature Control Register TC_MAJOR3[7:0]	04	00	W	Major programming features of the timing controller 3
Major feature Control Register TC_MAJOR4[7:0]	05	00	W	Major programming features of the timing controller 4
Major feature Control Register TC_MAJOR5[7:0]	06	00	W	Major programming features of the timing controller 5
Reserved	07-0C	00	W	
LK_COUNT	0D	00	W	Line drop counter
LK_VSTART	0F,0E	00,00	W	Line drop start
GPO0 Horizontal Start TC_GPO0_HSTART[10:0]	11, 10	00,94	W	Define the GPO0 horizontal start counter value.
GPO0 Horizontal Active TC_GPO0_HACTIVE[10:0]	13, 12	02,94	W	Define the GPO0 horizontal active duration counter value.
GPO0 Vertical Start TC_GPO0_VSTART[10:0]	15, 14	00,01	W	Define the GPO0 vertical start counter value.
GPO0 Vertical End TC_GPO0_VEND[10:0]	17, 16	03,00	W	Define the GPO0 vertical end duration counter value.
GPO0 Control Register TC_GPO0_CONTROL[7:0]	18	00	W	Define the GPO0 control value. TC_GPO0_CONTROL[1:0] defines = 00 : no logical operation = 01 : inverted = 10 : latch POL's value = 11 : latch POL's value, and then inverted
Reserved	19	00	W	
LP Horizontal Start TC_LP_HSTART[10:0]	1B, 1A	01,28	W	Define the LP signal horizontal start counter value.
LP Horizontal Active TC_LP_HACTIVE[10:0]	1D, 1C	00,1f	W	Define the LP signal horizontal active duration counter value.

REGISTER FUNCTION	ADDR (HEX) MSB:ODD LSB:EVEN	RESET VALUE	R/W	Description
LP Vertical End TC_LP_VEND[10:0]	1F, 1E	03,00	W	Define the LP signal vertical end counter value.
GPO1 Horizontal Start TC_GPO1_HSTART[10:0]	21, 20	00,94	W	Define the GPO1 horizontal start counter value.
GPO1 Horizontal Active TC_GPO1_HACTIVE[10:0]	23, 22	02,94	W	Define the GPO1 horizontal active duration counter value.
GPO1 Vertical Start TC_GPO1_VSTART[10:0]	25, 24	00,01	W	Define the GPO1 vertical start counter value
GPO1 Vertical End TC_GPO1_VEND[10:0]	27, 26	03,00	W	Define the GPO1 vertical end duration counter value.
GPO1 Control Register TC_GPO1_CONTROL[7:0]	28	00	W	Define the GPO1 control value TC_GPO1_CONTROL[3:0] = 0000 : no logical operation = 0001 : inverted = 0010 : latched POL's value = 0011 : latched POL's value, and then inverted
Reserved	29	00	W	
CLKV Horizontal Start TC_CLKV_HSTART[10:0]	2B, 2A	02,00	W	Define the CLKV signal horizontal start counter value.
CLKV Horizontal Active TC_CLKV_HACTIVE[10:0]	2D, 2C	01,00	W	Define the CLKV signal horizontal active duration counter value.
CLKV Vertical End TC_CLKV_VEND[10:0]	2F, 2E	03,01	W	Define the CLKV signal vertical end counter value. NOTE: The vertical start of the CLKV signal is defined by the position of STV pulse (so called Ti_mode). Also the V start value of CLKV is defined at TC_STVCLKV_VSTRAT[3:0].
STH Horizontal Start TC_STH_HSTART[10:0]	31, 30	00,93	W	Define the STH signal horizontal start counter value.
STH Vertical End TC_STH_VEND[10:0]	33, 32	03,00	W	Define the STH signal vertical end counter value
POL Horizontal Start TC_POL_HSTART[10:0]	35, 34	02,00	W	Define the POL signal horizontal start counter value. NOTE: The POL signal can be toggled every H line or every 2H lines.
POL Vertical End TC_POL_VEND[10:0]	37, 36	03,01	W	Define the POL signal vertical end counter value.
CLKH Horizontal Start TC_CLKH_HSTART[10:0]	39, 38	00,94	W	Define the CLKH horizontal start counter value. NOTE: To save power consumption, CLKH can be deactivated during the non-active display period. r.
CLKH Horizontal End TC_CLKH_HEND[10:0]	3B, 3A	02,94	W	Define the CLKH horizontal end duration counter value.
CLKH Vertical Start TC_CLKH_VSTART[10:0]	3D, 3C	00,01	W	Define the CLKH vertical start counter value.
CLKH Vertical End TC_CLKH_VEND[10:0]	3F, 3E	03,00	W	Define the CLKH vertical end duration counter value.
STV Horizontal Start TC_STV_HSTART[10:0]	41, 40	00,94	W	Define the STV signal horizontal start counter value.
STV Horizontal Active TC_STV_HACTIVE[11:0]	43, 42	00,14	W	Define the STV signal horizontal active counter value
STV and CLKV Vertical Start TC_STVCLKV_VSTRAT[7:0]	44	11	W	Define the vertical start counter value of STV and CLKV. TC_STVCLKV_VSTRAT[3:0] is for the V start value of CLKV and TC_STVCLKV_VSTRAT[7:4] is for the V start value of STV

REGISTER FUNCTION	ADDR (HEX) MSB:ODD LSB:EVEN	RESET VALUE	R/W	Description
TC_LNUM_AHEAD_DE[10:0]	46,45	00,01	W	Define the number of lines that is ahead DENA; the Vertical value is calculated from this point
TC_STH_WIDTH[7:0]	47	00	W	Define the width of STH pulse
Reserved	48-4F	00	W	
GPO2 Horizontal Start TC_GPO2_HSTART[10:0]	51, 50	00,94	W	Define the GPO2 horizontal start counter value.
GPO2 Horizontal Active TC_GPO2_HACTIVE[10:0]	53, 52	02,94	W	Define the GPO2 horizontal active duration counter value
GPO2 Vertical Start TC_GPO2_VSTART[10:0]	55, 54	00,01	W	Define the GPO2 vertical start counter value.
GPO2 Vertical End TC_GPO2_VEND[10:0]	57, 56	03,00	W	Define the GPO2 vertical end duration counter value
GPO2 Control Register TC_GPO2_CONTROL[7:0]	58	00	W	Define the GPO2 control value. TC_GPO2_CONTROL[1:0] = 0000 : no logical operation = 0001 : inverted = 0010 : latch POL's value = 0011 : latch POL's value, and then inverted
Reserved	59-FF	00	W	

5.8 DC-DC and PWG

3 pairs of PWG and Feedback signals are provided to control the DC-DC converter for high voltage generation. The basic structure is:



PWG_OUTOSC1 (PWG clock input control register 1, A6H)			Default
5:4	MODE[1:0]	The DC-DC force the PWG1's pulse width increment or decrement (recommended to use 11b)	00
3	DCDC_DIS	1: DCDC disable (low power consumption) 0: enable DCDC	1
2:0	PWG1_OSC_DIV	PWG1 clock divide ratio	011

PWG_OUTOSC2 (PWG clock input control register 2, A7H)			Default
5:4	MODE[1:0]	The DC-DC force the PWG2's pulse width increment or decrement (recommended to use 11b)	01
3	-	Reserved	0
2:0	PWG2_OSC_DIV	PWG2 clock divide ratio	000

PWG_OUTOSC3 (PWG clock input control register 3, A8H)			Default
5:4	MODE[1:0]	The DC-DC force the PWG3's pulse width increment or decrement (recommended to use 11b)	01
3	-	Reserved	0
2:0	PWG3_OSC_DIV	PWG3 clock divide ratio	001

PWG_OUTCTR1 (PWG pulse output control register 1, FAH)			Default
7:4	FC[3:0]	16 PWG1 pulse modulation parameters	1000
3	PWG_RSTN	0: PWG1 reset 1: PWG1 no reset	0
2	CKEN_ON	0: PWG1's XOSC is disabled 1: PWG1's XOSC will be controlled by CK_EN	1
1	VSET_EN	0: PWG1's VSET from DC-DC is disabled 1: PWG1's VSET from DC-DC is enabled	0
0	INV	0: PWG1's output no invert 1: PWG1's output invert	0
PWG_OUTCTR2 (PWG pulse output control register 2, FBH)			Default
7:4	FC[3:0]	16 PWG2 pulse modulation parameters	1000
3	PWG_RSTN	0: PWG2 reset 1: PWG2 no reset	0
2	CKEN_ON	0: PWG2's XOSC is disabled 1: PWG2's XOSC will be controlled by CK_EN	1
1	VSET_EN	0: PWG2's VSET from DC-DC is disabled 1: PWG2's VSET from DC-DC is enabled	0
0	INV	0: PWG2's output no invert 1: PWG2's output invert	1

PWG_OUTCTR3 (PWG pulse output control register 3, FCH)			Default
7:4	FC[3:0]	16 PWG3 pulse modulation parameters	1001
3	PWG_RSTN	0: PWG3 reset 1: PWG3 no reset	0
2	CKEN_ON	0: PWG3's XOSC is disabled 1: PWG3's XOSC will be controlled by CK_EN	1
1	VSET_EN	0: PWG3's VSET from DC-DC is disabled 1: PWG3's VSET from DC-DC is enabled	0
0	INV	0: PWG3's output no invert 1: PWG3's output invert	0

6 Electrical Specifications

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
V_{DD3}	IO Power Supply	-0.3 to 3.6	V
V_{DD2}	Core Power Supply	-0.25 to 2.75	V
V_{IN}	Input Voltage	-0.3 to V_{CC3}+0.3	V
V_{OUT}	Output Voltage	-0.3 to V_{CC3}+0.3	V
T_{STG}	Storage Temperature	-40 to 125	°C

*Stress beyond the absolute maximum ratings may cause permanent damage to the devices. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under DC Characteristics is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Recommended Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD3}	IO DC Power Supply	3.0	3.3	3.6	V
V_{DD2}	Core DC Power Supply	2.25	2.5	2.75	V
V_{IN}	DC Input Voltage	0		V_{CC3}	V
T_{OC}	Operating Classic Temperature	0	25	70	°C

6.3 DC Characteristics

V_{DD3}=3.0~3.6V; V_{DD2}=2.25~2.75V, V_{SS}=0V; T_{OC}=0~+70°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{RUN}	Supply current in run state	V_{CC3}=3.3V, V_{CC2}=2.5V,		t.b.f.		mA
I_{PD}	Power saving supply current	Power down mode		t.b.f.		µA
V_{IH}	Low-level input voltage		0.7* V_{CC}			V
V_{IL}	High-level input voltage				0.3* V_{CC3}	V
I_{IL}	Input leakage current		-1.0		1.0	µA
V_{OH}	Low-level output voltage		2.4			V
V_{OL}	High-level output voltage				0.4	V

6.4 ADC's DC Characteristics

ITEM	MIN.	TYP.	MAX.	Unit
Supply voltage (VDDA/VDD)	3.0	3.3	3.6	V
Resolution		10		bit
DNL			0.5	LSB
INL			1	LSB
Offset error			0.5	LSB
Input range	0		1(RGB) 1.3(Video)	V
Clock			20	MHz

6.5 DAC's DC Characteristics

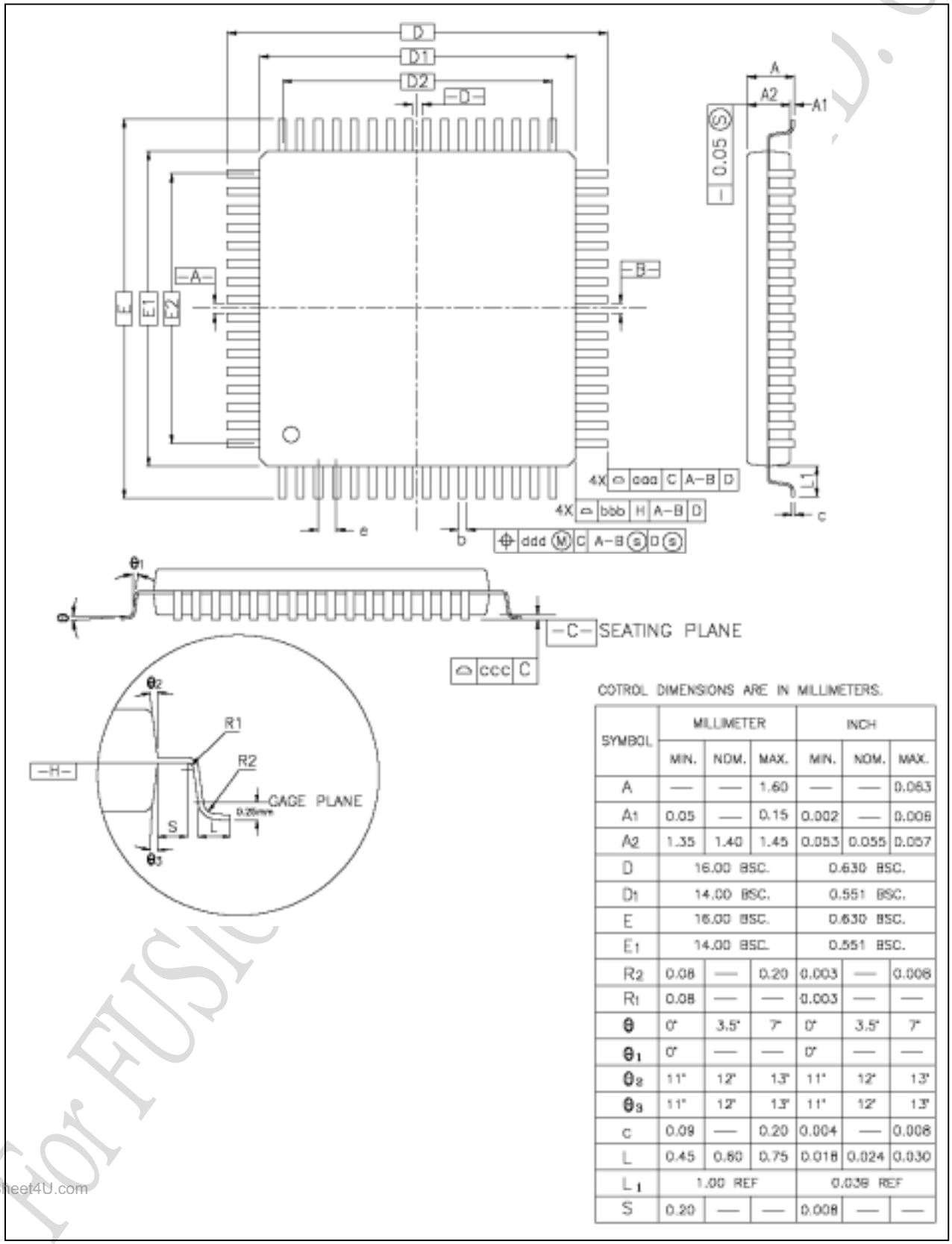
VCCA33_DAC1=VCCA33_DAC2=VCCA33_DAC3=3.3V; RL=37.5ohm, CL=10Pf; Temp=25oC

Parameter	Symbol	Min	Typ	Max	Unit
Operating range	VCCA33_DAC1 VCCA33_DAC2 VCCA33_DAC3	3.0	3.3	3.6	V
Max per channel output current			18.6		mA

Max output voltage			0.7		V
Integral non-linearity error	INL	-1 LSB	0.5 LSB	+1 LSB	LSB
Differential non-linearity error	DNL	-1 LSB	0.5 LSB	+1 LSB	LSB

7 Package Outline

LQFP128 (14mm x 14mm x 1.4mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—