DATA SHEET

TDA933xH series
I²C-bus controlled TV display processors

Preliminary specification
Supersedes data of 1998 Oct 22
File under Integrated Circuits, IC02

2000 May 08

Philips
Semiconductors

PHILIPS

I²C-bus controlled TV display processors TDA933xH series

FEATURES

Available in all ICs:

- Can be used in both single scan (50 or 60 Hz) and double scan (100 or 120 Hz) applications
- YUV input and linear RGB input with fast blanking
- Separate OSD/text input with fast blanking or blending
- Black stretching of non-standard luminance signals
- Switchable matrix for the colour difference signals
- RGB control circuit with Continuous Cathode Calibration (CCC), plus white point and black level offset adjustment
- Blue stretch circuit which offsets colours near white towards blue
- Internal clock generation for the deflection processing, which is synchronized by a 12 MHz ceramic resonator oscillator
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Slow start and slow stop of the horizontal drive pulses
- Low-power start-up option for the horizontal drive circuit
- Vertical count-down circuit
- Vertical driver optimized for DC-coupled vertical output stages
- Vertical and horizontal geometry processing
- Horizontal and vertical zoom possibility and vertical scroll function for application with 16 : 9 picture tubes
- Horizontal parallelogram and bow correction
- I²C-bus control of various functions
- Low dissipation.

GENERAL DESCRIPTION

The TDA933xH series are display processors for 'High-end' television receivers which contain the following functions:

- RGB control processor with Y, U and V inputs, a linear RGB input for SCART or VGA signals with fast blanking, a linear RGB input for OSD and text signals with a fast blanking or blending option and an RGB output stage with black current stabilization, which is realized with the CCC (2-point black current measurement) system.
- Programmable deflection processor with internal clock generation, which generates the drive signals for the horizontal, East-West (E-W) and vertical deflection. The circuit has various features that are attractive for the application of 16 : 9 picture tubes.
- The circuit can be used in both single scan (50 or 60 Hz) and double scan (100 or 120 Hz) applications.

In addition to these functions, the TDA9331H and TDA9332H have a multi-sync function for the horizontal PLL, with a frequency range from 30 to 50 kHz ($2f_H$ mode) or 15 to 25 kHz ($1f_H$ mode), so that the ICs can also be used to display SVGA signals.

The supply voltage of the ICs is 8 V. They are each contained in a 44-pin QFP package.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9330H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2
TDA9331H			
TDA9332H			

SURVEY OF IC TYPES

IC VERSION	VGA MODE	DAC OUTPUT
TDA9330H	no	I²C-bus controlled
TDA9331H	yes	proportional to VGA frequency
TDA9332H	yes	I²C-bus controlled

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltage	–	8.0	–	V
I_P	supply current (V_{P1} plus V_{P2})	–	50	–	mA
Input voltages					
$V_{i(Y)(b\text{-}w)}$	luminance input signal (black-to-white value)	–	1.0/0.315	–	V
$V_{i(U)(p\text{-}p)}$	U input signal (peak-to-peak value)	–	1.33	–	V
$V_{i(V)(p\text{-}p)}$	V input signal (peak-to-peak value)	–	1.05	–	V
$V_{i(RGB)(b\text{-}w)}$	RGB input signal (black-to-white value)	–	0.7	–	V
$V_{i(Hsync)}$	horizontal sync input (H_D)	–	TTL	–	V
$V_{i(Vsync)}$	vertical sync input (V_D)	–	TTL	–	V
$V_{i(IIC)}$	I²C-bus inputs (SDA and SCL)	–	CMOS 5 V	–	V
Output signals					
$V_{o(RGB)(b\text{-}w)}$	RGB output signal amplitude (black-to-white value)	–	2.0	–	V
$I_{o(hor)}$	horizontal output current	–	–	10	mA
$I_{o(ver)(p\text{-}p)}$	vertical output current (peak-to-peak value)	–	0.95	–	mA
$I_{o(EW)}$	E-W drive output current	–	–	1.2	mA

BLOCK DIAGRAM

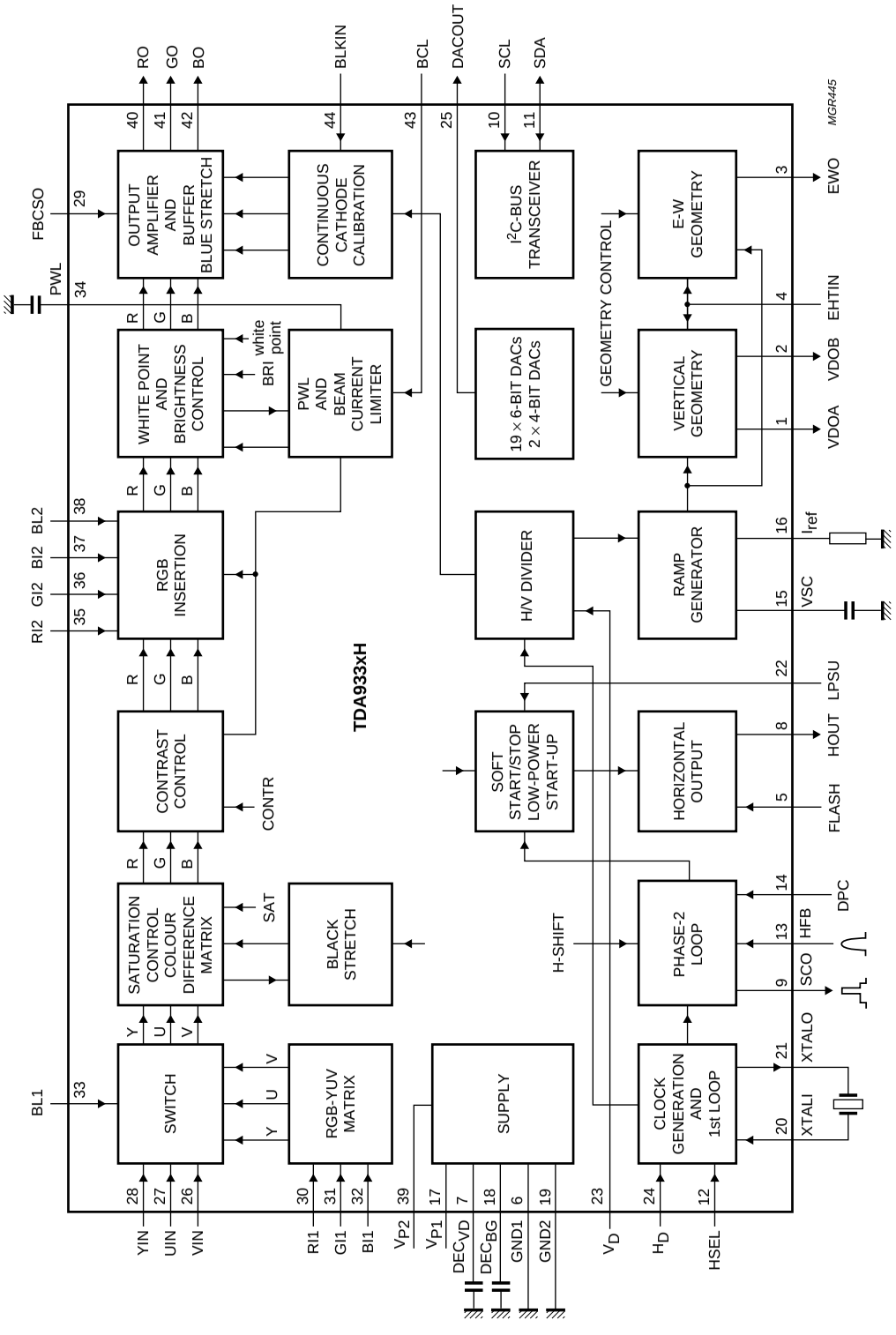


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
VDOA	1	vertical drive output A
VDOB	2	vertical drive output B
EWO	3	E-W output
EHTIN	4	EHT compensation input
FLASH	5	flash detection input
GND1	6	ground 1
DEC_{VD}	7	digital supply decoupling
HOUT	8	horizontal output
SCO	9	sandcastle pulse output
SCL	10	serial clock input
SDA	11	serial data input/output
HSEL	12	selection of horizontal frequency
HFB	13	horizontal flyback pulse input
DPC	14	dynamic phase compensation
VSC	15	vertical sawtooth capacitor
I_{ref}	16	reference current input
V_{P1}	17	positive supply 1 (+8 V)
DEC_{BG}	18	band gap decoupling
GND2	19	ground 2
XTALI	20	crystal input
XTALO	21	crystal output
LPSU	22	low-power start-up supply
V_D	23	vertical sync input
H_D	24	horizontal sync input
DACOUT	25	DAC output
VIN	26	V-signal input
UIN	27	U-signal input
YIN	28	luminance input
FBCSO	29	fixed beam current switch-off input
RI1	30	red 1 input for insertion
GI1	31	green 1 input for insertion
BI1	32	blue 1 input for insertion
BL1	33	fast blanking input for RGB-1
PWL	34	peak white limiting decoupling
RI2	35	red 2 input for insertion
GI2	36	green 2 input for insertion
BI2	37	blue 2 input for insertion
BL2	38	fast blanking/blending input for RGB-2
V_{P2}	39	positive supply 2 (+8 V)
RO	40	red output

SYMBOL	PIN	DESCRIPTION
GO	41	green output
BO	42	blue output
BCL	43	beam current limiting input
BLKIN	44	black current input

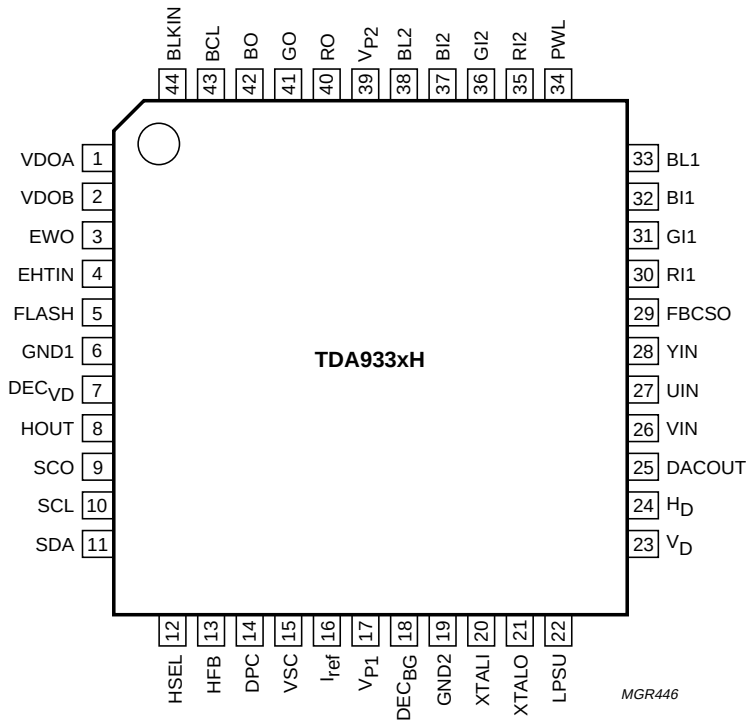


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

RGB control circuit

INPUT SIGNALS

The RGB control circuit of the TDA933xH contains three sets of input signals:

- YUV input signals, which are supplied by the input processor or the feature box. Bit GAI can be used to switch the luminance input signal sensitivity between 0.45 V (p-p) and 1.0 V (b-w). The nominal input signals for U and V are 1.33 V (p-p) and 1.05 V (p-p), respectively. These input signals are controlled on contrast, saturation and brightness.
- The first RGB input is intended for external signals (SCART in $1f_H$ and VGA in $2f_H$ applications), which have an amplitude of 0.7 V (p-p) typical. This input is also controlled on contrast, saturation and brightness.
- The second RGB input is intended for OSD and teletext signals. The required input signals have an amplitude of 0.7 V (p-p). The switching between the internal signal and the OSD signal can be realized via a blending function or via fast blanking. This input is only controlled on brightness.

Switching between the various sources can be realized via the I²C-bus and by fast insertion switches. The fast insertion switches can be enabled via the I²C-bus.

The circuit contains switchable matrix circuits for the colour difference signals so that the colour reproduction can be adapted for PAL/SECAM and NTSC. For NTSC, two different matrices can be chosen. In addition, a matrix for high-definition ATSC signals is available.

OUTPUT AMPLIFIER

The output signal has an amplitude of approximately 2 V (b-w) at nominal input signals and nominal settings of the controls. The required ‘white point setting’ of the picture tube can be realized by means of three separate gain settings for the RGB channels.

To obtain an accurate biasing of the picture tube, a CCC circuit has been developed. This function is realized by a 2-point black level stabilization circuit.

By inserting two test levels for each gun and comparing the resulting cathode currents with two different reference currents, the influence of the picture tube parameters such as the spread in cut-off voltage can be eliminated.

This 2-point stabilization is based on the principle that the ratio between the cathode currents is coupled to the ratio between the drive voltages according to: $\frac{I_{k1}}{I_{k2}} = \left(\frac{V_{dr1}}{V_{dr1}}\right)^{\gamma}$

The feedback loop makes the ratio between cathode currents I_{k1} and I_{k2} equal to the ratio between the reference currents (which are internally fixed) by changing the (black) level and the amplitude of the RGB output signals via two converging loops. The system operates in such a way that the black level of the drive signal is controlled to the cut-off point of the gun. In this way, a very good grey scale tracking is obtained. The accuracy of the adjustment of the black level is only dependent on the ratio of internal currents and these can be made very accurately in integrated circuits. An additional advantage of the 2-point measurement is that the control system makes the absolute value of I_{k1} and I_{k2} identical to the internal reference currents. Because this adjustment is obtained by adapting the gain of the RGB control stage, this control stabilizes the gain of the complete channel (RGB output stage and cathode characteristic). As a result, this 2-point loop compensates for variations in the gain figures during life.

An important property of the 2-point stabilization is that the offset and the gain of the RGB path are adjusted by the feedback loop. Hence, the maximum drive voltage for the cathode is fixed by the relationship between the test pulses, the reference current and the relative gain setting of the three channels. Consequently, the drive level of the CRT cannot be adjusted by adapting the gain of the RGB output stage. Because different picture tubes may require different drive levels, the typical ‘cathode drive level’ amplitude can be adjusted by means of an I²C-bus setting. Depending on the selected cathode drive level, the typical gain of the RGB output stages can be fixed, taking into account the drive capability of the RGB outputs (pins 40 to 42). More details about the design are given in the application report (see also Chapter “Characteristics”; note 11).

The measurement of the high and the low currents of the 2-point stabilization circuit is performed in two consecutive fields. The leakage current is measured in each field. The maximum allowable leakage current is 100 μA.

For extra flexibility, it also possible to switch the CCC circuit to 1-point stabilization with the OPC bit. In this mode, only the black level at the RGB outputs is controlled by the loop. The cathode drive level setting has no influence on the gain in this mode. This level should be set to the nominal value to get the correct amplitude of the measuring pulses.

Via the I²C-bus, an adjustable offset can be made on the black level of red and green channels with respect to the level that is generated by the black current control loop. These controls can be used to adjust the colour temperature of the dark part of the picture, independent of the white point adjustment.

When the TV receiver is switched on, the black current stabilization circuit is directly activated and the RGB outputs are blanked. The blanking is switched off as soon as the loop has stabilized (e.g. the first time that bit BCF changes from 1 to 0, see also Chapter “Characteristics”; note 15). This ensures that the switch-on time is reduced to a minimum and is only dependent on the warm-up time of the picture tube.

The black current stabilization system checks the output level of the three channels and indicates whether the black level of the lowest RGB output of the IC is in a certain window (WBC bit), below or above this window (HBC bit). This indication can be read from the I²C-bus and can be used for automatic adjustment of voltage V_{g2} during the production of the TV receiver.

When a failure occurs in the black current loop (e.g. due to an open circuit), status bit BCF is set. This information can be used to blank the picture tube to avoid damage to the screen.

The control circuit contains an average beam current limiting circuit and a peak white level (PWL) circuit. The PWL detects small white areas in the picture that are not detected by the average beam current limiter. The PWL can be adjusted via the I²C-bus. A low-pass filter is placed in front of the peak detector to prevent it from reacting to short transients in the video signal. The capacitor of the low-pass filter is connected externally so that the set maker can adapt the time constant as required. The IC also contains a soft clipper that limits the amplitude of the short transients in the RGB output signals. In this way, spot blooming on, for instance, subtitles is prevented. The difference between the PWL and the soft clipping level can be adjusted via the I²C-bus in a few steps.

The vertical blanking is adapted to the vertical frequency of the incoming signal (50 or 100 Hz or, 60 or 120 Hz). When the flyback time of the vertical output stage is greater than the 60 Hz blanking time, the blanking can be increased to the same value as that of the 50 Hz blanking. This can be set by means of bit LBM.

When no video is available, it is possible to insert a blue background. This feature can be activated via bit EBB.

Synchronization and deflection processing

HORIZONTAL SYNCHRONIZATION AND DRIVE CIRCUIT

The horizontal drive signal is obtained from an internal VCO which runs at a frequency of 440 times ($2f_H$ mode) or 880 times ($1f_H$ mode) the frequency of the incoming H_D signal. The free-running frequency of this VCO is calibrated by a crystal oscillator which needs an external 12 MHz crystal or ceramic resonator as a reference. It is also possible to supply an external reference signal to the IC (in this case, the external resonator should be removed).

The VCO is synchronized to the incoming horizontal H_D pulse (applied from the feature box or the input processor) by a PLL with an internal time constant. The frequency of the horizontal drive signal ($1f_H$ or $2f_H$) is selected by means of a switching pin, which must be connected to ground or left open circuit.

For HDTV applications, it is possible to change the free-running frequency of the horizontal drive output from 31.2 kHz to 33.7 kHz by means of bit HDTV.

For safety reasons, switching between $1f_H$ and $2f_H$ modes is only possible when the IC is in the standby mode.

For the TDA9331H and TDA9332H, it is also possible to set the horizontal PLL to a ‘multi-sync’ mode by means of bit VGA. In this mode, the circuit detects the frequency of the incoming sync pulses and adjusts the centre frequency of the VCO accordingly by means of an internal Digital-to-Analog-Converter (DAC). The frequency range in this mode is 30 to 50 kHz at the output.

The polarities of the incoming H_D and V_D pulses are detected internally. The detected polarity can be read out via status bits HPOL and VPOL.

The horizontal drive signal is generated by a second control loop which compares the phase of the reference signal (applied from the internal VCO) with the flyback pulse. The time constant of this loop is set internally. The IC has a dynamic horizontal phase correction input, which can be used to compensate phase shifts that are caused by beam current variations. Additional settings of the horizontal deflection (which are realized via the second loop) are the horizontal shift and horizontal parallelogram and bow corrections (see Chapter “Characteristics”; Fig.16). The adjustments are realized via the I²C-bus.

When no horizontal flyback pulse is detected during three consecutive line periods, status bit NHF is set (output status byte 01-D3; see Table 3).

The horizontal drive signal is switched on and off via the so-called slow-start/slow-stop procedure. This function is realized by varying the t_{on} of the horizontal drive pulse. For EHT generators without a bleeder, the IC can be set to a 'fixed beam current mode' via bit FBC. In this case, the picture tube capacitance is discharged with a current of approximately 1 mA. The magnitude of the discharge current is controlled via the black current feedback loop. If necessary, the discharge current can be enlarged with the aid of an external current division circuit. With the fixed beam current option activated, it is still possible to have a black screen during switch-off. This can be realized by placing the vertical deflection in an overscan position. This mode is activated via bit OSO.

An additional mode of the IC is the 'low-power start-up' mode. This mode is activated when a supply voltage of 5 V is supplied to the start-up pin.

The required current for this mode is 3 mA (typ.). In this condition, the horizontal drive signal has the nominal t_{off} and the t_{on} grows gradually from zero to approximately 30% of the nominal value. This results in a line frequency of approximately 50 kHz ($2f_H$) or 25 kHz ($1f_H$). The output signal remains unchanged until the main supply voltage is switched on and the I²C-bus data has been received. The horizontal drive then gradually changes to the nominal frequency and duty cycle via the slow-start procedure.

The IC can only be switched on and to standby mode when both standby bits (STB0 and STB1) are changed. The circuit will not react when only one bit changes polarity.

The IC has a general purpose bus controlled DAC output with a 6-bit resolution and with an output voltage range between 0.2 to 4 V. In the TDA9331H, the DC voltage on this output is proportional to the horizontal line frequency (only in VGA mode). This voltage can be used to control the supply voltage of the horizontal deflection stage, to maintain constant picture width for higher line frequencies.

VERTICAL DEFLECTION AND GEOMETRY CONTROL

The drive signals for the vertical and E-W deflection circuits are generated by a vertical divider, which derives its clock signal from the line oscillator. The divider is synchronized by the incoming V_D pulse, generated by the input processor or the feature box. The vertical ramp generator requires an external resistor and capacitor; the tolerances for these components must be small. In the normal mode, the vertical deflection operates in constant slope and adapts its amplitude, depending on the frequency of the incoming signal (50 or 60 Hz, or 100 or 120 Hz). When the TDA933xH is switched to the VGA mode, the amplitude of the vertical scan is stabilized and independent of the incoming vertical frequency. In this mode, the E-W drive amplitude is proportional to the horizontal frequency so that the correction on the screen is not affected.

The vertical drive is realized by a differential output current. The outputs must be DC-coupled to the vertical output stage (e.g. TDA8354).

The vertical geometry can be adjusted via the I²C-bus. Controls are possible for the following parameters:

- Vertical amplitude
- S-correction
- Vertical slope
- Vertical shift (only for compensation of offsets in output stage or picture tube)
- Vertical zoom
- Vertical scroll (shifting the picture in the vertical direction when the vertical scan is expanded)
- Vertical wait, an adjustable delay for the start of the vertical scan.

With regard to the vertical wait, the following conditions are valid:

- In the $1f_H$ TV mode, the start of the vertical scan is fixed and cannot be adjusted with the vertical wait
- In the $2f_H$ TV mode, the start of the vertical scan depends on the value of the Vertical Scan Reference (VSR) bus bit. If VSR = 0, the start of the vertical scan is related to the end of the incoming V_D pulse. If VSR = 1, it is related to the start. In both cases, the start of the scan can be adjusted with the vertical wait setting
- In the multi-sync mode (TDA9331H and TDA9332H both in $1f_H$ mode and $2f_H$ mode), the start of the vertical scan is related to the start of the incoming V_D pulse and can be adjusted with the vertical wait setting.

The minimum value for the vertical wait setting is 8 line periods. If the setting is lower than 8, the wait period will remain at 8 line periods.

The E-W drive circuit has a single-ended output. The E-W geometry can be adjusted on the following parameters:

- Horizontal width with increased range because of the 'zoom' feature
- E-W parabola/width ratio
- E-W upper corner/parabola ratio
- E-W lower corner/parabola ratio
- E-W trapezium.

The IC has an EHT compensation input which controls both the vertical and the E-W output signals. The relative control effect on both outputs can be adjusted via the I²C-bus (sensitivity of vertical correction is fixed; E-W correction variable).

To avoid damage to the picture tube in the event of missing or malfunctioning vertical deflection, a vertical guard function is available at the sandcastle pin (pin SCO). The vertical guard pulse from the vertical output stage (TDA835x) should be connected to the sandcastle pin, which acts as a current sense input. If the guard pulse is missing or lasts too long, bit NDF is set in the status register and the RGB outputs are blanked. If the guard function is disabled via bit EVG, only NDF status bit NHF is set.

The IC also has inputs for flash and overvoltage protection. More details about these functions are given in Chapter “Characteristics”; note 43.

I²C-BUS SPECIFICATION

The slave address of the IC is given in Table 1. The circuit operates up to clock frequencies of 400 kHz. Valid subaddresses: 00 to 1F, subaddress FE is reserved for test purposes. The auto-increment mode is available for subaddresses.

Table 1 Slave address (8C)

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	1	0	1/0

Table 2 Input control bits

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
RGB processing-1	00	MAT	EBB	SBL	RBL	BLS	BKS	IE1	IE2
RGB processing-2	01	MUS	FBC	OBL	AKB	CL3	CL2	CL1	CL0
Wide horizontal blanking	02	HBL	TFBC	GAI	STB0	HB3	HB2	HB1	HB0
Horizontal deflection	03	HDTV	VSR	0	STB1	POC	PRD	VGA[3]	ESS
Vertical deflection	04	OPC	VFF	LBM	DIP	OSO	SVF	EVG	DL
Brightness	05	0	0	A5	A4	A3	A2	A1	A0
Saturation	06	0	0	A5	A4	A3	A2	A1	A0
Contrast	07	0	0	A5	A4	A3	A2	A1	A0
White point R	08	0	0	A5	A4	A3	A2	A1	A0
White point G	09	0	0	A5	A4	A3	A2	A1	A0
White point B	0A	0	0	A5	A4	A3	A2	A1	A0
Peak white limiting	0B	0	0	SC1	SC0	A3	A2	A1	A0
Horizontal shift	0C	0	0	A5	A4	A3	A2	A1	A0
Horizontal parallelogram[1]	0D	0	0	0	0	A3	A2	A1	A0
E-W width	0E	0	0	A5	A4	A3	A2	A1	A0
E-W parabola/width	0F	0	0	A5	A4	A3	A2	A1	A0
E-W upper corner/parabola	10	0	0	A5	A4	A3	A2	A1	A0
E-W trapezium	11	0	0	A5	A4	A3	A2	A1	A0
E-W EHT compensation sensitivity	12	0	0	A5	A4	A3	A2	A1	A0
Vertical slope	13	0	0	A5	A4	A3	A2	A1	A0
Vertical amplitude	14	0	0	A5	A4	A3	A2	A1	A0
S-correction	15	0	0	A5	A4	A3	A2	A1	A0
Vertical shift	16	0	0	A5	A4	A3	A2	A1	A0
Vertical zoom	17	0	0	A5	A4	A3	A2	A1	A0
Vertical scroll	18	0	0	A5	A4	A3	A2	A1	A0
Vertical wait	19	0	0	0	A4	A3	A2	A1	A0
DAC output[2]	1A	0	0	A5	A4	A3	A2	A1	A0
Black level offset R	1B	0	0	0	0	A3	A2	A1	A0
Black level offset G	1C	0	0	0	0	A3	A2	A1	A0
Horizontal timing	1D	0	0	0	HDCL	LBL3	LBL2	LBL1	LBL0
E-W lower corner/parabola	1E	0	0	A5	A4	A3	A2	A1	A0
Horizontal bow[1]	1F	0	0	0	0	A3	A2	A1	A0

Notes

1. For zero parallelogram and bow correction use register value 7 DEC.
2. See Chapter “Characteristics”; note 47.
3. Bit VGA is not available in the TDA9330H.

Table 3 Output status bits

FUNCTION	SUBADDRESS (HEX)	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Output status bytes	00	POR	FSI	SL	XPR	NDF	IN1	IN2	WBC
	01	N2	ID2	ID1	ID0	NHF	BCF	FLS	NRF
	02	X	X	X	X	X	HPOL	VPOL	HBC

Input control bits

Table 4 Colour difference matrix

MAT	MUS	MATRIX POSITION
0	0	PAL
0	1	ATSC
1	0	NTSC Japan
1	1	NTSC USA

Table 5 Enable ‘blue-back’

EBB	MODE
0	blue-black switched off
1	blue-black switched on

Table 6 Service blanking

SBL	SERVICE BLANKING MODE
0	off
1	on

Table 7 RGB blanking

RBL	RGB BLANKING
0	not active
1	active

Table 8 Blue stretch

BLS	BLUE STRETCH MODE
0	off
1	on

Table 9 Black stretch

BKS	BLACK STRETCH MODE
0	off
1	on

Table 10 Enable fast blanking RGB-1

IE1	FAST BLANKING
0	not active
1	active

Table 11 Enable fast blanking RGB-2

IE2	FAST BLANKING
0	not active
1	active

Table 12 Fixed beam current switch-off

FBC	MODE
0	switch-off with blanked RGB outputs
1	switch-off with fixed beam current

Table 13 Blending function on OSD; note 1

OBL	MODE
0	OSD via fast blanking
1	OSD via blending function

Note

1. When bit OBL is set to 1, the blending function is always activated, independent of the setting of bit IE2.

Table 14 Black current stabilization

AKB	OPC	MODE
0	0	2-point control
0	1	1-point control
1	–	not active

Table 15 Cathode drive level (15 steps; 3.6 V/step)

CL3	CL2	CL1	CL0	SETTING OF CATHODE DRIVE AMPLITUDE(1)
0	0	0	0	41 V (b-w)
1	0	0	0	70 V (b-w)
1	1	1	1	95 V (b-w)

Note

1. The given values are valid for the following conditions:
   a) Nominal CVBS input signal.
   b) Settings for contrast and white point nominal.
   c) Black and blue stretch switched off.
   d) Gain of output stage such that no clipping occurs.
   e) Beam current limiting not active.
   f) Gamma of picture tube is 2.25.
   g) The tolerance on these values is approximately ±3 V.

Table 16 RGB blanking mode

HBL	MODE
0	normal blanking (horizontal flyback)
1	wide blanking

Table 17 Picture tube discharge time

TFBC	MODE
0	18.6 ms
1	25 ms

Note

1. See Chapter “Characteristics”; Fig.15

Table 18 Gain of luminance channel

GAI	MODE
0	normal gain [V_{28} = 1 V (b-w)]
1	high gain [V_{28} = 0.45 V (p-p)]

Table 19 Standby

STB0	STB1	CONDITION
0	0	horizontal drive off
0	1	no action
1	0	no action
1	1	horizontal drive on

Table 20 Position of wide blanking (14 steps; $1f_H$ mode 0.29 µs/step; $2f_H$ mode 0.145 µs/step)

HB3	HB2	HB1	HB0	TIMING OF BLANKING(1)	
				$1f_H$ MODE	$2f_H$ MODE
0	0	0	0	–2.03 µs	–1.015 µs
0	1	1	1	0 µs	0 µs
1	1	1	–	2.03 µs	1.015 µs

Note

1. See Chapter “Characteristics”; note 13.

Table 21 Horizontal free-running frequency in TV mode

HDTV	FREQUENCY	
	$1f_H$ MODE	$2f_H$ MODE
0	15.65 kHz	31.3 kHz
1	16.85 kHz	33.7 kHz

Table 22 Vertical scan reference in $2f_H$ TV mode

VSR	VERTICAL SCAN REFERENCE
0	end of V_D pulse
1	start of V_D pulse

Table 23 Synchronization mode

POC	MODE
0	synchronization active
1	synchronization not active

Table 24 Overvoltage input mode

PRD	OVERVOLTAGE MODE
0	detection mode
1	protection mode

Table 25 Multi-sync mode

VGA	MODE
0	horizontal frequency fixed by internal reference
1	multi-sync function switched on

Table 26 Extended slow start mode

ESS	EXTENDED SLOW START MODE
0	not active
1	active

Table 27 Long blanking mode

LBM	BLANKING MODE
0	adapted to standard (50 or 60 Hz)
1	fixed in accordance with 50 Hz standard

Table 28 Vertical free-running frequency in TV mode

VFF	FREQUENCY
0	50 Hz (SVF = 0) or 100 Hz (SVF = 1)
1	60 Hz (SVF = 0) or 120 Hz (SVF = 1)

Table 29 De-interlace phase

DIP	PHASE
0	delay of 1st field (start of synchronized V_D pulse coincides with H-flyback) with 0.5 H
1	delay of 2nd field with 0.5 H

Table 30 Switch-off in vertical overscan

OSO	MODE
0	switch-off undefined
1	switch-off in vertical overscan

Table 31 Select vertical frequency

SVF	MODE
0	vertical frequency is 50 or 60 Hz
1	vertical frequency is 100 or 120 Hz

Table 32 Enable vertical guard (RGB blanking)

EVG	VERTICAL GUARD MODE
0	not active
1	active

Table 33 Interlace

DL	STATUS
0	interlace
1	de-interlace

Table 34 Soft clipping level

SC1	SC0	VOLTAGE DIFFERENCE BETWEEN SOFT CLIPPING AND PWL
0	0	0% above PWL
0	1	5% above PWL
1	0	10% above PWL
1	1	soft clipping off

Table 35 Clamp pulse timing

HDCL	MODE(1)
0	normal timing
1	HDTV timing

Note

1. See Chapter “Characteristics”; note 13.

Table 36 Start line blanking (15 steps; 2 line locked clock period per step; 1 line period is 440 LLC pulses)

LBL3	LBL2	LBL1	LBL0	START LINE BLANKING(1)
0	0	0	0	+14 LLC
0	1	1	1	normal
1	1	1	1	–16 LLC

Note

1. See Chapter “Characteristics”; note 13.

Output status bits

Table 37 Power-on reset

POR	MODE
0	normal
1	power-down

Table 38 Field frequency indication

FSI	FREQUENCY
0	50 or 100 Hz
1	60 or 120 Hz

Table 39 Phase 1 (φ_1) lock indication

SL	INDICATION
0	not locked
1	locked

Table 40 X-ray protection

XPR	OVERVOLTAGE
0	no overvoltage detected
1	overvoltage detected

Table 41 Output of vertical guard

NDF	VERTICAL OUTPUT STAGE
0	OK
1	failure

Table 42 Indication of RGB-1 insertion

IN1	RGB INSERTION
0	no
1	yes

Table 43 Indication of RGB-2 insertion

IN2	RGB INSERTION
0	no
1	yes

Table 44 Indication of output black level inside/outside V_{g2} alignment window

WBC	CONDITION(1)
0	black current stabilization outside window
1	black current stabilization inside window

Note

1. See Chapter “Characteristics”; note 16.

Table 45 IC identification

ID2	ID1	ID0	IC VERSION
0	0	0	TDA9330H
0	0	1	TDA9332H
0	1	1	TDA9331H

Table 46 Mask version indication

N2	MASK VERSION
0	N1 version
1	N2 version

Table 47 Condition of horizontal flyback

NHF	CONDITION
0	flyback pulse present
1	flyback pulse not present

Table 48 Indication of failure in black current circuit

BCF	CONDITION
0	normal operation
1	failure in black current stabilization circuit

Table 49 Indication of flash detection

FLS	CONDITION
0	no flash-over detected
1	flash-over detected

Table 50 Locking of reference oscillator to crystal oscillator

NRF	CONDITION
0	reference oscillator is locked
1	reference oscillator is not locked

Table 51 Indication of output black level below or above the middle of V_{g2} alignment window

HBC	CONDITION(1)
0	black current stabilization below window
1	black current stabilization above window

Note

1. See Chapter “Characteristics”; note 16.

Table 52 Polarity of H_D input pulse

HPOL	POLARITY
0	positive
1	negative

Table 53 Polarity of V_D input pulse

VPOL	POLARITY
0	positive
1	negative

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	9.0	V
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_{sol}	soldering temperature	for 5 s	–	260	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	60	K/W

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611E-part E"*.

ESD protection

All pins are protected against ESD by internal protection diodes, and meet the following specification:

- Human body model (R = 1.5 kΩ; C = 100 pF): all pins > ±3000 V
- Machine model (R = 0 Ω; C = 200 pF): all pins > ±300 V.

Latch-up performance

At an ambient temperature of 50 °C all pins meet the following specification:

- Positive stress test: $I_{trigger} \geq 100$ mA or $V_{pin} \geq 1.5 \times V_{CC(max)}$
- Negative stress test: $I_{trigger} \leq -100$ mA or $V_{pin} \leq -0.5 \times V_{CC(max)}$.

At an ambient temperature of 70 °C, all pins meet the specification as mentioned above, with the exception of pin 32, which can withstand a negative stress current of at least 50 mA.

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
MAIN SUPPLY; PINS 17 AND 39						
V_{P1}	supply voltage		7.2	8.0	8.8	V
V_{POR}	power-on reset voltage level	note 1	5.8	6.1	6.5	V
I_{P1}	supply current	pin 17 plus pin 39	44	50	58	mA
		pin 17	–	22	–	mA
		pin 39	–	28	–	mA
P_{tot}	total power dissipation		–	400	–	mW
LOW-POWER START-UP; PIN 22						
V_{P2}	supply voltage	note 2	4.5	5.0	5.5	V
I_{P2}	supply current		–	3.0	4.5	mA
RGB control circuit						
LUMINANCE INPUT; PIN 28						
$V_{i(Y)(b\text{-}w)}$	luminance input voltage (black-to-white value)	GAI = 0	–	1.0	1.5	V
Z_i	input impedance		10	–	–	MΩ
C_i	input capacitance		–	–	5	pF
$I_{i(Y)(clamp)}$	input current during clamping		–25	0	+25	µA
U/V INPUTS; PINS 27 AND 26						
$V_{i(U)(p\text{-}p)}$	U input signal amplitude (peak-to-peak value)		–	1.33	2.0	V
$V_{i(V)(p\text{-}p)}$	V input signal amplitude (peak-to-peak value)		–	1.05	1.6	V
Z_i	input impedance		10	–	–	MΩ
C_i	input capacitance		–	–	5	pF
$I_{i(UV)(clamp)}$	input current during clamping		–20	0	+25	µA
RGB-1 INPUT (SCART/VGA); PINS 30 TO 32; note 3						
$V_{i(b\text{-}w)}$	input signal amplitude (black-to-white value)		–	0.7	1.0	V
ΔV_o	difference between black level of YUV and RGB-1 signals at the outputs		–	–	10	mV
Z_i	input impedance		10	–	–	MΩ
C_i	input capacitance		–	–	5	pF
$I_{i(clamp)}$	input current during clamping		–25	0	+25	µA
Δt_d	delay difference for the three channels	note 5	–	0	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FAST BLANKING INPUT (RGB-1); PIN 33						
$V_{i(BL1)}$	input voltage	no data insertion	0	–	0.45	V
		data insertion	0.9	–	3.0	V
Δt_d	delay difference between insertion to RGB out and RGB in to RGB out	data insertion; note 5	–	10	20	ns
$I_{i(BL1)}$	input current	source current; note 6	–	–0.12	–0.2	mA
SS_{int}	suppression of internal RGB signals	insertion; f_i = 0 to 10 MHz; notes 5 and 7	50	55	–	dB
SS_{ext}	suppression of external RGB signals	no insertion; f_i = 0 to 10 MHz; notes 5 and 7	50	55	–	dB
RGB-2 INPUT (OSD/TEXT); PINS 35 TO 37						
$V_{i(b-w)}$	input signal amplitude (black-to-white value)		–	0.7	1.0	V
ΔV_o	difference between black level of YUV/RGB-1 and RGB-2 signals at the outputs		–	–	tbf	mV
Z_i	input impedance		10	–	–	MΩ
C_i	input capacitance		–	–	5	pF
$I_{i(clamp)}$	input current during clamping		–40	0	+40	μA
Δt_d	delay difference for the three channels	note 5	–	0	–	ns
BLENDING (FAST BLANKING) INPUT (RGB-2); PIN 38; note 8						
Blending function (OBL = 1)						
$V_{i(BL2)(1)}$	input voltage	no data insertion	0	–	0.05	V
		50% insertion	0.69	0.725	0.76	V
		100% insertion	1.42	1.47	3.0	V
		active blending range	0.31	–	1.14	V
$Ins_{(osd)}$	percentage of data insertion	V_i = 0.31 V	0	1	4	%
		V_i = 0.725 V	45	50	55	%
		V_i = 1.14 V	96	99	100	%
		internal signal is 50%	48	50	52	%
$V_{i(max)}$	slope of blending curve	50% insertion	–	160	–	%/V
Fast blanking function (OBL = 0)						
$V_{i(BL2)(0)}$	input voltage	no data insertion	0	–	0.3	V
		data insertion	0.9	–	3.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General						
Δt_d	delay difference between insertion to RGB out and RGB in to RGB out	data insertion; note 5	–	20	26	ns
$I_{i(BL2)}$	input current	source current; note 6	–	–1	–5	μA
SS_{int}	suppression of internal RGB signals	insertion; f_i = 0 to 10 MHz; notes 5 and 7	50	55	–	dB
SS_{ext}	suppression of external RGB signals	no insertion; f_i = 0 to 10 MHz; notes 5 and 7	50	55	–	dB
COLOUR DIFFERENCE MATRICES; note 3						
PAL/SECAM mode; the matrix results in the following signal						
G – Y	G – Y		– 0.51 (R – Y) – 0.19 (B – Y)			
ATSC mode; the matrix results in the following signal; note 4						
G – Y	G – Y		– 0.30 (R – Y) – 0.10 (B – Y)			
NTSC mode; the matrix results in the following modified colour difference signals						
MUS bit = 0 (Japan)						
R – Y	(R – Y)*		1.39 (R – Y) – 0.07 (B – Y)			
G – Y	(G – Y)*		– 0.46 (R – Y) – 0.15 (B – Y)			
B – Y	(B – Y)*		B – Y			
MUS bit = 1 (USA)						
R – Y	(R – Y)*		1.32 (R – Y) – 0.12 (B – Y)			
G – Y	(G – Y)*		– 0.42 (R – Y) – 0.25 (B – Y)			
B – Y	(B – Y)*		– 0.03 (R – Y) +1.08 (B – Y)			
CONTROLS						
Saturation control; note 9						
CR_{sat}	saturation control range	small signal gain; 63 steps; see Fig.5	0	–	300	%
$CR_{sat(nom)}$	I²C-bus setting for nominal saturation	YUV input signal	–	20 DEC	–	
$CR_{sat(min)}$	minimum saturation	I²C-bus setting 0	–	–50	–	dB
Contrast control; note 9						
CR_{contr}	contrast control range	63 steps; see Fig.6	–	18	–	dB
	tracking between the three channels over a control range of 10 dB		–	–	0.5	dB
Brightness control; note 9						
CR_{bri}	brightness control range	63 steps; see Fig.7	–	±1.1	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BLACK LEVEL STRETCHER; note 10						
$\Delta V_{bl(max)}$	maximum black level shift	A-to-A; see Fig.8	15	21	27	IRE
ΔV_{bl}	black level shift	at 100% peak white	–1	0	+1	IRE
		at 50% peak white	–1	–	+3	IRE
		at 15% peak white	6	8	10	IRE
RGB AMPLIFIER OUTPUTS: PINS 40 TO 42						
$V_{40\text{-}42(b\text{-}w)}$	output signal amplitude (black-to-white value)	at nominal luminance input signal and nominal contrast, cathode drive level and white-point adjustment; note 11	–	2.0	–	V
V_o	output voltage range		1	–	$V_{CC} - 2$	V
Z_o	output impedance	note 12	–	120	150	Ω
I_{sink}	sink current	emitter follower output	–	2	–	mA
$V_{o(RED)(p\text{-}p)}$	output signal amplitude for the 'red' channel (peak-to-peak value)	at nominal settings for contrast and saturation control and no luminance signal at the input (R–Y, PAL); note 11	–	2.1	–	V
$V_{bl(nom)}$	nominal black level voltage		–	2.5	–	V
V_{bl}	black level voltage	when black level stabilization is switched off (via AKB bit)	–	2.5	–	V
$t_{W(blank)}$	width of video blanking pulse with bit HBL active	at $1f_H$; note 13	14.4	14.7	15.0	µs
		at $2f_H$; note 13	7.2	7.35	7.5	µs
CR_{bl}	control range of the black current stabilization	notes 15 and 16	–	±1	–	V
V_{blank}	blanking voltage level	difference with black level; note 11	–0.4	–0.5	–0.6	V
$V_{blank(leak)}$	blanking voltage level during leakage measurement		–	–0.1	–	V
$V_{blank(l)}$	blanking voltage level during low measuring pulse		–	0.25	–	V
$V_{blank(h)}$	blanking voltage level during high measuring pulse		–	0.38	–	V
$\Delta V_{(RGB)(mp)}$	adjustment range of the ratio between the amplitudes of the RGB drive voltage and the measuring pulses	note 11	–	±6	–	dB
$V_{bl(WBC)}$	black level at the output at which bit WBC is set to 1	nominal value	2.4	2.5	2.6	V
		window; note 16	–	±100	–	mV
$\Delta bl/\Delta T$	variation of black level with temperature	note 5	–	1.0	–	mV/K
CR_{bl}	black level offset adjustment range on red and green channels	15 steps; 10 mV/step	± 70	± 75	± 80	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{bl}	relative variation in black level between the three channels during variations of	note 5				
	supply voltage (±10%)	nominal controls	–	–	20	mV
	saturation (50 dB)	nominal contrast	–	–	20	mV
	contrast (20 dB)	nominal saturation	–	–	20	mV
	brightness (±0.5 V)	nominal controls	–	–	20	mV
	temperature (range 40 °C)		–	–	20	mV
S/N	signal-to-noise ratio of the output signals	notes 5 and 17	60	–	–	dB
$B_{o(Y)(10pF)}$	luminance bandwidth of output signals	with 10pF load capacitance; note 12				
		RGB-1 input; at –3 dB	22	25	–	MHz
		RGB-2 input; at –3 dB	29	33	–	MHz
		luminance input; at –3 dB	23	26	–	MHz
$B_{o(Y)(25pF)}$	luminance bandwidth of output signals	with 25pF load capacitance				
		RGB-1 input; at –3 dB	20	23	–	MHz
		RGB-2 input; at –3 dB	23	26	–	MHz
		luminance input; at –3 dB	21	24	–	MHz
WHITE-POINT ADJUSTMENT						
I^2C_{nom}	I²C-bus setting for nominal gain		–	32 DEC	–	
ΔG_{RGB}	adjustment range of RGB drive levels	CL control bits; see Table 15	±3.2	±3.6	±4.0	dB
ΔG_v	gain control range to compensate spreads in picture tube characteristics	white point controls	–	±3	–	dB
2-POINT BLACK CURRENT STABILIZATION; INPUT PIN 44; note 18						
$I_{ref(l)}$	amplitude of low reference current		–	8	–	µA
$I_{ref(h)}$	amplitude of high reference current		–	20	–	µA
I_L	acceptable leakage current		–	±100	–	µA
V_{Iref}	voltage on measurement pin	pin 44; loop closed	3.15	3.3	3.45	V
$I_{scan(max)}$	maximum current during scan	pin 44; loop open circuit note 18	–	–	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BEAM CURRENT LIMITING; INPUT PIN 43						
V_{bias}	internal bias voltage		3.5	3.6	3.7	V
V_{CR}	contrast reduction starting voltage		3.1	3.3	3.5	V
$V_{dif(CR)}$	voltage difference for full contrast reduction		2.0	2.2	2.4	V
V_{bri}	brightness reduction starting voltage		1.6	1.8	2.0	V
$V_{dif(BR)}$	voltage difference for full brightness reduction		–	1	–	V
$I_{ch(int)}$	internal charge current		1.5	2.0	2.5	µA
$I_{dch(max)}$	maximum discharge current when the PWL is active		3.5	4.0	4.5	mA
PEAK WHITE LIMITER; note 19						
$I_{ch(PWL)}$	charge current PWL filter pin	pin 34; $1f_V$ mode	13	16	19	µA
		pin 34; $2f_V$ mode	26	32	38	µA
$I_{dch(PWL)}$	discharge current PWL filter pin	pin 34; $1f_V$ mode	52	64	76	µA
		pin 34; $2f_V$ mode	100	120	140	µA
$V_{i(Y)(b-w)}$	Y-input signal amplitude at which peak white limiter is activated (black-to-white value)	PWL range, 15 steps; at maximum contrast	0.65	–	1.0	V
$V_{o(RGB)(b-w)}$	RGB output signal amplitude at which peak white limiter is activated (black-to-white value)	PWL range, 15 steps; nominal setting of white point controls; note 20	2.2	–	3.4	V
SOFT CLIPPER; note 21						
$\Delta G_{v(sc)}$	soft clipper gain reduction	at maximum contrast; see Fig.9	–	15	–	dB
$V_{o(clip-pwl)}$	output level compared to PWL for 100 IRE peak signal	(A+B)/A; see Fig.9	–	118	–	%
BLUE STRETCH; note 22						
ΔG_{RG}	decrease of small signal gain for red and green channels		–	17	–	%
FIXED BEAM CURRENT SWITCH-OFF; notes 23, 24 and 25						
V_{FBCSO}	detection level		1	1.5	2	V
$V_{i(FBCSO)(max)}$	maximum input voltage		–	–	5.5	V
I_{dch}	discharge current when the fixed beam current function is activated	sink current pin 44; note 26	0.85	1.0	1.15	mA
$V_{o(max)}$	maximum output voltage at the RGB outputs	2-point stabilization; note 26	–	6.0	–	V
		1-point stabilization; note 26	–	5.6	–	V
t_{dch}	discharge time of picture tube when switching to standby	TFBC = 0; see Fig.15	–	18.6	–	ms
		TFBC = 1; see Fig.15	–	25	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Horizontal synchronization and deflection						
H_D INPUT SIGNAL; PIN 24						
V_{IL}	LOW-level of input voltage	note 27	–	–	0.8	V
V_{IH}	HIGH-level of input voltage	note 27	2.0	–	5.5	V
$I_{i(HD)}$	input current		–10	–	+10	μA
$t_{r(HD)}$	rise time		–	–	100	ns
$t_{f(HD)}$	fall time		–	–	100	ns
$t_{W(HD)}$	pulse width		200 ns	–	1/4 line	
INTERNAL REFERENCE SIGNAL; CRYSTAL OR RESONATOR CONNECTED TO PINS 20 AND 21; note 28						
f_{xtal}	resonator frequency		–	12	–	MHz
$R_{S(xtal)}$	resonator series resistance	C_L = 60 pF	–	–	30	Ω
$V_{i(stab)(p-p)}$	stabilized input signal (peak-to-peak value)		0.5	0.8	1.0	V
$g_{m(max)}$	maximum transconductance		4	5	–	mA/V
Z_i	input impedance		50	–	–	kΩ
C_i	input capacitance		–	–	10	pF
C_o	output capacitance		–	–	5	pF
EXTERNAL REFERENCE SIGNAL; INPUT PIN 20						
f_{XTALI}	input signal frequency		–	12	–	MHz
$V_{i(XTALI)(p-p)}$	input signal amplitude (peak-to-peak value)	AC coupled	0.8	–	2	V
FIRST CONTROL LOOP; note 29						
$f_{o(nom)}$	free-running frequency	$1f_H$ mode; note 30	–	15.65	–	kHz
		$2f_H$ mode; note 30	–	31.3	–	kHz
		$2f_H$ mode; HDTV = 1; note 30	–	33.7	–	kHz
Δf_{nom}	tolerance on free-running frequency	note 30	–	–	±1	%
$f_{h/cr}$	holding/catching range of PLL	$1f_H$ mode	±0.75	±0.8	±0.85	kHz
		$2f_H$ mode	±1.5	±1.6	±1.7	kHz
Δt_{line}	maximum line time difference per line	$1f_H$ mode	–2	–	+2	μs
		$2f_H$ mode	–1	–	+1	μs
f_{contr}	frequency control range in multi-sync mode	$1f_H$ mode	15	–	25	kHz
		$2f_H$ mode	30	–	50	kHz
Δf_{corr}	maximum speed of frequency correction in multi-sync mode		–	–	100	kHz/s
V_{HSEL}	voltage on pin HSEL	$1f_H$ mode	0	–	1	V
		$2f_H$ mode; pin must be left open circuit	4	5	5.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SECOND CONTROL LOOP; PIN 14						
$\Delta\varphi_i/\Delta\varphi_o$	control sensitivity (loop gain)	$\Delta t_i/\Delta t_0$	500	–	–	µs/µs
k_{cor}	correction factor k	note 31	–	0.5	–	
t_{contr}	control range from start of horizontal output to mid flyback	$1f_H$ mode; note 32	0	–	23.6	µs
		$2f_H$ mode; note 32	0	–	11.8	µs
$t_{H(shift)}$	horizontal shift range	$1f_H$ mode; 63 steps	–	±4.5	–	µs
		$2f_H$ mode; 63 steps	–	±2.25	–	µs
$\Delta\varphi$	control sensitivity for dynamic phase compensation	$1f_H$ mode	–	0.4	–	µs/V
		$2f_H$ mode	–	0.2	–	µs/V
$V_{i(DP)(comp)}$	input voltage range for dynamic phase compensation	pin 14; note 33	1.5	4	6.5	V
Z_i	input impedance	pin 14; note 33		100		kΩ
$t_{par(cor)(max)}$	maximum range of parallelogram correction	$1f_H$ mode; end of field; flyback width 11 µs; note 34	±0.48	±0.54	±0.60	µs
		$2f_H$ mode; end of field; flyback width 5.5 µs; note 34	±0.24	±0.27	±0.30	µs
$t_{bow(cor)(max)}$	maximum range of bow correction	$1f_H$ mode; end of field; flyback width 11 µs; note 34	±0.48	±0.54	±0.60	µs
		$2f_H$ mode; end of field; flyback width 5.5 µs; note 34	±0.24	±0.27	±0.30	µs
HORIZONTAL FLYBACK INPUT; PIN 13						
$V_{sw(HBLNK)}$	switching level for horizontal blanking		0.2	0.3	0.4	V
$V_{sw(p2)}$	switching level for phase detection		3.8	4.0	4.2	V
$V_{i(HFB)(max)}$	maximum input voltage		–	–	V_P	V
Z_i	input impedance		10	–	–	MΩ
HORIZONTAL OUTPUT; PIN 8, OPEN COLLECTOR; note 35						
V_{OL}	LOW-level output voltage	I_o = 10 mA	–	–	0.3	V
$I_{o(hor)}$	maximum allowed output current		–	–	10	mA
$V_{o(max)}$	maximum allowed output voltage		–	–	V_P	V
δ	duty factor	V_o = LOW (t_{on})	51.6	51.8	52.0	%
t_{on}	switch-on time of horizontal drive pulse	TV mode, HDTV = 0, ESS = 0	155	159	163	ms
t_{off}	switch-off time of horizontal drive pulse	TV mode, HDTV = 0, ESS = 0	48	50	52	ms
$t_{on(ess)}$	switch-on time for extended slow start	TV mode, HDTV = 0, ESS = 1	1150	1175	1200	ms

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Δt	jitter (σ)	$1f_H$ mode; note 36	–	1.4	–	ns
		$2f_H$ mode; note 36	–	1.0	–	ns
SANDCASTLE OUTPUT; PIN 9; note 37						
$V_{SCO(0)}$	zero level		0	0.5	1.0	V
I_{sink}	sink current		0.5	0.7	0.9	mA
$V_{o(SCO)}$	output voltage	during clamp pulse	4.2	4.5	4.8	V
		during blanking	2.3	2.5	2.7	V
I_{source}	source current		0.5	0.7	0.9	mA
$I_{i(grd)}$	guard pulse input current required to stop the blanking after a vertical blanking period	note 38	1.0	–	3.5	mA
$t_{W(1)}$	pulse width in $1f_H$ mode	clamp pulse, 22 LLC pulses	–	3.2	–	µs
		vertical blanking (50/60 Hz)	–	22/17	–	lines
$t_{W(2)}$	pulse width in $2f_H$ mode	clamp pulse, 22 LLC pulses	–	1.6	–	µs
		clamp pulse, HDTV = 1, HDCL = 1, 18 LLC; see Fig.11	–	1.22	–	µs
		vertical blanking; depends on VWAIT setting; see Fig.13	–		–	
$t_{d(bk-HD)}$	delay between start H_D pulse and start of clamp pulse	$1f_H$ mode, 37 LLC pulses	–	5.4	–	µs
		$2f_H$ mode, 37 LLC pulses	–	2.7	–	µs
		$2f_H$ mode, HDCL = 1, 14 LLC pulses, see Fig.11	–	0.94	–	µs
Vertical synchronization and geometry processing						
V_D INPUT SIGNAL; PIN 23						
V_{IL}	LOW-level of input voltage		–	–	0.8	V
V_{IH}	HIGH-level of input voltage		2.0	–	5.5	V
$I_{i(VD)}$	input current		–10	–	+10	µA
$t_{r(VD)}$	rise time		–	–	100	ns
$t_{f(VD)}$	fall time		–	–	100	ns
$t_{W(VD)}$	pulse width		0.5	–	63.5	lines
VERTICAL DIVIDER AND RAMP GENERATOR; PINS 15 AND 16; note 39						
N_h	number of lines per field (VGA mode is valid only for TDA9331H and TDA9332H)	$1f_H$ TV mode	244	–	511.5	lines
		$1f_H$ VGA mode	175	–	450	lines
		$2f_H$; $2f_V$; TV mode	244	–	511.5	lines
		$2f_H$; $1f_V$; TV mode	488	–	1023.5	lines
		$2f_H$ VGA mode	350	–	900	lines

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$N_{h(nom)}$	divider value when not locked (number of lines per field) (VGA mode is valid only for TDA9331H and TDA9332H)	$1f_H$ or $2f_H$; $2f_V$; TV mode; VFF = 0	–	312.5	–	lines
		$1f_H$ or $2f_H$; $2f_V$; TV mode; VFF = 1	–	262.5	–	lines
		$2f_H$; $1f_V$; TV mode; VFF = 0	–	625	–	lines
		$2f_H$; $1f_V$; TV mode; VFF = 1	–	525	–	lines
		$1f_H$; VGA mode	–	288	–	lines
		$2f_H$; VGA mode	–	576	–	lines
$V_{saw(p-p)}$	sawtooth amplitude (peak-to-peak value)	VS = 1FH; C = 100 nF; R = 39 kΩ	–	3.0	–	V
I_{dch}	discharge current		–	1.2	–	mA
$I_{ch(ext)(R)}$	charge current set by external resistor	R = 39 kΩ; VS = 1FH; SVF = 0	–	16	–	µA
		R = 39 kΩ; VS = 1FH; SVF = 1	–	32	–	µA
$Slope_{vert}$	vertical slope	control range (63 steps)	−20	–	+20	%
ΔI_{ch}	charge current increase	60/50 Hz or 120/100 Hz	18.0	19.0	20.0	%
V_{rampL}	LOW-voltage level of ramp		–	2.3	–	V
VERTICAL DRIVE OUTPUTS; PINS 1 AND 2						
$I_{o(ver)(p-p)}$	differential output current (peak-to-peak value)	VA = 1FH	0.88	0.95	1.02	mA
I_{CM}	common mode current		360	400	440	µA
$V_{o(VDO)}$	output voltage range		0	–	4.0	V
Lin_{vert}	vertical linearity	upper/lower ratio; note 40	0.99	1.01	1.03	
DE-INTERLACE						
D_{1stfld}	first field delay	DIP = 0; note 41	–	0.5H	–	
E-W WIDTH; note 42						
CR	control range	63 steps	100	–	65	%
$I_{o(eq)}$	equivalent output current	VGA = 0; note 42	0	–	700	µA
$V_{o(EW)}$	E-W output voltage range		1.0	–	8.0	V
$I_{o(EW)}$	E-W output current range		0	–	1200	µA
E-W PARABOLA/WIDTH						
CR	control range	63 steps	0	–	22	%
$I_{o(eq)}$	equivalent output current	E-W = 3FH	0	–	440	µA
E-W CORNER/PARABOLA						
CR	control range	63 steps	−43	–	0	%
$I_{o(eq)}$	equivalent output current	PW = 3FH; E-W = 3FH	−190	–	0	µA
E-W TRAPEZIUM						
CR	control range	63 steps	−5	–	+5	%
$I_{o(eq)}$	equivalent output current		−100	–	+100	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
E-W EHT TRACKING						
$V_{i(EHTIN)}$	input voltage		1.2	–	2.8	V
m_{scan}	scan modulation range		–7	–	+7	%
φ_{EW}	sensitivity	63 steps	0	–	9	%/V
VERTICAL AMPLITUDE						
CR	control range	63 steps; SC = 00H	80	–	120	%
$I_{o(eq)(diff)(p-p)}$	equivalent differential vertical drive output current (peak-to-peak value)	SC = 00H	760	–	1140	µA
VERTICAL SHIFT						
CR	control range	63 steps	–5	–	+5	%
$I_{o(eq)(diff)(p-p)}$	equivalent differential vertical drive output current (peak-to-peak value)		–50	–	+50	µA
S-CORRECTION						
CR	control range	63 steps	0	–	30	%
VERTICAL EHT TRACKING/OVERVOLTAGE PROTECTION						
V_i	input voltage		1.2	–	2.8	V
m_{scan}	scan modulation range		±4.5	±5	±5.5	%
φ_{vert}	vertical sensitivity		5.7	6.3	6.9	%/V
$I_{o(eq)(EW)}$	EW equivalent output current		+100	–	–100	µA
$V_{ov(det)}$	overvoltage detection level	note 43	3.7	3.9	4.1	V
VERTICAL ZOOM MODE (OUTPUT CURRENT VARIATION WITH RESPECT TO NOMINAL SCAN); note 44						
F_{zoom}	vertical zoom factor	63 steps	0.75	–	1.38	
F_{lim}	output current limiting and RGB blanking		1.01	1.05	1.08	
VERTICAL SCROLL; note 45						
CR	control range (percentage of nominal picture amplitude)	63 steps	–18	–	+19	%
VERTICAL WAIT; note 46						
$t_{d(scan)}$	delay of start vertical scan	23 steps	8	–	31	lines
FLASH DETECTION INPUT; PIN 5; note 43						
$V_{i(FLASH)}$	input voltage range		0	–	V_P	V
$V_{FLASH(det)}$	voltage detection level		–	2	–	V
$V_{det(hys)}$	detection level hysteresis		–	0.2	–	V
$t_{W(FLASH)}$	pulse width		200	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I²C-bus control inputs/outputs; pins 10 and 11						
V_{IL}	LOW-level input voltage		–	–	1.5	V
V_{IH}	HIGH-level input voltage		3.5	–	5.5	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	–	0	–	µA
I_{IH}	HIGH-level input current	V_{IH} = 5.5 V	–	0	–	µA
V_{OL}	LOW-level output voltage	SDA; I_{OL} = 6 mA	–	–	0.6	V
DAC OUTPUT; PIN 25; note 47						
$V_{o(min)}$	minimum output voltage		0.15	0.3	0.4	V
$V_{o(max)}$	maximum output voltage		3.7	4.0	4.3	
Z_o	output impedance	note 47	0.3	–	10	kΩ
I_o	output current		–	–	2	mA

Notes

1. The normal operation of the IC is guaranteed for a supply voltage between 7.2 and 8.8 V. When the supply voltage drops below the POR level, status bit POR is set and the horizontal output is switched off. When the supply voltage is between 7.2 V and the POR level, the horizontal frequency is kept in the specified holding range.
2. For the low power start-up mode, a voltage of 5 V has to be supplied to pin 22. The current that is required for this function is about 3.0 mA. After the start-up voltage is applied, the signal at the horizontal drive output will have nominal t_{off}, while t_{on} grows gradually from zero to about 30% of the nominal value, resulting in a line frequency of approximately 50 kHz (2fH) or 25 kHz (1fH). The start-up mode is continued as soon as the main supply voltage is switched on and the I²C-bus data has been received. After status bit POR has been read out, bits STB must be set to 1 within 24 ms, to continue slow start. If bits STB are not sent within 24 ms, the horizontal output will be automatically switched off via slow stop. It is also possible to first set bits STB to 1, before reading bit POR. Start-up of the horizontal output will then continue 24 ms after bit POR is read. When the main supply is present, the 5 V supply on pin 22 can be removed. If low power start-up is not used, pin 22 should be connected to ground. More information can be found in the application report.
3. The RGB to YUV matrix on the RGB-1 input is the inverse of the YUV to RGB matrix for PAL. For a one-on-one transfer of all three channels from the RGB-1 input to the RGB output, the PAL colour difference matrix should be selected (MAT = 0, MUS = 0).
4. The colorimetry that is used for high definition ATSC signals is described in document ANSI/SMPTE 274M-1995. The formula to compute the luminance signal from the RGB primary components differs from the formula that is used for the PAL system. The consequence is that a different matrix is needed to calculate the internal G – Y signal from the R – Y and B – Y signals, see the formulas below:

   $Y = 0.2126R + 0.7152G + 0.0722B$

   $R - Y = 0.7874R - 0.7152G - 0.0722B$ (1.575 maximum amplitude)

   $B - Y = -0.2126R - 0.7152G + 0.9278B$ (1.856 maximum amplitude)

   The G – Y signal can be derived from the formula for Y:

   $G - Y = -0.2973(R - Y) - 0.1010(B - Y)$

ATSC signals are transmitted as YP_BP_R signals. The colour-difference components P_B and P_R are amplitude corrected versions of B – Y and R – Y:

$$P_B = \frac{0.5(B-Y)}{1-0.0722} = \frac{(B-Y)}{1.856}$$

$$P_R = \frac{0.5(R-Y)}{1-0.2126} = \frac{(R-Y)}{1.575}$$

Note that the "YUV" input of the TDA933xH is actually a Y, –(R – Y) and –(B – Y) input. When the TV set has an input for a YPBPR signal with amplitudes of 0.7 V for all three components, the signals should be amplified to Y, –(B – Y) and –(R – Y) signals as follows:

$$Y_{in,IC} = \frac{1}{0.7} \times Y_{in,TV} = 1.43 Y_{in,TV}$$

$$-(B-Y)_{in,IC} = \frac{1.856}{0.7} \times P_{Bin,TV} = -2.65 P_{B\,in,TV}$$

$$-(R-Y)_{in,IC} = \frac{1.575}{0.7} \times P_{Rin,TV} = -2.25 P_{R\,in,TV}$$

5. This parameter is not tested during production but is guaranteed by the design and qualified by means of matrix batches which are made in the pilot production period.
6. The inputs for RGB-1 and RGB-2 insertion (pins 33 and 38) both supply a small source current to the pins. If the pins are left open circuit, the input voltage will rise above the insertion switching level.
7. This parameter is measured at nominal settings of the various controls.
8. The switching of the OSD (RGB-2) input has two modes, which can be selected via the I²C-bus:
   a) Fast switching between the OSD signal and the internal RGB signals.
   b) Blending (fading) function between the OSD signal and the internal RGB signals. The blending control curve is given in Fig.4. The blender input is optimized for the blender output of the SAA5800 (ArtistIC).
9. The saturation, contrast and brightness controls are active on the YUV signals and on the first RGB input signals. Nominal contrast is specified with the contrast DAC in position 32 DEC, nominal saturation with the saturation DAC in position 22 DEC. The second RGB input (which is intended to be used for OSD and teletext display) can only be controlled on brightness.
10. For video signals with a black level that deviates from the back-porch blanking level, the signal is 'stretched' to the blanking level. The amount of correction depends on the IRE value of the signal (see Fig.8). The black level is detected by means of an internal capacitor. The black level stretcher can be switched on and off via bit BKS in the I²C-bus. The values given in the specification are valid only when the luminance input signal has an amplitude of 1 V (b-w).
11. Because of the 2-point black current stabilization circuit, both the black level and the amplitude of the RGB output signals depend on the drive characteristic of the picture tube. The system checks whether the returning measuring currents meet the requirement and adapts the output level and gain of the circuit as necessary. Therefore, the typical values of the black level and amplitude at the output are just given as an indication for the design of the RGB output stage.
    a) The 2-point black level system adapts the drive voltage for each cathode such that the two measuring currents have the right value. The consequence is that a change in the gain of the output stage will be compensated by a gain change of the RGB control circuit. Because different picture tubes may require different drive voltage amplitudes, the ratio between the output signal amplitude and the inserted measuring pulses can be adapted via the I²C-bus. This is indicated in the parameter 'Adjustment range of RGB drive levels'.
    b) Because of the dependence of the output signal amplitude on the application, the peak-white and soft-clipping limiting levels have been related to the input signal amplitude.

c) The signal amplitude at the RGB outputs of the TDA933xH depends on the gain of the RGB amplifiers. The gain of the RGB amplifiers should be 35 to get the nominal signal amplitude of 2 V (b-w) at the RGB outputs for a cathode drive level of 70 V (b-w) and the nominal setting of the drive level bits (CL_{3210} = 1000, see Table 15).

12. The bandwidth of the video channels depends on the capacitive load at the RGB outputs. For $2f_H$ or VGA applications, external (PNP) emitter followers on the RGB outputs of the TDA933xH are required, to avoid reduction of the bandwidth by the capacitance of the wiring between the TDA933xH and the RGB power amplifiers on the picture tube panel. If emitter followers are used, it should be possible to obtain the bandwidth figures that are mentioned for 10 pF load capacitance.
13. The timing of the horizontal blanking pulse on the RGB outputs is illustrated in Fig.10.
    a) The start of the blanking pulse is determined by an internal counter blanking that starts 40 LLC (line locked clock) pulses before the centre of the horizontal flyback pulse. This is 5.8 μs for 1fH and 2.9 μs for 2fH TV mode. The end of the blanking is determined by the trailing edge of the flyback pulse. If required, the start of the counter blanking can be adjusted in 15 steps with bus bits LBL3 to LBL0. This can be useful when HDTV or VGA signals are applied to the IC.
    b) When the reproduction of 4 : 3 pictures on a 16 : 9 picture tube is realized by reducing the horizontal scan amplitude, the edges of the picture may be slightly disturbed. This effect can be prevented by adding an additional blanking pulse to the RGB signals. This blanking pulse is derived from the horizontal oscillator and is directly related to the incoming H_D pulse (independent of the flyback pulse). The additional blanking pulse overlaps the normal blanking signal by approximately 1 μs ($1f_H$) or 0.5 μs ($2f_H$) on both sides. This wide blanking is activated by bit HBL. The phase of this blanking can be controlled in 15 steps by bits HB3 to HB0.
14. When a YUV or RGB signal is applied to the IC and no separate horizontal or vertical timing pulses are available, an external sync separator circuit is needed. The TDA933xH has an edge triggered phase detector circuit on the H_D input that uses the start of the H_D pulse as timing reference. To avoid horizontal phase disturbances during the vertical blanking period, it is important that the sync separator does not generate extra horizontal sync pulses during the vertical sync pulse on the video signal.
15. Start-up behaviour of the CCC loop. After the horizontal output is released via bits STB, the RGB outputs are blanked and the CCC loop is activated. Because the picture tube is cold, the measured cathode currents are too small, and both gain and offset are set at the maximum value so that the CCC loop gets out of range and status bit BCF is set to 1. Once the picture tube is warm, the loop comes within range and the set signal for bit BCF is removed. Status bit BCF is set if the voltage of at least one of the cut-off measurement lines at the RGB outputs is lower than 1.5 V or higher than 3.5 V. The RGB outputs are unblanked as soon as bit BCF changes from 1 to 0. To avoid a bright picture after switch-on with a warm picture tube, reset of bit BCF is disabled for 0.5 s after switch-on of the horizontal output. If required, the blanking period of the RGB outputs can be increased by forcing the blanking level at the RGB outputs via RBL = 1. When status bit BCF changes from 1 to 0, bit RBL can be set to 0 after a certain waiting period.
16. Voltage V_{g2} of the picture tube can be aligned with the help of status bits WBC and HBC. Bit WBC becomes 1 if the lowest of the three RGB output voltages during the cut-off measurement lines is within the alignment window of ±0.1 V around 2.5 V. Bit HBC is 0 if the lowest cut-off level is below 2.6 V, and 1 if this level is above 2.6 V.
    a) Voltage V_{g2} should be aligned such that bit WBC becomes 1. If bit WBC is 0, bit HBC indicates in which direction voltage V_{g2} should be adjusted. If bit HBC = 0, the DC level at the RGB outputs of the IC is too low and voltage V_{g2} should be adjusted lower until bit WBC becomes 1. If HBC = 1, the DC level is too high and voltage V_{g2} should be adjusted higher until bit WBC becomes 1.
    b) It should be noted that bit WBC is only meant for factory alignment of voltage V_{g2}. If the value of bit WBC depends on the video content, this is not a problem. Correct operation of the black current loop is guaranteed as long as status bit BCF = 0, meaning that the DC level of the measurement lines at the RGB outputs of the IC is between 1.5 and 3.5 V.
17. Signal-to-noise ratio (S/N) is specified as a peak-to-peak signal with respect to RMS noise (bandwidth 10 MHz).
18. This is a current input. When the black current feedback loop is closed (only during measurement lines or during fixed beam current switch off), the voltage at this pin is clamped at 3.3 V. When the loop is open circuit, the input is not

clamped and the maximum sink current is approximately 100 μA. The voltage on the pin must not exceed the supply voltage.

19. The control circuit contains a PWL circuit and a soft clipper.
    a) The detection level of the PWL can be adjusted via the I²C-bus in a control range between 0.65 and 1.0 V (b-w). This amplitude is related to the Y input signal, typical amplitude 1 V (b-w), at maximum contrast setting. The detector measures the amplitude of the RGB signals after the contrast control. The output signal of the PWL detector is filtered by an external capacitor, so that short transients in the video signal do not activate the limiting action. Because the capacitor is externally available at pin 34, the set maker can adapt the filter time constant as required. The contrast reduction of the PWL is obtained by discharging the external capacitor at the beam current limiting input (pin 43). To avoid the PWL circuit from reducing the contrast of the main picture when the amplitude of the inserted RGB2 signal is too high, the output current of the PWL detector is disabled when the fast blanking input (pin 38) is high. In blending mode (OBL = 1), the PWL detector is disabled when the blending voltage is above the 50% insertion level. The soft clipper circuit will still limit the peak voltage at the RGB outputs.
    b) In addition to the PWL circuit, the IC contains a soft clipper function which limits short transients that exceed the PWL. The difference between the PWL and the soft clipping level can be adjusted between 0 and 10% in three steps via the I²C-bus, with bus bits SC1 and SC0 (soft clipping level equal or higher than the PWL). It is also possible to switch off the soft clipping function.
20. The above-mentioned output amplitude range at which the PWL detector is activated is valid for nominal settings of the white point controls, and when the CCC loop is switched off or set to 1-point stabilization mode. In 2-point stabilization mode, the mentioned range is only valid when the gain of the RGB output stages is dimensioned such that the RGB output amplitudes are 2 V (b-w) for nominal contrast setting, see also note 11.
21. The soft clipper gain reduction is measured by applying a sawtooth signal with rising slope and 1 V (b-w) at the luminance input. To prevent the beam current limiter from operating, a DC voltage of 3.5 V must be applied to pin 43. The contrast is set at the maximum value, the PWL at the minimum value, and the soft clipping level is set at 0% above the PWL (SC_{10} = 00). The tangents of the sawtooth waveform at one of the RGB outputs is now determined at the beginning and end of the sawtooth. The soft clipper gain reduction is defined as the ratio of the slopes of the tangents for black and white, see Fig.9.
22. When the blue stretch function is activated (via I²C-bus bit BLS), the gain of the red and green channels is reduced for input signals that exceed a value of 80% of the nominal amplitude. The result is that the white point is shifted to a higher colour temperature.
23. Switch-off behaviour of TDA933xH. For applications with an EHT generator without bleeder resistor, the picture tube capacitance can be discharged with a fixed beam current when the set is switched off. The magnitude of the discharge current is controlled via the black current loop. The fixed beam current mode can be activated with bit FBC. With the fixed beam current option activated, it is still possible to have a black screen during switch-off. This is realized by placing the vertical deflection in the overscan position. This mode is activated by bit OSO. There are two possible situations for switch-off (see notes 24 and 25).
24. The set is switched to standby via the I²C-bus. In this situation, the procedure is as follows:
    a) Vertical scan is completed.
    b) Vertical flyback is completed.
    c) Slow stop of the horizontal output is started, by gradually reducing the ‘on-time’ at the horizontal output from nominal to zero.
    d) At the same moment, the fixed beam current is forced via the black current loop (if FBC = 1).
    e) If OSO = 1, the vertical deflection stays in overscan position; if OSO = 0, the vertical deflection keeps running.
    f) The slow stop time is approximately 50 ms, the fixed beam current flows for 18.6 ms or 25 ms, depending on the value of bit TFBC, see Fig.15.
25. The set is switched off via the mains power switch. When the mains supply is switched off, the supply voltage of the line deflection circuit of the TV set will decrease. A detection circuit must be made that monitors this supply voltage.

When the supply voltage suddenly decreases, pin FBCSO (fixed beam current switch-off) of the TDA933xH must be pulled high. In this situation, the procedure is as follows:

a) Vertical scan is completed.

b) Vertical flyback is completed.

c) The fixed beam current is forced via the black current loop (if FBC = 1). The horizontal output keeps running. As the supply voltage for the line transformer decreases, the EHT voltage will also decrease.

d) If OSO = 1, the vertical deflection stays in overscan position; if OSO = 0, the vertical deflection keeps running.

e) When the supply voltage of the TDA933xH drops below the POR level, horizontal output and fixed beam current are stopped.

26. The discharge current for the picture tube can be increased with an external current division circuit on the black current input (pin 44). The current division should only be active for high cathode currents, so that the operation of the black current stabilization loop is not affected. When the feedback current supplied to pin 44 is less than 1mA, the DC level at the RGB outputs will go to the maximum value of 6.0 V (2-point black current stabilization) or 5.6 V (1-point or no black current stabilization).

27. A stable switching of the H_D input is realized by using a Schmitt trigger input.

28. The simplified circuit diagram of the oscillator is given in Fig.3. To ensure that the oscillator will start-up, the ceramic resonator must fulfil the following condition: $C_L^2 \times R_i \leq 1.1 \times 10^{-19}$.

    Example: When the resonator is loaded with 60 pF (this is a typical value for a 12 MHz resonator), the series resistance of the resonator must be smaller than 30 Ω.
    A suitable ceramic resonator for use with the TDA933xH is the Murata CST12.0MT, which has built-in load capacitances C_a and C_b. For higher accuracy, it is also possible to use a quartz crystal, which is even less critical with respect to start-up because of its lower load capacitance.

29. Pin HSEL must be connected to ground in a $1f_H$ application; it must be left open circuit for a $2f_H$ application. The TDA9331H and TDA9332H can be switched to a multi-sync mode, in which the horizontal frequency can vary between 15 and 25 kHz ($1f_H$ mode) or 30 and 50 kHz ($2f_H$ mode).

30. The indicated tolerance on the free-running frequency is only valid when an accurate reference frequency (obtained with an accurate 12 MHz crystal) is used. The tolerance of the reference resonator must be added to obtain the real tolerance on the free-running frequency.

31. The correction factor k of the phase-2 loop is defined as the amount of correction per line period of a phase error between the horizontal flyback pulse and the internal phase-2 reference pulse. When k = 0.5, the phase error between the flyback pulse and the internal reference is halved each line period.

32. The control range of the second control loop depends on the line frequency. The maximum control range from the rising edge of HOUT to the centre of the flyback pulse is always 37% of one line period, for the centre position of the dynamic phase compensation (4.0 V at pin 14).

33. The dynamic phase compensation input (pin 14) is connected to an internal reference voltage of 4.0 V via a resistor of 100 kΩ. If dynamic phase compensation is not used, this pin should be decoupled to ground (pin 19) via a capacitor of 100 nF.

34. The range of parallelogram and bow correction is proportional to the width of the horizontal flyback pulse. For zero correction, use DAC setting 7 DEC or 0111 (bin). The effect of the corrections is shown in Fig.16.

35. For safe operation of the horizontal output transistor and to obtain a controlled switch-on time of the EHT, the horizontal drive starts up in a slow start mode. The horizontal drive starts with a very short ‘on-time’ of the horizontal output transistor (line locked clock pulse, i.e. 72 ns), the ‘off-time’ of the transistor is identical to the ‘off-time’ in normal operation. The starting frequency during switch-on is therefore approximately twice the normal value. The t_{on} is slowly increased to the nominal value in approximately 160 ms (see Fig.15). When the nominal frequency is reached, the PLL is closed such that only very small phase corrections are necessary. This ensures safe operation of the output stage.

a) For picture tubes with Dynamic Astigmatic Focusing (DAF) guns, the rise of the EHT voltage between 75 and 100% is preferred to be even slower than the rise time from 0 to 75%. This can be realized by activating bit ESS, at which the total switch-on time of the horizontal output pulse is approximately 1175 ms.

b) During switch-off, the slow-stop function is active. This is realized by decreasing the t_{on} of the output transistor complementary to the start-up behaviour. The switch-off time is approximately 50 ms. The slow-stop procedure is synchronized to the start of the first new vertical field after reception of the switch-off command. During the slow-stop period, the fixed beam current switch-off can be activated (see also note 23). This current is active during a part of the slow stop period, see Fig.15.

c) The horizontal output is gated with the flyback pulse so that the horizontal output transistor cannot be switched on during the flyback pulse. This protection is not active during the switch-on or switch-off period.

36. This parameter is not tested during production and is just given as application information for the designer of the television receiver.

37. The rise and fall times of the blanking pulse and clamping pulse at the sandcastle output (pin 9) depend on the capacitive load. The value of the source current during the rising edge or sink current during the falling edge is 0.7 mA (typical value).

38. The vertical guard pulse from the vertical output stage should fall within the vertical blanking period (see Figs 12 and 13) and should have a width of at least one line period. For the detection of a missing pulse, a guard current value of 1 mA during normal operation is sufficient. If the RGB outputs must also be blanked if the guard pulse lasts longer than the vertical blanking period, the guard current must have a value between 2.6 mA and 3.5 mA.

39. Switching between the $1f_V$ or the $2f_V$ mode is realized via bit SVF.

40. The vertical linearity is measured on the differential output current at the vertical drive output (pins 1 and 2) for zero S-correction. The linearity is defined as the ratio of the upper and lower half amplitudes at the vertical output. The upper amplitude is measured between lines 27 and 167, the lower amplitude between lines 167 and 307 for a 50 Hz video signal.

41. The field detection mechanism is explained in Fig.17.

a) The incoming V_D pulse is synchronized with the internal clock signal CK2H that is locked to the incoming H_D pulse. If the synchronized V_D pulse of a field coincides with the internally generated horizontal blanking signal HBLNK, then this is field 1. If the synchronized V_D pulse does not coincide with HBLNK, then this is field 2. Signals CK2H and HBLNK are both output signals of the horizontal divider circuit that is part of the line-locked clock generator. A reliable field detection is important for correct interlacing and de-interlacing and for the correct timing of the measurement lines of the black current loop. For the best noise margin, the edges of the V_D pulse should be on approximately $\frac{1}{4}$ and $\frac{3}{4}$ of the line, referred to the rising edges of the H_D input signal.

b) If bus bit VSR = 0, the end of the V_D pulse is used as reference for both field detection and start of vertical scan. If VSR = 1, the starting edge is used.

42. Output range percentages mentioned for E-W control parameters are based on the assumption that the E-W modulator is dimensioned such that 400 μA variation in E-W output current of the IC is equivalent to 20% variation in picture width. In VGA mode, the E-W output current is proportional to the applied line frequency.

43. The IC has protection inputs for flash protection and overvoltage protection.

a) The flash protection input is used to switch the horizontal drive output off immediately if a picture tube flashover occurs, to protect the line output transistor. An external flash detection circuit is needed. When the flash input is pulled HIGH, the horizontal output is switched off and status bit FLS is set. When the input turns LOW again, the horizontal output is switched on immediately without I²C-bus intervention via the slow start procedure.

b) The overvoltage (X-ray) protection is combined with the EHT compensation input. When this protection is activated, the horizontal drive can be directly switched off (via the slow stop procedure). It is also possible to continue the horizontal drive and only set status bit XPR in output byte 01 of the I²C-bus. The choice between the two modes of operation is made via bit PRD.

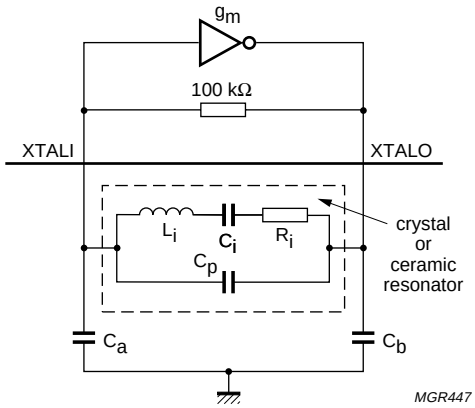
44. The ICs have a zoom adjustment possibility for the horizontal and vertical deflection. For this reason, an extra DAC is included in the vertical amplitude control, which controls the vertical scan amplitude between 0.75 and 1.38 of the

nominal scan. At an amplitude of 1.05 times the nominal scan, the output current is limited and the blanking of the RGB outputs is activated, see Fig.14. In addition to the variation of the vertical amplitude, the picture can be vertically shifted on the screen via the 'scroll' function. The nominal scan height must be adjusted at a position of 19H (25 DEC) of the vertical 'zoom' DAC and 1FH (31 DEC) for the vertical 'scroll' DAC.

45. The vertical scroll function is active only in the expand mode of the vertical zoom, i.e. at a DAC position larger than 10H (16 DEC).
46. With the vertical wait function, the start of the vertical scan can be delayed with respect to the incoming vertical sync pulse. The operation is different for the various scan modes, see Table 54 and Figs 12 and 13. The minimum value for the vertical wait is 8 line periods. If the setting is lower than 8, the wait period will remain 8 line periods.
47. In the TDA9330H and TDA9332H, the DAC output is I²C-bus controlled. In the TDA9331H, the DAC output voltage is proportional to the centre frequency of the line-oscillator. In TV mode, the output voltage will always be at the minimum value. In VGA mode, the output is at the minimum value for the lowest centre frequency (32 kHz) and at the maximum value for the highest centre frequency (48 kHz). The output impedance of the DAC output depends on the output voltage. The output consists of an emitter follower with an internal resistor of 50 kΩ to ground.

Table 54 Operation of the vertical wait function

MODE	START OF VERTICAL SCAN
$1f_H$; TV mode	fixed; see Fig.12
$2f_H$; TV mode; VSR = 0	end of V_D plus vertical wait setting
$2f_H$; TV mode; VSR = 1	start of V_D plus vertical wait setting
$1f_H$; multi sync mode	start of V_D plus vertical wait setting
$2f_H$; multi sync mode	start of V_D plus vertical wait setting



$$f_{osc} = \frac{1}{2\pi\sqrt{L_i \times \frac{C_i \times C_L}{C_i + C_L}}}$$

$$C_L = C_p + \frac{C_a \times C_b}{C_a + C_b}$$

Requirement for start-up:
$C_L^2 \times R_i \leq 1.1 \times 10^{-19}$

Fig.3 Simplified diagram of crystal oscillator.

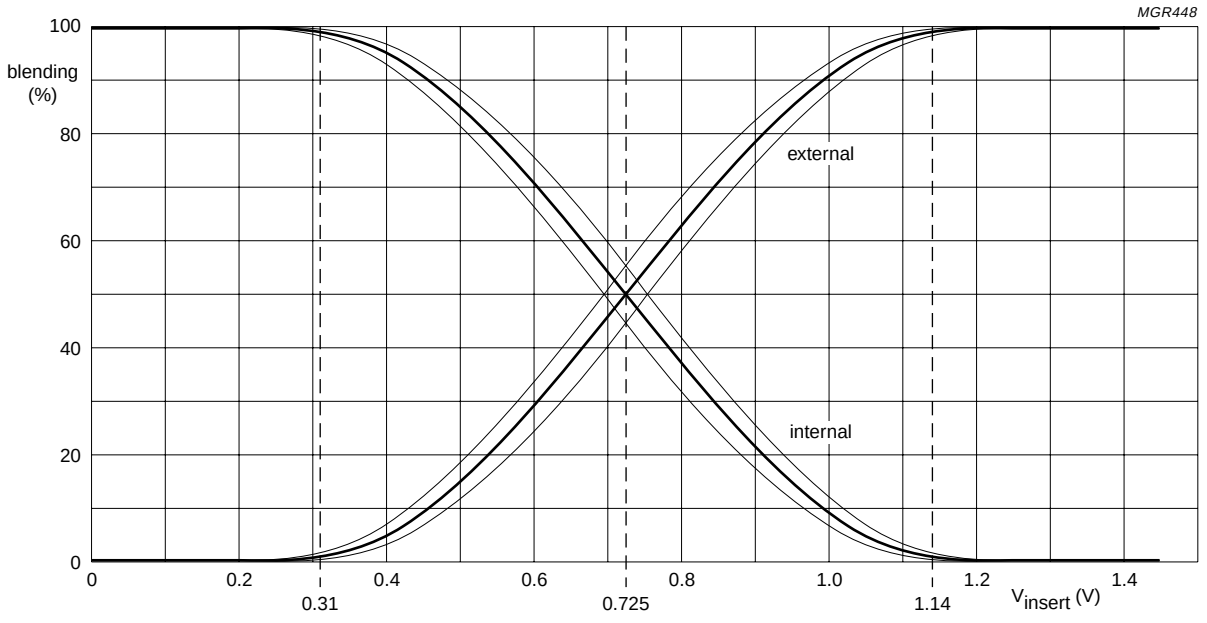


Fig.4 Blending characteristic (typical curve and minimum/maximum limits).

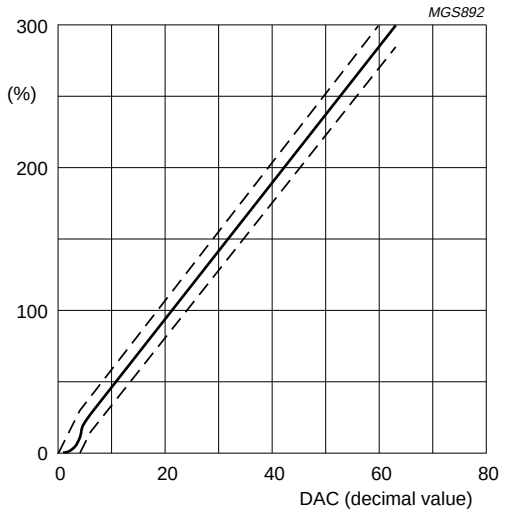


Fig.5 Saturation control curve.

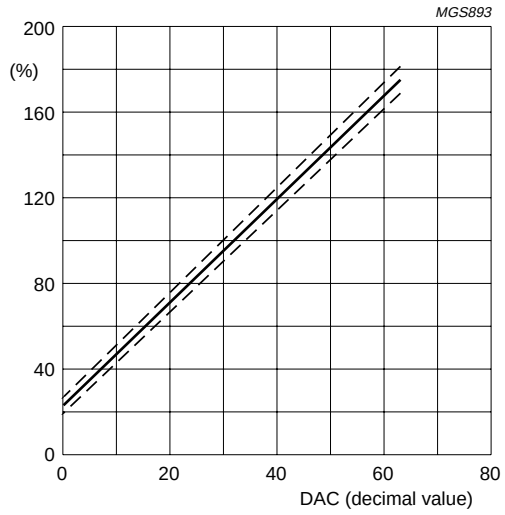
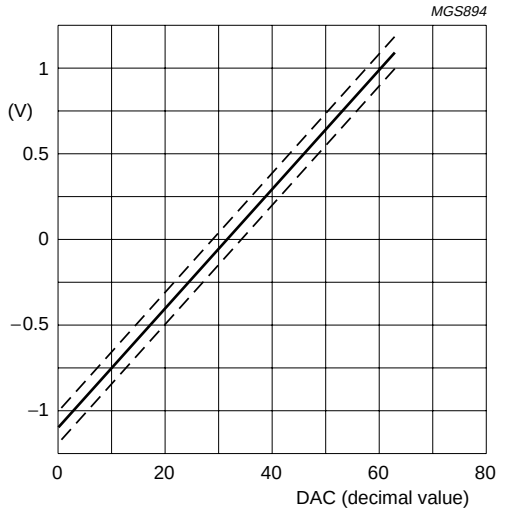
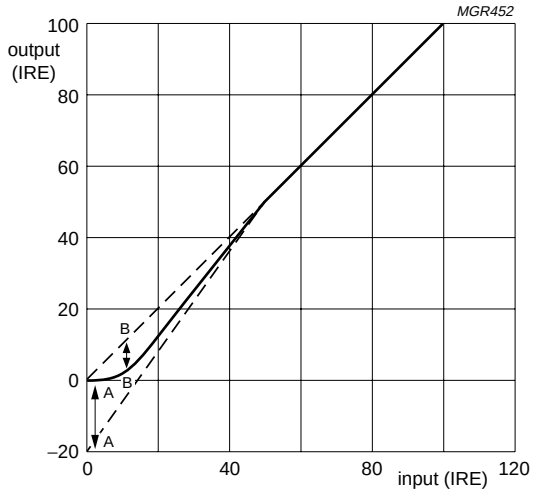


Fig.6 Contrast control curve.



Conditions: settings for cathode drive and white point nominal; gain of RGB amplifiers such that the amplitude at the RGB outputs is 2 V (b-w); relative to cutoff level.

Fig.7 Brightness control curve.



A-to-A: maximum black level shift.
B-to-B: level shift at 15% of peak white.

Fig.8 I/O relation of black level stretch circuit.

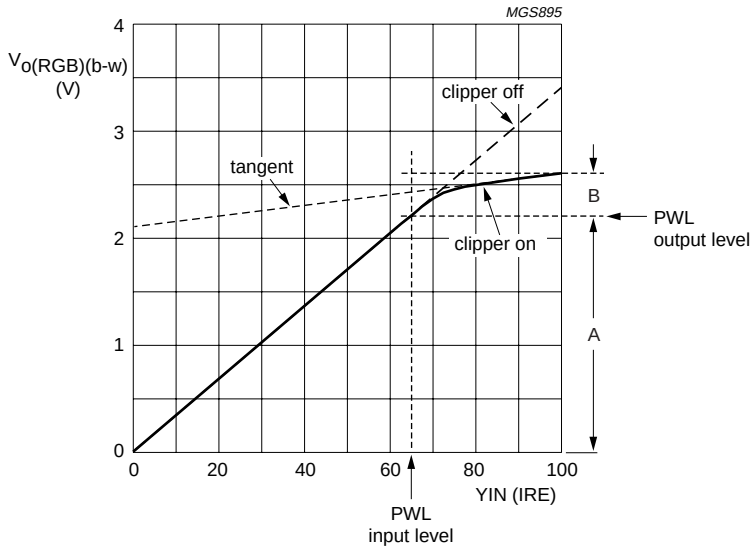
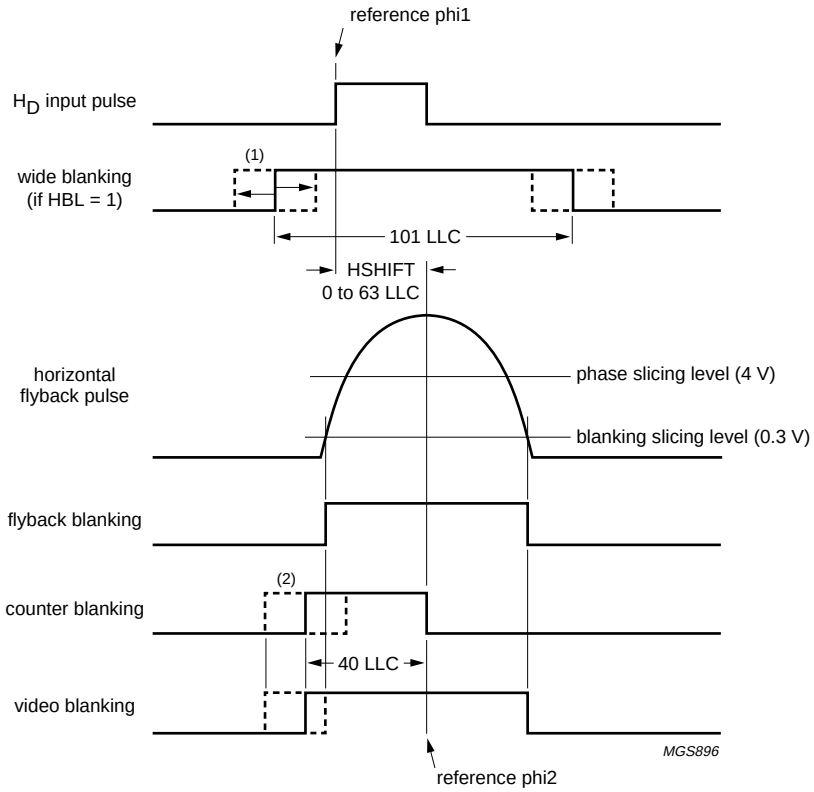
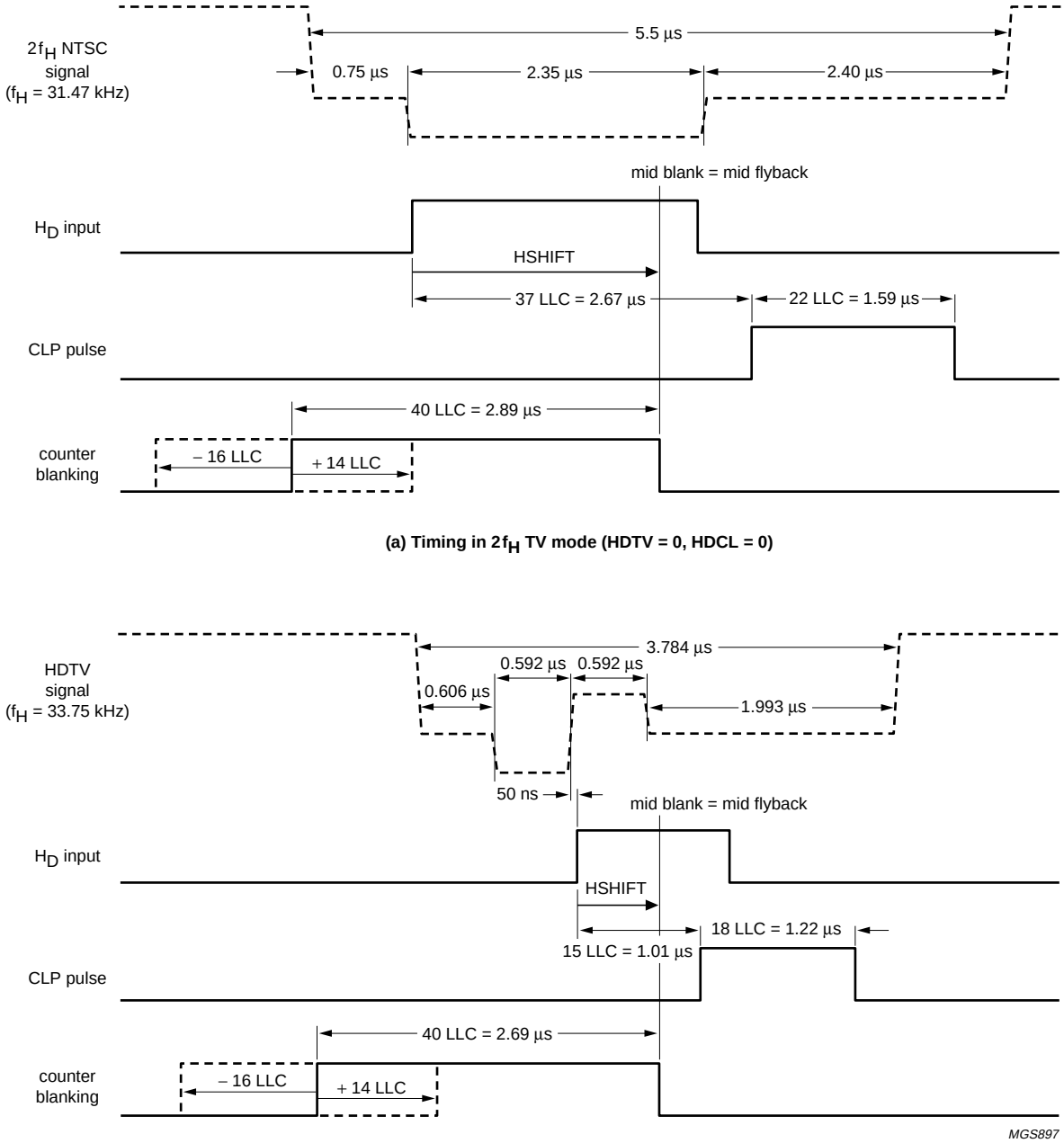


Fig.9 Soft clipper characteristic.



1) Position of wide blanking can be adjusted with bus bits HB3 to HB0.
2) Start of line blanking can be adjusted with bus bits LBL3 to LBL0.

Fig.10 Timing of horizontal blanking (1 line period is 440 LLC pulses).



(a) Timing in $2f_H$ TV mode (HDTV = 0, HDCL = 0)

(b) Timing in HDTV mode (HDTV = 1, HDCL = 1)

Video signals are shown as illustration only. All horizontal timing signals in the IC are solely related to the start of the H_D pulse that is applied to the IC.

All horizontal timing signals are generated with the help of the internal line locked clock (LLC). One line period is always divided into 440 line locked clock pulses. Time periods depicted in the figure are only valid for line frequencies mentioned.

Fig.11 Timing of clamp pulse and line blanking in $2f_H$ TV mode and HDTV mode.

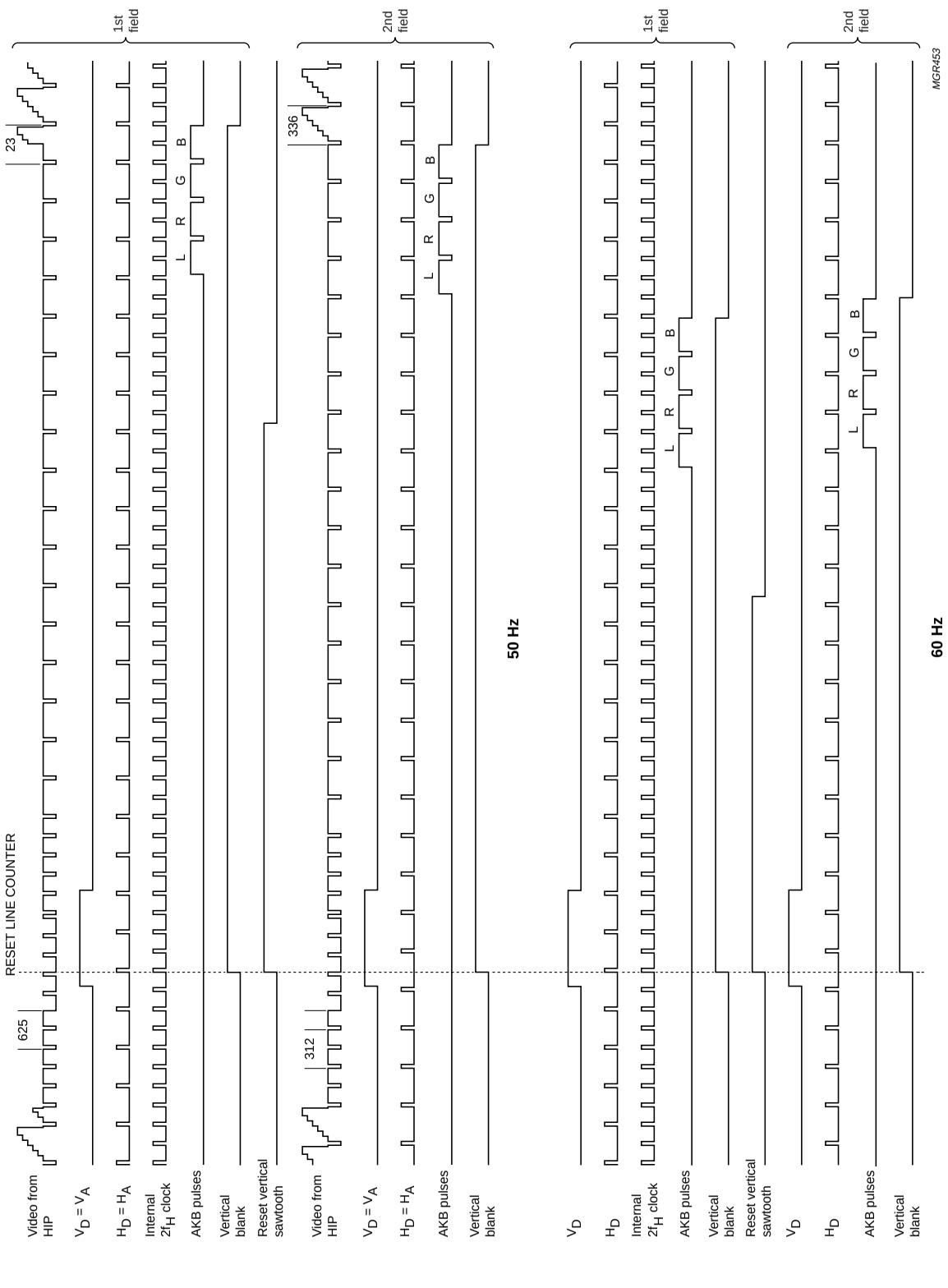


Fig.12 Vertical timing pulses for $1f_H$ TV mode.

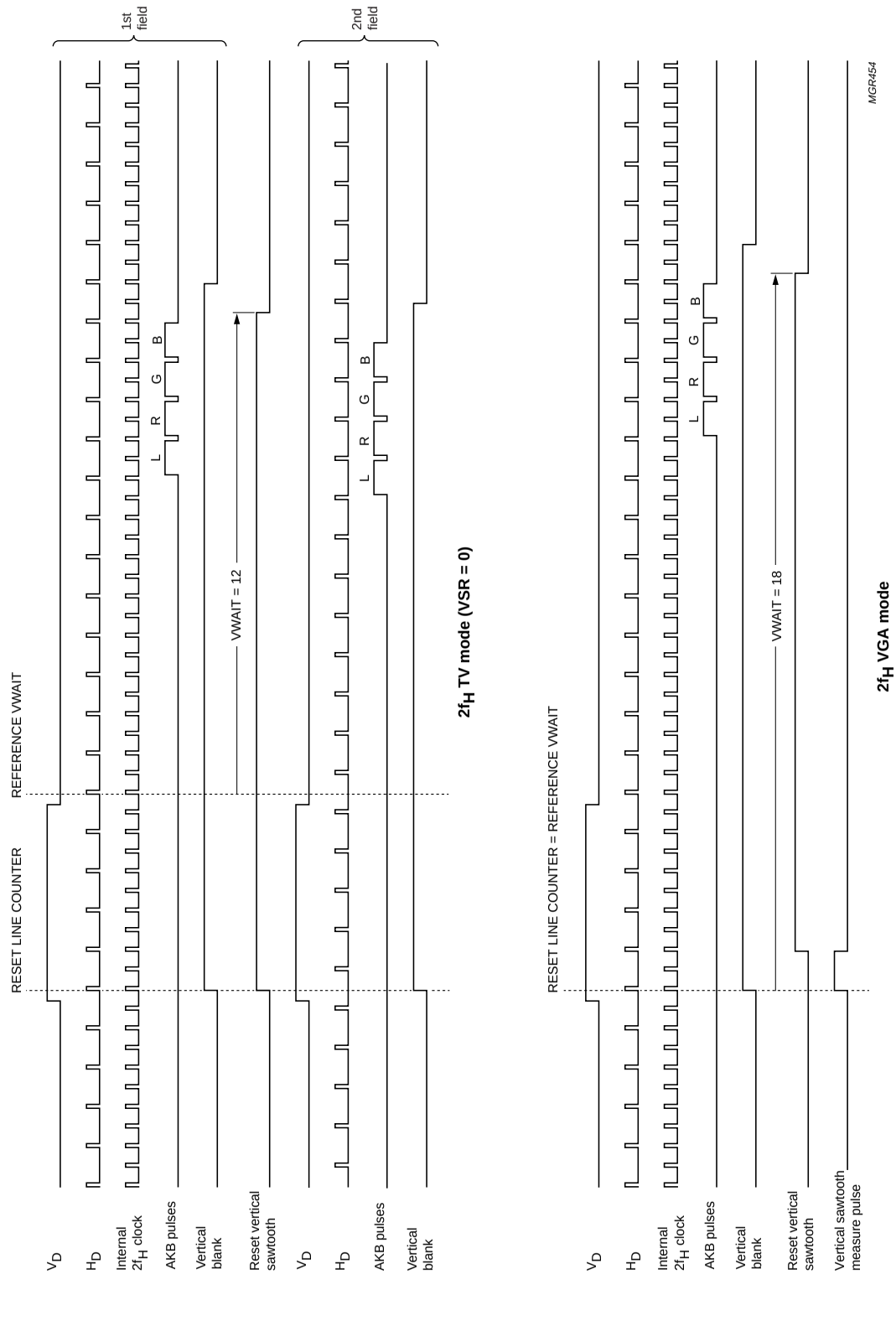


Fig.13 Vertical timing pulses for $2f_H$ TV mode and VGA mode.

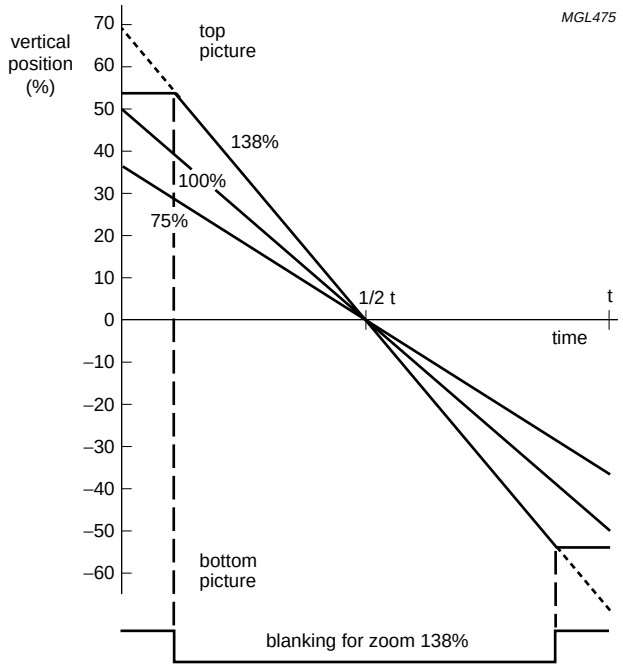


Fig.14 Vertical drive waveform and blanking pulse for different zoom factors.

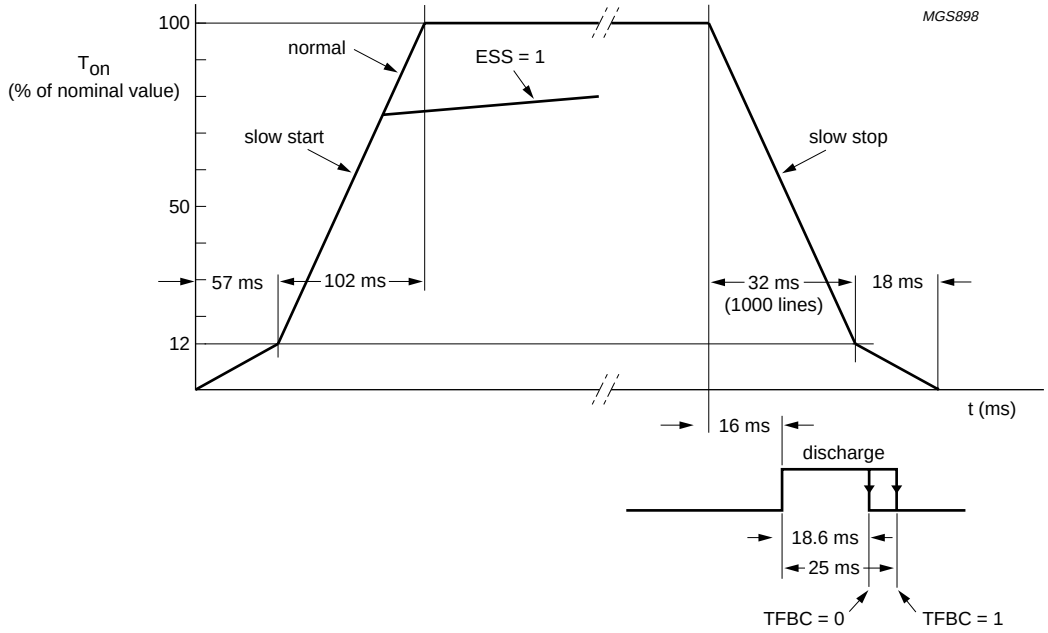
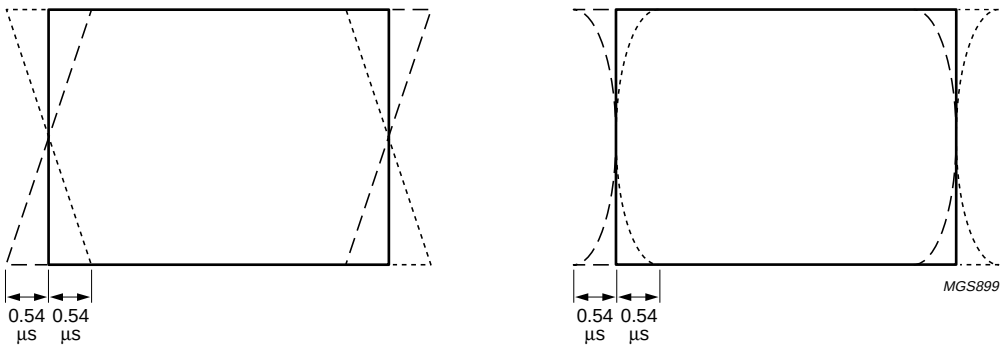
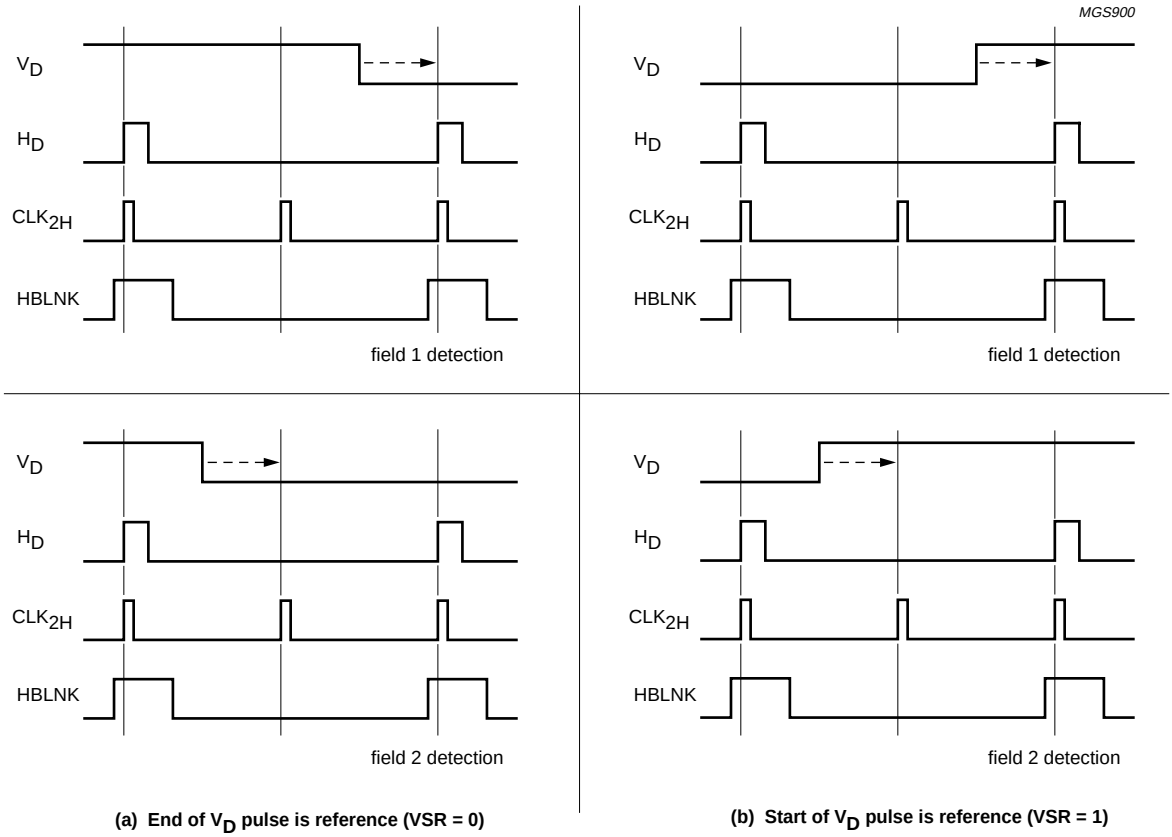


Fig.15 Slow start behaviour of horizontal output, and slow stop behaviour and timing of picture tube discharge pulse when IC is switched to standby via I²C-bus.



(a) Parallelogram correction. **(b) Bow correction.**

Fig.16 Horizontal parallelogram and bow correction (figures for $1f_H$ mode).



(a) End of V_D pulse is reference (VSR = 0)

(b) Start of V_D pulse is reference (VSR = 1)

See also Chapter “Characteristics”; note 41.

Fig.17 Field detection mechanism.

TEST AND APPLICATION INFORMATION

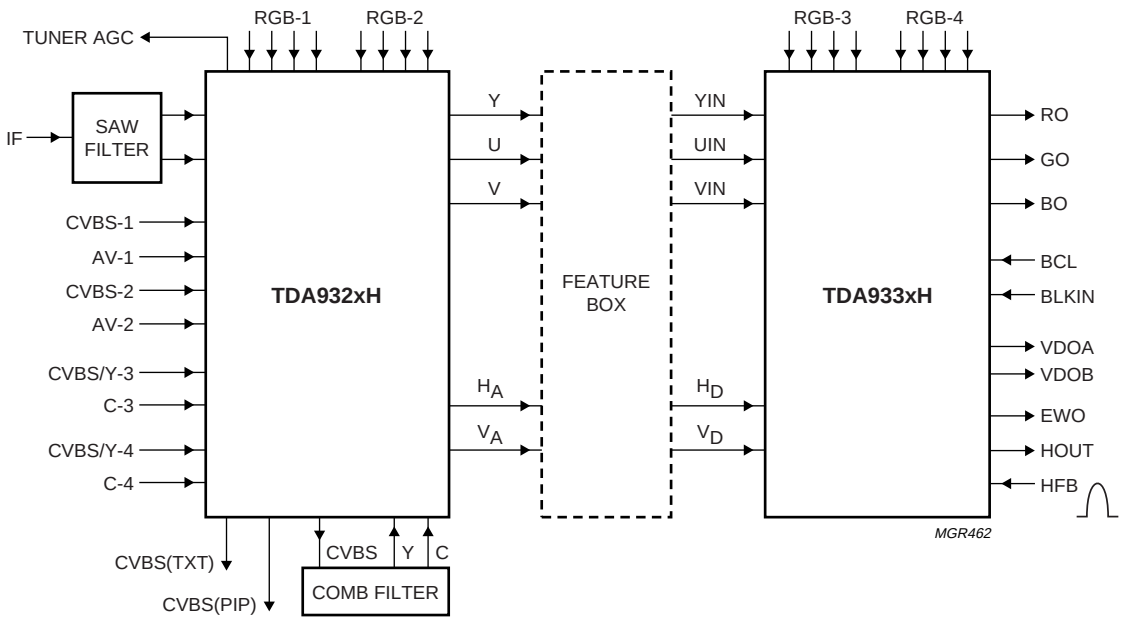
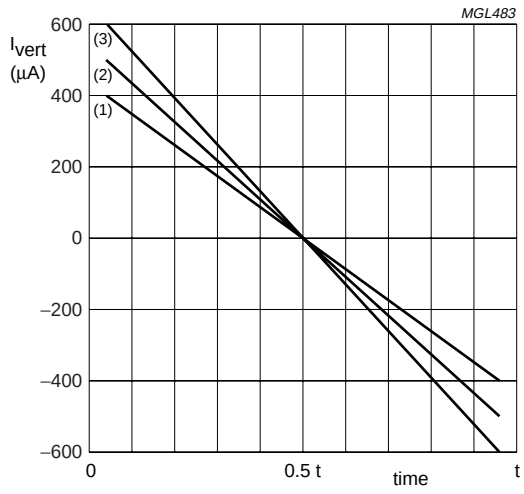
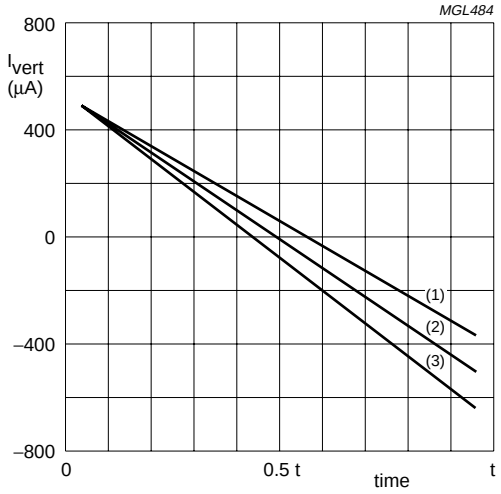


Fig.18 Application diagram.



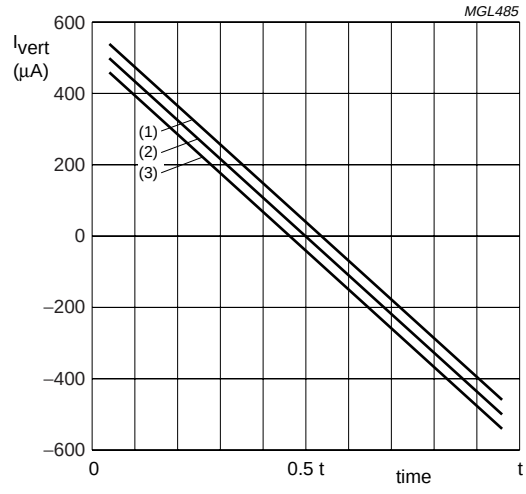
VSH = 31; SC = 0; $I_{VERT} = I_{2(VDOB)} - I_{1(VDOA)}$.
(1) VA = 0.
(2) VA = 31.
(3) VA = 63.

Fig.19 Control range of vertical amplitude.



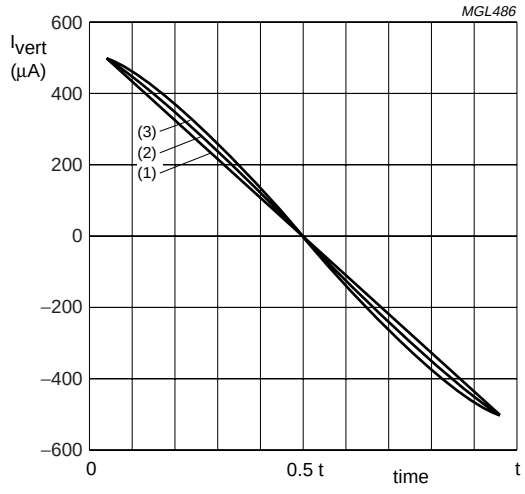
VA = 31; VHS = 31; SC = 0.
(1) VS = 0.
(2) VS = 31.
(3) VS = 63.

Fig.20 Control range of vertical slope.



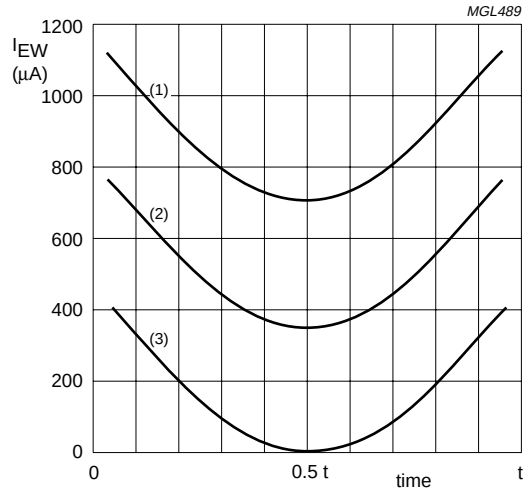
VA = 31; SC = 0.
(1) VSH = 0.
(2) VSH = 31.
(3) VSH = 63.

Fig.21 Control range of vertical shift.



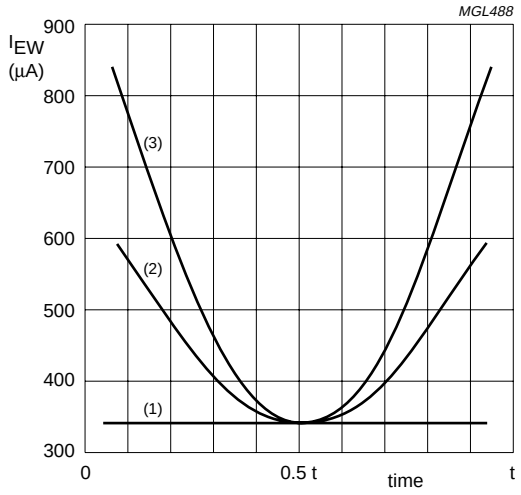
VA = 31; VHS = 31.
(1) SC = 0.
(2) SC = 31.
(3) SC = 63.

Fig.22 Control range of S-correction.



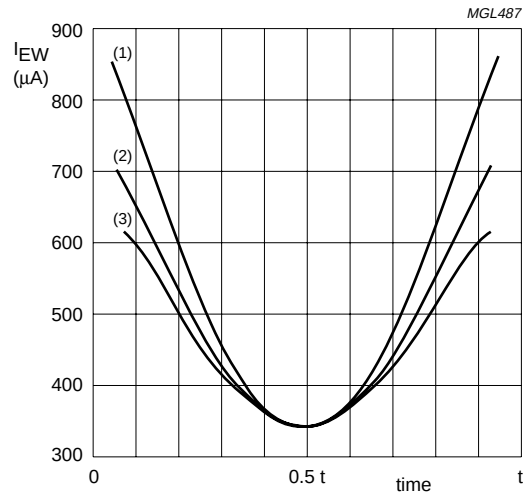
PW = 31; CP = 31.
(1) EW = 0.
(2) EW = 31.
(3) EW = 63.

Fig.23 Control range of E-W width.



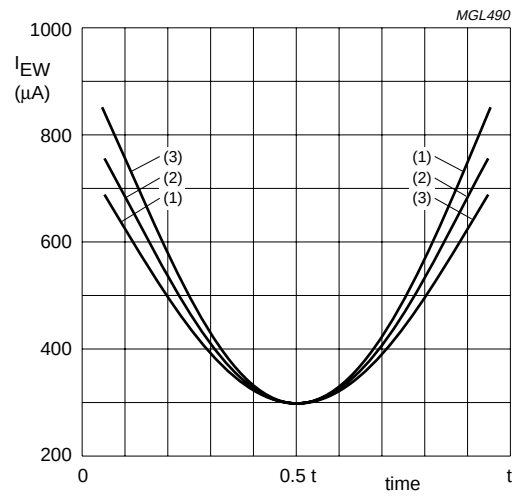
EW = 31; CP = 31.
(1) PW = 0.
(2) PW = 31.
(3) PW = 63.

Fig.24 Control range of E-W parabola/width ratio.



EW = 31; PW = 63.
(1) CP = 0.
(2) CP = 31.
(3) CP = 63.

Fig.25 Control range of E-W corner/parabola ratio.



EW = 31; PW = 31.
(1) TC = 0.
(2) TC = 31.
(3) TC = 63.

Fig.26 Control range of E-W trapezium correction.

Adjustment of geometry control parameters

The deflection processor of the TDA933xH offers 15 control parameters for picture alignment, as follows:

For the vertical picture alignment;

- S-correction
- Vertical amplitude
- Vertical slope
- Vertical shift
- Vertical zoom
- Vertical scroll
- Vertical wait.

For the horizontal picture alignment;

- Horizontal shift
- Horizontal parallelogram
- Horizontal bow
- E-W width with extended range for the zoom function
- E-W parabola/width ratio
- E-W upper corner/parabola ratio
- E-W lower corner/parabola ratio
- E-W trapezium correction.

It is important to notice that the ICs are designed for use with a DC-coupled vertical deflection stage. This is why a vertical linearity alignment is not necessary (and therefore not available).

For a particular combination of picture tube type, vertical output stage and E-W output stage, the required values for the settings of S-correction and E-W corner/parabola ratio must be determined. These parameters can be preset via the I²C-bus and do not need any additional adjustment. The rest of the parameters are preset with the mid-value of their control range, i.e. 1FH, or with the values obtained by previously-adjusted TV sets on the production line.

The vertical shift control is intended to compensate offsets in the external vertical output stage or in the picture tube. It can be shown that, without compensation, these offsets will result in a certain linearity error, especially with picture tubes that need large S-correction. In 1st-order approximation, the total linearity error is proportional to the value of the offset and to the square of the S-correction that is needed. The necessity to use the vertical shift alignment depends on the expected offsets in the vertical output stage and picture tube, on the required value of the S-correction and on the demands upon vertical linearity.

To adjust the vertical shift and vertical slope independently of each other, a special service blanking mode can be entered by setting bit SBL HIGH. In this mode, the RGB outputs are blanked during the second half of the picture. There are two different methods for alignment of the picture in the vertical direction. Both methods use the service blanking mode.

The first method is recommended for picture tubes that have a marking for the middle of the screen. With the vertical shift control, the last line of the visible picture is positioned exactly in the middle of the screen. After this adjustment, the vertical shift should not be changed any more. The top of the picture is positioned by adjusting the vertical amplitude, and the bottom by adjusting the vertical slope.

The second method is recommended for picture tubes that have no marking for the middle of the screen. For this method, a video signal is required in which the middle of the picture is indicated (e.g. the white line in the circle test pattern). The beginning of the blanking is positioned exactly on the middle of the picture using the vertical slope control. The top and bottom of the picture are then positioned symmetrically with respect to the middle of the screen by adjusting the vertical amplitude and vertical shift. After this adjustment, the vertical shift has the correct setting and should not be changed any more.

If the vertical shift alignment is not required, VSH should be set to its mid-value, i.e. VSH = 1FH (31 DEC). The top of the picture is then positioned by adjusting the vertical amplitude and the bottom of the picture by adjusting the vertical slope.

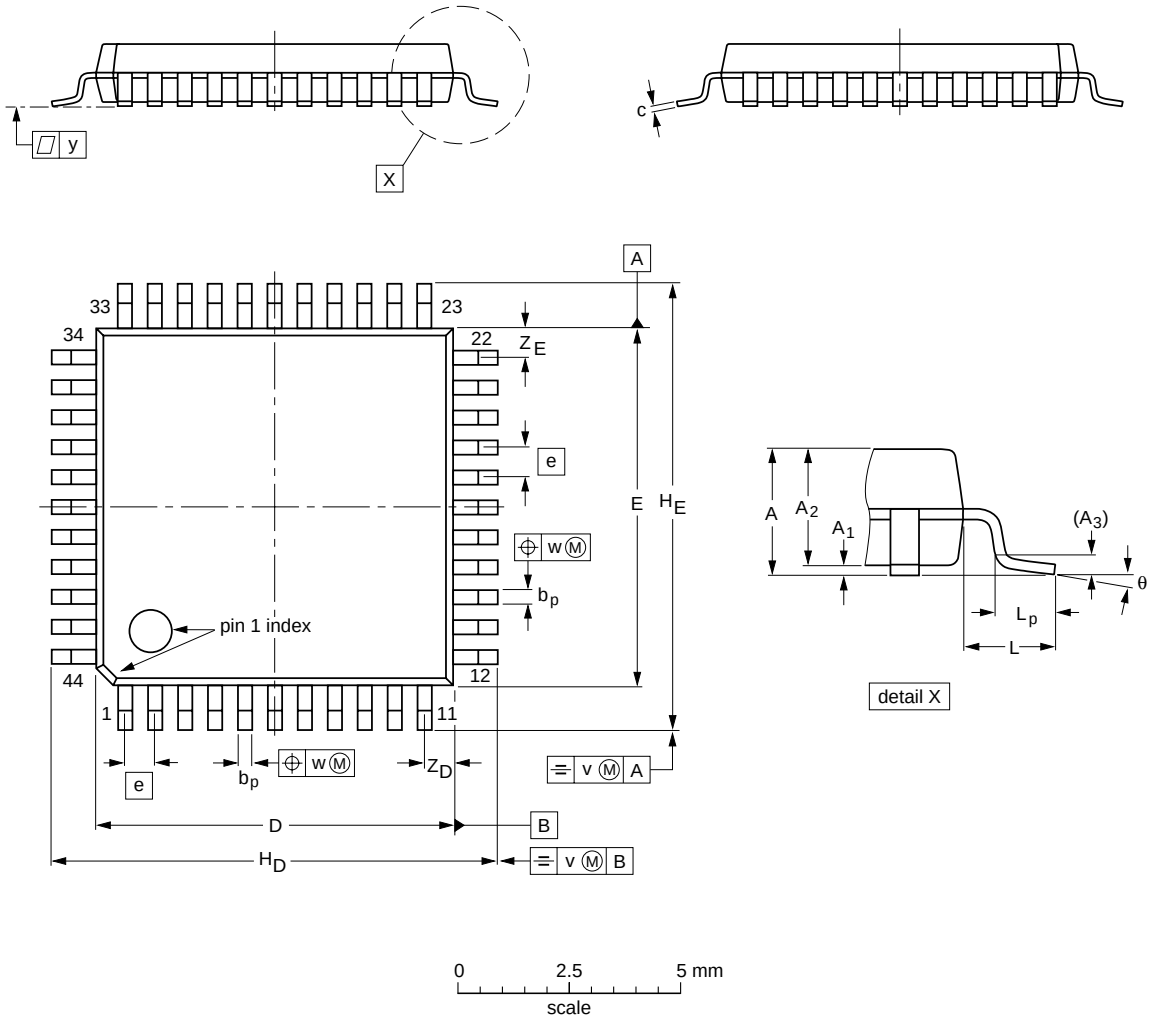
After the vertical picture alignment, the picture is positioned in the horizontal direction by adjusting the E-W width, E-W parabola/width ratio and horizontal shift. Finally (if necessary), the left and right-hand sides of the picture are aligned in parallel by adjusting the E-W trapezium control.

Additional horizontal corrections are possible using the parallelogram and bow controls.

To obtain the correct range of the vertical zoom function, the vertical geometry should be adjusted at a nominal setting of the zoom DAC at position 19H (25 DEC) and the vertical scroll DAC at 1FH (31 DEC).

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax.+381 11 3342 553

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

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Printed in The Netherlands 753504/02/pp56 Date of release: 2000 May 08 Document order number: 9397 750 06406

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